NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY

GREATER NOIDA

(NAAC ACCREDITED)

Approved by AICTE and Affiliated to Dr. A.P.J. Abdul Kalam Technical University, Uttar Pradesh, Lucknow

LABORATORY MANUAL

DIGITAL SYSTEM DESIGN LAB
(AEC0351)

BACHELOR OF TECHNOLOGY

SEMESTER III **YEAR: II**

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
(NBA ACCREDITED)

Vision & Mission of the Institute

Vision:

To be an institute of academic excellence in digital arena with global outreach delivering socially responsible professionals to become a university and an entrepreneurial hub.

Mission:

- To impart quality education and hone student's skills and competencies making them future ready.
- To foster an ecosystem for research, product development, innovation, incubation and entrepreneurship.
- To instill values and ethics to produce socially responsible technocrats addressing global problems.
- To develop an environment for sharing and exchange of resources globally for lifelong learning.

Vision & Mission of the Department

Vision:

To prepare the students for global competence, with core knowledge in Electronics and Communication Engineering having focus on research to meet the needs of Industry and Society.

Mission:

M1 To become dynamic and vigorous knowledge hub with an exposure to state-of-art technologies for connecting world.

M2 To provide in-depth knowledge of Electronics and Communication Engineering ensuring the effective teaching learning process.

M3 To train students to take up innovative projects in group with sustainable and inclusive technology relevant to the industry and social needs.

M4 To empower students to become skilled and ethical entrepreneurs.

M5 To promote and adapt professional development in a perpetual demanding environment and nurture the best minds for the future.

Program Educational Objectives (PEOs)

PEO1 To have an excellent scientific and engineering breadth so as to comprehend, analyze, design and solve real-life problems using state-of-the-art technology.

PEO2 To lead a successful career in industries or to pursue higher studies or to understand entrepreneurial endeavours.

PEO3 To effectively bridge the gap between industry and academics through effective communication skill, professional attitude and a desire to learn.

Program Specific Outcomes (PSOs)

PSO1 To apply the knowledge of mathematics, science and electronics & communication engineering to work effectively in the industry based on same or related area.

PSO2 To use their skills to work in modern electronics & communication engineering tools, software and equipments to design solutions for complex problems in the related field that meet the specified needs of the society.

PSO3 To function effectively as an individual and as a member or leader of a team by qualifying through examinations like GATE, IES, PSUs, TOEFL, GMAT and GRE etc.

Program Outcomes (POs)

PO1 **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization for the solution of complex engineering problems.

PO2 **Problem analysis:** Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3 **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for public health and safety, and cultural, societal, and environmental considerations.

PO4 **Conduct investigations of complex problems:** Use research based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of information to provide valid conclusions.

PO5 **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools, including prediction and modeling to complex engineering activities, with an understanding of the limitations.

PO6 **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7 **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8 **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9 **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10 **Communication:** Communicate effectively on complex engineering activities with the engineering community and with the society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11 **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12 **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

COURSE OBJECTIVES

Lab Objective: The student will learn about		
1.	To verify truth table of various type of logic gates.	K1,K2,K3
2.	To design and verify different type of combinational circuits.	K2,K3
3.	To understand and verify truth table of various type of flip-flops.	K1,K3
4.	To learn and design the different type of sequential circuits.	K1,K2,K3

COURSE OUTCOMES

Lab Outcome: After successful completion of this LAB students will be able to		
CO 1	Understand and verify truth table of various type of logic gates.	K1, K2, K3
CO 2	Design & analyze modular combinational circuits with MUX/DEMUX, decoder and encoder.	K2, K3
CO 3	Design & verify truth table of various types of flipflops.	K1, K3
CO 4	Design & analyze different types of sequential logic circuits	K1, K2, K3
CO 5	Design & build mini project using digital ICs.	K2, K3, K6

MAPPING OF CO's WITH PO'S

PO's CO's	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
AEC0301.1	3	2	-	-	-	-	-	-	2	2	-	2	3	2	-
AEC0301.2	3	3	3	-	-	-	-	-	2	2	-	2	3	3	3
AEC0301.3	3	2	-	-	-	-	-	-	2	2	-	2	3	2	-
AEC0301.4	3	3	3	-	-	-	-	-	2	2	-	2	3	3	3
AEC0301.5	3	3	3	2	2	2	2	2	3	3	3	3	3	3	3
Average	3	2.6	3	2	2	2	2	2	2.2	2.2	3	2.2	3	2.6	3

GENERAL SAFETY GUIDELINES

Following safety guidelines must be followed while performing lab experiments:

- Student entry in the lab is ensured strictly as per the allocated time slots or seeking prior proper permission from the lab faculty or instructor.
- Students are expected to conduct themselves in a responsible manner while working in the laboratory.
- They should keep their bags on the shelf provided outside the lab and carry only essential items such as lab record, manual, pen-pencil, copy and calculator etc. inside the lab.
- Students are not allowed to carry food items (not even chewing gum), beverages and water bottles while working in the laboratory.
- They are expected to observe good housekeeping practices and ensure equipment, sitting stools and components to be handled carefully and kept at proper place after finishing the work to keep the lab clean and tidy.
- While working in the lab
  - Avoid stretching electrical cables and connectors while using the equipment.
  - Rig the circuit and get it verified from the lab instructor before connecting it to power source.
  - Pay proper attention towards earthing of electrical equipment. Ensure proper ventilation in the lab while working.
  - Ensure use of wire clippers, insulating tape, plug-pins to prevent any electrical shocking hazards.
  - In case of any short circuit, sensing burning smell or observing any smoke switch off power supply and immediately report to the faculty/lab instructor available in the lab.
- In case of any minor injury please contact the lab instructor or lab faculty. The first aid Box is available in the department in front of Room No 208.

In case of any fire emergency, contact the faculty or lab instructor. For your information, the fire safety equipment is available on each floor near notice board

LIST OF EXPERIMENTS

Sr. No.	Name of Experiment	CO
1	Introduction to digital system design lab- nomenclature of digital ICs, specifications, Concept of V_{cc} and ground, verification of the truth tables of logic gates using TTL ICs.	1
2	Implementation of the given Boolean function using TTL logic gates (NOT gate, AND gate and OR) in SOP and POS forms for following Boolean expressions: i. Y1 = AB' + A'B for SOP ii. Y2 = (A'+B).(A+B') for POS	1
3	Implementation of half adder and full adder using TTL logic gates (EXOR-7486, AND-7408, OR-7432) and verify its truth table.	2
4	Implementation of 4-bit parallel adder using 7483 IC and verify the output for the given inputs. (i) A = 1011, B = 1001 (ii) A = 0011, B = 0010	2
5	Implementation of 2:4 Decoder using logic gates (NOT gate- 7404, AND gate- 7408) and verify its truth table.	2
6	Implementation of and 4:2 Encoder using logic gate (OR gate-7432) and verify its truth table.	2
7	Implementation of 4:1 multiplexer and 1:4 demultiplexer using logic gates (AND gate-7408, NOT gate-7404 and OR gate-7432) and verify their truth table.	2
8	Verification of truth tables of RS, JK, T and D flip-flops using NAND gate (7400) & NOR gates (7402).	3
9	Design 4-bit synchronous and asynchronous counter using JK flipflops (7476) and AND gates (7408) and verify their truth table.	4
10	Design a mini project using real time digital integrated circuits and other components.	5

EXPERIMENT NO-1

AIM: -Introduction to digital system design lab- nomenclature of digital ICs, specifications, Concept of V_{cc} and ground, verification of the truth tables of logic gates using TTL ICs.

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APPARATUS REQURIED:-

Digital lab kits, single strand wire, breadboard TTL ICs.

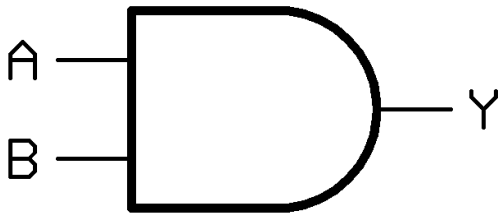
SL No.	COMPONENT	SPECIFICATION	QTY
1	AND GATE	IC 7408	1
2	OR GATE	IC 7432	1
3	NOT GATE	IC 7404	1
4	NAND GATE 2 I/P	IC 7400	1
5	NOR GATE	IC 7402	1
6	X-OR GATE	IC 7486	1
7	IC TRAINER KIT	…	1
8	PATCH CORD	…..	1

THEORY:

Logic gates are electronic circuits which perform logical functions on one or more inputs to produce one output. There are seven logic gates. When all the input combinations of a logic gate are written in a series and their corresponding outputs written along them, then this input/ output combination is called Truth Table. OR, AND and NOT are basic gates. NAND, NOR are known as universal gates.

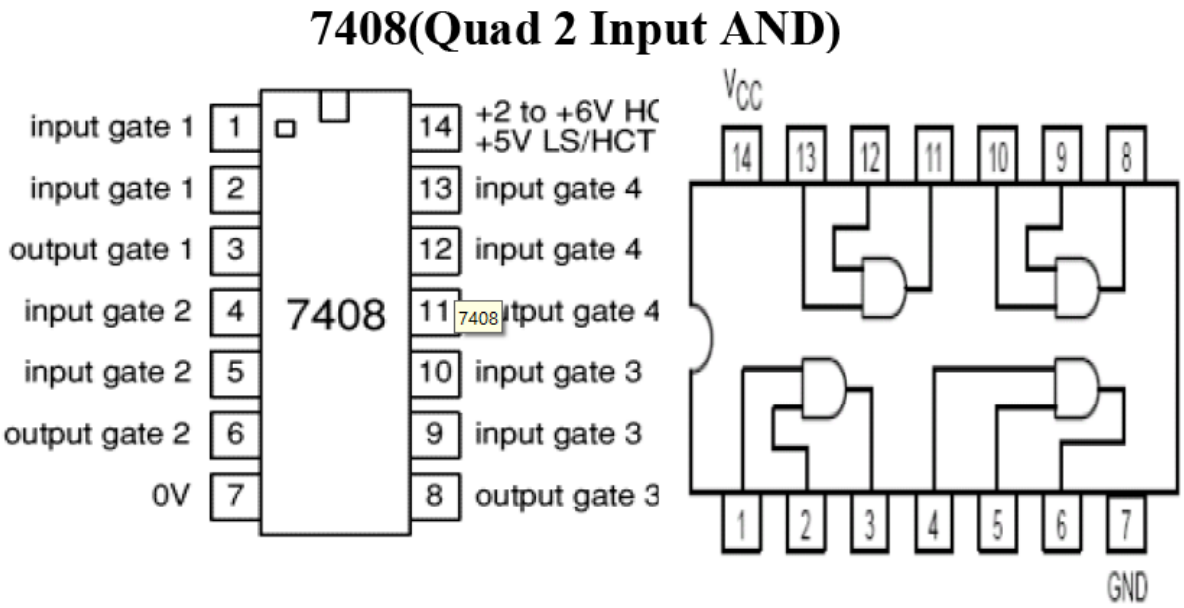
AND GATE:

The AND gate performs a logical multiplication commonly known as AND function. The output is high when both the inputs are high. The output is low level when any one of the inputs is low.



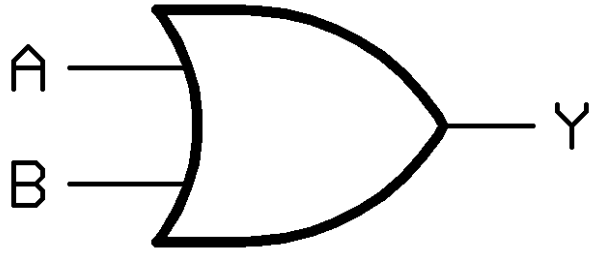
Inputs		Outputs
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Pin diagram of 2 input AND Gate:



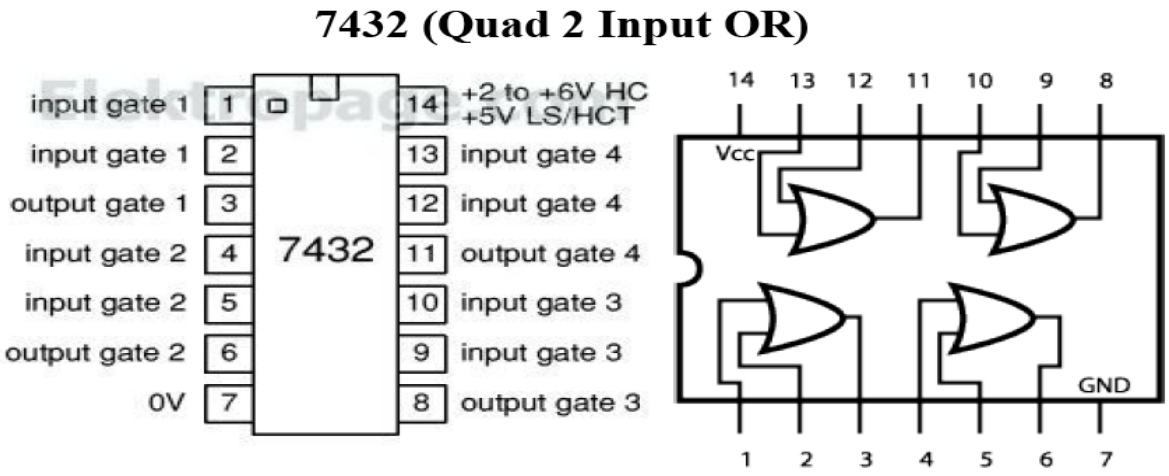
OR GATE:

The OR gate performs a logical addition commonly known as OR function. The output is high when any one of the inputs is high. The output is low level when both the inputs are low.

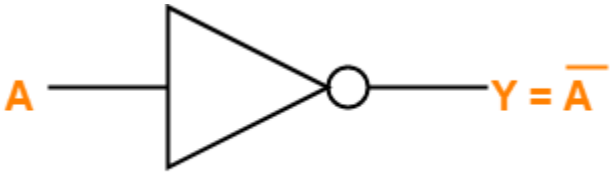


Inputs		Outputs
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Pin diagram of 2 input OR Gate:

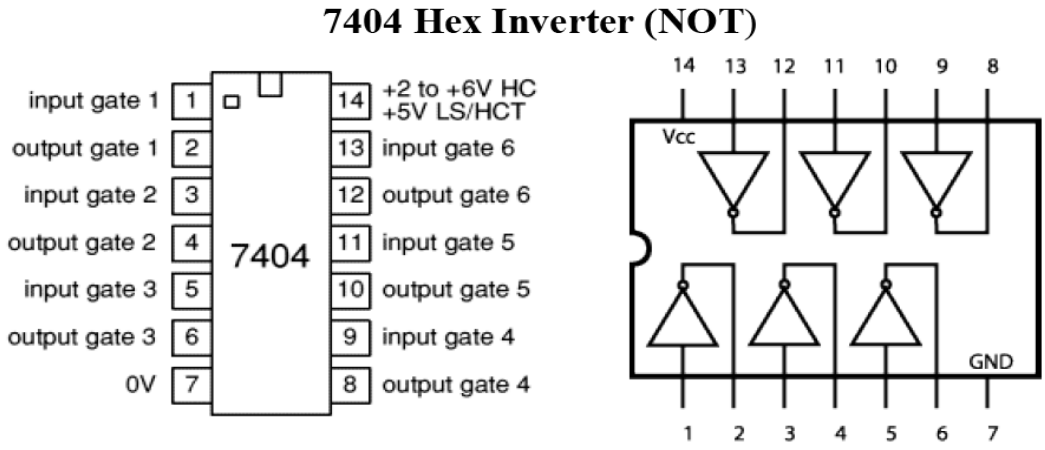


NOT GATE: The NOT gate called as an inverter. The output is high when input is low. The output is low when input is high.

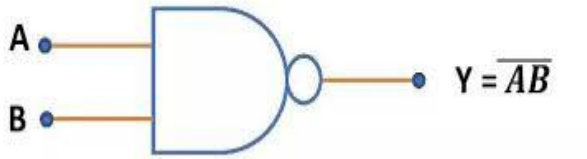


Inputs	Outputs
A	**Y**
1	0
0	1

Pin diagram of 2 input NOT Gate:

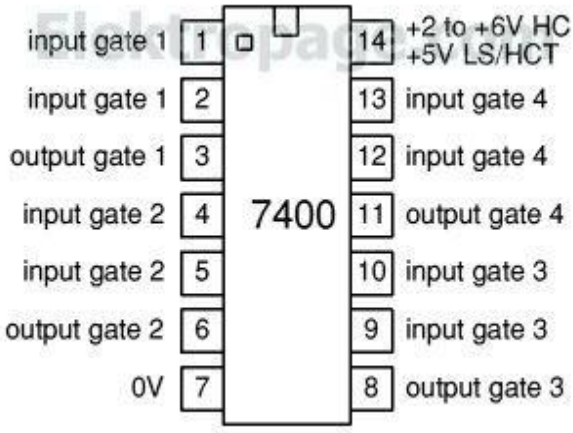


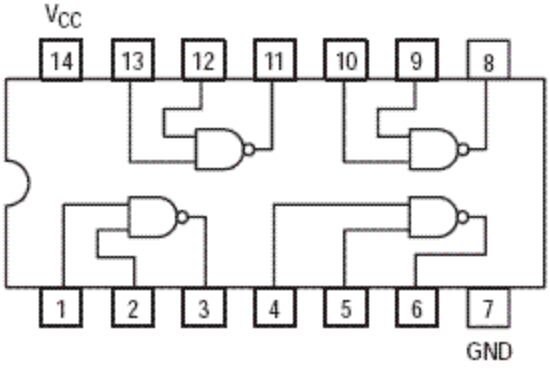
NAND GATE: NAND gate is a combination of AND & NOT gate. The output is high when both the inputs are low and any of the input is low. The output is low when both the inputs are high



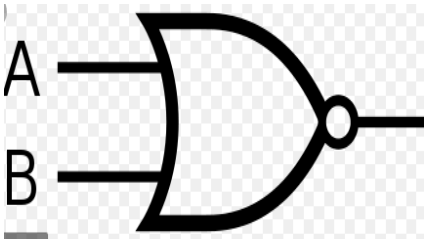
Inputs		Outputs
A	**B**	**Y**
0	0	1
0	1	1
1	0	1
1	1	0

Pin diagram of 2 input NAND Gate:



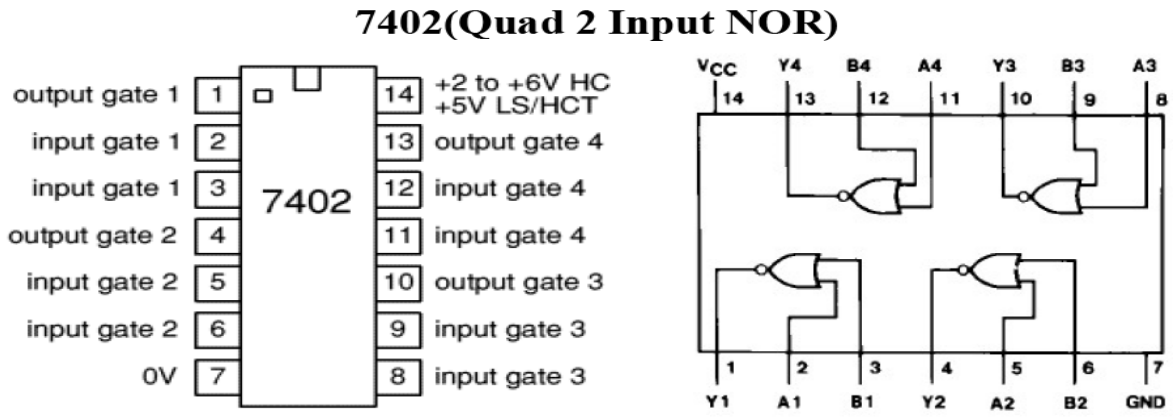


NOR GATE: The NOR gate is a contraction of OR-NOT. The output is high when both inputs are low. The output is low when one or both inputs are high.

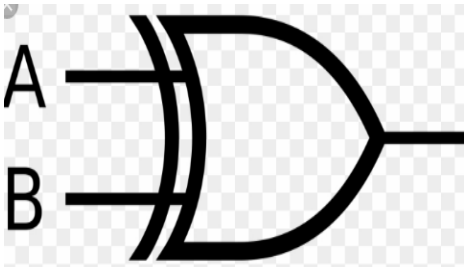


Inputs		Outputs
A	**B**	**Y**
0	0	1
0	1	0
1	0	0
1	1	0

Pin diagram of 2 input NOR Gate:

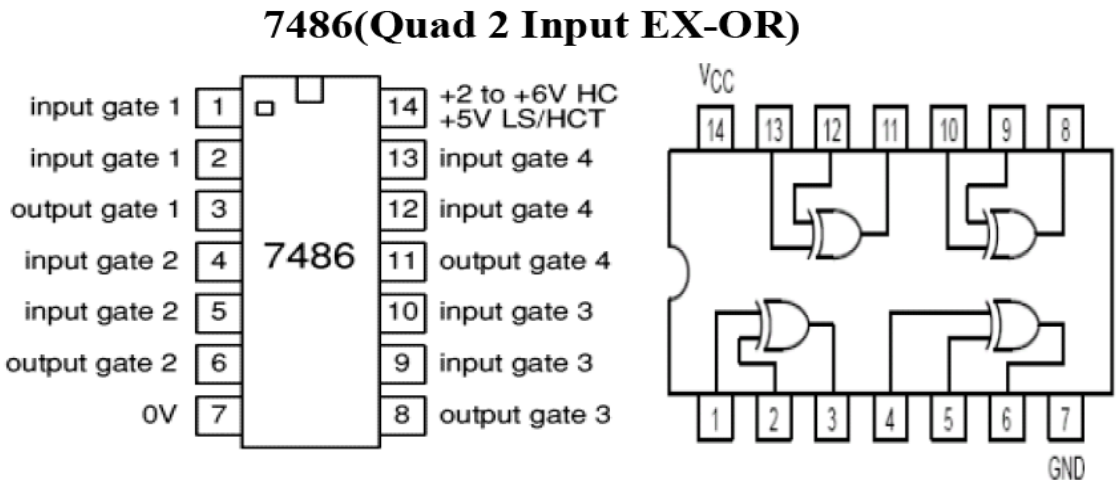


EX-OR GATE: The output is high when any one of the inputs is high. The output is low when both the inputs are low and both the inputs are high.



Inputs		Outputs
A	**B**	**Y**
0	0	0
0	1	1
1	0	1
1	1	0

Pin diagram of 2 input EX-OR Gate:



PRECAUTIONS:

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The V_{cc} and ground should be applied carefully at the specified pinonly.

RESULT: Logics gate has been studied and verified.

Quiz Questions with answer.

Q1. What is Digital Gate?

Ans: Digital gates are basically electronic components which are used for switching and manipulating binary data

Q2. What is the use of logic gates?

Ans: In electronics, a logic gate is an idealized or physical device implementing a Boolean function; that is, it performs a logical operation on one or more binary inputs and produces a single binary output.

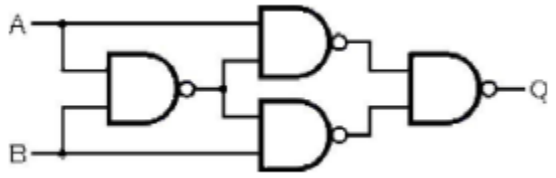
Q3: What is truth table?

A3ns: Truth table is a table from which we can get o/p of different gates

Q4. What is universal gate?

Ans: A universal gate is a gate which can implement any Boolean function without need to use any other gate type. The NAND and NOR gates are universal gates. In practice, this is advantageous since NAND and NOR gates are economical and easier to fabricate and are the basic gates used in all IC digital logic families

Q5. Draw the EX-OR gate by using the NAND gate?



EXPERIMENT NO: 2

AIM: Implementation of the given Boolean function using TTL logic gates (NOT gate, AND gate and OR) in SOP and POS forms for following Boolean expressions:
(i) Y1 = AB' + A'B for SOP
(ii) Y2 = (A'+B) (A+B') for POS

APPARATUS REQUIRED: Digital lab kit, single strand wire, ICs, breadboard &connecting wire.

THEORY:

A Boolean function is an algebraic form of Boolean expression. A Boolean function of n-variables is represented by f(x1, x2, x3….xn). By using Boolean laws and theorems, we can simplify the Boolean functions of digital circuits. A different ways of representing a Boolean function is given below.

- Sum-of-Products (SOP) Form
- Product-of-sums (POS) form
- Canonical forms

There are two types of canonical forms:

- Sum-of-min terms or Canonical SOP
- Product-of- max terms or Canonical POS

Boolean functions can be represented by using NAND gates and also by using K-map (Karnaugh map) method. We can standardize the Boolean expressions by using by two standard forms.

SOP form – Sum Of Products form

POS form – Product Of Sums form

SUM OF PRODUCT (SOP) FORM:

The sum-of-products (SOP) form is a method (or form) of simplifying the Boolean expressions of logic gates. In this SOP form of Boolean function representation, the variables are operated by

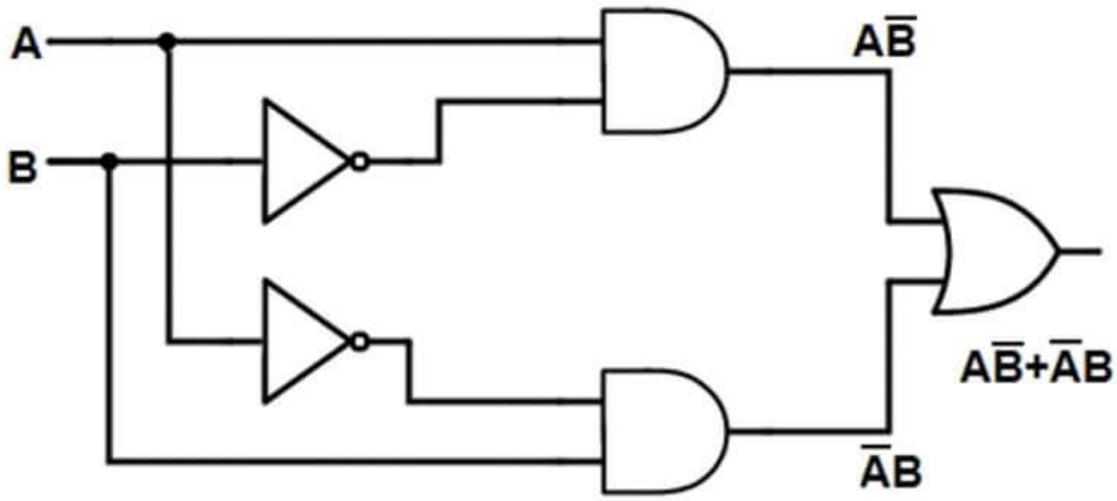
AND (product) to form a product term and all these product terms are ORed (summed or added) together to get the final function.

A sum-of-products form can be formed by adding (or summing) two or more product terms using a Boolean addition operation. Here the product terms are defined by using the AND operation and the sum term is defined by using OR operation.

The sum-of-products form is also called as Disjunctive Normal Form as the product terms are ORed together and Disjunction operation is logical OR. Sum-of-products form is also called as Standard SOP.

Implementation of Y= A'B +AB'

A	B	A'	B'	AB'	A'B	AB'+A'B
0	0	1	1	0	0	0
0	1	1	0	0	1	1
1	0	0	1	1	0	1
1	1	0	0	1	0	0



PRODUCT OF SUM (POS) FORM:

The product of sums form is a method (or form) of simplifying the Boolean expressions of logic gates. In this POS form, all the variables are ORed, i.e. written as sums to form sum terms.

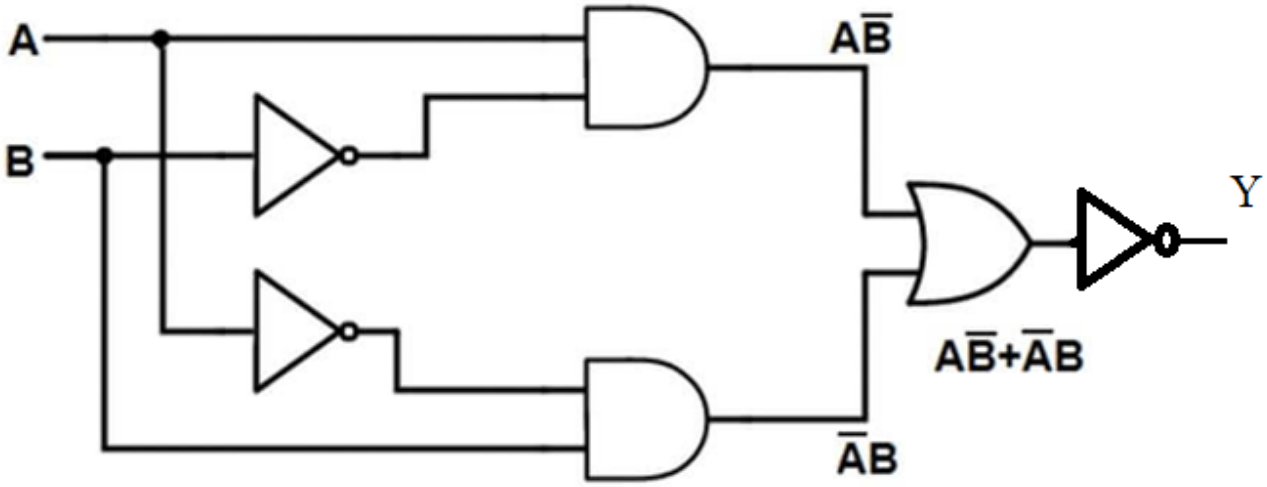
All these sum terms are ANDed (multiplied) together to get the product-of-sum form. This form is exactly opposite to the SOP form. So this can also be said as "Dual of SOP form".

Here the sum terms are defined by using the OR operation and the product term is defined by using AND operation. When two or more sum terms are multiplied by a Boolean OR operation, the resultant output expression will be in the form of product-of-sums form or POS form.

The product-of-sums form is also called as Conjunctive Normal Form as the sum terms are ANDed together and Conjunction operation is logical AND. Product-of-sums form is also called as Standard POS.

IMPLEMENTATION OF F= (A'+B)(A+B')

A	**B**	**A'**	**B'**	**AB'**	**A'B**	**AB'+A'B**	**(AB'+A'B)'= (A'+B)(A+B')**
0	0	1	1	0	0	0	1
0	1	1	0	0	1	1	0
1	0	0	1	1	0	1	0
1	1	0	0	0	0	0	1



PRECAUTIONS:

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The V_{cc} and ground should be applied carefully at the specified pin only.

RESULT: SOP and POS form has been studied and verified.

Quiz Questions with answer.

Q1. What is SOP and POS form?

Ans: The term "Sum of Products" or "SOP" is widely used for the canonical form that is a disjunction (OR) of minterms. Its De Morgan dual is a "Product of Sums" or "POS" for the canonical **form** that is a conjunction (AND) of maxterms.

Q2: What is difference between SOP and POS?

Ans: The main difference between SOP and POS is that the SOP is a way of representing a Boolean expression using min terms or product terms while the POS is a way of representing a Boolean expression using max terms or sum terms

Q3. What is SOP K map?

Ans: A minterm is a Boolean expression resulting in 1 for the output of a single cell, and 0's for all other cells in a Karnaugh map, or truth table.

Q4. Convert the following SOP expression to an equivalent POS expression.

Ans : $A\,B\,C + A\,\overline{B}\,\overline{C} + A\,\overline{B}\,C + A\,B\,\overline{C} + \overline{A}\,\overline{B}\,C$

$(A + B + C)(A + \overline{B} + C)(A + \overline{B} + \overline{C})$

Q5. What is canonical SOP?

Ans: Canonical SOP form means Canonical Sum of Products form. In this form, each product term contains all literals. So, these product terms are nothing but the min terms. Hence, canonical SOP form is also called as sum of min terms form.

EXPERIMENT NO: 3

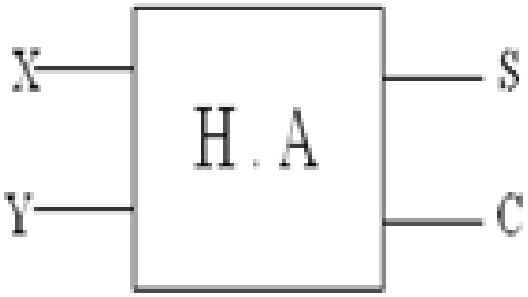
AIM: Implementation of half adder and full adder using TTL logic gates (EXOR- 7486, AND-7408, OR-7432) and verify its truth table.

APPARATUS REQUIRED: IC 740, 7486& Connecting leads.

THEORY:

Half adder is a combinational arithmetic circuit that adds two numbers and produces a sum bit(S) and carry bit (C) as the output. If A and B are the input bits, then sum bit(S) is the X-OR of A and B and the carry bit (C) will be the AND of A and B.

The block diagram of half adder is:



Truth Table for half adder is:

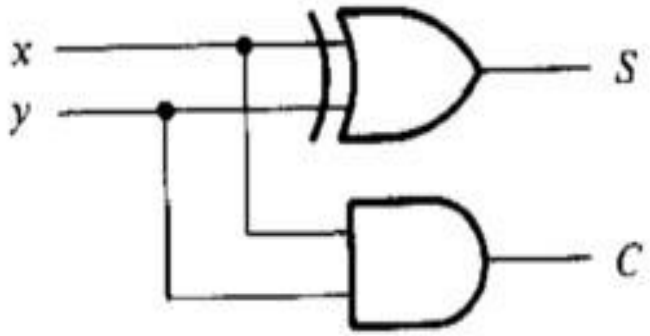
Inputs		Outputs	
X	Y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Boolean equations for sum and carry are:

$$S = \overline{X}Y + X\overline{Y}$$

$$C = XY$$

Logic diagram of half adder:



(b) $S = x \oplus y$
$C = xy$

Full adder is developed to overcome the drawbacks of Half Adder circuit. It can add two one-bit numbers A and B, sum S and carry C.
The full adder is a three input and two output combinational circuit

Truth Table for full adder is:

Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

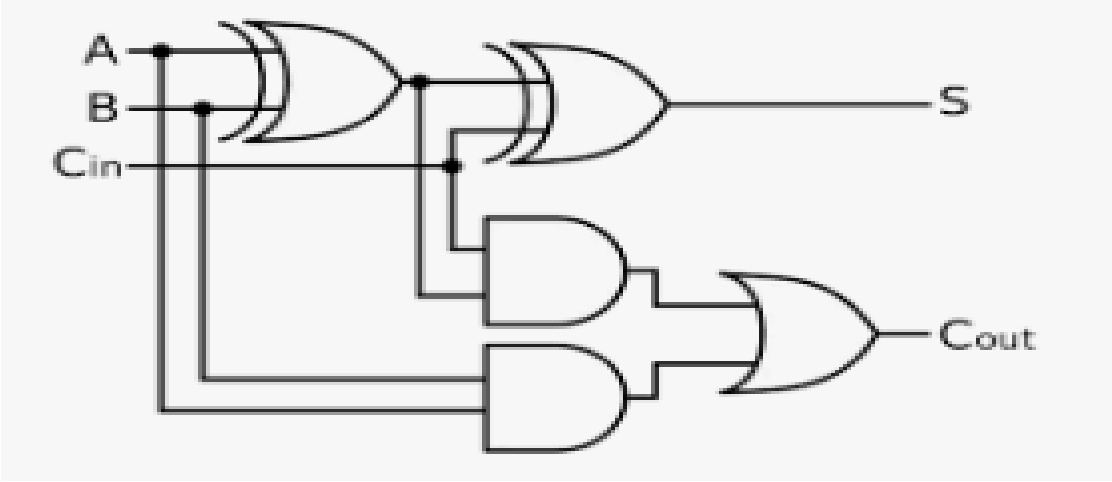
The block diagram of full adder is:

Boolean equations for sum and carry are:

$$Sum = A \text{ XOR } B \text{ XOR } C_{in}$$

$$Carry = AB + BC_{in} + C_{in} A$$

Logic diagram of half adder:



RESULT- Half adder and full adder has been studied and verified.

PRECAUTIONS:

1. Make the connections according to the IC pin diagram.
2. The connections should be tight.
3. The V_{cc} and ground should be applied carefully at the specified pin only.

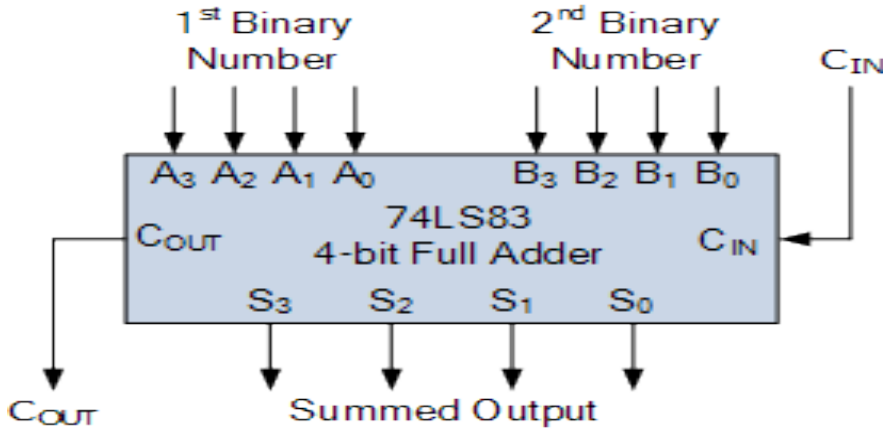
EXPERIMENT NO: 4

AIM: Implementation of 4-bit parallel adder using 7483 IC and verify the output for the given inputs.
(i) A = 1011, B = 1001
(ii) A = 0011, B = 0010

APPRATUS REQUIRED – Digital trainer kit, IC 7483 (4-bit parallel adder).

BRIEF THEORY–A 4-bit adder is a circuit which adds two 4-bits numbers, say, A and B. In addition, a 4-bit adder will have another single-bit input which is added to the two numbers called the carry-in(C_{in}). The output of the 4-bit adder is a 4-bit sum (S) and a carry-out (C_{out})bit.

PIN CONFIGURATION-



Pin diagram of IC 7483

TRUTH TABLE:

A3	A2	A1	A0	B3	B2	B1	B0	C4	S3	S2	S1	S0
1	0	1	1	1	0	0	1	1	0	1	0	0
0	0	1	1	0	0	1	0	0	0	1	0	1

PROCEDURE –

1. Make the connections as per the logic diagram.
2. Connect +5v and ground according to pin configuration.
3. Apply diff combinations of inputs to the i/p terminals.
4. Note o/p for summation.
5. Verify the truth table.

RESULT- Binary 4-bit full adder is studied and verified.

PRECAUTIONS:

1. Make the connections according to the IC pin diagram.
2. The connections should be tight.
3. The V_{cc} and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Q 1 What do you understand by parallel adder?

Ans. If we place full adders in parallel, we can add two-or four-digit numbers or any other size desired i.e. known as parallel adder.

Q2 What happens when an *N*-bit adder adds two numbers whose sum is greater than or equal to 2^N

Ans. Overflow.

Q3. Is Excess-3 code is weighted code or not?

Ans. Excess-3 is not a weighted code.

Q4 What is IC no. of parallel adder?

Ans. IC 7483.

Q5 What is the difference between Excess-3 & Natural BCD code?

Ans. Natural BCD code is weighted code but Excess-3 code is not weighted code.

EXPERIMENT – 5

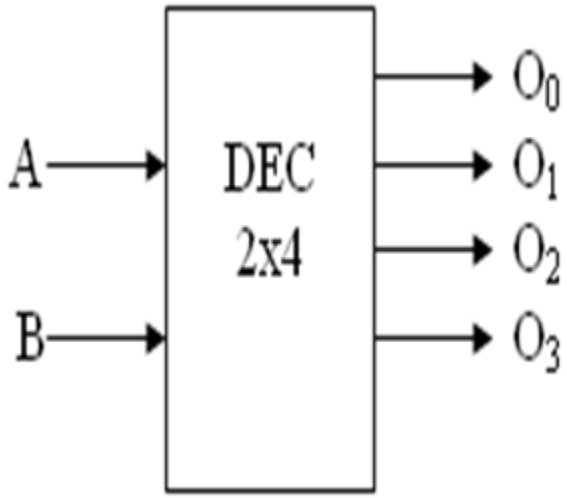
AIM: Implementation of 2:4 Decoder using logic gates (NOT gate- 7404, AND gate- 7408) and verify its truth table.

APPARATUS REQUIRED: IC 7447, 7-segment display, IC 74139 and connecting leads.

THEORY:

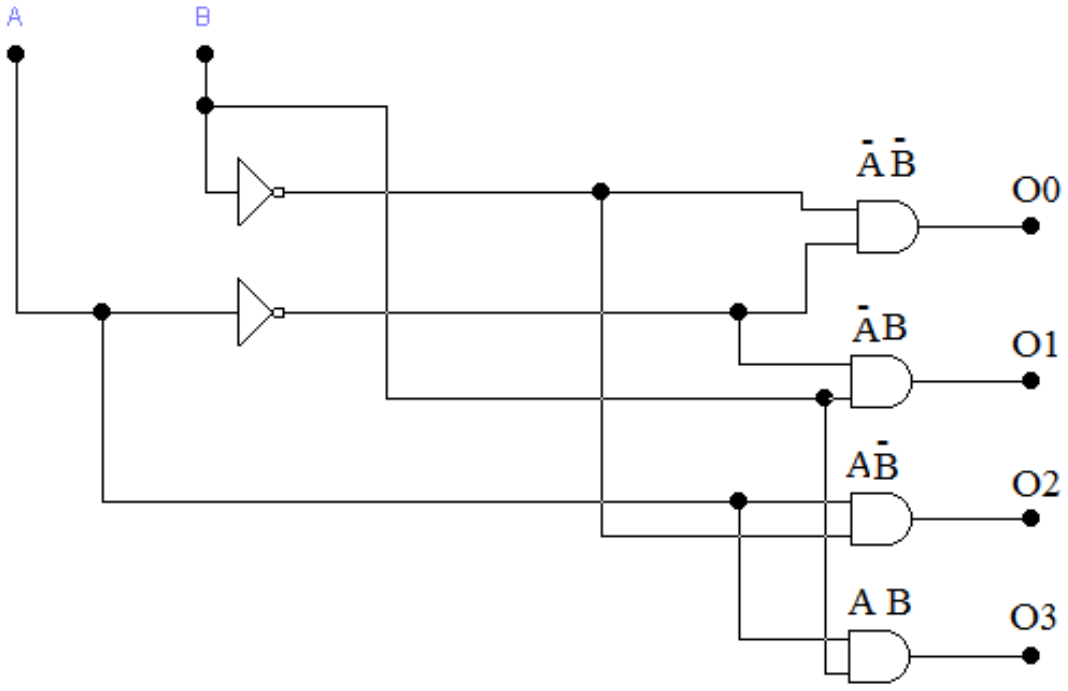
DECODER: A decoder is a device which does the reverse operation of an encoder, undoing the encoding so that the original information can be retrieved. The same method used to encode is usually just reversed in order to decode. It is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines. In digital electronics, a decoder can take the form of a multiple-input, multiple-output logic circuit that converts coded inputs into coded outputs, where the input and output codes are different. e.g. n-to-2^n, binary-coded decimal decoders. Enable inputs must be on for the decoder to function, otherwise its outputs assume a single "disabled" output code word.

BLOCK DIAGRAM OF 2X4 DECODER



TRUTH TABLE OF 2X4 DECODER

Inputs		Outputs			
A	B	O_0	O_1	O_2	O_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1



2x4 Decoder logical diagram

PROCEDURE:

1) Connect the circuit as shown in figure.
2) Apply Vcc & ground signal to every IC.
3) Observe the input & output according to the truth table.

OBSERVATION TABLE:

Inputs			Outputs							
a	b	C	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1
Output function			$\bar{a}\bar{b}\bar{c}$	$\bar{a}\bar{b}c$	$\bar{a}b\bar{c}$	$\bar{a}bc$	$a\bar{b}\bar{c}$	$a\bar{b}c$	$ab\bar{c}$	abc

RESULT: Decoder has been studied and verified.

PRECAUTIONS:

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The V_{cc} and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Q. 1 What do you understand by decoder?

Ans. A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2n unique output lines. Most IC decoders include one or more enable inputs to control the circuit operation.

Q. 2 What is the main difference between decoder and demultiplexer?

Ans. In decoder we have n input lines as in demultiplexer we have n select lines.

Q. 3 Why Binary is different from Gray code?

Ans. Gray code has a unique property that any two adjacent gray codes differ by only a single bit.

Q.4 Write down the method of Binary to Gray conversion.

Ans. Using the Ex-Or gates.

Q. 5 Convert 0101 to Decimal**.**

Ans. 5

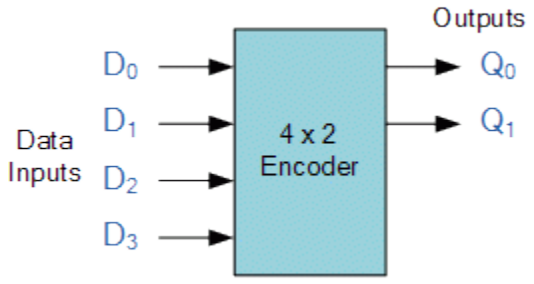
EXPERIMENT – 6

AIM: Implementation of and 4:2 Encoder using logic gate (OR gate-7432) and verify its truth table.

APPARATUS REQUIRED: OR gate IC 7432, Connecting wires, Power supply, Bread board etc.

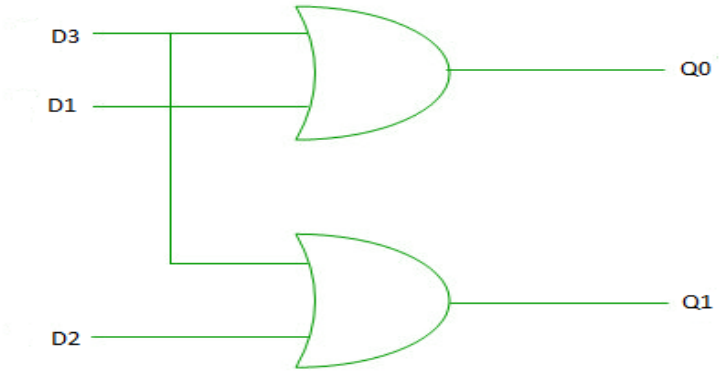
THEORY: An encoder is a combinational logic circuit. It is the reverse of a decoder function. It has '2^n' input and '**n**' output lines. An encoder accepts an active level on one of its inputs representing a digit such as a decimal/ octal digit and it convert to coded output. Encoder is used at the starting stage to encode the message into a unique code. Encoder encodes different types of messages into various forms. In digital circuits it encodes a decimal value into a binary word. The encoded binary word has number of bits associated with it. The number of bits depends upon the decimal value which is being encoded.

BLOCK DIAGRAM AND TRUTH TABLE OF ENCODER:



Inputs				Outputs	
D_3	D_2	D_1	D_0	Q_1	Q_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1
0	0	0	0	x	x

LOGIC DIAGRAM OF ENCODER:



PROCEDURE:

1. Connect the supply to the bread board through connecting wires, also connect circuit as per circuit diagram.
2. Give the input to D_0 TO D_3.
3. Observe the output Q_0 and Q_1 on the bread board through LED's.
4. For different combinations of inputs observe the output and match the truth table.

RESULT: The truth table of encoder is verified.

PRECAUTIONS:

- All connections should be made neat and tight.
- Power supply and ICs should be handled with carefully.
- While making connections main supply should be kept switched off.
- Never touch live and naked wires.

Viva-voice Questions:

1. What is an encoder?

Ans **:**An encoder is a combinational circuit which has 2^n input and n output lines.

2. What is priority encoder?

Ans **:** In priority encoder if two or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence.

3. What is the basic difference between an encoder and a decoder?

Ans **:** An encoder is a combinational circuit which has 2^n input and n output lines while a decoder is a circuit which has n input lines and 2^n output lines .

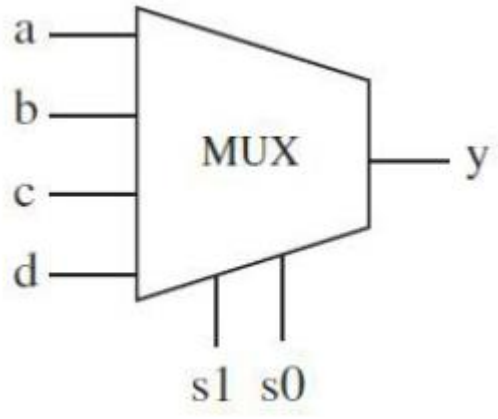
EXPERIMENT NO: 7

AIM: Implementation of 4:1 multiplexer and 1:4 demultiplexer using logic gates (AND gate-7408, NOT gate-7404 and OR gate-7432) and verify their truth table.

APPARATUS REQUIRED: OR gate IC 7432, AND gate IC 7408, Connecting wires, Power supply, Bread board etc.

THEORY:

A **multiplexer (MUX)** is a device that accepts data from one of many input sources for transmission over a common shared line. To achieve this MUX has several data lines and a single output along with data select inputs, which permit digital data on any of the inputs to be switched to the output line. The logic symbol for a 1 to 4 data selector/multiplexer is shown in figure.

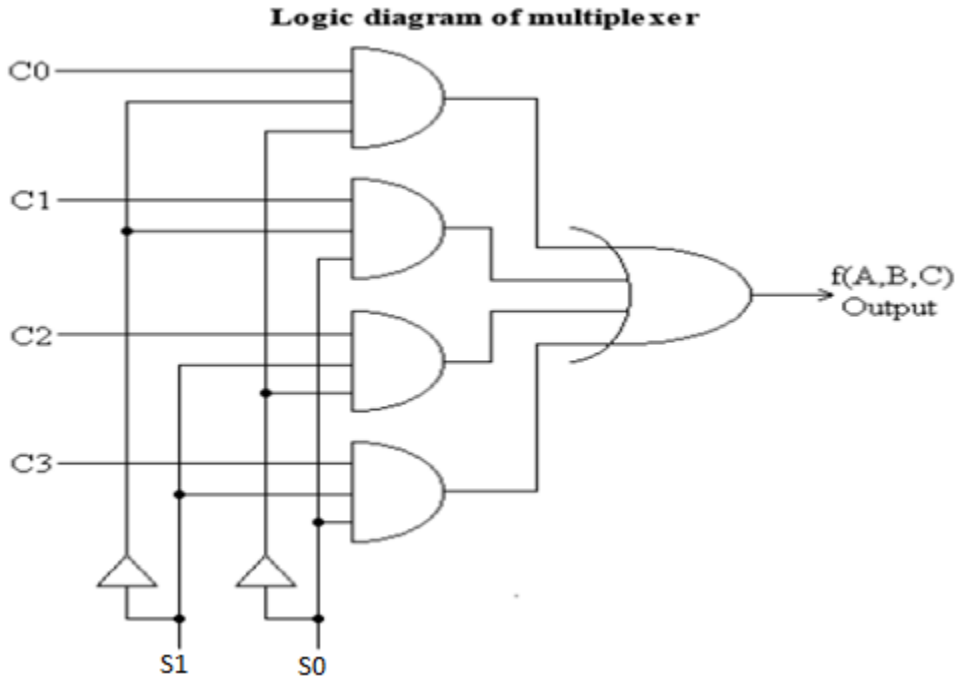


The selection lines decide the number of input lines of particular multiplexer. If the number of 'n' input lines is equal to **'2^m'**then 'm' select lines are required to select one of the **'n'**input line.

Note that if a binary zero appears on the data select lines then data on input line D_0 will appear on the output. Thus data output Y is equal to D_0 if and only if S_1=0 and S_0=0. Y= D_0 S_1' S_0'.

Similarly the data output is equal to D_1, D_2 and D_3 for Y= D_1 S_1' S_0, Y= D_2 S_1 S_0' and Y= D_3 S_1 S_0 respectively. Thus the total multiplexer logic expression formed from ORing terms i.

The implementation of this equation is as shown in figure.



TRUTH TABLE		
DATA SELECT INPUT		**INPUT SELECTED**
S1	**S0**	
0	0	C0
0	1	C1
1	0	C2
1	1	C3

DEMULTIPLEXER: Demultiplexer means generally one into many. A demultiplexer is a logic circuit with one input and many outputs. By applying control signals, we can steer the input signal to one of the output lines. The circuit has one input signal ,m control signal and n output signals. Where 2^n=m. It functions as an electronic switch to route an incoming data signal to one of several output.

LOGIC DIAGRAM:

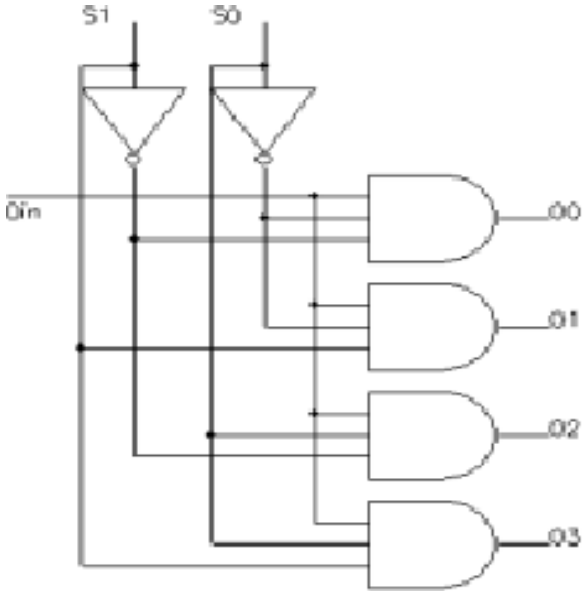


Fig: 1:4 Demultiplexer

PROCEDURE:

1. Connect the circuit as shown in figure.
2. Apply Vcc & ground signal to every IC.
3. Observe the input & output according to the truth table.

RESULT: The truth table of 4x1 multiplexer and 1X4 demultiplexer is verified.

PRECAUTIONS:

- All ICs should be checked before starting the experiment.
- All connections should be made neat and tight.
- Power supply and ICs should be handled with carefully.
- While making connections main supply should be kept switched off.
- Never touch live and naked wires.
- After completing the experiment switch off the power supply.

Viva-voice Questions:

Q1. What is de-multiplexer?

Ans. The de-multiplexer is the inverse of the multiplexer, in that it takes a single data input and n address inputs. It has 2^n outputs. The address input determines which data output is going to have the same value as the data input. The other data outputs will have the value 0.

Q2. What is the main difference between decoder and de-multiplexer?

Ans. In decoder we have n input lines as in de-multiplexer we have n select lines.

Q3. Why Binary is different from Gray code?

Ans. Gray code has a unique property that any two adjacent gray codes differ by only a single bit.

Q4. What is a multiplexer?

Ans . An multiplexer accepts two or more streams of data and combines them into one stream.

Q5. How many select lines will a 16x1 multiplexer will have?

Ans . 4

Q6. What is the function of enable input on a multiplexer chip?

Ans. :To activate the entire chip.

Q7. Why multiplexer is called as data selector?

Ans.: Because multiplexer selects one of several input signals and directs to the output.

Q8. Give the applications of multiplexer.

Ans.: Multiplexer are used in data routing, data selection, parallel to serial conversion and waveform generation.

EXPERIMENT NO - 8

AIM –Verification of truth tables of RS, JK, T and D flip-flops using NAND gate (7400) & NOR gates (7402).

APPARATUS REQUIRED: IC 7400, 7402 Digital Trainer & Connecting leads.

THEORY:

R S FLIP-FLOP: There are two inputs to the flip-flop defined as R and S. When I/Ps R=0 and S=0 then O/P remains unchanged. When I/Ps R=0 and S=1 the flip-flop is switches to the stable state where O/P is 1 i.e. SET. The I/P condition is R = 1 and S = 0 the flip-flop is switched to the stable state where O/P is 0 i.e. RESET. The I/P condition is R = 1 and S = 1 the flip-flop is switched to the stable state where O/P is forbidden.

J K FLIP-FLOP: For purpose of counting, the JK flip-flop is the ideal element to use. The variable J and K are called control I/Ps because they determine what the flip-flop does when a positive edge arrives. When J and K are both 0s , both AND gates are disabled and Q retains its last value.

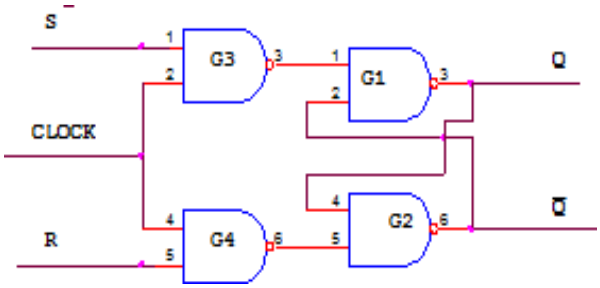
- **D**

  FLIP –FLOP: This kind of flip flop prevents the value of D from reaching the Q output until clock pulses occur. When the clock is low, both AND gates are disabled D can change value without affecting the value of Q. On the other hand, when the clock is high ,.In this case, Q is forced to equal the value of D. When the clock again goes low, Q retains or stores the last value of D. a D flip flop is a bi-stable circuit whose D input is transferred to the output after a clock pulse is received.

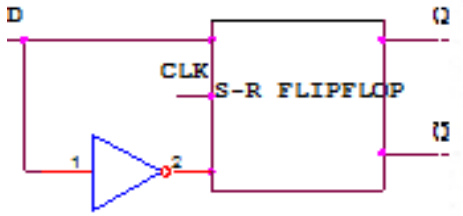
- **T**

  FLIP-FLOP: The T or "toggle" flip-flop changes its output on each clock edge, giving an output which is half the frequency of the signal to the T input. It is useful for constructing binary counters, frequency dividers, and general binary addition devices. It can be made from a J-K flip-flop by tying both of its inputs high.

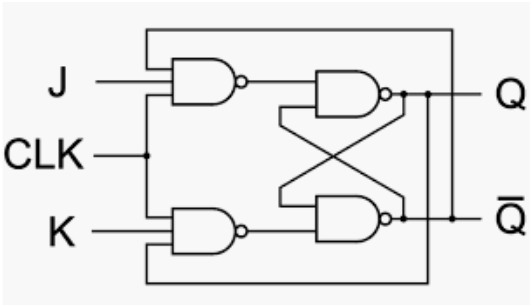
CIRCUIT DIAGRAM:



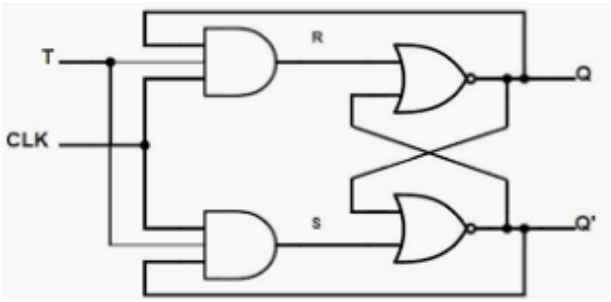
SRFlipFlop



D Flip Flop



JKFlipFlop



T Flip Flop

PROCEDURE:

1. Connect the circuit as shown infigure.
2. Apply Vcc& ground signal to every IC.
3. Observe the input & output according to the truthtable.

TRUTH TABLE:

SR FLIP FLOP:

CLOCK	S	R	Q_{n+1}
1	0	0	NO CHANGE
1	0	1	0
1	1	0	1
1	1	1	?

D FLIPFLOP:

D	Q_{n+1}
0	0
1	1

JK FLIPFLOP

CLOCK	J	K	Q_{n+1}
1	0	0	NO CHANGE
1	0	1	0
1	1	0	1
1	1	1	Qn’

T FLIPFLOP

CLOCK	T	Q_{n+1}
1	0	NO CHANGE
1	1	Qn’

RESULT: Truth table has been verified on digital trainer.

PRECAUTIONS:

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The V_{cc} and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Q1. Flip-Flop is stable or bistable.

Ans. Bistable.

Q2. What are the I/Ps of JK flip–flop where this race round condition occurs?

Ans. Both the inputs are 1.

Q3. When RS flip-flop is said to be in a SET state?

Ans. When the output is 1.

Q4. When RS flip-flop is said to be in a RESET state?

Ans. When the output is 0.

Q5.What is the truth table of JK flip-flop?

J	**K**	**Q_{n+1}**
0	0	Q_n
0	1	0
1	0	1
1	1	’ Q_n

EXPERIMENT NO -9

AIM: Design 4-bit synchronous and asynchronous counter using JK flip flops (7476) and AND gates (7408) and verify their truth table.

APPARATUS REQUIRED: Digital trainer kit and 4 JK flip flop each IC7 476(i.e dual JK flip flop) and two AND gates IC 7408.

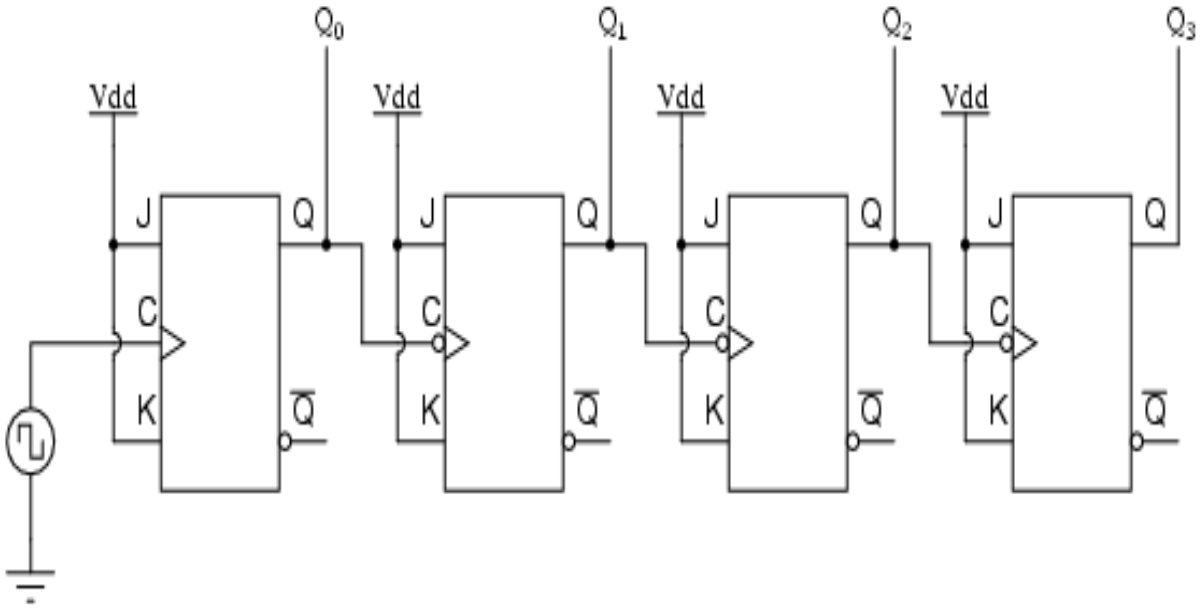
THEORY:

4-bit asynchronous counter:

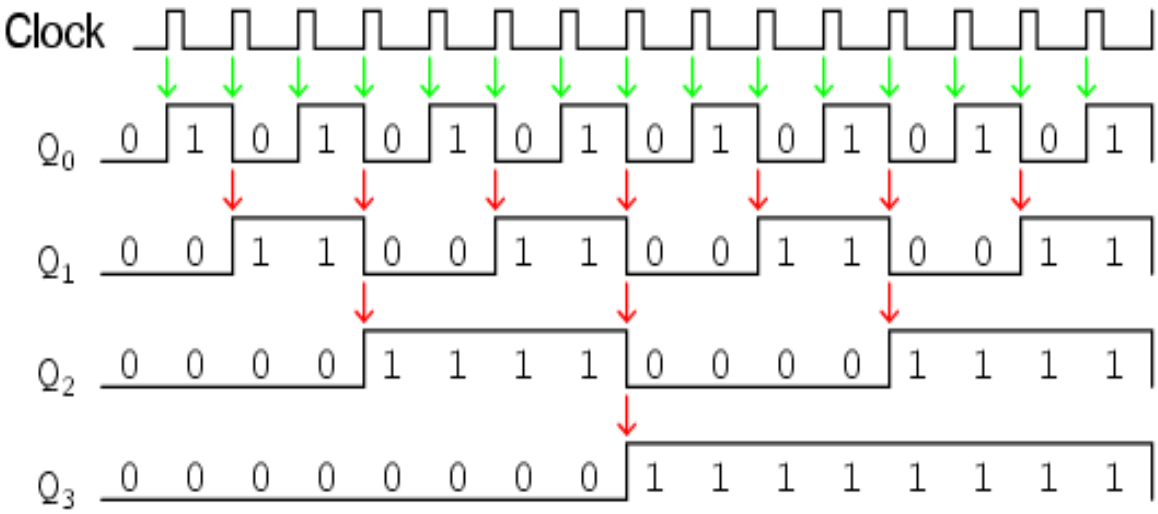
A counter is a sequential logic circuit that goes through a prescribed sequence of states upon the application of input pulses. The prescribed sequence can be a binary sequence or any other sequence. A counter that goes through 2N (N is the number of flip-flops in the series) states is called a binary counter. The modulus of a counter is the number of different states it is allowed to have. Counter modulus is normally 2N unless controlled by a feedback circuit which limits the number of possible states (an example being the decimal counter). Counters are very widely used in almost all computers and other digital electronic systems.

Counters arranged so that the output of one flip-flop generates the clock input of the next higher stage are generally called asynchronous counters (or ripple counter). In other words, in asynchronous counters, the CLK inputs of all flip-flops (except the first one) are triggered not by the incoming pulses but rather by the transition that occurs in other flip-flops. Therefore, the change of state of a particular flip-flop is dependent upon the present state of other flip-flops. Fig. 1 shows a count-up ripple counter. When a transition from, say, 0111 to 1000 occurs, the one-to-zero transition of the low-order three bits ripples from bit to bit.

A four-bit "up" counter



Waveform of 4 bit Asynchronous counter



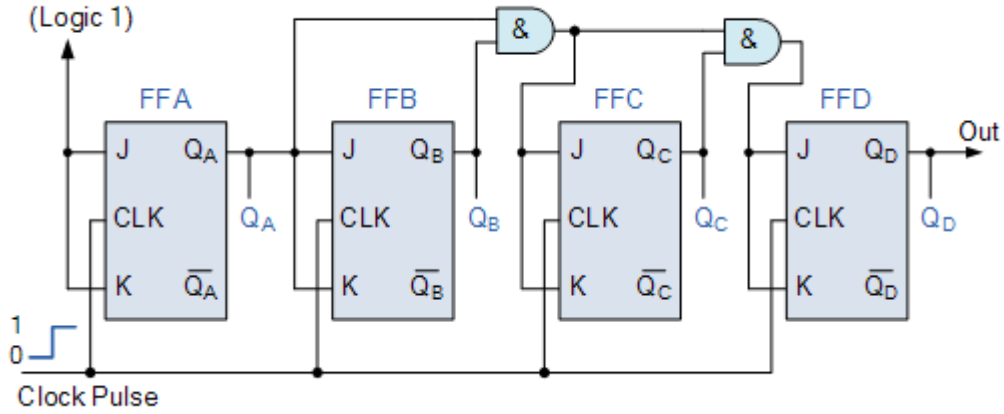
State table of 4 bit Asynchronous counter

State	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
0	0	0	0	0

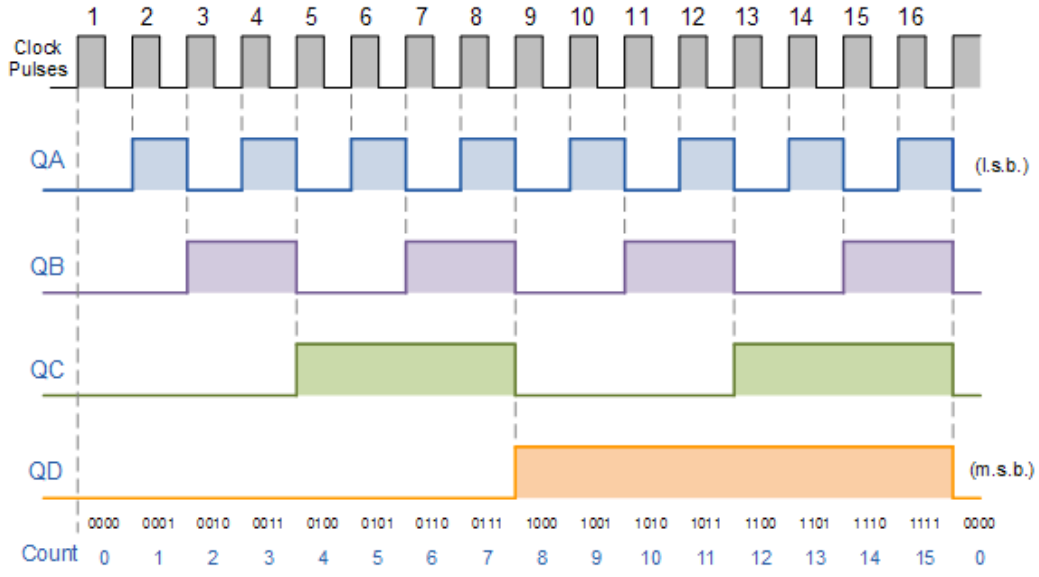
4-BIT SYNCHRONOUS COUNTER:

Synchronous generally refers to something which is coordinated with others based on time. Synchronous signals occur at same clock rate and all the clocks follow the same reference clock.

In asynchronous Counter, we have seen that the output of that counter is directly connected to the input of next subsequent counter and making a chain system, and due to this chain system propagation delay appears during counting stage and create counting delays. In synchronous counter, the clock input across all the flip-flops use the same source and create the same clock signal at the same time. So, a counter which is using the same clock signal from the same source at the same time is called Synchronous counter.



In the above image, the basic Synchronous counter design is shown which is Synchronous up counter. A 4-bit Synchronous up counter start to count from 0 (0000 in binary) and increment or count upwards to 15 (1111 in binary) and then start new counting cycle by getting reset. Its operating frequency is much higher than the same range Asynchronous counter. Also, there is no propagation delay in the synchronous counter just because all flip-flops or counter stage is in parallel clock source and the clock triggers all counters at the same time.



PROCEDURE:

i) Connections are given as per circuit diagram.

ii) Logical inputs are given as per circuit diagram.

iii) Observe the output and verify the truth table.

RESULTS: Asynchronous and synchronous counter is verified

PRECAUTIONS:

i) All the connections should be made properly.

ii) IC should not be reserved.

Quiz Questions with answer.

Q.1 What do you understand by counter?

Ans. Counter is a register which counts the sequence in binary form.

Q.2 What is asynchronous counter?

Ans. Clock input is applied to LSB FF. The output of first FF is connected as clock to next FF.

Q.3 What is synchronous counter?

Ans. Where Clock input is common to all FF.

Q.4 Which flip flop is used in asynchronous counter?

Ans. All Flip-Flops are toggling FF.

Q-5. What do you understand by modulus?

Ans. The total no.of states in counter is called as modulus .If counter is modulus-n, then it has n different states.

Q-6 How many flip-flops are required to make a MOD-32 binary counter?

Ans .5.

Q-7 The terminal count of a modulus-11 binary counter is_____.

Ans. 1010.

Q-8. Synchronous counters eliminate the delay problems encountered with asynchronous counters because the:

Ans. Input clock pulses are applied simultaneously to each stage.

Q9. Synchronous construction reduces the delay time of a counter to the delay of:

Ans. A single flip-flop and agate.

Q10. What is the difference between a 7490 and a 7492?

Ans. 7490 is a MOD-10, 7492 is a MOD-12.

EXPERIMENT NO -10

AIM: Design a mini project using real time digital integrated circuits and other components.
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**This has to be done by students, they can select project of their interest for mini project*