Noida Institute of Engineering and Technology, Greater Noida

Memory & Programmable Logic Devices

Unit: 5

DIGITAL LOGIC & CIRCUIT DESIGN

SUBJECT CODE: ACSE0304

B Tech 3rd Semester

Ms. Nidhi Sharma
Assistant Professor

Department of Electronics and Communication Engineering

Brief Introduction

Mr. Ms. Nidhi Sharma

Ms. Nidhi Sharma

- PhD Amity University, Pursuing
- M.Tech AKTU, Lucknow, India
- B.Tech. Kurukshetra University, Kkr. , Haryana

Research Interests

VLSI Design, Communication System, Internet of Things.

Industrial Experiance: (2.5 Years)

Academic Experience: (17+ years)

Publication : 08 (Peer Reviewed journals), 05(International Conference), 01 National conference.

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

Evaluation Scheme

Sl. No.	Subject Codes	Subject Name	Periods			Evaluation Schemes				End Semester		Total	Credit
			L	T	P	CT	TA	TOTAL	PS	TE	PE		
WEEKS COMPULSORY INDUCTION PROGRAM													
1	AAS0301A	Engineering Mathematics-III	3	1	0	30	20	50		100		150	4
2	ACSE0306	Discrete Structures	3	0	0	30	20	50		100		150	3
3	ACSE0304	Digital Logic & Circuit Design	3	0	0	30	20	50		100		150	3
4	ACSE0301	Data Structures	3	1	0	30	20	50		100		150	4
5	ACS0301	Introduction to Cloud Computing	3	0	0	30	20	50		100		150	3
6	ACSE0305	Computer Organization and Architecture	3	0	0	30	20	50		100		150	3
7	ACSE0354	Digital Logic & Circuit Design Lab	0	0	2				25		25	50	1
8	ACSE0351	Data Structures Lab	0	0	2				25		25	50	1
9	ACS0351	Cloud Computing lab	0	0	2				25		25	50	1
10	ACSE0359	Internship Assessment-I	0	0	2				50			50	1
11	ANC0301/ ANC0302	Cyber Security*/ Environmental Science*(Non Credit)	2	0	0	30	20	50		50		100	0
12		MOOCs (For B.Tech. Hons. Degree)											
		GRAND TOTAL										**1100**	**24**

Course Contents / Syllabus

UNIT-I: Digital System and Binary Numbers: Number System and its arithmetic, Signed binary numbers, Binary codes, Cyclic codes, Hamming Code, Simplification of Boolean Expression: K-map method up to five variable, SOP and POS Simplification Don't Care Conditions, NAND and NOR implementation, Quine Mc-Clusky Method (Tabular Method).

UNIT II : Combinational Logic: Combinational Circuits: Analysis Procedure, Design Procedure, Code Converter, Binary Adder-Subtractor, Decimal Adder, Binary Multiplier, Magnitude Comparator, Decoders, Encoders Multiplexers, Demultiplexers.

UNIT III: Sequential Logic and Its Applications: Storage elements: Latches & Flip Flops, Characteristic Equations of Flip Flops, Excitation Table of Flip Flops, Flip Flop Conversion, Registers, Shift Registers, Ripple Counters, Synchronous Counters, Other Counters: Johnson & Ring Counter.

UNIT IV: Synchronous & Asynchronous Sequential Circuits: Analysis of clocked Sequential Circuits with State Machine Designing, State Reduction and Assignments, Design Procedure. Analysis procedure of Asynchronous Sequential Circuits, Circuit with Latches, Design Procedure, Reduction of State and flow Table, Race-free State Assignment, Hazards.

UNIT-V: Memory & Programmable Logic Devices: Basic concepts and hierarchy of Memory, Memory Decoding, RAM: SRAM, DRAM, ROM: PROM, EPROM, Auxiliary Memories, PLDs: PLA, PAL; Circuit Implementation using ROM, PLA and PAL; CPLD and FPGA..

Branch wise Application

- RAM is utilized in the computer as a scratchpad, buffer, and main memory.
- It offers a fast operating speed.
- It is also popular for its compatibility
- It offers low power dissipation
- ROM is used to store data.
- ROM is used to store firmware software.
- ROM is also used to update the firmware software of the computer.
- ROM is also used in electronic devices such as keypad mobile phones, children's handheld games, VCRs, DVDs, and digital watches.
- ROM is also used in home appliances such as smart televisions, washing machines, microwaves, induction stoves, and TV remotes.
- Rom is also used in the automobile industry such as digital speed meters.
- ROM is used in many electronic devices such as monitors, keyboards, mouse, printers, scanners, plotters, calculators, and fax machines

Course Objective

Course Objective: The student will be able to learn about
To Apply concepts of Digital Binary System and implementation of Gates
To Analyze and design of Combinational logic circuits
To Analyze and design of Sequential logic circuits with their applications
To Implement the Design procedure of Synchronous & Asynchronous Sequential Circuits
To Apply the concept of Programmable Logic devices with circuit implementation

Course outcomes

Course Outcomes: At the end of this course students will able to:	
CO1	Apply concepts of Digital Binary System and implementation of Gates
CO2	Design and analyze combinational circuits with MUX / DEMUX, Decoder & Encoder
CO3	Design and analyze of Sequential logic circuits with their applications
CO4	Implement the Design procedure of Synchronous & Asynchronous Sequential Circuits
CO5	Apply the concept of Programmable Logic devices with circuit implementation

Program Outcomes

S. No.	Description
1.	**Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization for the solution of complex engineering problems.
2.	**Problem analysis:** Identify, formulate, research literature, and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3.	**Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for public health and safety, and cultural, societal, and environmental considerations.
4.	**Conduct investigations of complex problems:** Use research based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of information to provide valid conclusions.
5.	**Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools, including prediction and modeling to complex engineering activities, with an understanding of the limitations.

Program Outcomes

	Description
	6.The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice. **7. Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development. **8. Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice. **9. Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings. **10. Communication:** Communicate effectively on complex engineering activities with the engineering community and with the society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions. **11. Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments. **12. Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

COs-POs Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	-	-	-	-	-	-	-	-	-	2
CO2	3	3	2	-	-	-	-	-	-	-	-	2
CO3	2	3	2	2	-	-	-	-	-	-	-	2
CO4	3	3	3	2	-	-	-	-	-	-	-	2
CO5	3	2	1	-	-	-	-	-	-	-	-	2
AVERAGE	2.8	2.6	2	2	-	-	-	-	-	-	-	2

PSOs

On successful completion of graduation degree the Electronics and Communication, graduates will be able to:

1. **Engineering knowledge:** Apply the knowledge of mathematics, science and electronics & communication engineering to work effectively in the industry based on same or related area.
2. **Design/development of solutions:** Use their skills to work in modern electronics & communication engineering tolls, software and equipment's to design solutions for complex problems in the related field that meet the specified needs of the society.
3. **Individual and team work:** Function effectively as an individual and as a member or leader of a team by qualifying through examinations like GATE, IES, PSUs, TOEFL, GMAT and GRE etc.

COs-PSOs Mapping

CO	PSO1	PSO2	PSO3
CO1	3	3	3
CO2	3	3	2
CO3	3	3	-
CO4	3	3	-
CO5	3	3	-

PEOs

Program Education Objectives

The Program Educational Objectives (PEOs) of B.Tech (ECE) program are as follows:

PEO-1 To have excellent scientific and engineering breadth so as to comprehend, analyze, design and solve real- life problems using state-of-the-art technology.

PEO-2 To lead a successful career in industries or to pursue higher studies or to understand entrepreneurial endeavors.

PEO-3 To effectively bridge the gap between industry and academics through effective communication skill, professional attitude and a desire to learn.

Result analysis

Not Applicable

Question Paper Template

Printed page: .... Subject Code: .....

Roll No: | | | | | | | | | | | | |

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

B.Tech/B.Voc./MBA/MCA/M.Tech (Integrated)

(SEM:.... SESSIONAL EXAMINATION –I)(2021-2022)

Subject Name: .....

Time: 1.15Hours Max. Marks:30

General Instructions:

- All questions are compulsory. Answers should be brief and to the point.
- This Question paper consists of .....pages & ...5 .....questions.
- It comprises of three Sections, A, B, and C. You are to attempt all the sections.
- Section A Question No. 1 is objective type questions carrying 1 mark each, Question No. 2 is very short ~~answer~~ type carrying 2 mark each. You are expected to answer them as directed.
- Section B Question No.3 is Short answer type questions carrying 5 marks each. You need to attempt ~~any~~ two out of three questions given.
- Section C Question No. 4 &5are Long answer type (within unit choice) questions carrying 6marks each. You need to attempt any one part a or b.
- Students are instructed to cross the blank sheets before handing over the answer sheet to the invigilator.
- No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.

		SECTION – A	[5]	
1.	**Attempt all parts**		(4×1=4)	CO
	a.		(1)	
	b.		(1)	
	c.		(1)	
	d.		(1)	
2.	**Attempt all parts**		(2×2=4)	CO
	a.		(2)	
	b.		(2)	
		SECTION – B		
3.	**Answer any two of the following-**		[2×5=10]	CO
	a.		(5)	
	b.		(5)	
	c.		(5)	

Page 1 of 2

		SECTION – C		
4	**Answer any one of the following-(Any one can be applicative if applicable)**		[2×6=12]	CO
	a.	**Question-**	(6)	
	b.	**Question-**	(6)	
5.	**Answer any one of the following-**			
	a.		(6)	
	b.		(6)	

Page 2 of 2

Prerequisite and Recap

- Basic knowledge of logic gates.
- Basic Knowledge of flip-flops.
- Basic knowledge of combinational circuits.
- Basic knowledge of Sequential circuits.

Brief introduction about the subject with videos

- This course is intended to provide the students with a comprehensive understanding of the fundamental of digital logic circuit. The design of circuits and systems whose input and outputs are represented as discrete variables. These variables are commonly binary i.e.., two states in nature. Design at the circuit level is usually done with truth table and state tables. Students will be able to analyze design and implement combinational and sequential circuits.

https://www.youtube.com/watch?v=BoIOLczVulQ&list=PLyqSpQzTE6M_dZdF7Bd-UncI5_L_1VkXF

https://www.youtube.com/watch?v=oNh6V91zdPY&list=PLbRMhDVUMnge4gDT0vBWjCb3Lz0HnYKkX

https://www.youtube.com/watch?v=CeD2L6KbtVM&list=PL803563859BF7ED8C

Unit 5 Content

Memory & Programmable Logic Devices: Basic concepts and hierarchy of Memory, Memory Decoding, RAM: SRAM, DRAM, ROM: PROM, EPROM, Auxiliary Memories, PLDs: PLA, PAL; Circuit Implementation using ROM, PLA and PAL; CPLD and FPGA.

Unit 5 Objective

• To Apply the concept of Programmable Logic devices with circuit implementation.

Topic Objective/Topic outcome

- **Topic**: Basic concepts and hierarchy of Memory

- **CO Covered :** CO5

- **Topic Objective :** The objective of Basic concepts and hierarchy of Memory is to understand the basic elements of memory, its working principle and its hierarchy.

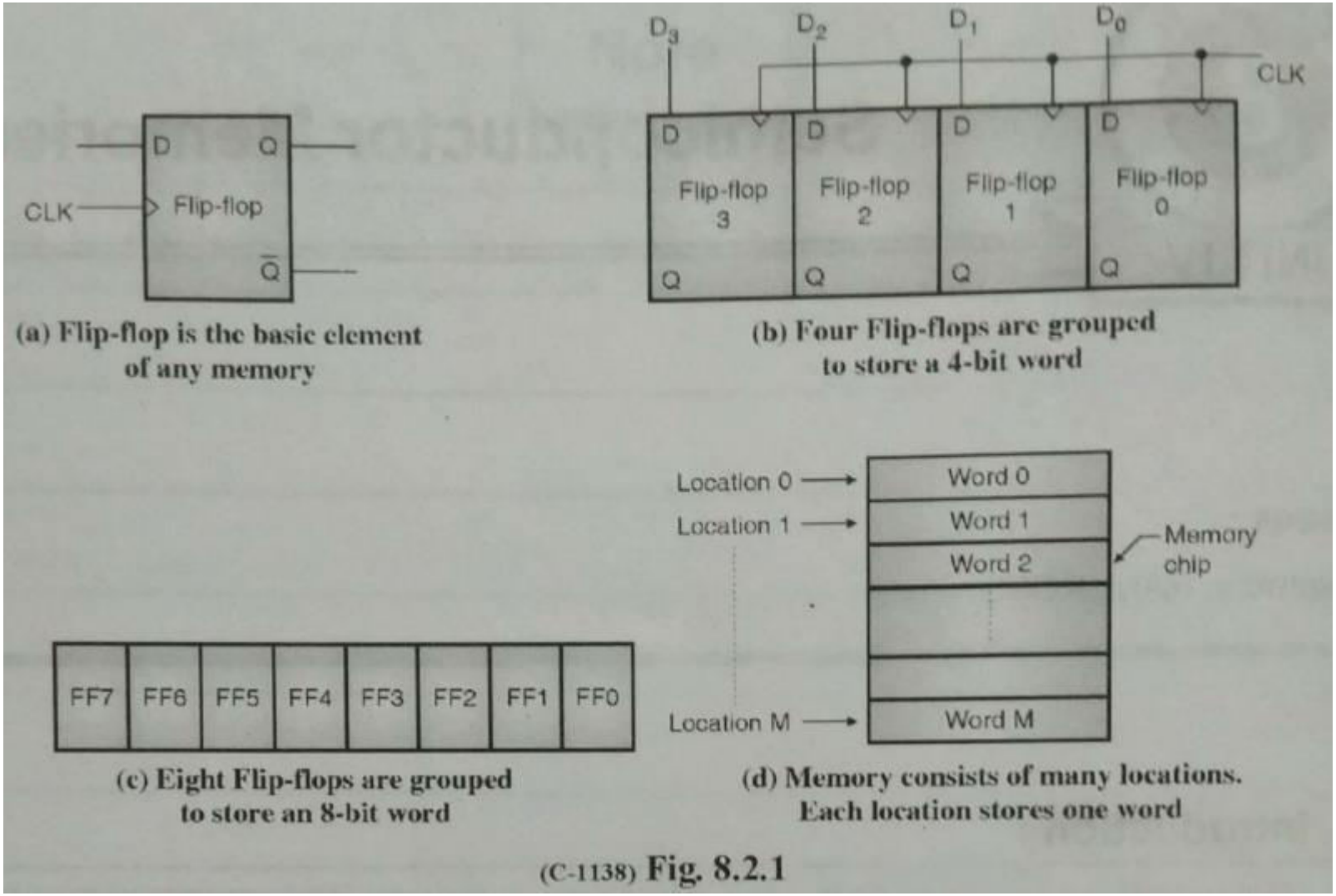
- **Topic outcome:** At the end of the course, the student will be able to understand about memory basic concepts and its hierarchy.

Memory

Memory: A memory unit is a device to which binary information is transferred for storage and from which information is retrieved when needed for processing.

- In digital electronic, memory is a semiconductor device used for digital data storage, such as computer memory, where data is stored memory cells on a silicon integrated circuit memory chip. There are different types of memories using different semiconductor technologies.
- All memory structures have an address bus and a data bus.
- Advantages of semiconductor memories :
  - Small size
  - High speed
  - Better reliability
  - Low cost
  - Ease of expansion of memory size
- Flip flop is equivalent to a single bit memory cell. So the basic element of a semiconductor memory is a flip-flop. Each flip-flop is capable of storing one binary bit i.e. 0 or 1 only.

Memory



(a) Flip-flop is the basic element of any memory

(b) Four Flip-flops are grouped to store a 4-bit word

(c) Eight Flip-flops are grouped to store an 8-bit word

(d) Memory consists of many locations. Each location stores one word

(C-1138) **Fig. 8.2.1**

Memory

Memory size :

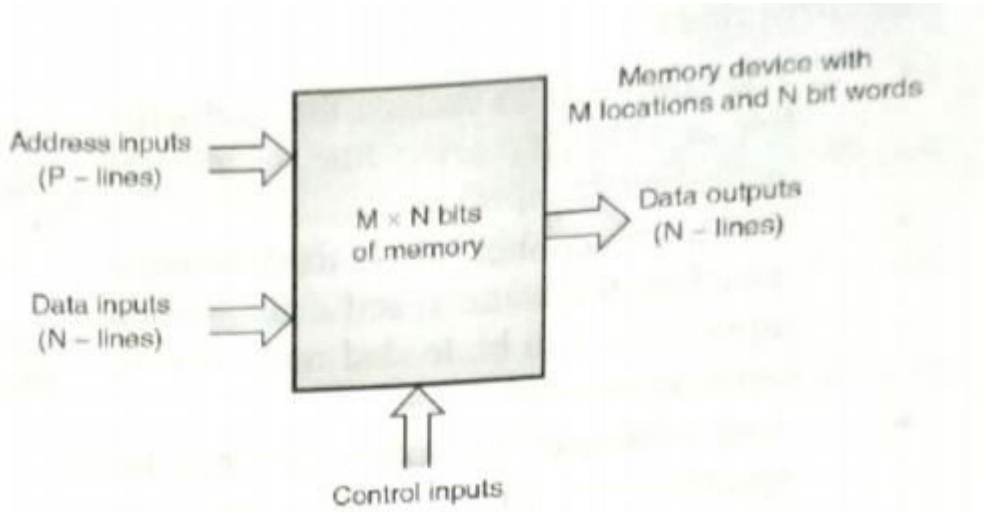
- The no of locations and numbers of bits per word will vary from memory to memory. For e.g if a memory chip is capable of storing M words with each word having N bits in it then the size of the memory will be M*N.
- The commonly used values of no of words per chip are 64,256,512,1024.
- Memories with higher no of words or large word size can be formed by cascading a no of chips of smaller size.
- There are three types of inputs to an M*N memory device
  - Address input line
  - Data input lines
  - Control inputs

Data inputs : There are N-number of data input lines. The data is stored is put on these lines word by word with each word N-bit long. Data inputs are also called as data bus.

Memory

Address inputs :

- There are "P" no of address input lines. These lines are used to specify the address of the required memory location for reading the already stored data or writing a new data.
- To access any one of the M possible locations, we need P address lines such that $2^P = M$.



(C-1139) **Fig. 8.2.2 : Block diagram of memory device**

Memory

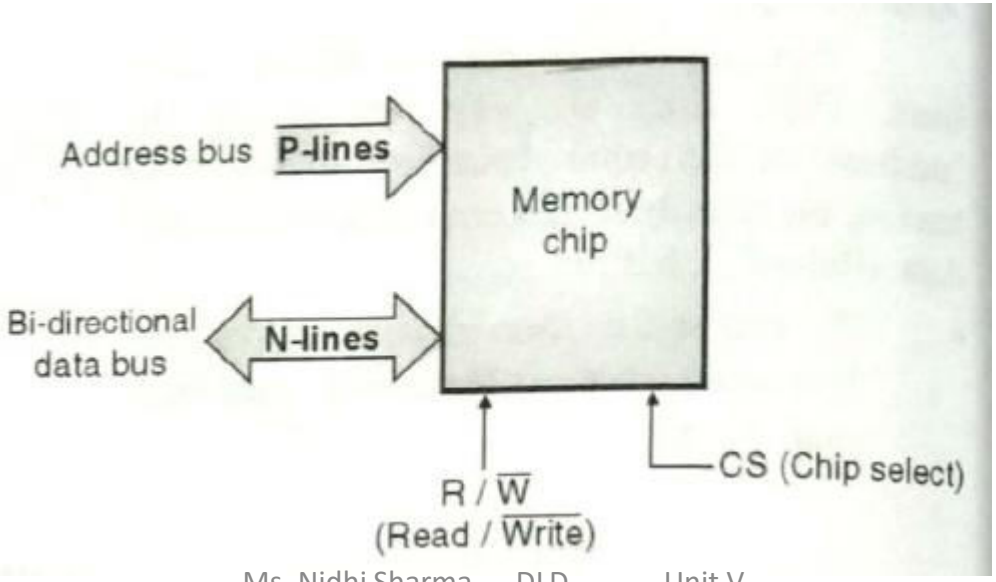
Data output lines :

- The data available in the selected memory location can be “read” on the data output lines.
- The no of data lines is N i.e. is equal to the no of bits per word. The output data lines are also called as output data bus.
- Input and output data buses are unidirectional. That means the data flows only in one direction.
- In most of the memory chips the same set of data lines is used for data input as well as data output.
- Such a data bus is called as bi-directional data bus and it is represented with arrows on both sides.

Memory

Control lines :

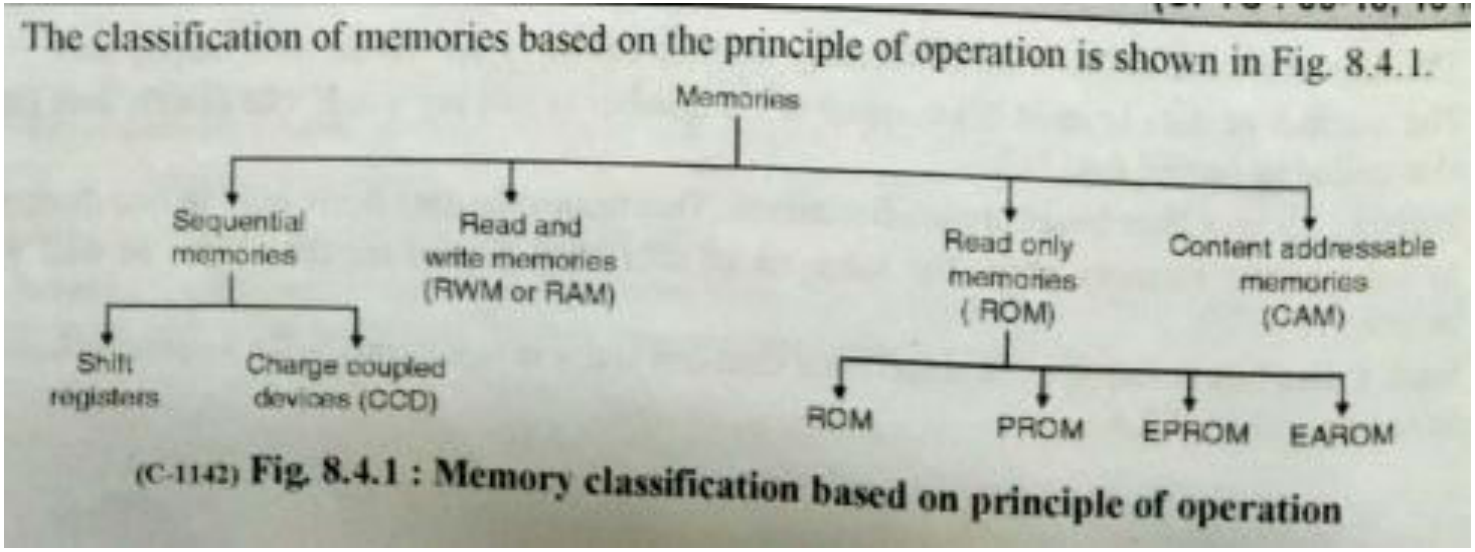
- The control lines include read/write line and the chip select line.
- The bi-directional bus is used as input data bus for some specific time when input data is to be loaded into memory (write operation)and it is used as output data bus for specific time when the stored data is to be read (read operation).
- With R/W = 1 ,the data bus acts as an output data bus and with R/W = 0, it acts as the input data bus.



Memory

Classification of memories.

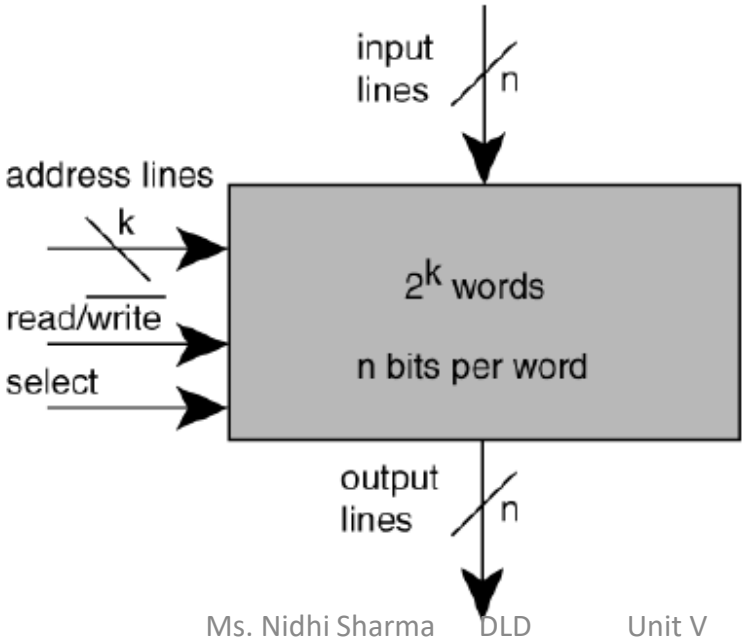
- The memory devices can be classified, on the basis of various parameters. The parameters used as basis of classification are as follows
  - Principle of operation
  - Physical characteristics (Volatile, Non-volatile)
  - Mode of access (Sequential, random)
  - Technology used for fabrication(BJT, MOS)



RAM

RAM (random access memory):

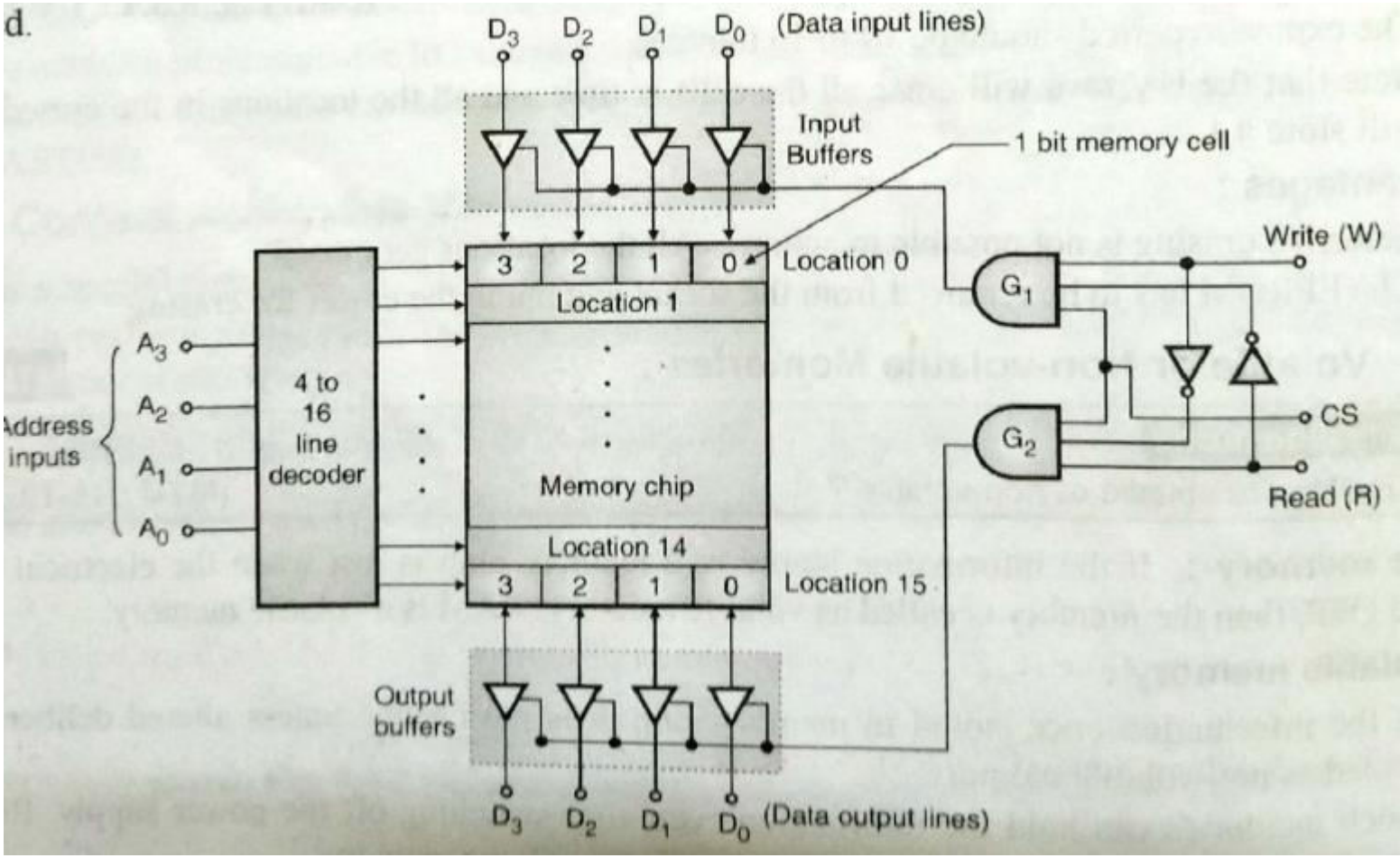
- It is a read/write memory which stores data until the machine is working. As soon as the machine is switched off, data is erased.
- RAM is volatile, i.e. data stored in it is lost when we switch off the computer or if there is a power failure. Hence, a backup Uninterruptible Power System (UPS) is often used with computers.



Cont…

Internal organization of RAM:

- The internal organization of 16 x 4 memory chip is given in figure.



Cont…

- 4 address lines to have 16 addresses. For this 4:16 decoder is used.
- There are 16 locations of storing a 4 bit word.
- K(kilo) is 2^{10} = 1024 , M(mega) is equal to 2^{20} and G(giga) is equal to 2^{30}
- Input/output buffers are connected between data input and memory & between memory and data output.
- Control logic consists of 2 NAND gates and 2 NOT gates. The inputs to this circuit are read, write and chip select.

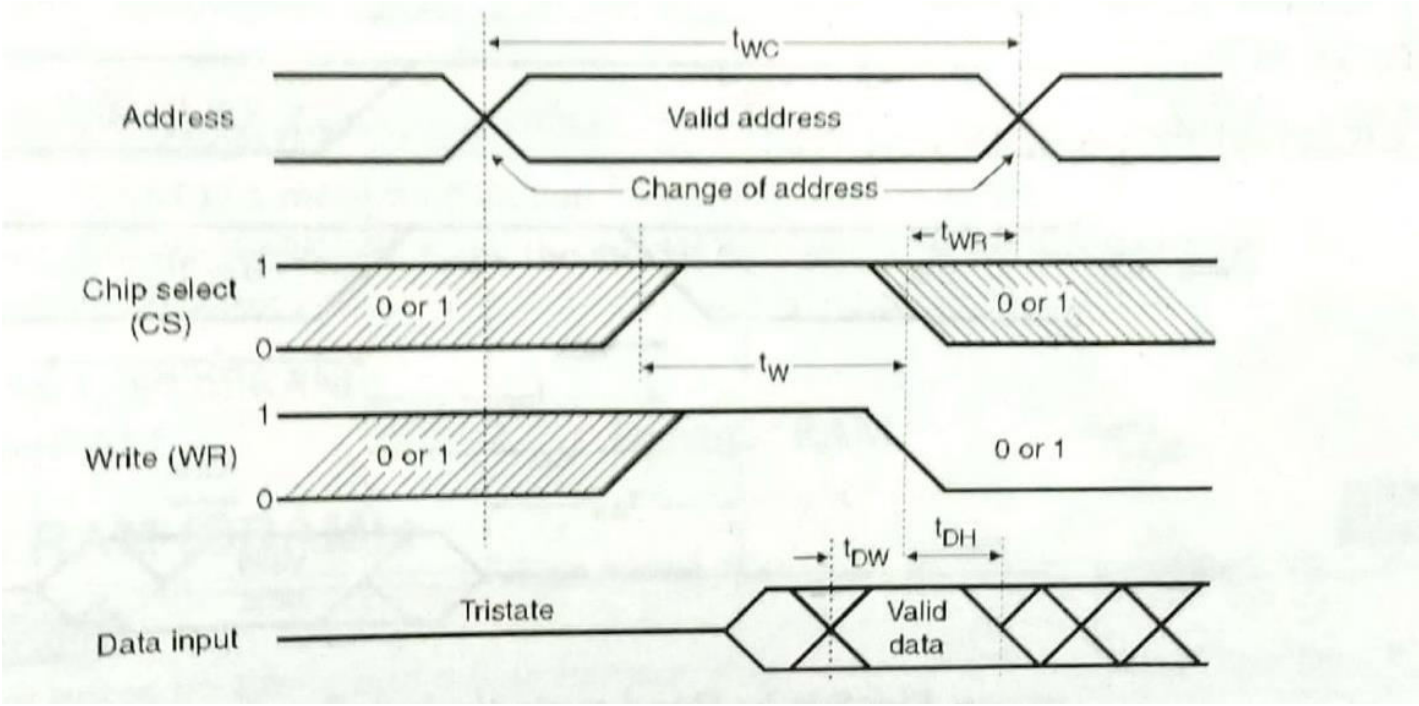
Write Operations:

- The sequence of events taking place for writing the desired data (1001) at the desired memory location (0110) is as follows:
- Adjust $A_3\,A_2\,A_1\,A_0$ = 0110 and $D_3\,D_2\,D_1\,D_0$ = 1001
- Make CS =1, W =1 and R = 0. This will enable G_1 and disable G_2
- Hence input buffers are enabled and output buffers are disabled and this will load 1001 to 0110 location.

Cont…

- The output buffer is disabled so no data is available at data output.
- Data which is originally present at the selected memory location is cleared off first and then data present at the data input will replace it.

Timing diagram of Write Cycle:



Cont…

Important definitions:

- Write Cycle time (t_{wc}) : Minimum amount of time for which the valid address must be present for writing data in the memory.
- Write Pulse time (t_w) : Minimum length of write pulse.
- Write Release time (t_{WR}) : Minimum amount of time for which address must be valid after write pulse ends.
- Data hold up time (t_{DH}) : Minimum amount of time for which data must be valid after write pulse ends.
- Data set up time (t_{DW}) : Minimum amount of time for which data must be valid before write pulse ends.

Cont…

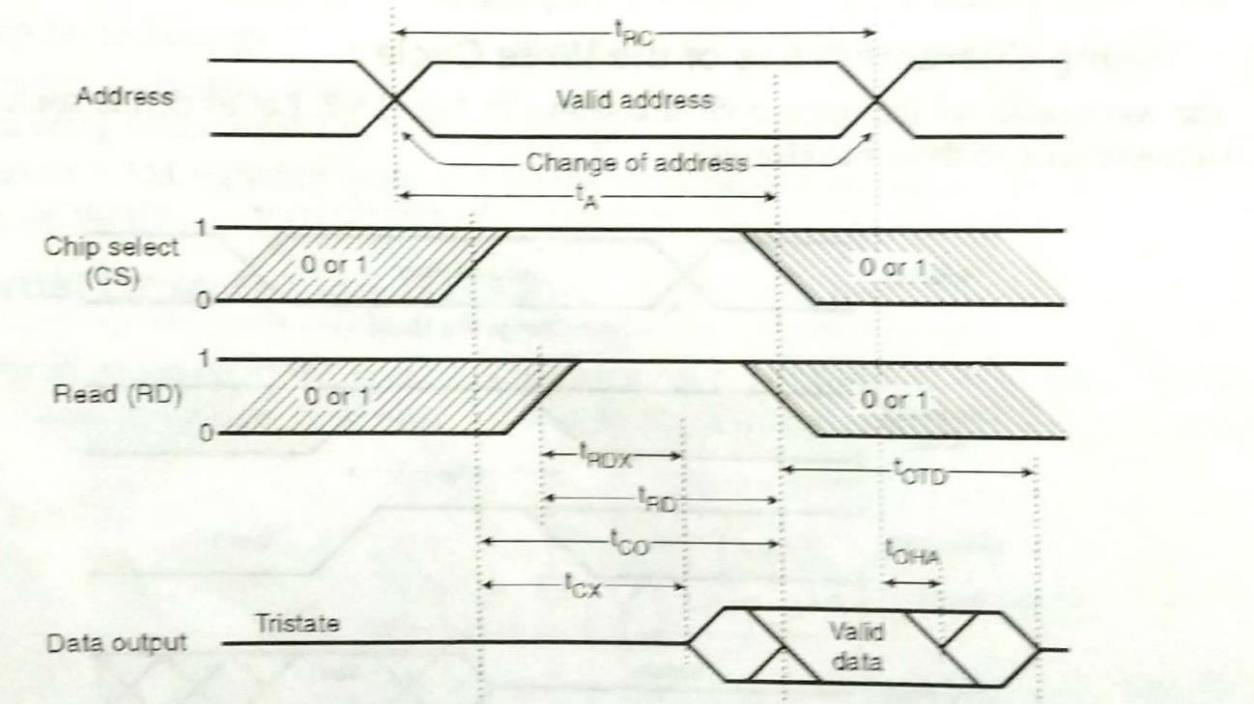
Read Operations:

- Read operation is essential for reading the contents of a selected memory location.
- For read operation Cs =1, R=1 and W=0.
- This will enable G_2 and disable G_1.
- Hence input buffers are disabled and output buffers are enabled.
- This enabled buffer will make the data of selected location available on the output lines.

Cont…

Timing Characteristics of Read Cycle:

- Apply chip select.
- Address of the memory location is applied to the address line.
- Now apply R = 1 and W=0



Cont…

Important definitions:

- Read Cycle time (t_{RC}) : Minimum amount of time valid address should be present for reading.
- Access time (t_x) : Minimum time gap between the instant valid address present on address line and the instant valid data present at the output.
- Read to output valid time (t_{RD}) : Maximum time delay between the begging of read pulse and availability of valid data on data bus.
- Read to output active time (t_{RDX}): Maximum time delay between the begging of read pulse and the output buffers coming to active state.
- Chip Select to output valid time (t_{RD}) : Maximum time delay between the begging of chip select pulse and availability of valid data on data bus.
- Chip Select to output active time (t_{RDX}): Maximum time delay between the begging of Chip select pulse and the output buffers coming to active state.
- Output Tristate from read (t_{OTD}): Maximum time delay between the end of Read pulse and output buffers going to High-z state.

Cont…

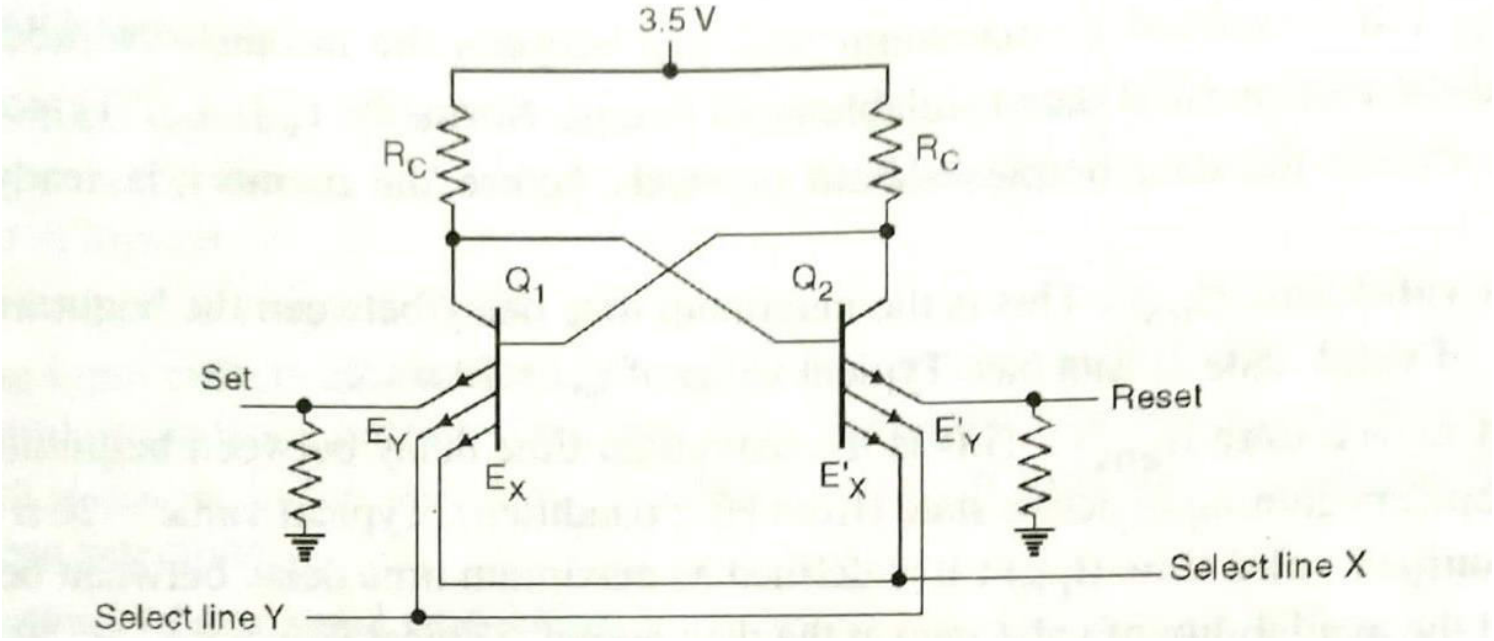
Types of RAM:

- SRAM
- DRAM

SRAM (static Random Access Memory):

- Formed from cross coupled inverters working as latch.
- Here Latch will store information as long as power supplied.
- Inherently synchronous.
- Fast , 12 ns access time.
- Fast, 4 ns access time in ECL from Cypress

SRAM



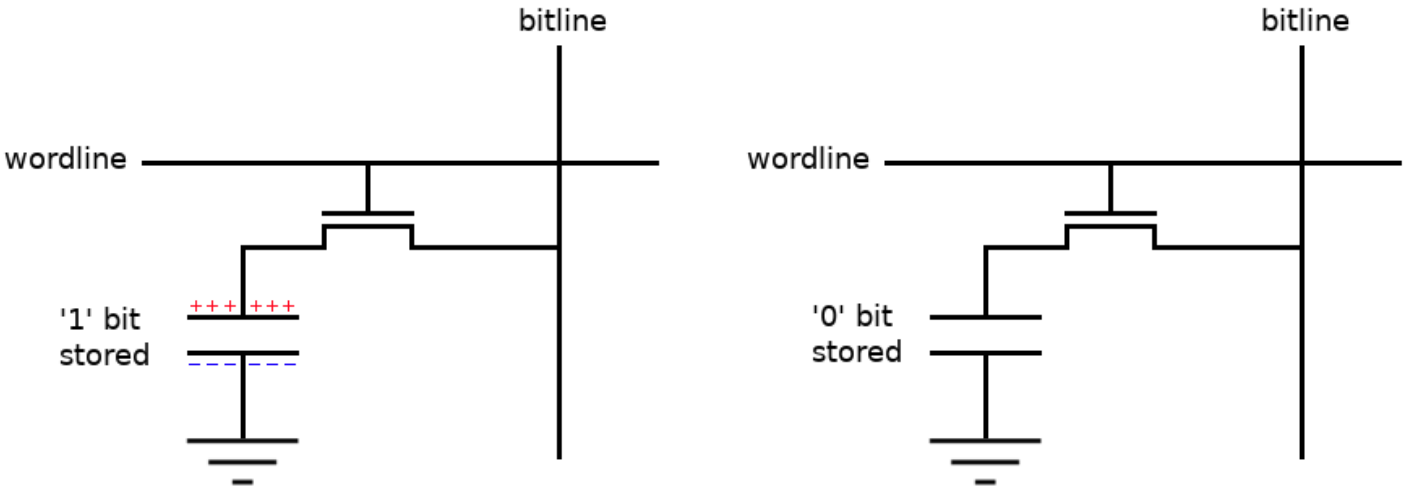
Operation of SRAM:

- Q_1 and Q_2 are cross couples inverters.
- '1' is said to be stored if Q_2 is OFF and Q_1 is ON.
- '0' is said to be stored if Q_1 is OFF and Q_2 is ON.
- Here transistors act as switches.
- A large number of such cells are connected in the matrix to form a memory chip.

DRAM

DRAM (dynamic):

- Data is Stored in the form of charge on a capacitor gated by a transistor
- High packing density, large cheap memory,
- Cheap + economies of scale = very cheap. Commodity item.
- Faster than hard disk, 70 ns.
- It is used in main memory



Cont…

Operation of DRAM:

• When Both bit line and word lines are high, MOSFET acts as closed switch and charges the capacitor.

• When Both bit line and word lines are low, MOSFET turns off and the capacitor retain its charge.

Parameter	SRAM	DRAM
Full Form	Static Random Access Memory	Dynamic Random Access Memory
Read & Write speed	Faster	Slower than SRAM
Storage component	Uses transistor to store single bit of information	Uses separate capacitor to store each bit of data
Price	Expensive than DRAM	Economical than SRAM
Power consumption	More	Less
Refresh	No need to refresh for maintaining data	Needs to be refreshed thousands of time every second
Used in	Cache memory	Main memory
Internal structure	Complex	Simpler than SRAM
Density	Less dense	Highly dense
Storage per bit	Can store many bits per chip	Cannot store many bits per chip

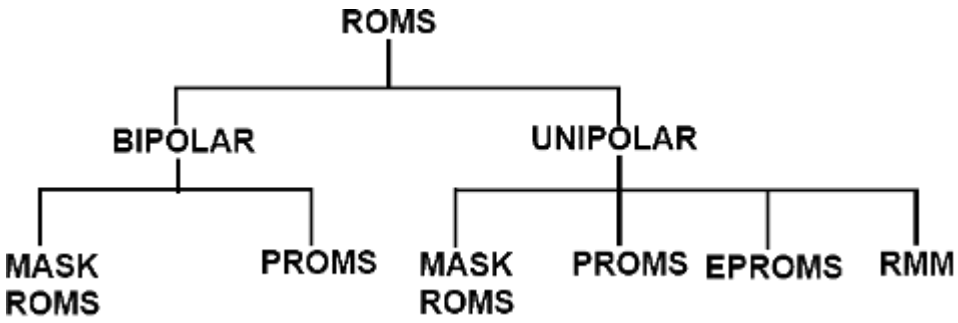
Memory

- **ROM: Read-only memory (ROM):** ROM is a class of storage medium used in computers and other electronic devices. Data stored in ROM cannot be modified, or can be modified only slowly or with difficulty.
- Programmable Read Only Memories (PROM) have fixed AND array with 2N outputs implementing all N-literal minterms.
- ROM holds programs and data permanently even when computer is switched off.
- Data can be read by the CPU in any order so ROM is also direct access.
- The contents of ROM are fixed at the time of manufacture.
- Stores a program called the bootstrap loader that helps start up the computer.
- Access time of between 10 and 50 nanoseconds.
- ROM has N input bits, 2N words by M bits, Implement M arbitrary functions of N variables.

ROM

ROM: Read-only memory (ROM) Manufacturing :

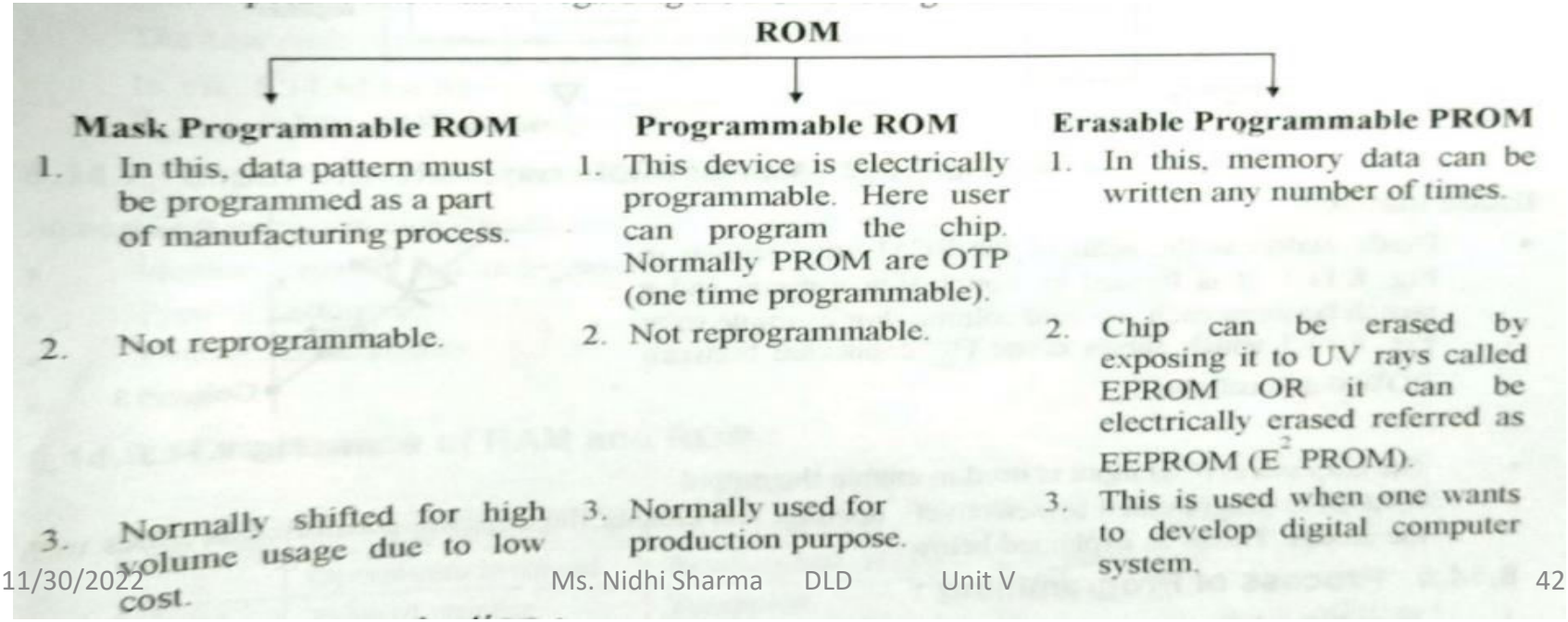
- The technologies used for Rom Manufacturing are :
  - Bipolar technology
  - MOS technology
- Bipolar ROMs are faster and they have higher driving capability whereas MOS ROMs require less area and consume less power. The improved MOS ROMs have improved speeds.



Cont…

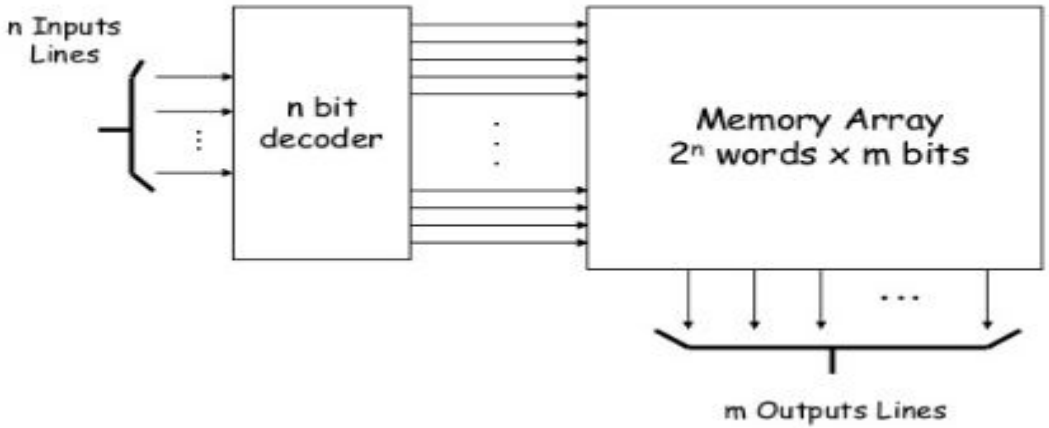
ROM programming :

- The process of entering information into ROM is called as ROM programming. The ROM can be classified based on the programming process as follows :
  - Mask programmable ROMs
  - Programmable ROMs
  - Erasable programmable ROMs



Cont…

ROM Internal Structure:



- **A Rom** is an array of selectively unidirectional contacts. The contacts can be open or closed selectively to program the required information into a ROM.
- A 16-bit ROM is shown in figure. It uses two 2-4 address decoders, 16 locations and 1 –data output.so this is a 16*1 ROM.

Cont…

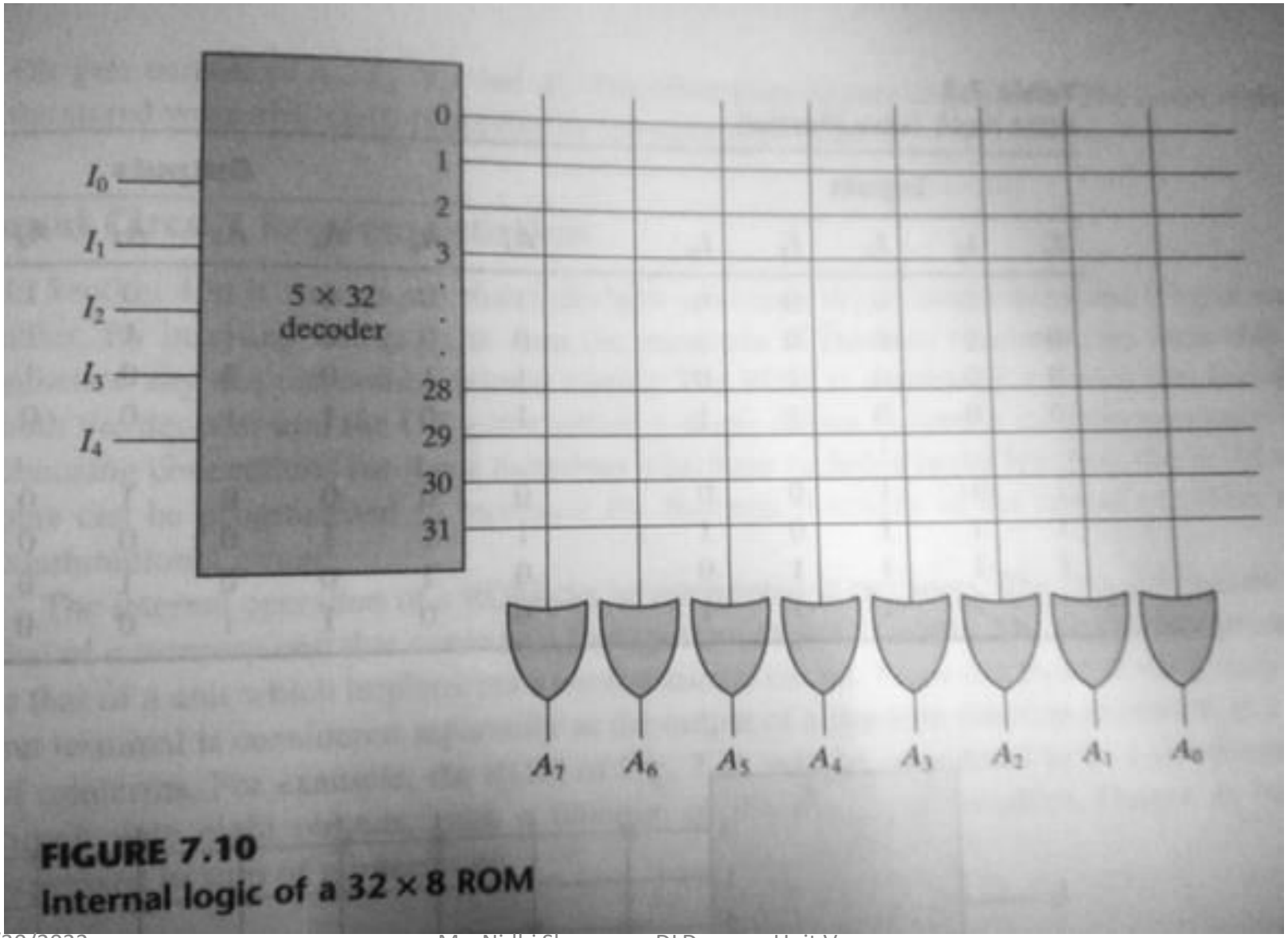
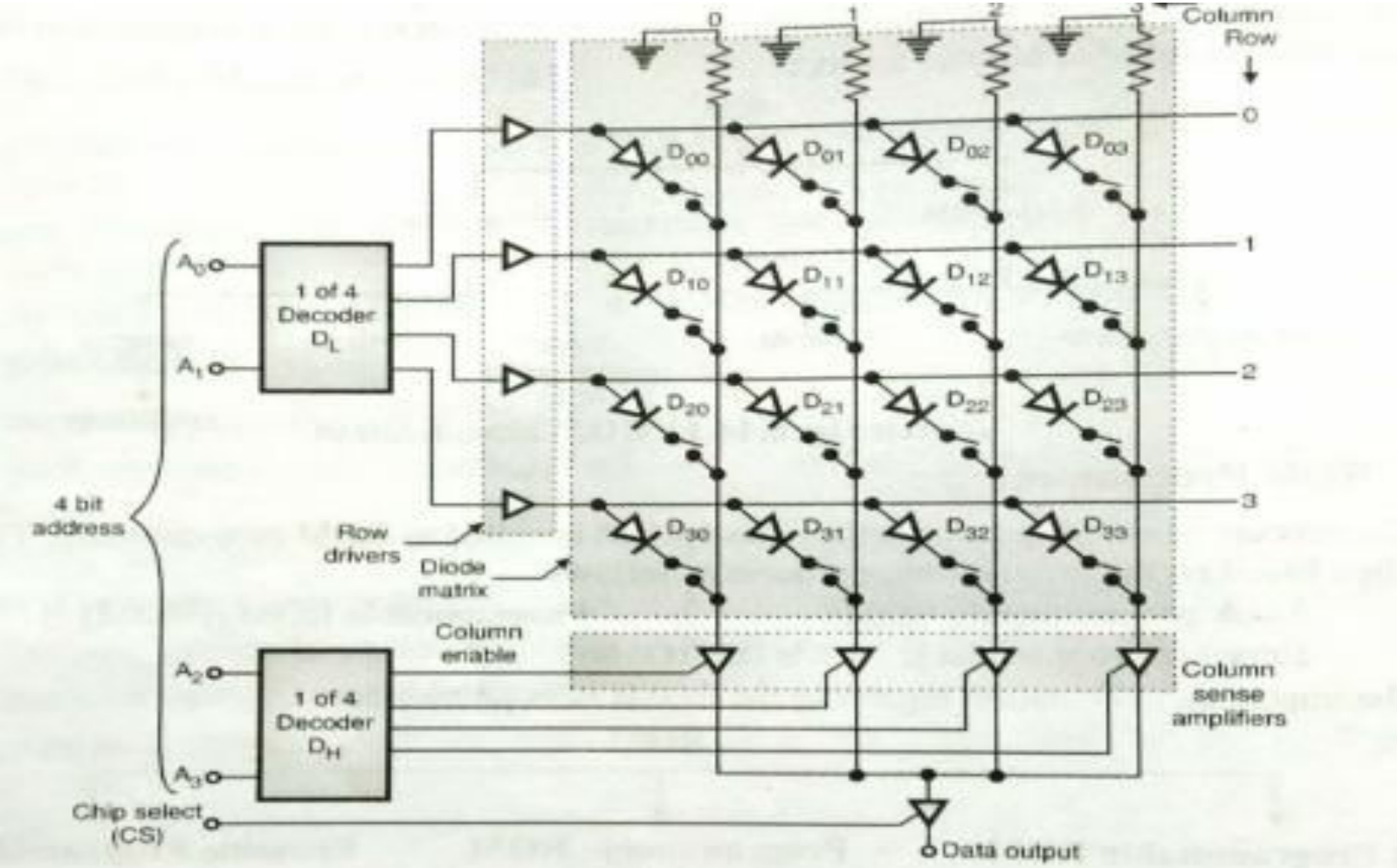


FIGURE 7.10
Internal logic of a 32 × 8 ROM

Cont…



(C-1145) **Fig. 8.14.2 : A 16-bit ROM array**

Cont…

- The method of addressing is called as two dimensional ,X-Y or coincident selection, addressing.
- A unidirectional switch is include at the junction of every row and column.
- The lower two address bits(A_1 , A_0) are decode by the decoder $D_{L.}$ The outputs of this decoder are used to select one out of the four rows.
- The high two address bits (A_1 , A_0) are decode by the decoder D_H . The four outputs of this decoder are used to select one out of four column sense amplifiers.

Process of programming :

- If switch of D_{03} is in closed position and the address input is 1100, then row 0 is activated through D_L and the column 3 through $D_{H.}$
- The sense amplifier of column is enabled.
- This gives output = logic 1 if CS=1.
- Thus a logic is stored at the address 1100.
- On the other hand if the witch in series with D_{03} is open, then a logic 0 is stored at the address 1100.

Cont…

Use of other devices in place of Diodes

- The ROM implemented using transistors is called as a bipolar memory and that implemented using MOSFET is called as MOS memory.
- The base emitter junction of transistor is forward biased hence it acts as a diode.

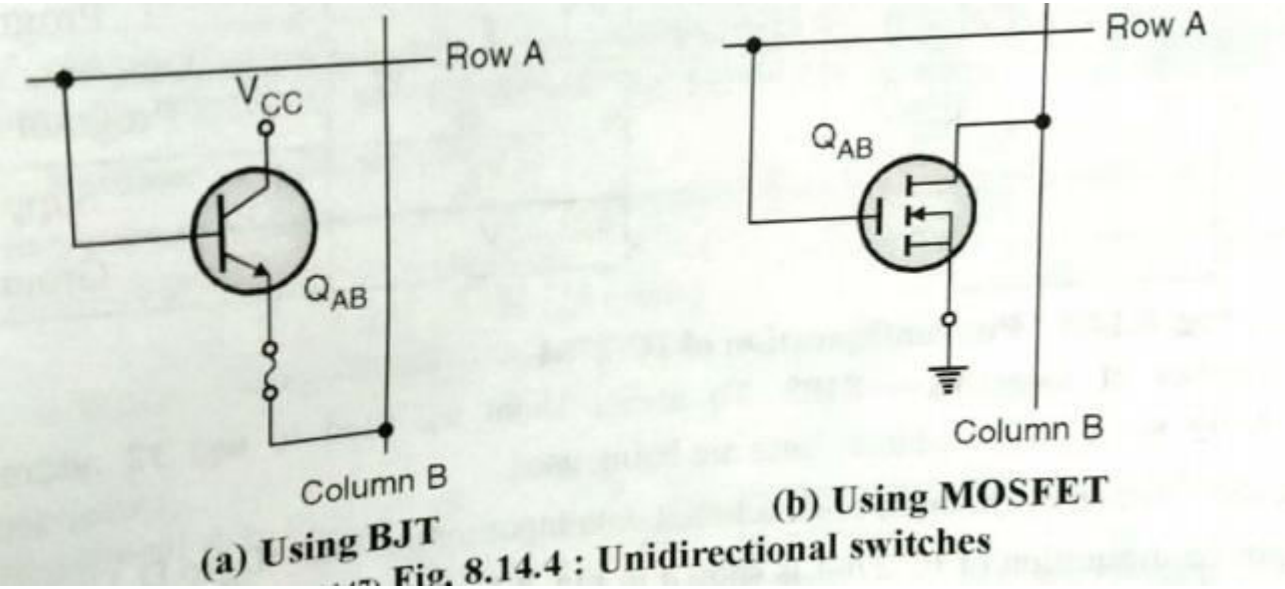
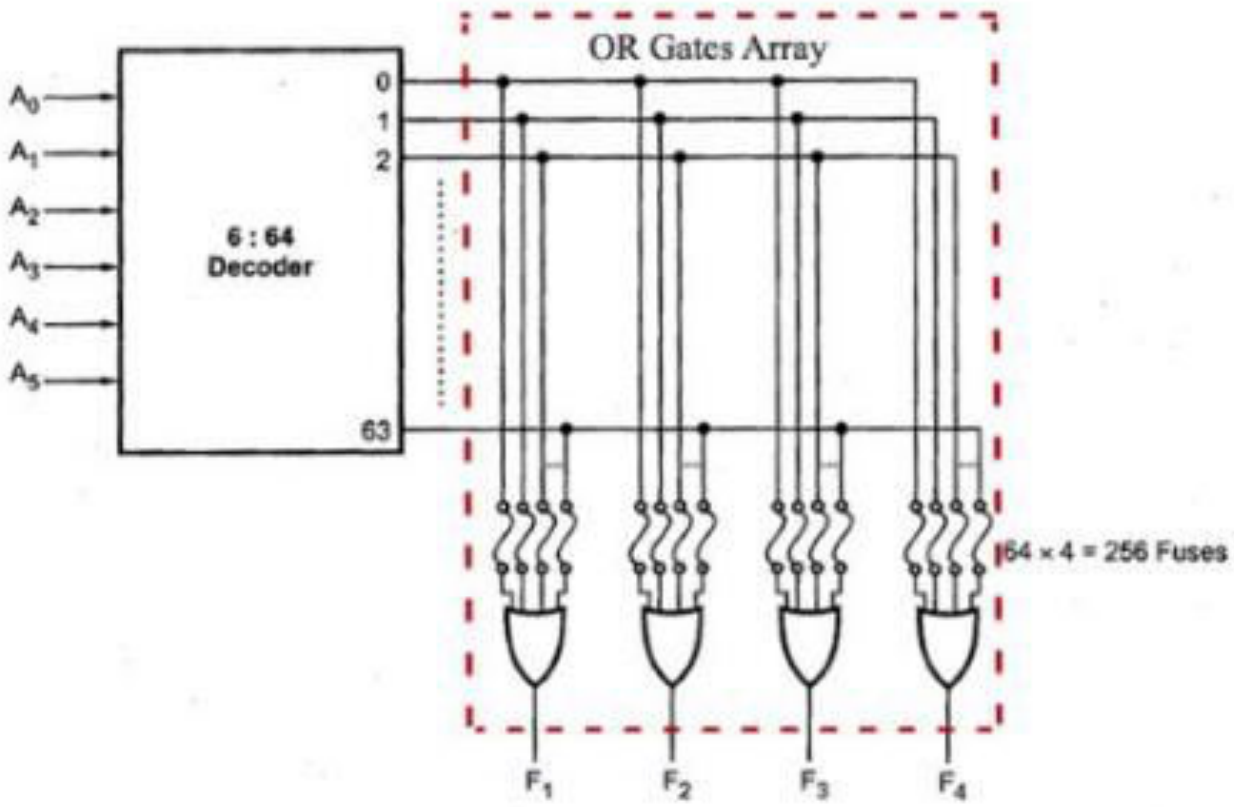


Fig. 8.14.4 : Unidirectional switches

Cont…

ROM Memory array:



Internal construction of 64x4 ROM

Cont…

Types of ROM

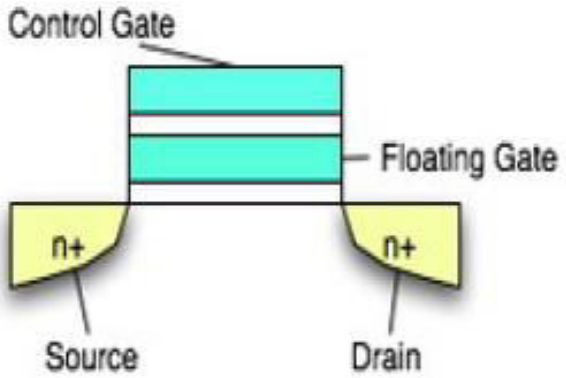
1. Programmable Read Only Memory (PROM)

- Empty of data when manufactured.
- May be permanently programmed by the user.
- The process of writing your data to the PROM involves a special piece of equipment called a device programmer.
- The device programmer writes data to the device one word at a time by applying an electrical charge to the input pins of the chip.
- Once a PROM has been programmed in this way, its contents can never be changed. If the code or data stored in the PROM must be changed, the current device must be discarded.
- As a result, PROMs are also known as one-time programmable (OTP) devices.

Cont…

2. Erasable Programmable Read Only Memory (EPROM)

- Can be programmed, erased and reprogrammed.
- The EPROM chip has a small window on top allowing it to be Erased by shining ultra-violet light on it.
- After reprogramming the window is covered to prevent new contents being erased.
- Access time is around 45 – 90 nanoseconds.
- Though more expensive than PROMs, their ability to be reprogrammed makes.
- EPROMs an essential part of the software development and testing process.



Cont…

3. Electrically Erasable Programmable Read Only Memory (EEPROM)

- Reprogrammed electrically **without using ultraviolet light**
- The data is stored in the form of charge. Presence of charge represents And its absence represents 0.
- It is possible to erase and program a particular memory location. This is called selective erasing.
- Access times between 45 and 200 nanoseconds

Cont…

Comparison between EPROM and EEPROM

Sr. No.	Parameter	EPROM	EEPROM
1.	Technique used for erasing	Exposure to ultraviolet light	A voltage of 20 to 25 Volts is applied
2.	Selective erasing	Not possible. All the locations get erased.	Possible. A particular location only can be erased.
3.	Time required for erasing.	Long 10 to 15 min.	Short 10 ms
4.	Need to remove PROM from circuit	It is necessary to remove the PROM	Not necessary to remove PROM.
5.	Cost	Less expensive	Very expensive

Daily Quiz

- Which of the following is the smallest entity of memory?

  (a) Block
  (b) Cell
  (c) Instance
  (d) Set

- The primary memory (also called main memory) of a personal computer consists of

  (a) RAM only
  (b) ROM only
  (c) both RAM and ROM
  (d) Cache memory

Daily Quiz

- Which of the following statements are not correct about the main memory of a computer?

  (a) In main memory, data gets lost when power is switched off.
  (b) Main memory is faster than secondary memory but slower than registers.
  (c) They are made up of semiconductors.
  (d) All are correct

- Which of the following memory is non-volatile?

  (a) RAM
  (b) ROM
  (c) Cache
  (d) ROM and Cache

Weekly Assignment

- Draw the basic circuit diagram of static RAM and explain its operation.
- Explain the difference between EPROM and EEPROM.
- Draw the 1-bit SRAM cell.
- Mention about SRAM and its usage.
- What are the various serial access memories?

Topic link

- https://www.youtube.com/watch?v=_eAL-v5oNOw
- https://www.youtube.com/watch?v=X-XwOXdUPU4
- https://www.youtube.com/watch?v=cIlKSD8ptAk

Topic Objective/Topic outcome

Topic: PLDs: PLA, PAL; Circuit Implementation using ROM, PLA and PAL

- **CO Covered :** CO5
- **Topic Objective :** The objective of PLDs: PLA, PAL; Circuit Implementation using ROM, PLA and PAL is to understand programmable logic devices and Circuit Implementation using ROM, PLA and PAL
- **Topic outcome:** At the end of the Topic , the student will be able to understand programmable logic devices and Circuit Implementation using ROM, PLA and PAL .

Programmable Logic Devices

Programmable Logic Devices (PLDs):

PLDs are the integrated circuits which can be programmed by the users as per their requirements. Therefore it is possible to implement a combinational or sequential circuits using the PLD ICs. They contain an array of AND gates & another array of OR gates.

Advantages of PLDs

- Reduced space requirements
- Reduction in power requirement
- Increased speed of switching
- Better security
- Higher density
- Low production cost
- Modification can be carried out within a short span of time.

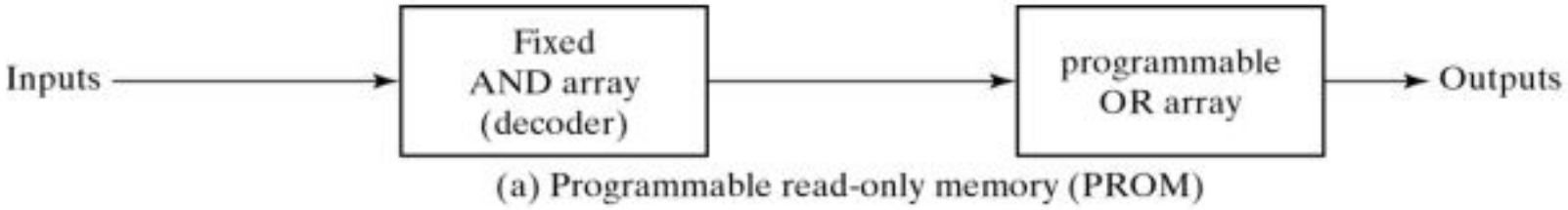
Cont…

There are three kinds of PLDs based on the type of arrays, which has programmable feature.

- Programmable Read Only Memory
- Programmable Array Logic
- Programmable Logic Array

PLD	AND Plane	OR Plane
PROM	Fixed	Programmable
PLA	Programmable	Programmable
PAL	Programmable	Fixed

Cont…



(a) Programmable read-only memory (PROM)

(b) Programmable array logic (PAL)

(c) Programmable logic array (PLA)

Fig. 7-13 Basic Configuration of Three PLDs

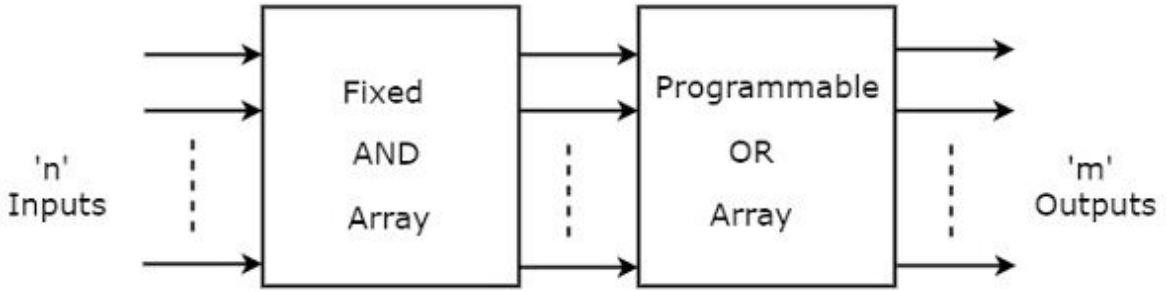
Cont…

- The process of entering the information into these devices is known as programming. Basically, users can program these devices or ICs electrically in order to implement the Boolean functions based on the requirement. Here, the term programming refers to hardware programming but not software programming.

PROM

1. Programmable Read Only Memory PROM:

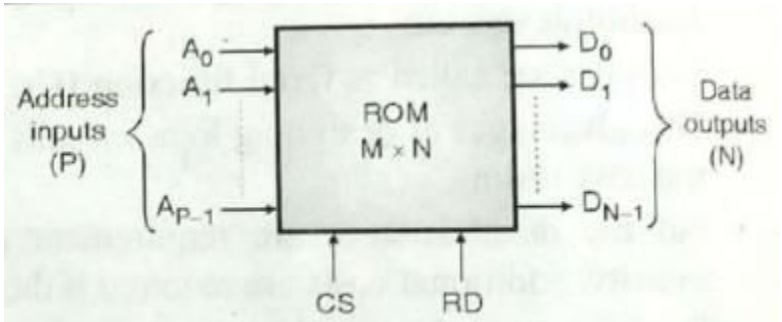
- ROM is a memory device, which stores the binary information permanently. That means, we can't change that stored information by any means later. If the ROM has programmable feature, then it is called as Programmable ROM (PROM). The user has the flexibility to program the binary information electrically once by using PROM programmer.
- PROM is a programmable logic device that has fixed AND array & Programmable OR array. The block diagram of PROM is shown in the following figure.



Cont…

ROM use as PLD :

- It can be programmed only once by the manufacturer as per the requirement of the user.
- A ROM of size M*N is shown in fig.it has M no of locations and each location can store N bit word.
- There are P no of address lines to access M locations hence the relation between P and M is given by $\mathbf{2^P = M}$.
- There are N no of data lines, on which the stored data can be outputted, when the read(RD) input is active.

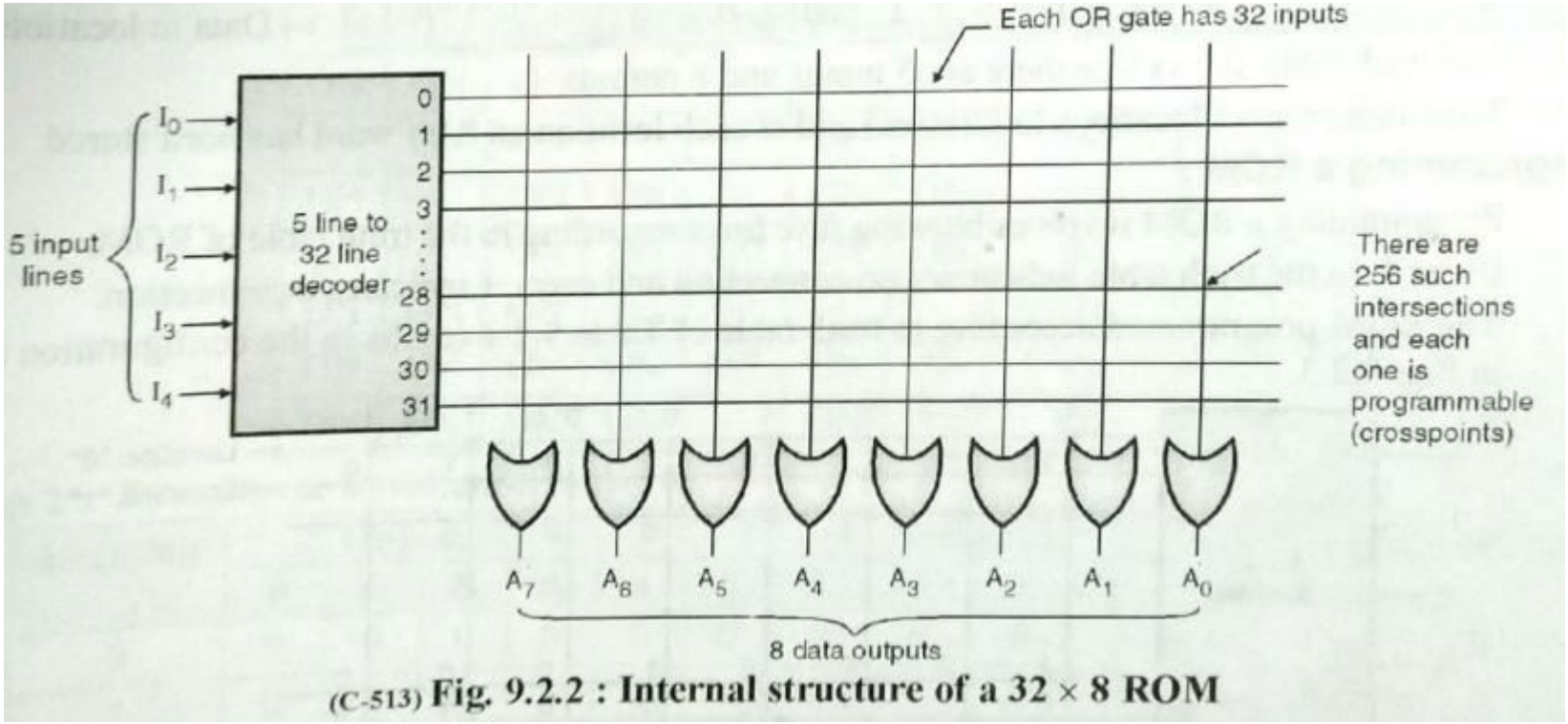


10) **Fig. 9.2.1(a) : Block diagram of a ROM**

Cont…

Internal logic of a ROM :

Let us understand the internal logic of a 32 *8 ROM. A 32*8 ROM consist of 32 words of 8 bit each.



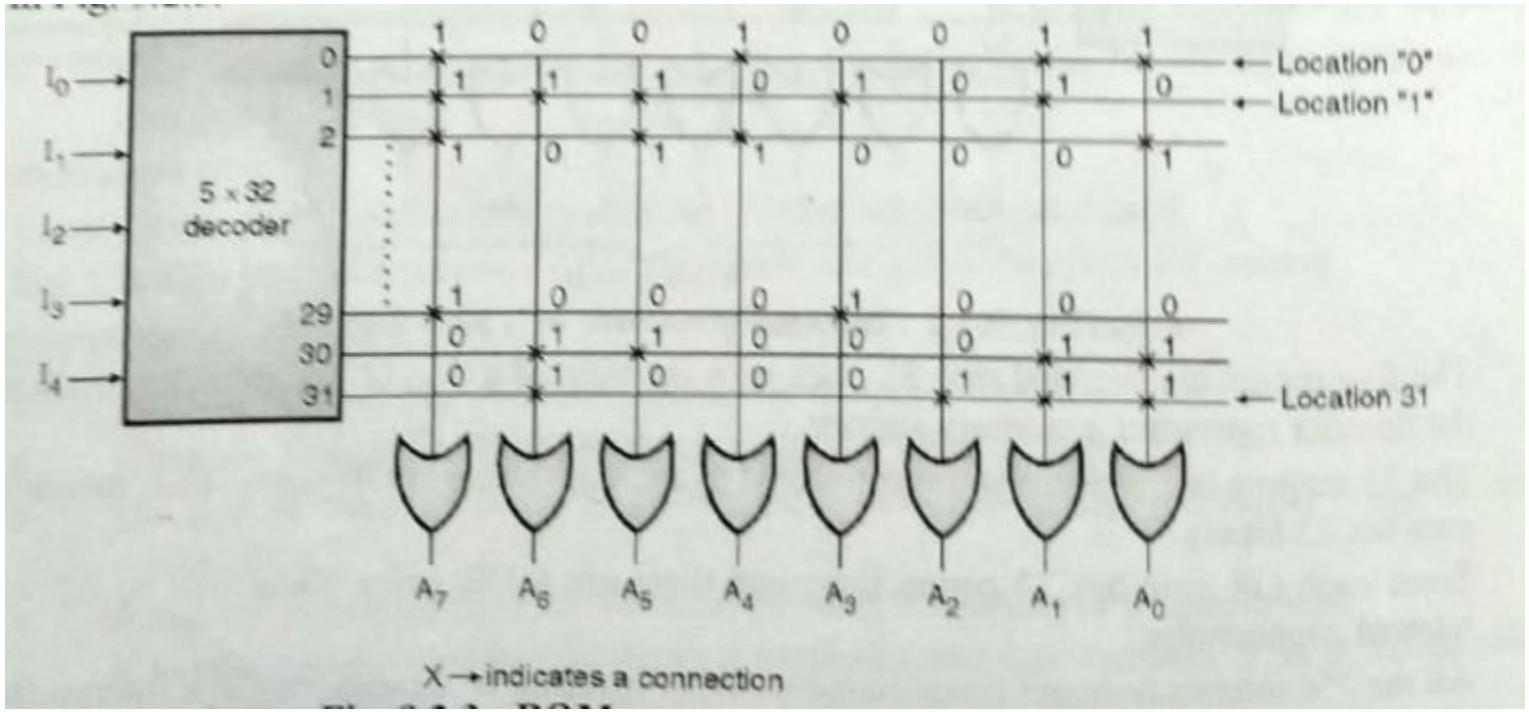
(C-513) **Fig. 9.2.2 : Internal structure of a 32 × 8 ROM**

Cont…

- To access 32 locations ,we have 5 input lines.
- The five inputs are decoded into 32 lines with the help of 5*32 decoder. Each output of the decoder represents a memory address.
- The 32 outputs of the decoder are connected to each of the eight OR gates. That means each OR gate 32 inputs.
- Since each OR gate has 32 connections and there are 8 OR gates, there will be 32*8 = 256 internal connections.
- All the 256 intersections are programmable.it means that each intersection is equivalent to a switch which can be either turned ON or OFF. An ON switch represents connection between the two intersecting line whereas an OFF switch represents that there is no connection between those points.
- The programmable intersection is called as a **crosspoint**.
- The **crosspoint** can be implemented with the help of various physical devices. But the simplest method is to use a **fuse link** that is normally intact and hence connect the two lines. It is equivalent to a closed switch.
- Whenever the switch is to be open circuited , we have to blow this fuse.

Cont…

- To access 32 locations ,we have 5 input lines.
- The five inputs are decoded into 32 lines with the help of 5*32 decoder..



Cont…

Inputs					Outputs				
I4	I3	I2	I1	I0	A7	A6	A5	A4	A3
0	0	0	0	0	1	0	1	1	0
0	0	0	0	1	0	0	0	1	1
0	0	0	1	0	1	1	0	0	0
0	0	0	1	1	1	0	1	1	0
		⋮					⋮		
1	1	1	0	0	0	0	0	0	1
1	1	1	0	1	1	1	1	0	0
1	1	1	1	0	0	1	0	0	1
1	1	1	1	1	0	0	1	1	0

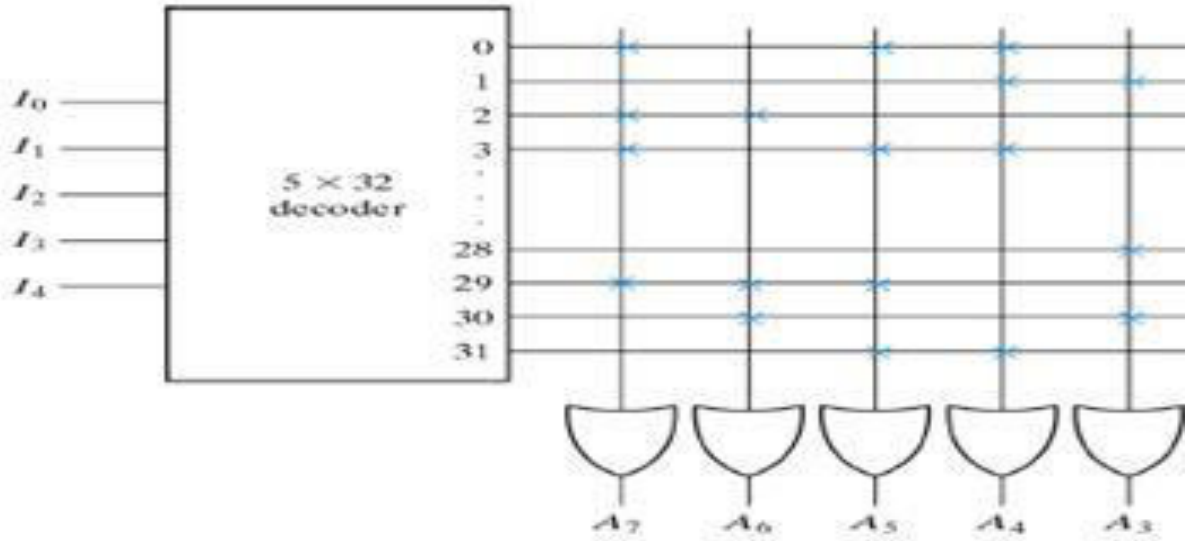
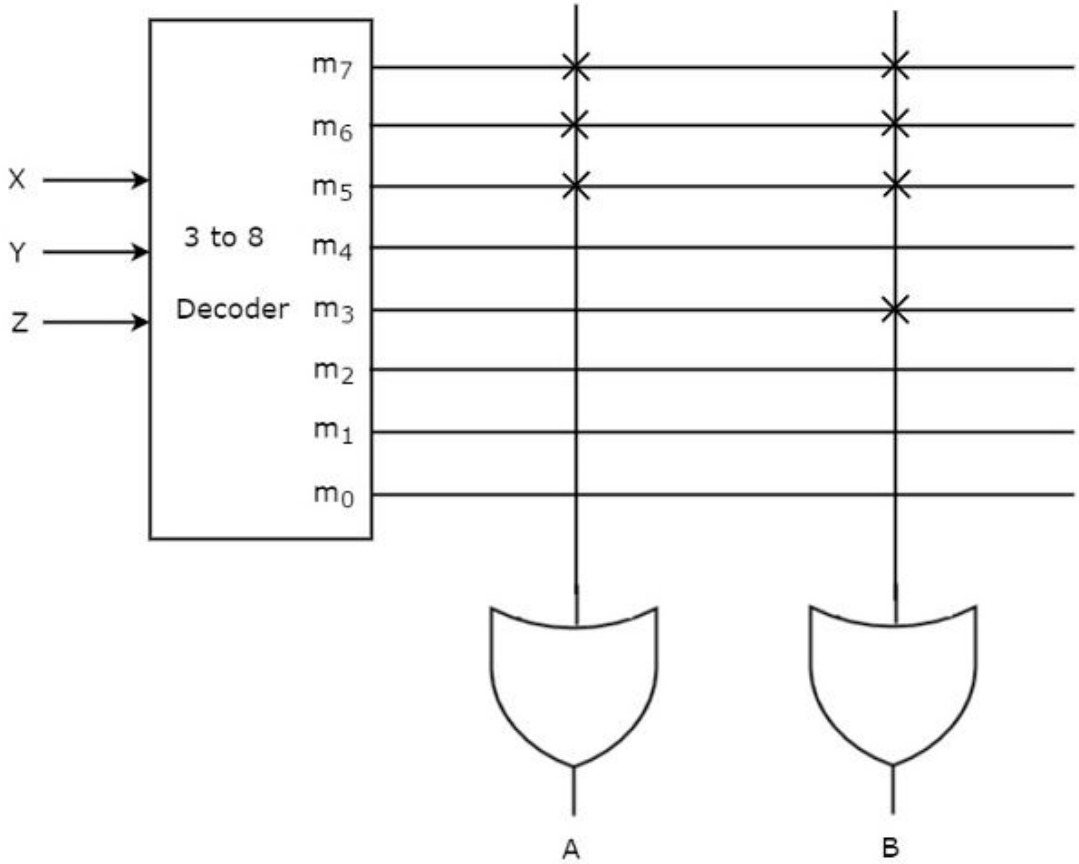


Fig. 7-11 Programming the ROM According to T

Cont…

Example: Implement the following Boolean functions using PROM.

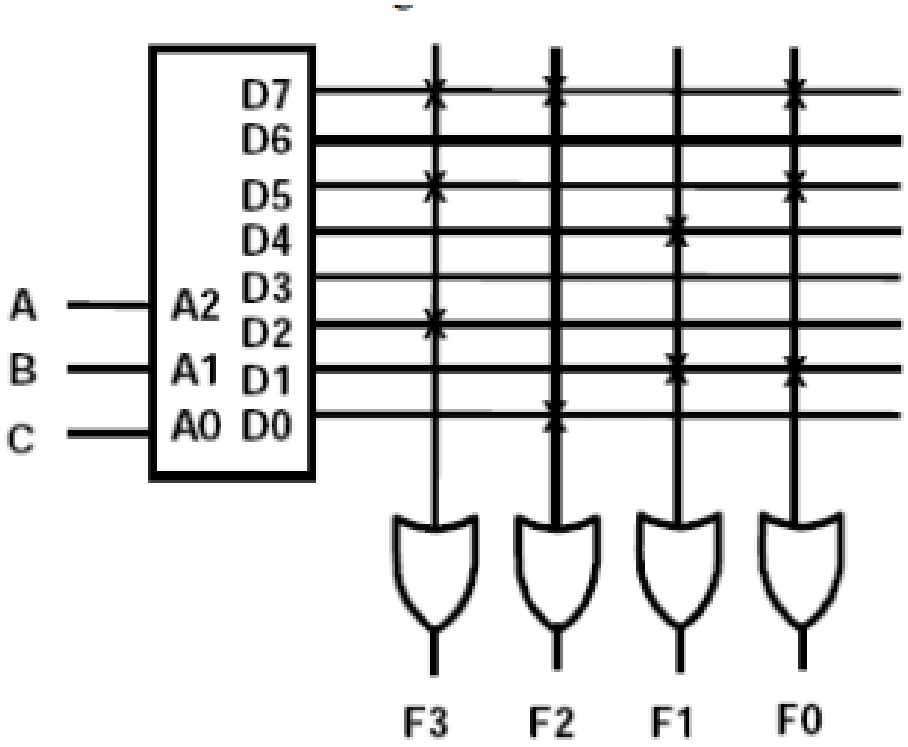
$A(X,Y,Z)=\sum m(5,6,7)$ $B(X,Y,Z)=\sum m(3,5,6,7)$



Cont…

Example: Implement the following Boolean functions using PROM.

$F0 = \sum m(1,5,7)$, $F1 = \sum m(1,4)$, $F2 = \sum m(0, 7)$, $F3 = \sum m(2,5,7)$



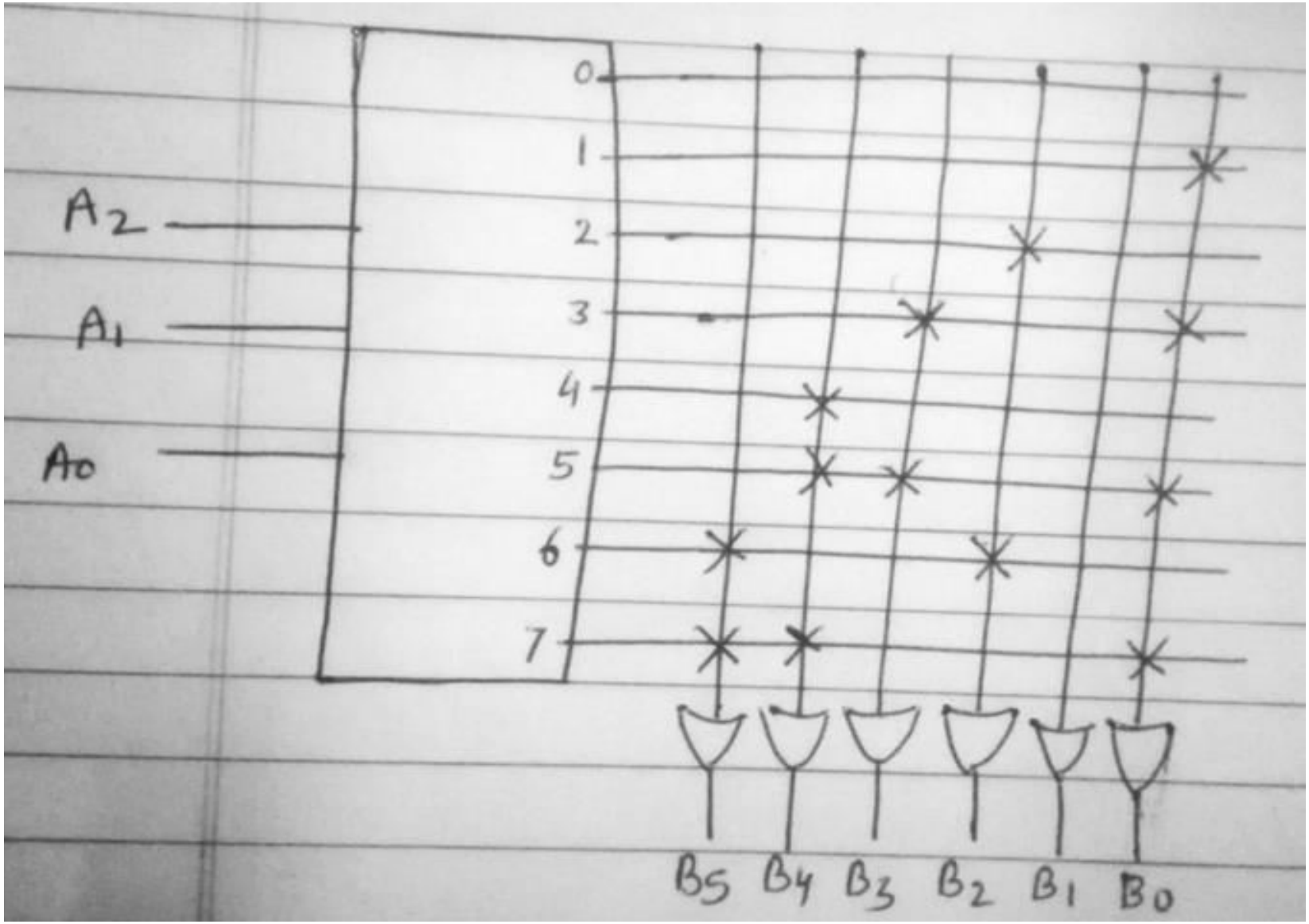
Cont…

Example: Design a combinational circuit using a ROM. The circuit accepts a 3- bit number and generates an output binary number equal to the square of the input number.

Table 7-4
Truth Table for Circuit of Example 7-1

Inputs			Outputs						
A_2	A_1	A_0	B_5	B_4	B_3	B_2	B_1	B_0	Decimal
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1	1
0	1	0	0	0	0	1	0	0	4
0	1	1	0	0	1	0	0	1	9
1	0	0	0	1	0	0	0	0	16
1	0	1	0	1	1	0	0	1	25
1	1	0	1	0	0	1	0	0	36
1	1	1	1	1	0	0	0	1	49

Cont…



Cont…

Advantages of ROM as PLD :

- Design becomes extremely easy
- It is possible to change or modify the design quickly
- Reduces cost
- Modification takes less time than SSI/MSI.

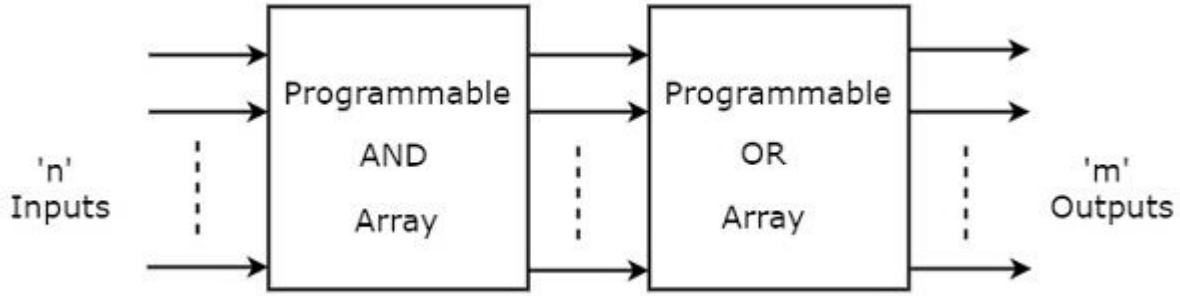
Disadvantages of ROM as PLD :

- Increase in power requirement
- Complete circuit is not utilized
- Increase in size with increase in no of input variables.

PLA

3. Programmable Logic Array (PLA):

- PLA is a programmable logic device that has both Programmable AND array & Programmable OR array. Hence, it is the most flexible PLD. The **block diagram** of PLA is shown in the following figure.



- Here, the inputs of AND gates and OR gates are programmable. That means each AND gate has both normal and complemented inputs of variables.

Cont…

Implementation of combinational circuits using PLA :

Steps to be followed :

1. Prepare the truth table
2. Write the Boolean expression in SOP form
3. Obtain the minimum SOP form to reduce the number of product terms to a minimum.
4. Decide the input connections of AND matrix for generating the required product terms
5. Then decide the input connections of OR matrix to generate the required sum terms.
6. Decide the connections to invert/non-invert matrix.
7. Program the PLA**.**

PLA

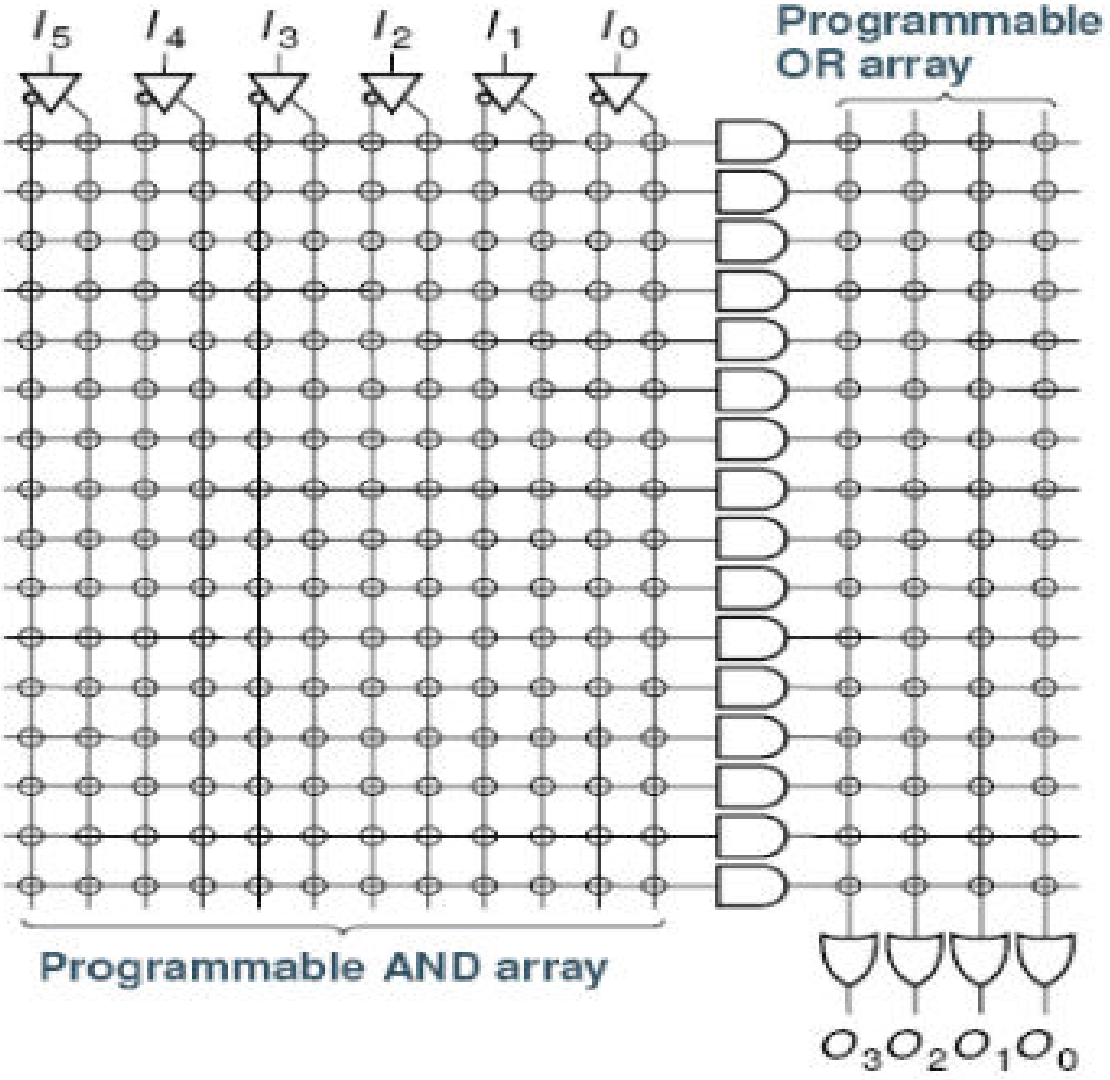


Fig. 4.2: PLA Structure

Cont…

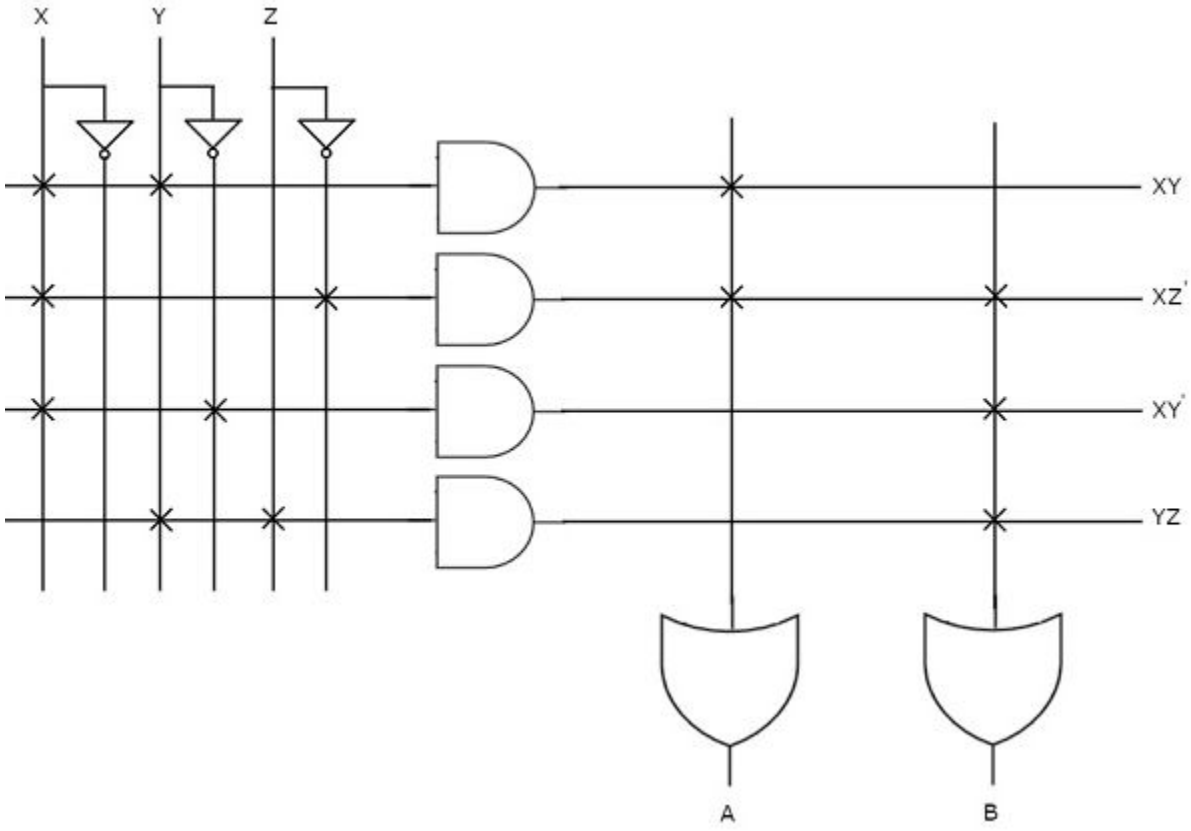
How to specify the size of a PLA :

- The size of a PLA is specified as M*P*N where M denotes the number of inputs, P corresponds to the number of product terms and N denotes the number of outputs**.**

Cont…

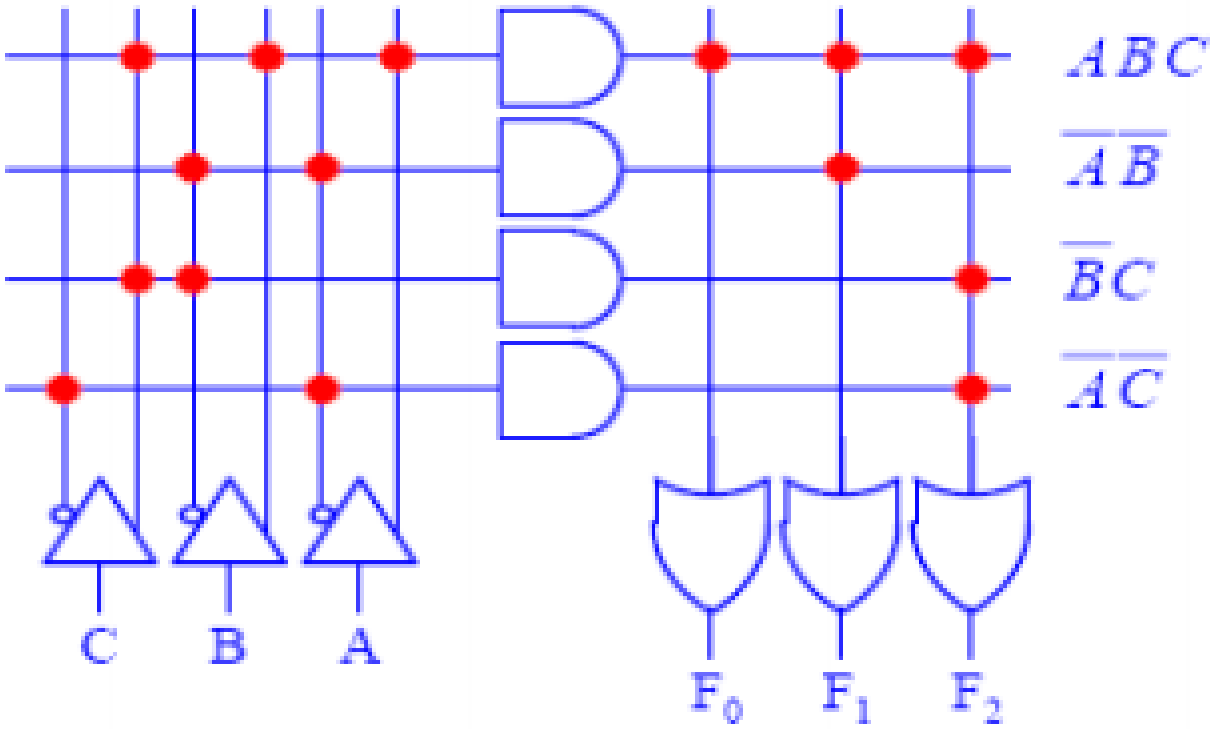
Example: Let us implement the following Boolean functions using PLA.

A=XY+XZ′, B=XY′+YZ+XZ′



Cont…

Example: Implement the following functions using PLA which is shown in
F0 = ABC , F1 = ABC + A'B' , F2 = ABC + B'C' + A'C'



Cont…

Programming Table:

1. First: lists the product terms numerically
2. Second: specifies the required paths between inputs and AND gates.
3. Third: specifies the paths between the AND and OR gates.
4. For each output variable, we may have a T(ture) or C(complement) for programming the XOR gate

Simplification of PLA :

- Careful investigation must be undertaken in order to reduce the number of distinct product terms, PLA has a finite number of AND gates.
- Both the true and complement of each function should be simplified to see which one can be expressed with fewer product terms and which one provides product terms that are common to other functions.

Cont…

Example: Implement the following functions using PLA which is shown in
F1 = AB'+AC+A'BC' , F2 = (AC+BC)'

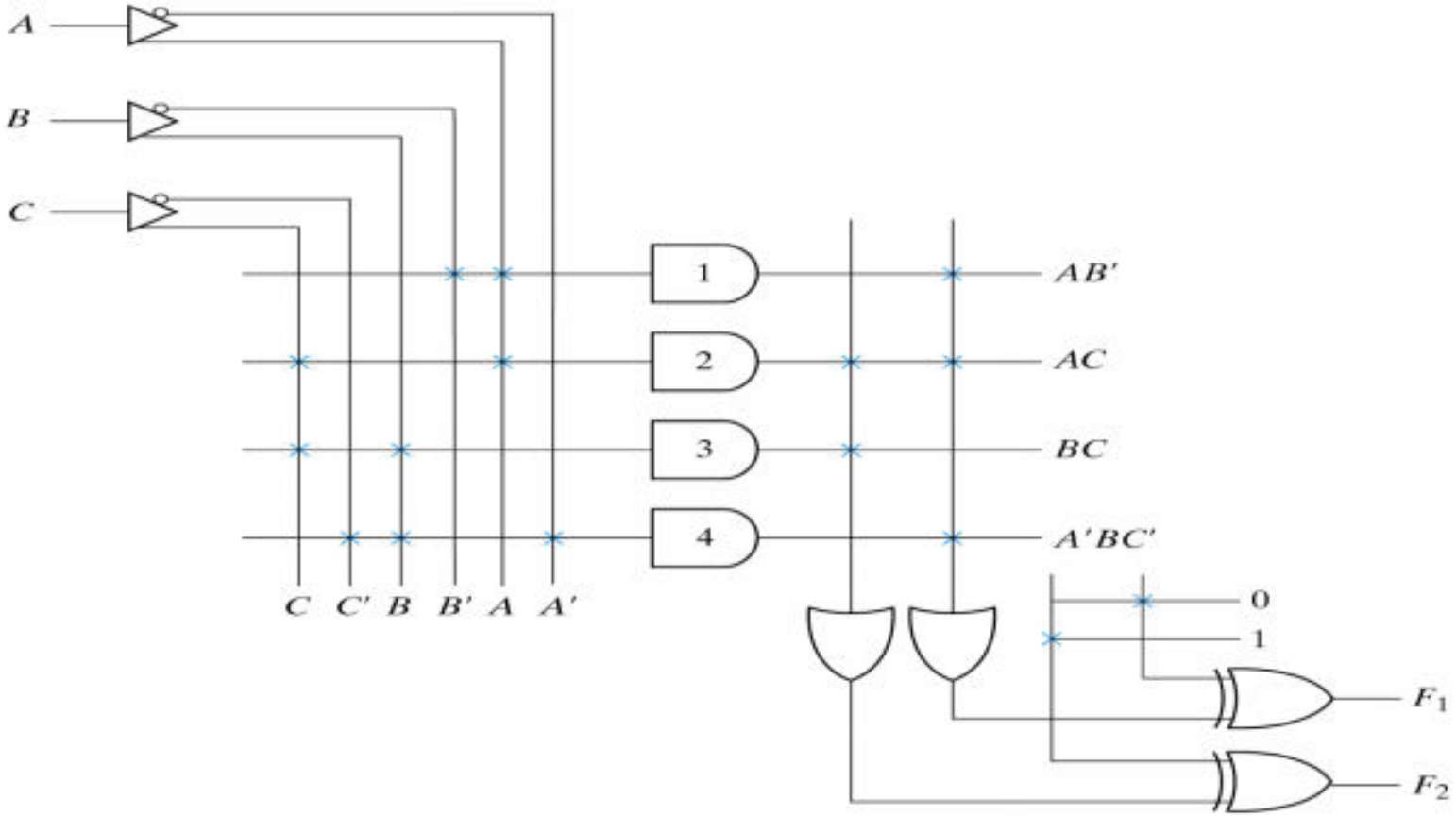
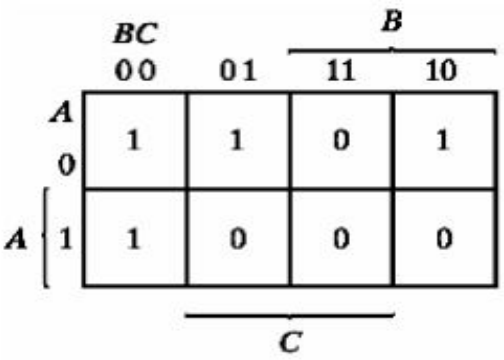


Fig. 7-14 PLA with 3 Inputs, 4 Product Terms, and 2 Outputs

Cont…

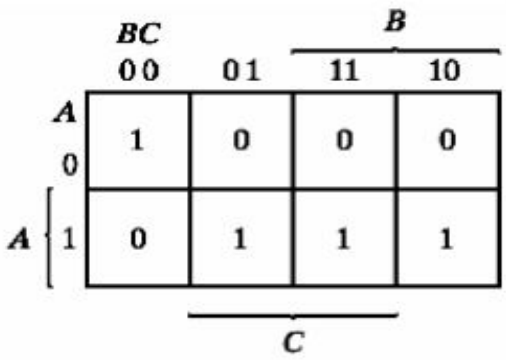
Example: Implement the following functions using PLA which is shown in F1(A, B, C) = ∑(0, 1, 2, 4) F2(A, B, C) = ∑(0, 5, 6, 7)



A \ BC	00	01	11	10
0	1	1	0	1
1	1	0	0	0

$F_1 = A'B' + A'C' + B'C'$

$F_1 = (AB + AC + BC)'$



A \ BC	00	01	11	10
0	1	0	0	0
1	0	1	1	1

$F_2 = AB + AC + A'B'C'$

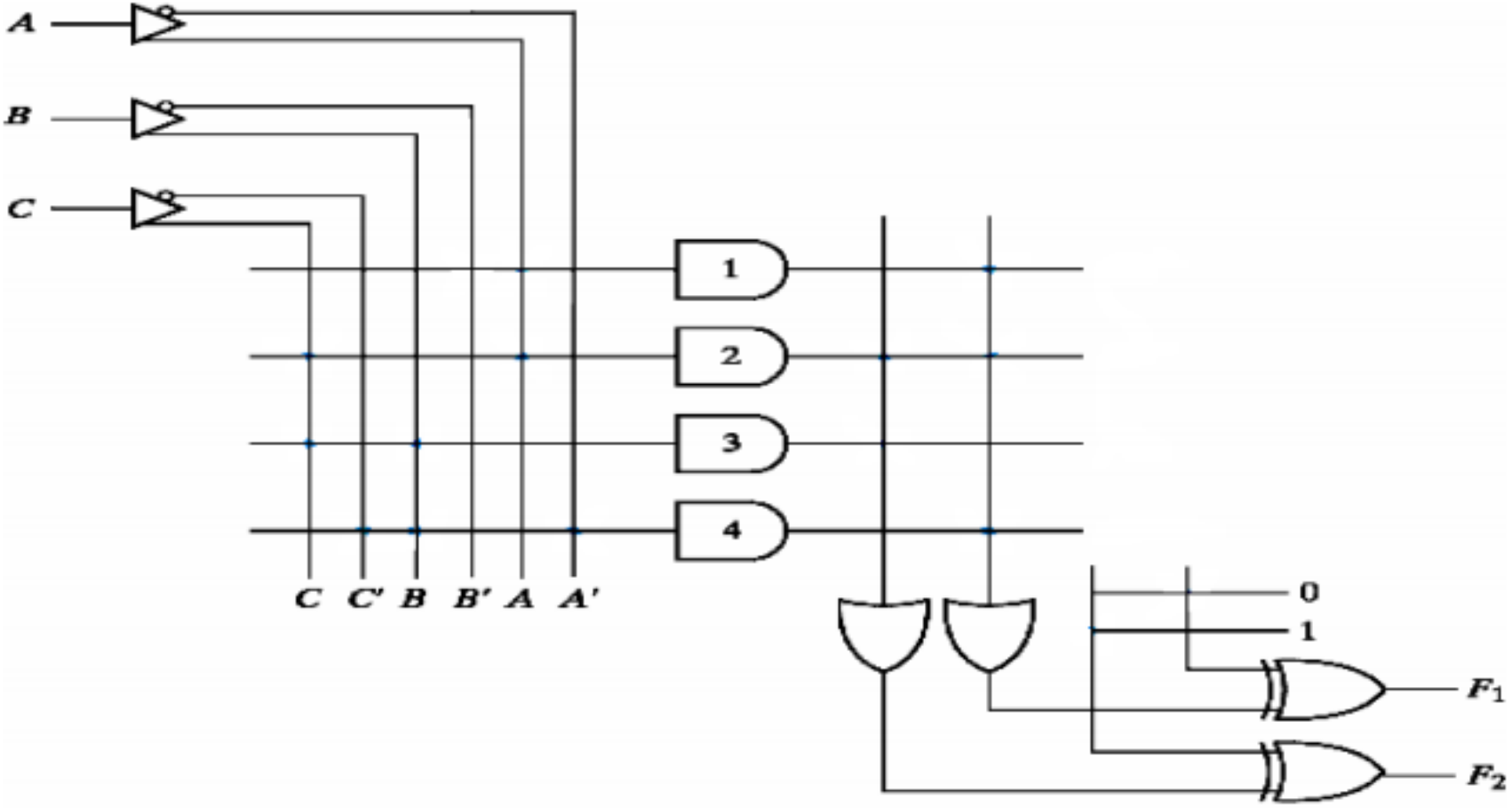
$F_2 = (A'C + A'B + AB'C')'$

PLA table by simplifying the function:

PLA table by simplifying the function:

- Both the true and complement of the functions are simplified in sum of products.
- We can find the same terms from the group terms of the functions of F1, F1',F2 and F2' which will make the minimum terms.
- F1 = (AB + AC + BC)' F2 = AB + AC + A'B'C

Cont…



Cont…

Disadvantage:

- Often, the product term count limits the application of a PLA. Two-level multiple-output optimization reduces the number of product terms in an implementation, helping to fit it into a PLA.

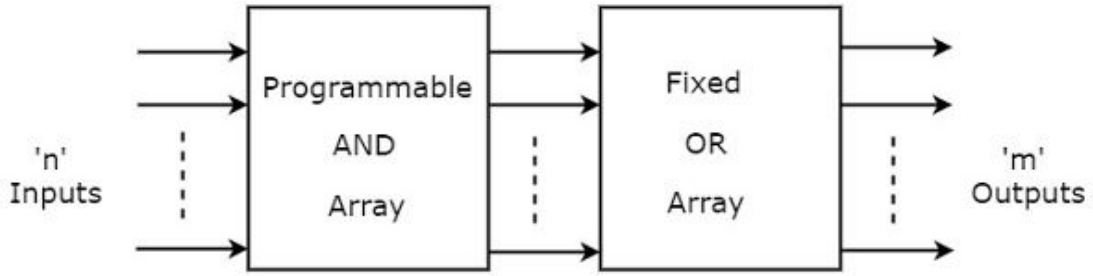
Advantages:

- A PLA can have large N and M permitting implementation of equations that are impractical for a ROM (because of the number of inputs, N required.
- A PLA has all of its product terms connectable to all outputs, overcoming the problem of the limited inputs to the PAL Ors.
- Some PLAs have outputs that can be complemented, adding POS functions

PAL

2. Programmable Array Logic (PAL):

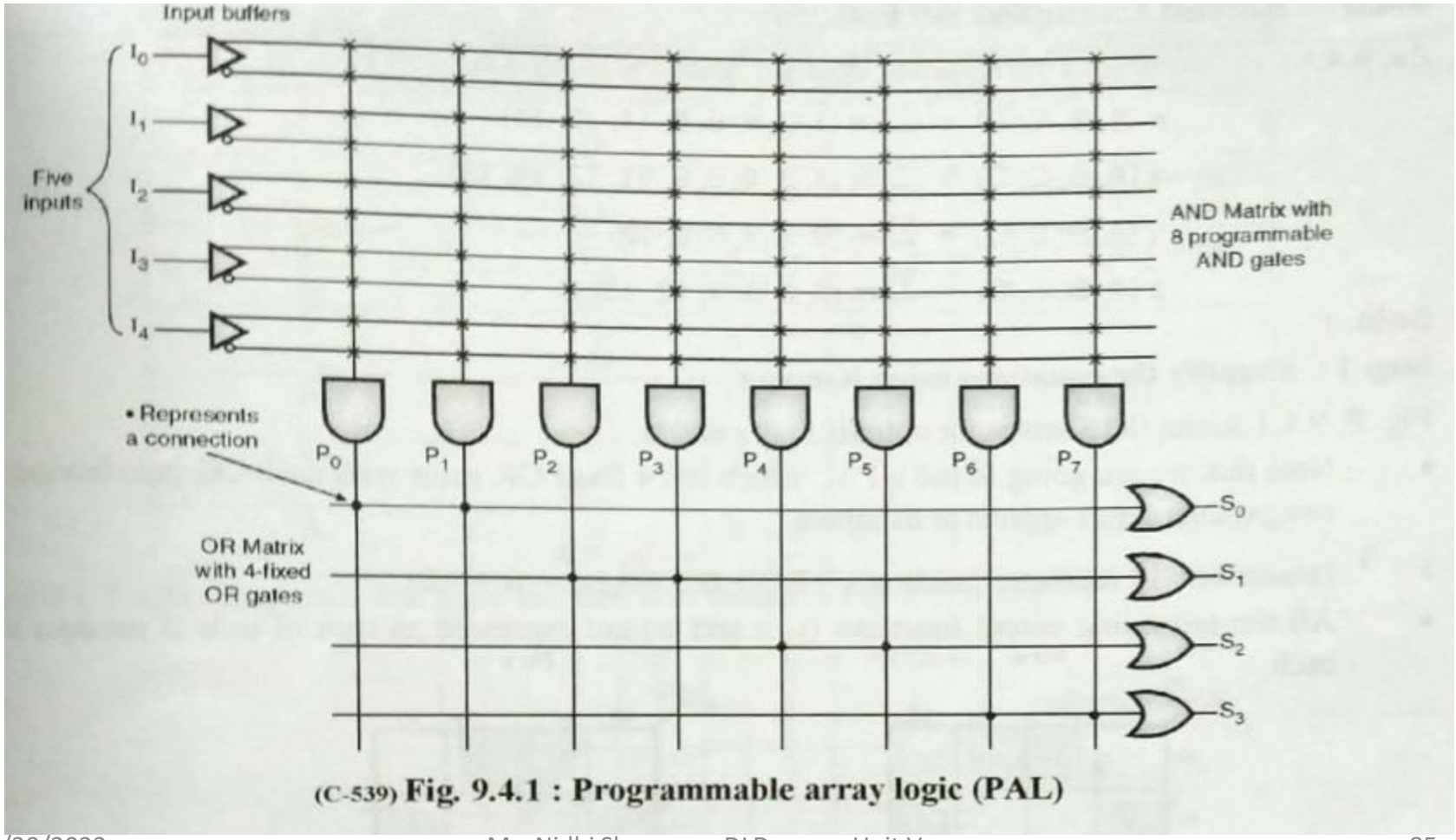
- PAL is a programmable logic device that has Programmable AND array & fixed OR array. The advantage of PAL is that we can generate only the required product terms of Boolean function instead of generating all the min terms by using programmable AND gates. The **block diagram** of PAL is shown in the following figure.



- Here, the inputs of AND gates are programmable. And the inputs of OR gates are not of programmable type That means each AND gate has both normal and complemented inputs of variables and OR gate will be of fixed type.

Cont…

- The configuration of a PAL with 5-inputs, 8 –AND gate and 4-fixed OR gates.



(C-539) **Fig. 9.4.1 : Programmable array logic (PAL)**

Cont…

- **Input buffers:**
  - There are 5 input buffers one per input. The buffer produce inverted and non-inverted versions of corresponding inputs.
  - Input buffers are used for reducing the loading on inputs.
- **AND matrix :**
  - There are 8 programmable AND gates in the AND matrix.
  - These AND gates can be programmed by opening the suitable fuse links to generate 8 product terms
- **OR matrix :**
  - The OR matrix consist of four fixed OR gates. That means we cannot programmed them.
  - Each OR gate receives inputs from the outputs of only two AND gates.

PAL

- When designing with a PAL, the Boolean functions must be simplified to fit into each section.
- Unlike the PLA, a product term cannot be shared among two or more OR gates. Therefore, each function can be simplified by itself without regard to common product terms.
- The output terminals are sometimes driven by three-state buffers or inverters

PAL

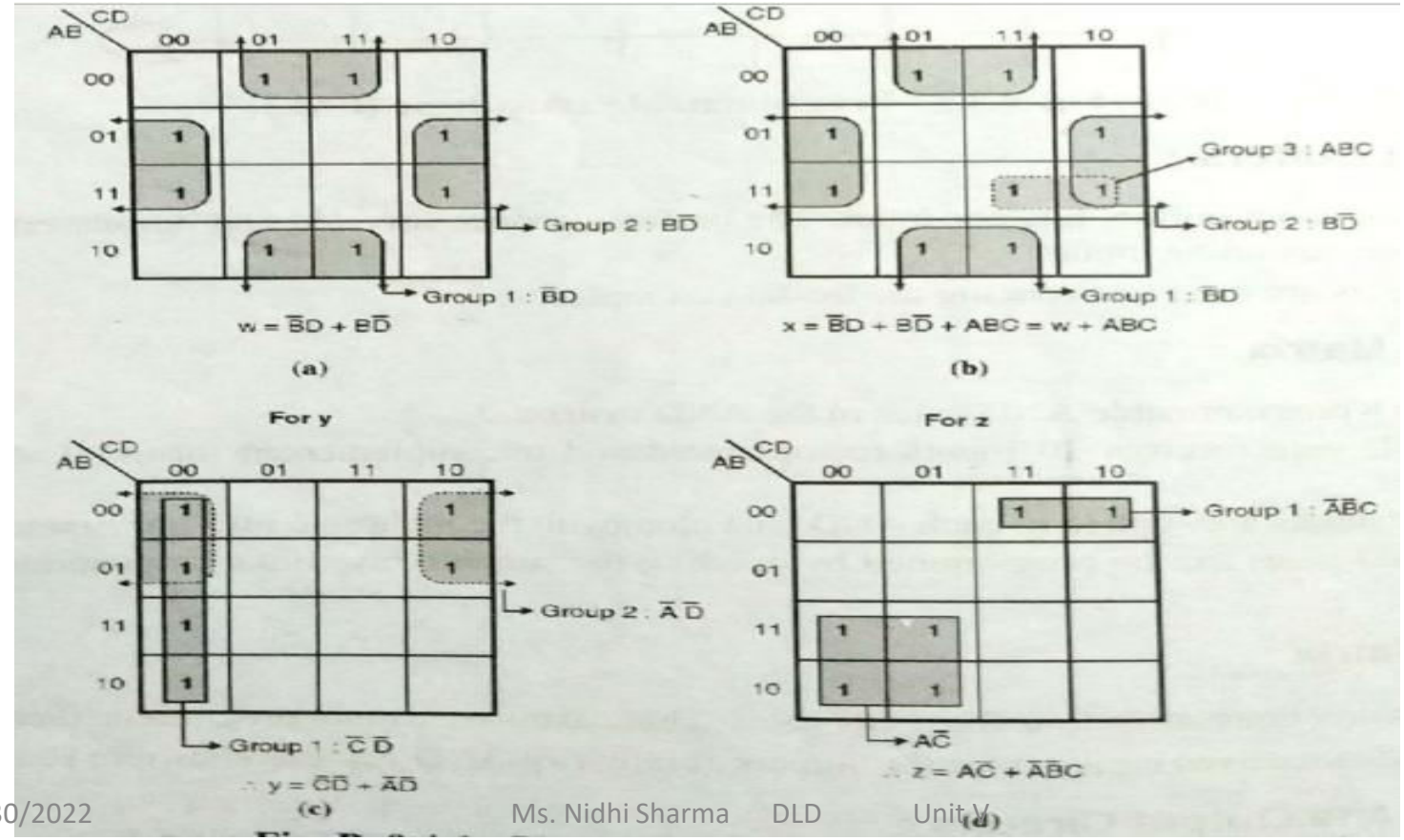
Ex. 9.4.1 : Implement the following Boolean functions using a suitable PAL.

$$w(A, B, C, D) = \sum m(1, 3, 4, 6, 9, 11, 12, 14)$$

$$x(A, B, C, D) = \sum m(1, 3, 4, 6, 9, 11, 12, 14, 15)$$

$$y(A, B, C, D) = \sum m(0, 2, 4, 6, 8, 12)$$

$$z(A, B, C, D) = \sum m(2, 3, 8, 9, 12, 13)$$

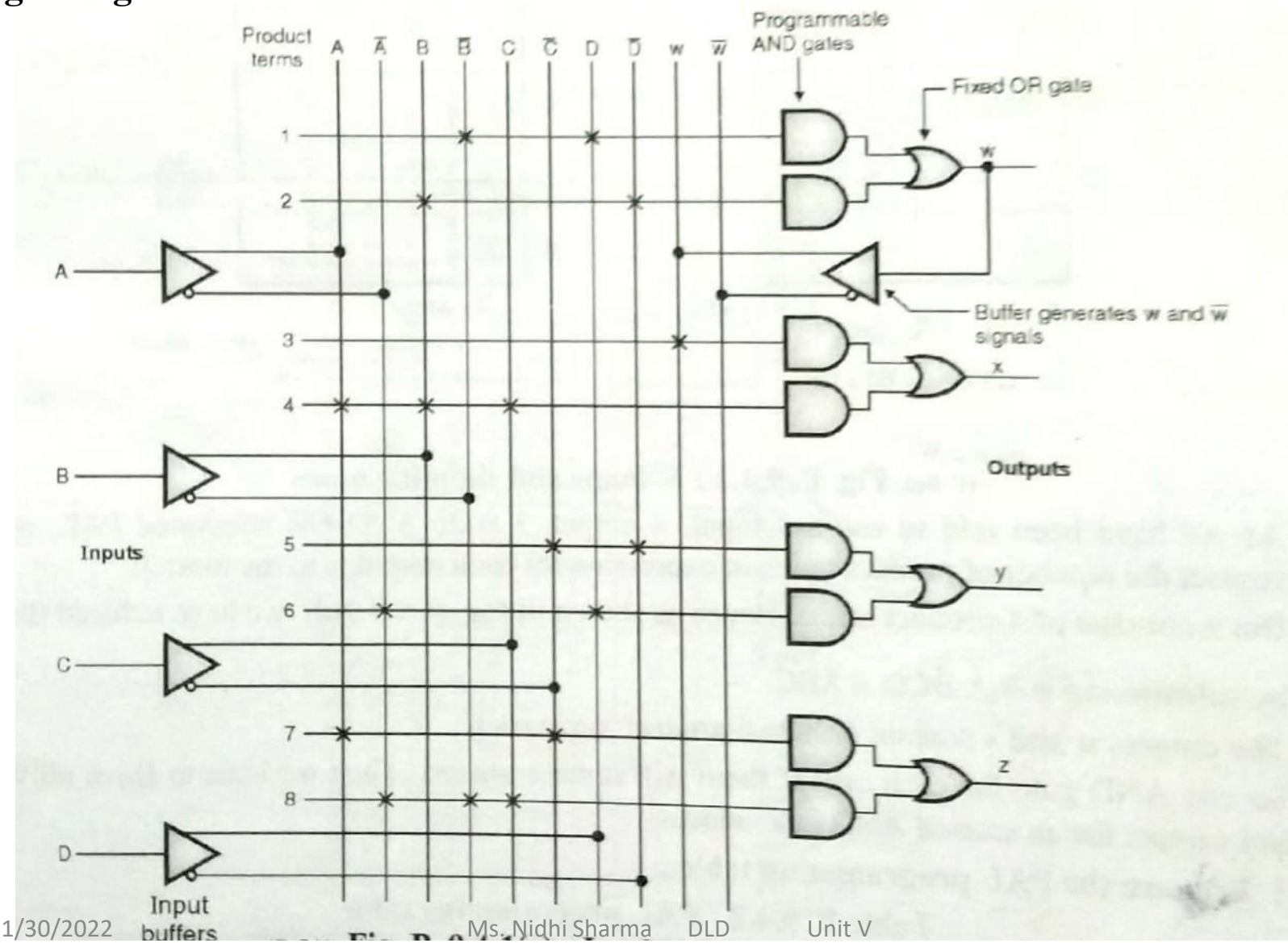


Cont…

Product term No.	Product term	AND inputs					Outputs
		A	B	C	D	w	
1	$\bar{B}D$	–	0	–	1	–	$w = \bar{B}D + B\bar{D}$
2	$B\bar{D}$	–	1	–	0	–	
3	w	–	–	–	–	1	$x = w + ABC$
4	ABC	1	1	1	–	–	
5	$\bar{C}\bar{D}$	–	–	0	0	–	$y = \bar{C}\bar{D} + \bar{A}\bar{D}$
6	$\bar{A}\bar{D}$	0	–	–	1	–	
7	$\bar{A}C$	1	–	0	–	–	$z = \bar{A}C + \bar{A}\bar{B}C$
8	$\bar{A}\bar{B}C$	0	0	1	–	–	

Cont…

Logic diagram



Cont…

Design a combinational circuit using a suitable PAL considering the following Boolean expressions. Use a PAL with four inputs, four outputs and three wide AND-OR structure.

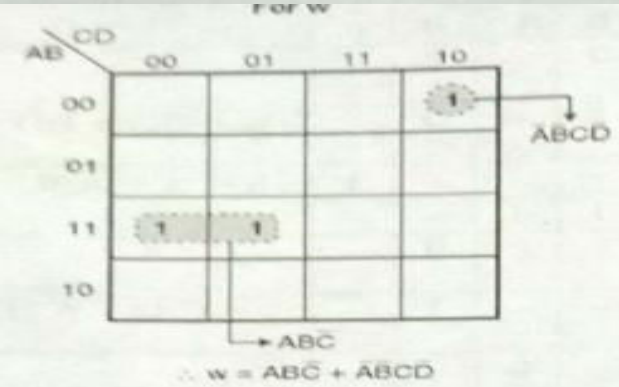
$w(A, B, C, D) = \sum m(2, 12, 13)$

$x(A, B, C, D) = \sum m(7, 8, 9, 10, 11, 12, 13, 14, 15)$

$y(A, B, C, D) = \sum m(0, 2, 3, 4, 5, 6, 7, 8, 10, 11, 15)$

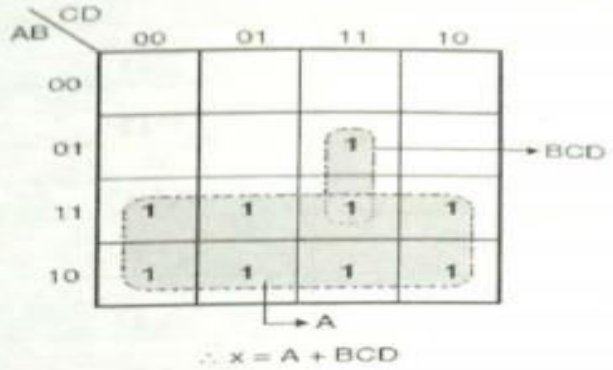
$z(A, B, C, D) = \sum m(1, 2, 8, 12, 13)$

For w



$\therefore w = AB\bar{C} + \bar{A}BCD$

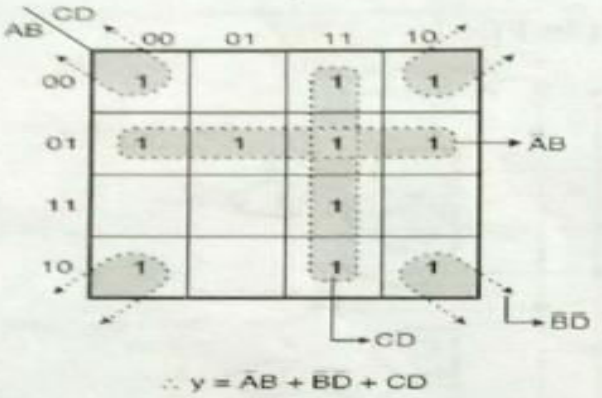
(a)



$\therefore x = A + BCD$

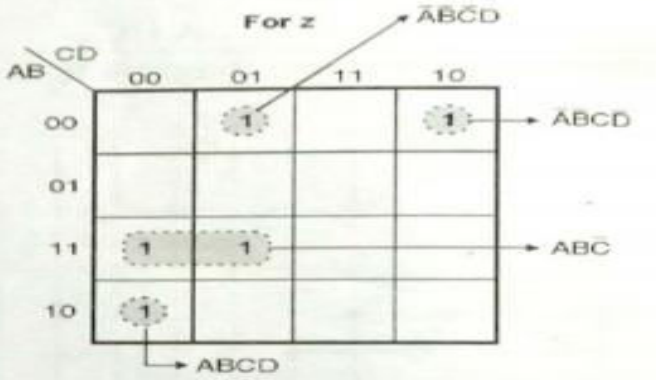
(b)

For y



$\therefore y = A\bar{B} + \bar{B}\bar{D} + CD$

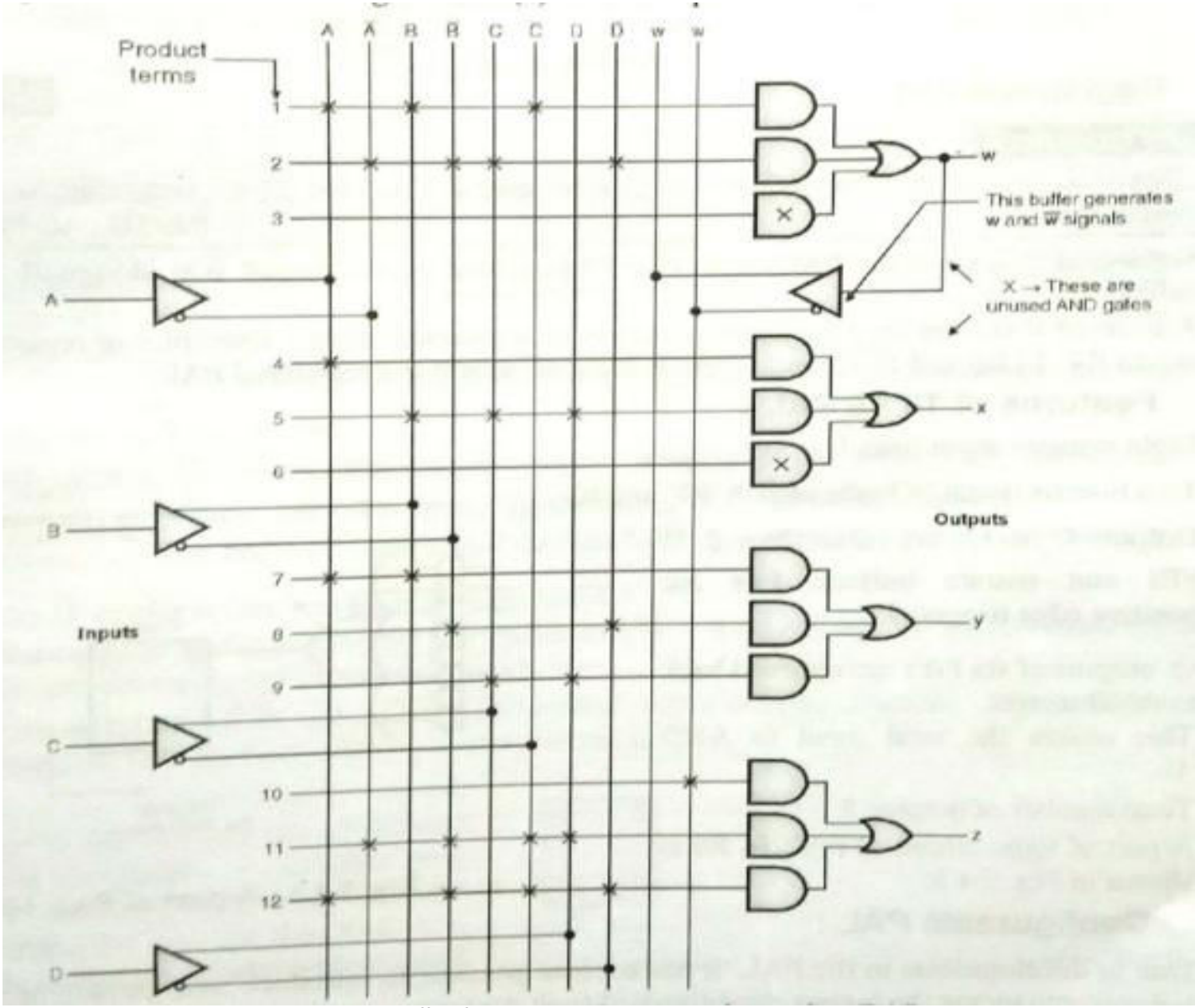
For z



$z = ABCD + \underbrace{\bar{A}BCD + AB\bar{C}}_{w} + \bar{A}B\bar{C}\bar{D}$

$= w + \bar{A}BCD + \bar{A}B\bar{C}\bar{D}$

Cont…


A A B B C C D D w w
Product terms
1
2
3
4
5
6
7
8
9
10
11
12
A
B
C
D
Inputs
w
This buffer generates w and w̄ signals
X → These are unused AND gates
x
Outputs
y
z

Cont…

Disadvantage:

- ROM guaranteed to implement any M functions of N inputs. PAL may have too few inputs to the OR gates. In that case Complete circuit is not utilized.

Advantages:

- For given internal complexity, a PAL can have larger N and M
- Some PALs have outputs that can be complemented, adding POS functions.
- PAL has outputs from OR terms as internal inputs to all AND terms, making implementation of multi-level circuits easier.

Comparison of PROM, PAL and PLA

Comparison of PROM, PLA and PAL

PROM	PLA	PAL
AND array is fixed and OR array is programmable.	Both AND and OR arrays are programmable.	OR array is fixed and AND array is programmable.
Cheaper and simple to use.	Costliest and complex than PAL and PROMs,	Cheaper and simpler.
Ail minterms are decoded.	AND array can be programmed to get desired minterms.	AND array can be programmed to get desired minterms.
Onfy Boolean functions in Standard SOP form can be implemented using PROM	Any Boolean functions In SOP form can be implemented using PLA.	Any Boolean functions In SOP form can be implemented using PLA.

Daily Quiz

- The inputs in the PLD is given through _____
  a) NAND gates
  b) OR gates
  c) NOR gates
  d) AND gates

- PLA contains _____
  a) AND and OR arrays
  b) NAND and OR arrays
  c) NOT and AND arrays
  d) NOR and OR arrays

Daily Quiz

- A PLA is similar to a ROM in concept except that _____
  a) It hasn't capability to read only
  b) It hasn't capability to read or write operation
  c) It doesn't provide full decoding to the variables
  d) It hasn't capability to write only

- The difference between a PAL & a PLA is _____
  a) PALs and PLAs are the same thing
  b) The PLA has a programmable OR plane and a programmable AND plane, while the PAL only has a programmable AND plane
  c) The PAL has a programmable OR plane and a programmable AND plane, while the PLA only has a programmable AND plane
  d) The PAL has more possible product terms than the PLA

Weekly Assignment

- What is programmable logic array?
- Explain difference between PLA and PAL.
- What are the draw backs of PLAs? How PLAs are used to implement combinational and sequential logic circuits?
- Design a PAL to realize a full Adder circuit.
- Compare various programmable devices .

Topic link

- https://www.youtube.com/watch?v=gCAYY0fHPq4
- https://www.youtube.com/watch?v=PkFX7NjgEdA
- https://www.youtube.com/watch?v=dovxQZ5S5sk

Topic Objective/Topic outcome

Topic: FGPA

- **CO Covered :** CO5
- **Topic Objective :** The objective of topic FGPA is understand about FPGA working, designing and its applications.
- **Topic outcome:** At the end of the Topic , the student will be able to understand working and designing of FPGA.

FPGA

FPGA: A **field-programmable gate array** (**FPGA**) is an integrated circuit designed to be configured by a customer or a designer after manufacturing – hence the term "field-programmable".

- The FPGA configuration is generally specified using a hardware description language (HDL).
- FPGAs contain an array of programmable logic blocks, and a hierarchy of "reconfigurable interconnects" that allow the blocks to be "wired together", like many logic gates that can be inter-wired in different configurations. Logic blocks can be configured to perform complex combinational functions, or merely simple logic gates like AND and XOR.
- In most FPGAs, logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory.

FPGA

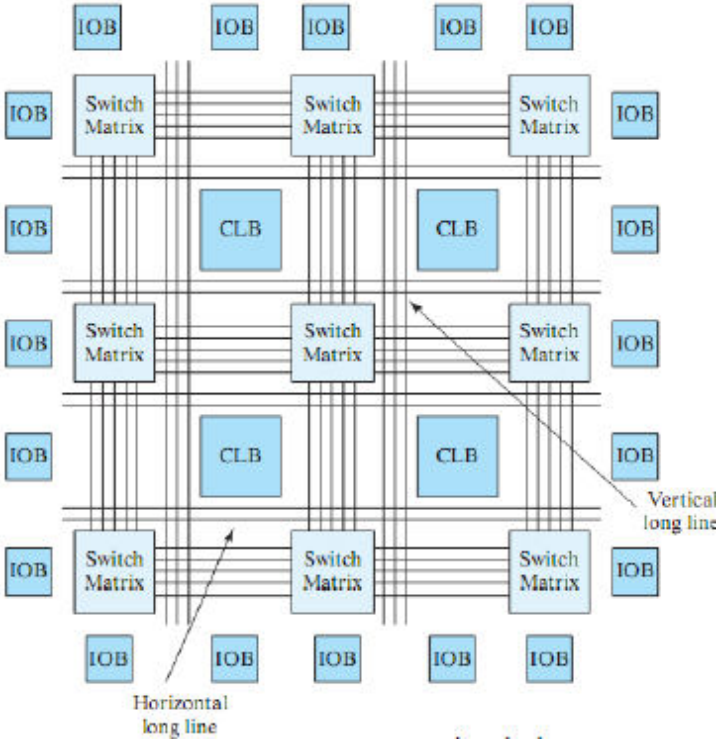
- Many FPGAs can be reprogrammed to implement different logic functions, allowing flexible reconfigurable computing as performed in computer software.
- FPGAs can be reprogrammed to desired application or functionality requirements after manufacturing.
- FPGAs have the greatest logic capacity.
- Consist of an array of anywhere from 64 to thousands of logic gates groups that are sometimes called logic blocks.
- Two basics classes of FPGA are course grained and fine grained.
- FPGAs come in packages ranging up to 1000 pins or more.

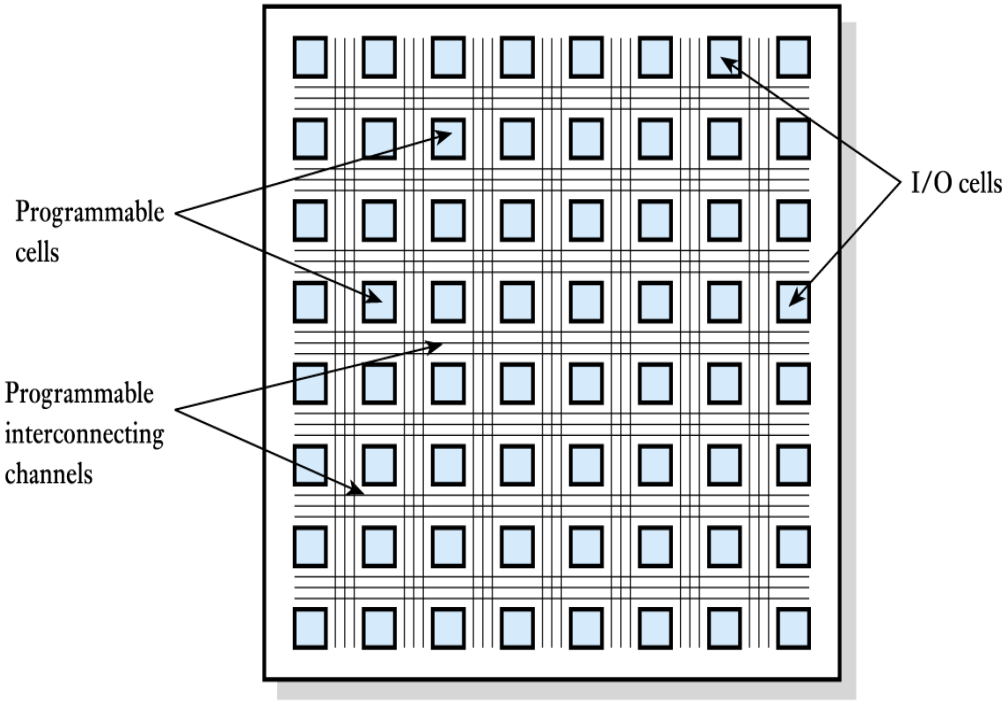
Cont…

Xilinx FPGAs

- Configurable Logic Block (CLB)
- Programmable logic and FFs
- Programmable Interconnects
- Switch Matrices
- Horizontal/vertical lines
- I/O Block (IOB)
- Programmable I/O pins

Cont…



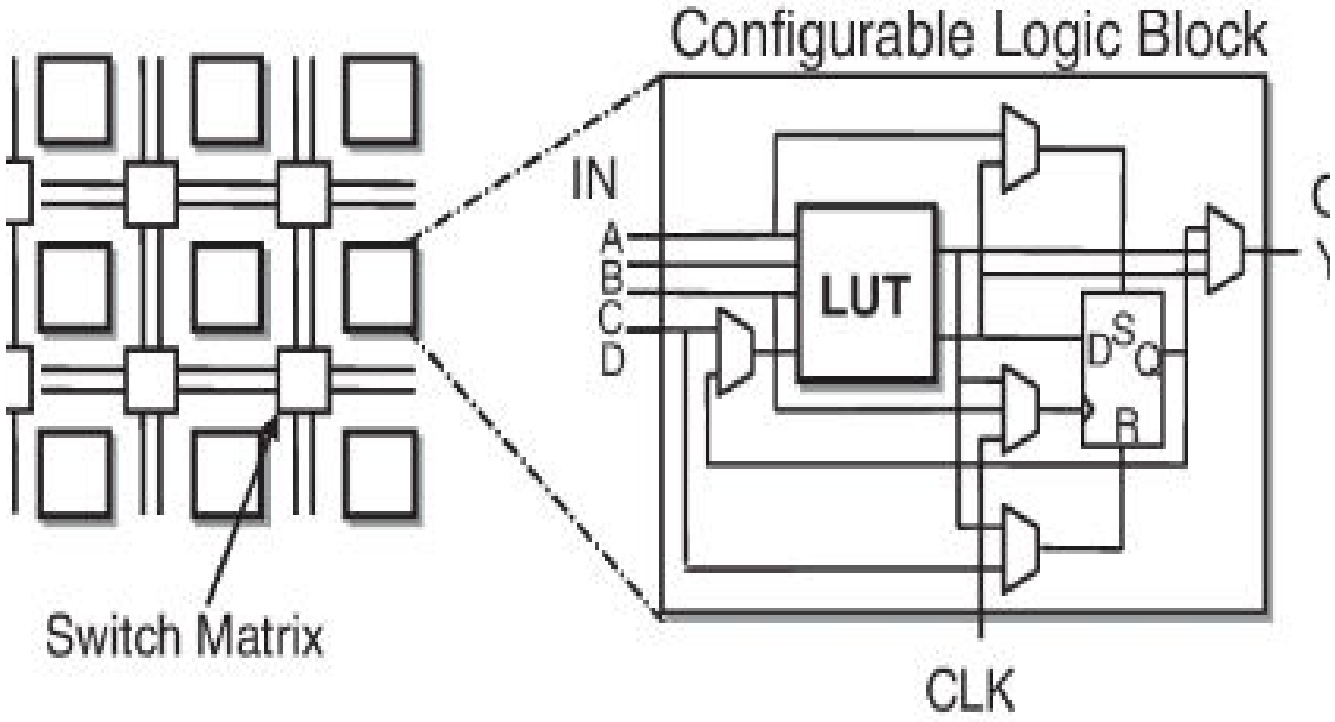


Field programmable gate arrays

FPGA

- The CLBs need to interact with one another and with external circuitry. For these purposes, the FPGA uses a matrix of programmable interconnects and input/output (I/O) blocks. The FPGA's "program" is stored in SRAM cells that influence the functionality of the CLBs and control the switches that establish the connection pathways.
- **CLB**: The general idea is that CLBs include look-up tables, storage elements (flip-flops or registers), and multiplexers that allow the CLB to perform Boolean, data-storage, and arithmetic operations.
- **I/O Block**: An I/O block consists of various components that facilitate communication between the CLBs and other components on the board. These include pull-up/pull-down resistors, buffers, and inverters. I/O blocks have buffers for compatibility with TTL and CMOS signal levels. It can be used as input, output and bidirectional blocks.
- **Interconnect resources:** A grid of switch matrix is there to provide general purpose interconnect for routing.

FPGA


Configurable Logic Block
IN
A
B
C
D
LUT
D
S
Q
R
Switch Matrix
CLK

CLB

Cont…

FPGA KIT

Cont…

FPGA Applications

- Due to their programmable nature, FPGAs are an ideal fit for many different markets. As the industry leader, Xilinx provides comprehensive solutions consisting of FPGA devices, advanced software, and configurable, ready-to-use IP cores for markets and applications such as:
- **Aerospace & Defence** - Radiation-tolerant FPGAs along with intellectual property for image processing, waveform generation.
- **Audio** - Xilinx FPGAs and targeted design platforms enable higher degrees of flexibility, faster time-to-market, and lower costs for a wide range of audio, communications, and multimedia applications.
- **Security** - Xilinx offers solutions that meet the evolving needs of security applications, from access control to surveillance and safety systems.

Cont…

- **Automotive** - Automotive silicon and IP solutions for gateway and driver assistance systems, comfort, convenience, and in-vehicle infotainment.
- **Broadcast** - Adapt to changing requirements faster and lengthen product life cycles with Broadcast Targeted Design Platforms and solutions for high-end professional broadcast systems.
- **Consumer Electronics** - Cost-effective solutions enabling next generation, full-featured consumer applications, digital flat panel displays, information appliances, home networking, and residential set top boxes.
- **Data Centre** - Designed for high-bandwidth, low-latency servers, networking, and storage applications to bring higher value into cloud deployments.
- **Medical** - For diagnostic, monitoring, and therapy applications, the Virtex FPGA and Spartan® FPGA families can be used to meet a range of processing, display, and I/O interface requirements.

Cont…

- **Industrial** - Xilinx FPGAs and targeted design platforms for Industrial, Scientific and Medical (ISM) enable higher degrees of flexibility, faster time-to-market, and lower overall cost for a wide range of applications such as industrial imaging and surveillance, industrial automation, and medical imaging equipment.
- **Video & Image Processing** - Xilinx FPGAs and targeted design platforms enable higher degrees of flexibility, faster time-to-market, and lower overall cost for a wide range of video and imaging applications.

Daily Quiz

- Which type of device FPGA are?
  a) SLD
  b) SROM
  c) EPROM
  d) PLD

- The FPGA refers to _____
  a) First programmable Gate Array
  b) Field Programmable Gate Array
  c) First Program Gate Array
  d) Field Program Gate Array

Daily Quiz

- In FPGA, vertical and horizontal directions are separated by _____
  a) A line
  b) A channel
  c) A strobe
  d) A flip-flop

- Which of the following are applications of PLAs?
- A. Configurable PALs
  B. Registered PALs
  C. FPGA programs
  D. All of the these
  E. Both A & B

Weekly Assignment

- Explain Architecture of FPGA in detail.
- Discuss any two types of programming technology used in FPGA design.
- Explain FPGA Prototyping.
- Write the Comparison between FPGA and CPLD.
- Explain difference between FPGA and PLD.

Topic link

- https://www.youtube.com/watch?v=EDbutwR35bg&list=PLbMVogVj5nJSY-1XxFHgwgtj2F7mB7NuV
- https://www.youtube.com/watch?v=BNLV5wZgg8c
- https://www.youtube.com/watch?v=FWE0-FOoE4s&list=PLUtfVcb-iqn-EkuBs3arreilxa2UKIChl

MCQs

1. Which of the following is the largest unit of storage?

- Gigabyte (GB)
- Kilobyte (KB)
- Megabyte (MB)
- **Terabyte (TB)**

2. The complex programmable logic device contains several PLD blocks and _____

- A language compiler
- AND/OR arrays
- **Global interconnection matrix**
- Field-programmable switches

MCQs

4 If a PAL has been programmed once _____

- Its logic capacity is lost
- Its outputs are only active HIGH
- Its outputs are only active LOW
- **It cannot be reprogrammed**

5. Which one has programmable AND as well as programmable OR?

- PAL
- **PLA**
- PROM
- None of the above

MCQs

5. Applications of PLAs are _____

- Registered PALs
- Configurable PALs
- PAL programming
- **All of the Mentioned**

6. What is memory decoding?

- The process of Memory IC used in a digital system is overloaded with data
- The process of Memory IC used in a digital system is selected for the range of address assigned
- The process of Memory IC used in a digital system is selected for the range of data assigned
- The process of Memory IC used in a digital system is overloaded with data allocated in memory cell

MCQs

7. The first step in the design of memory decoder is _____

- Selection of a EPROM
- Selection of a RAM
- **Address assignment**
- Data insertion

8. Why antifuses are implemented in a PLD?

- To protect from high voltage
- To increase the memory
- **To implement the programmes**
- As a switching devices

MCQ s

9. Why did PROM introduced?

- To increase the storage capacity
- To increase the address locations
- **To provide flexibility**
- To reduce the size

10. Which of the following is programmed electrically by the user?

- ROM
- EPROM
- **PROM**
- EEPROM

Glossary questions

- Choose the correct one from the given answers for the following questions:
  = (Output lines, Programmable Array Logic, AND gates
  AND and OR arrays)

  A. The inputs in the PLD is given through _____
  B. PAL refers to _____
  C. Outputs of the AND gate in PLD is known as _____
  D.PLA contains _____

Cont…

- Choose the correct one from the given answers for the following questions:
  = (a global interconnection matrix; NOT, AND, OR;
  PLD ; it cannot be reprogrammed)
- A. (Once a PAL has been programmed:
  B. PLAs, CPLDs, and FPGAs are all which type of device?
  C. The basic programmable logic array (PLA) contains a set of _____ gates, _____ gates, and _____ gates.
- D. The complex programmable logic device (CPLD) contains several PLD blocks and:

Cont…

- Choose the correct one from the given answers for the following questions: = (Address; Combinational circuit; They do not lose memory when power is removed;
  Decoder and OR gates)

  A. The ROM is a _____

  B. ROM is made up of _____

  C. Why are ROMs called non-volatile memory?

  D.In ROM, each bit is a combination of the address variables is called _____

Cont…

- Choose the correct one from the given answers for the following questions:
  = (Within CPU;5; Registers; Both registers and main memory)

  A. Memories are classified into _____ categories.
  B. Secondary memory is also known as _____
  C. In a computer, registers are present _____
  D.Which of the following has the lowest access time?

Cont…

- Choose the correct one from the given answers for the following questions: =(Floppy disk; Semiconductors; Both Secondary Memory and Auxiliary Memory ; Secondary Memory)

  A. Main memories of a computer, usually made up of _____

  B. As the storage capacity of the main memory is inadequate, which memory is used to enhance it?

  C. Which memories are if magnetic memory type?

  D.Which of the following comes under secondary memory/ies?

Old Question Papers

(SEM-III) THEORY EXAMINATION 2019-20
DIGITAL SYSTEM DESIGN

Time: 3 Hours ***Total Marks: 100***

Note: Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief. **2 x 10 = 20**

Qno.	Question	Marks	CO
a.	The solution to the quadratic equation $k^2 - 11k + 22 = 0$ are x = 3 and x = 6. What is the base of the number system?	2	1
b.	Simplify the expression F (A, B, C, D) = ACD+$\bar{A}$ B + $\bar{D}$ by K- Map.	2	1
c.	Construct half subtractor using logic gates.	2	2
d.	Implement a 4:1 multiplexer using 2:1 multiplexer.	2	2
e.	What do you mean by race around condition in JK Flip Flop?	2	3
f.	Distinguish between Leach and Flip Flop.	2	3
g.	What is logic family? Give the classification of logic families in brief.	2	4
h.	Describe figure of merit & noise immunity of TTL & CMOS ICs.	2	4
i.	What are the advantages and disadvantages of flash type ADC?	2	5
j.	The basic step of a 9-bit DAC is 10.3 mV. If 000000000 represents 0Volts, what is the output for an input of 101101111?	2	5

SECTION B

2. Attempt any *three* of the following: **3 x 10 = 30**

Qno.	Question	Marks	CO
a.	Design an excess-3 to BCD code converter.	10	1
b.	Implement a full adder by using 8:1 multiplexer.	10	2
c.	Design a sequential circuit with two Flip Flops, A & B and one input x. When x=0, the State of the circuit remains the same when x=1 the circuit passes through the state transitions from 00 to 01 to 11 to 10 back to 00 & repeat.	10	3
d.	Compare TTL and CMOS logic families and also draw CMOS NOR gate.	10	4
e.	Explain the operation of successive approximation ADC. Discuss it merits and demerits.	10	5

SECTION C

3. Attempt any *one* part of the following: **1 x 10 = 10**

Qno.	Question	Marks	CO
a.	Minimize the logic function using Quine-McCluskey Method $F(A, B, C, D, E) = \sum m(8,9,10,11,13,15,16,18,21,24,25,26,27,30,31)$	10	1
b.	Simplify the logic expression using K-Map $F(A,B,C,D,E,F) = \sum m(0,5,7,8,9,12,13,23,24,25,28,29,37,40,42,44,46,55,56,57,60,61)$	10	1

Old Question Papers

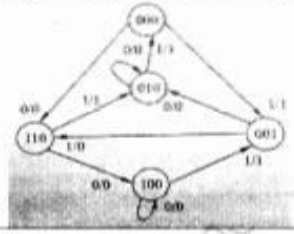
Printed Page 2 of 2 | Sub Code:KEC302

Paper Id: 130322 | Roll No:

4. Attempt any *one* part of the following: 1 x 10 = 10

Qno.	Question	Marks	CO
a.	Design a 4-bit parallel binary Adder/Subtractor circuit.	10	2
b.	Design a 4-bit comparator circuit using logic gates.	10	2

5. Attempt any *one* part of the following: 1 x 10 = 10

Qno.	Question	Marks	CO
a.	Discuss Mealy and Moore FSM. What do you mean by excitation table?	10	3
b.	For the given state diagram design the circuit using T flip flop 	10	3

6. Attempt any *one* part of the following: 1 x 10 = 10

Qno.	Question	Marks	CO
a.	Draw three input standard TTL NAND gate circuit and explain its operation.	10	4
b.	Implement the following function using PLA $F_1 = \sum m(0,3,4,7)$ $F_2 = \sum m(1,2,5,7)$	10	4

7. Attempt any *one* part of the following: 1 x 10 = 10

Qno.	Question	Marks	CO
a.	With a neat diagram explain the operation of R-2R DAC.	10	5
b.	With a neat sketch explain the operation of Flash ADC.	10	5

Sessional Paper-1

Printed page: 2 of 2 **Subject Code:**MACSE0304
Roll No: | | | | | | | | | | | | | |

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY ,GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

M.tech. (Int.) CSE

(SEM:III, SESSIONAL EXAMINATION –I)(2021-2022)

Subject Name: Digital Logic & Circuit Design

Time: 1.15Hours **Max. Marks:30**

General Instructions:

- All questions are compulsory. Answers should be brief and to the point.
- This Question paper consists of 2 pages &5questions.
- It comprises of three Sections, A, B, and C. You are to attempt all the sections.
- Section A -Question No- 1 is objective type questions carrying 1 mark each, Question No- 2 is very short answer type carrying 2 mark each. You are expected to answer them as directed.
- Section B - Question No-3 is Short answer type questions carrying 5 marks each. You need to attempt any two out of three questions given.
- Section C -Question No. 4 &5are Long answer type (within unit choice) questions carrying 6marks each. You need to attempt any one part *a or b.*
- Students are instructed to cross the blank sheets before handing over the answer sheet to the invigilator.
- No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.

		SECTION – A	[8]	CO	Blooms Level
1.	**Attempt all parts**		**(4×1=4)**	**CO**	**K**
	a.	The XOR gates output will be low if two inputs are _____ a) 00 b) 01 c) 10 d) None of these	**(1)**	**CO1**	**K2**
	b.	A universal logic gate is one which can be used to generate any logic function. Which of the following is a universal logic gate? a) OR b) AND c) XOR d) NAND	**(1)**	**CO1**	**K1**
	c.	2's Complement of a binary number $(10101110)_2$ a) 01010001 b) 11010001 c) 01010010 d) 11010111	**(1)**	**CO1**	**K2**
	d.	DeMorgan's theorem states that _____ a) (A.B)' = A' + B' b) (A + B)' = A'. B c) A' + B' = A'.B' d) (A.B)' = A' + B	**(1)**	**CO1**	**K1**

Sessional Paper-2

Printed page: .... **Subject Code: MACSE0304**

Roll No: | | | | | | | | | | | | | |

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY ,GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

M.tech. (Int.) CSE

(SEM:...III..SESSIONAL EXAMINATION –I)(2021-2022)

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- No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.

		SECTION – A	[8]	CO	Blooms Level
1.	**Attempt all parts**		**(4×1=4)**	**CO**	**K**
	a.	A universal logic gate is one which can be used to generate any logic function. Which of the following is a universal logic gate? a) OR b) AND c) XOR d) NAND	**(1)**	**CO1**	**K1**
	b.	The NOR gate output will be high if the two inputs are _____ a) 00 b) 01 c) 10 d) 11	**(1)**	**CO1**	**K1**
	c.	Excess-3 code of 739 is: a) 1010 0110 1100 b) 1101 1001 1000 c) 1101 0110 1100 d) 1010 1001 1000	**(1)**	**CO1**	**K2**
	d.	Binary equivalent of gray code 101011 is: a) 110010 b) 101010	**(1)**	**CO1**	**K2**

Expected Questions for University Exam

- Design X = AB' + B'AC & Y = A'BC + ABC using PLA.
- Design 3 bit multiplier using PROM.
- Differentiate between SRAM and DRAM.
- Design Full adder using PROM.
- Differentiate between PLA & PAL.
- Implement 2:1 MUX using PAL
- What is programmable logic array?

Expected Questions for University Exam

- What is programmable logic array?
- What are the draw backs of PLAs? How PLAs are used to implement combinational and sequential logic circuits?
- Explain the detailed Architecture of CPLD and its Implementations .
- Draw the basic circuit diagram of static RAM and explain its operation
- Design a PAL to realize a full Adder circuit.
- Draw the structure of a 4×4 static RAM and explain it's operation.

FACULTY VIDEO LINKS, YOUTUBE & NPTEL VIDEO LINKS AND ONLINE COURSES DETAILS

Youtube/other Video Links:

- https://www.youtube.com/watch?v=_eAL-v5oNOw
- https://www.youtube.com/watch?v=X-XwOXdUPU4
- https://www.youtube.com/watch?v=cIlKSD8ptAk
- https://www.youtube.com/watch?v=EDbutwR35bg&list=PLbMVogVj5nJSY-1XxFHgwgtj2F7mB7NuV
- https://www.youtube.com/watch?v=BNLV5wZgg8c
- https://www.youtube.com/watch?v=FWE0-FOoE4s&list=PLUtfVcb-iqn-EkuBs3arreilxa2UKIChl

References

1. R.P. Jain, “Modern Digital Electronics,” Tata McGraw Hill, 4th edition, 2009.
2. A. Anand Kumar, “Fundamental of Digital Circuits,” PHI 4th edition, 2018.
3. W.H. Gothmann, “Digital Electronics- An Introduction to Theory and Practice,” PHI, 2nd edition, 2006.

Thank You