Sequential Circuit Design

Unit: 03

DIGITAL LOGIC & CIRCUIT DESIGN

SUBJECT CODE: ACSE0304

B Tech III Sem

Ms. Nidhi Sharma
Associate Professor

Department of Electronics and Communication Engineering

Brief Introduction

Ms. Nidhi Sharma

- PhD Amity University, Pursuing
- M.Tech AKTU, Lucknow, India
- B.Tech. Kurukshetra University, Kkr. , Haryana

Research Interests

VLSI Design, Communication System, Internet of Things.

Industrial Experiance: (2.5 Years)

Academic Experience: (17+ years)

Publication : 08 (Peer Reviewed journals), 05(International Conference), 01 National conference.

Evaluation Scheme

Sl. No.	Subject Codes	Subject Name	Periods			Evaluation Schemes				End Semester		Total	Credit
			L	T	P	CT	TA	TOTAL	PS	TE	PE		
WEEKS COMPULSORY INDUCTION PROGRAM													
1	AAS0301A	Engineering Mathematics-III	3	1	0	30	20	50		100		150	4
2	ACSE0306	Discrete Structures	3	0	0	30	20	50		100		150	3
3	ACSE0304	Digital Logic & Circuit Design	3	0	0	30	20	50		100		150	3
4	ACSE0301	Data Structures	3	1	0	30	20	50		100		150	4
5	ACS0301	Introduction to Cloud Computing	3	0	0	30	20	50		100		150	3
6	ACSE0305	Computer Organization and Architecture	3	0	0	30	20	50		100		150	3
7	ACSE0354	Digital Logic & Circuit Design Lab	0	0	2				25		25	50	1
8	ACSE0351	Data Structures Lab	0	0	2				25		25	50	1
9	ACS0351	Cloud Computing lab	0	0	2				25		25	50	1
10	ACSE0359	Internship Assessment-I	0	0	2				50			50	1
11	ANC0301/ ANC0302	Cyber Security*/ Environmental Science*(Non Credit)	2	0	0	30	20	50		50		100	0
12		MOOCs (For B.Tech. Hons. Degree)											
		GRAND TOTAL										**1100**	**24**

Course Contents / Syllabus

UNIT-I: Digital System and Binary Numbers: Number System and its arithmetic, Signed binary numbers, Binary codes, Cyclic codes, Hamming Code, Simplification of Boolean Expression: K-map method up to five variable, SOP and POS Simplification Don't Care Conditions, NAND and NOR implementation, Quine Mc-Clusky Method (Tabular Method).

UNIT II : Combinational Logic: Combinational Circuits: Analysis Procedure, Design Procedure, Code Converter, Binary Adder-Subtractor, Decimal Adder, Binary Multiplier, Magnitude Comparator, Decoders, Encoders Multiplexers, Demultiplexers.

UNIT III: Sequential Logic and Its Applications: Storage elements: Latches & Flip Flops, Characteristic Equations of Flip Flops, Excitation Table of Flip Flops, Flip Flop Conversion, Registers, Shift Registers, Ripple Counters, Synchronous Counters, Other Counters: Johnson & Ring Counter.

UNIT IV: Synchronous & Asynchronous Sequential Circuits: Analysis of clocked Sequential Circuits with State Machine Designing, State Reduction and Assignments, Design Procedure.
Analysis procedure of Asynchronous Sequential Circuits, Circuit with Latches, Design Procedure, Reduction of State and flow Table, Race-free State Assignment, Hazards.

UNIT-V: Memory & Programmable Logic Devices: Basic concepts and hierarchy of Memory, Memory Decoding, RAM: SRAM, DRAM, ROM: PROM, EPROM, Auxiliary Memories, PLDs: PLA, PAL; Circuit Implementation using ROM, PLA and PAL; CPLD and FPGA..

CONTENT

- Course Objective
- Unit Objective
- Course Outcome
- Co and Po Mapping
- Topic Objective
- Prerequisite
- SR,JK,D,T, Master – Slave JK Flip Flop
- State Table
- State Diagram
- State Reduction
- Analysis of Sequential Circuit
- Design of Sequential Circuits
- Ripple, Synchronous Counter
- Shift Register
- Finite State Machine
- Daily quiz & MCQs
- Old Question Papers
- Recap
- Video Links
- Weekly Assignments
- References

Course Objective

The intended objectives of this course are given as follows:

- To learn number representation and conversion between different representation.
- To analyze logic processes and implement logical operations using combinational logic circuits.
- To learn concepts of sequential circuits and analyze sequential circuits in terms of state machine.
- To learn to design synchronus and asynchronus circuits.
- To learn concept of memories and PLDs.

Unit Objective

The intended objectives of this unit are:

1. To learn various flip flops and their specifications.
2. To differentiate between latches and flip flops.
3. To analyze and design synchronous sequential circuits.
4. To explain shift registers and counters.

Course Outcome

At the end of this course students will able to:

- Develop a digital logic and apply it to solve real life problems.
- Design and analyze modular combinational circuits with MUX/ DEMUX, Decoder & Encoder.
- Design and analyze different sequential circuits and their applications.
- Classify digital logic families, memories and implement logic circuits through programmable logic devices.
- Understand and analyze ADC and DAC.

CO-PO and PSO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
ACSE0304.1	3	2	-	-	-	-	-	-	-	-	-	2
ACSE0304.2	3	3	2	-	-	-	-	-	-	-	-	2
ACSE0304.3	2	3	2	2	-	-	-	-	-	-	-	2
ACSE0304.4	3	3	3	2	-	-	-	-	-	-	-	2
ACSE0304.5	3	2	1	-	-	-	-	-	-	-	-	2
AVERAGE	2.8	2.6	2	2	-	-	-	-	-	-	-	2

Course Outcome	PSO1	PSO2	PSO3
ACSE0304.1	3	-	3
ACSE0304.2	2	-	3
ACSE0304.3	2	-	3
ACSE0304.4	2	-	3
ACSE0304.5	2	-	3
Average	2.2	-	3

ROAD MAP

PRE REQUISITE

INTRODUCTION (CONCEPTS / THEORY)

NUMERICAL PRACTICE

QUIZZES, ASSIGNMENTS & UNIT TESTS

LABORATORY

PERFORMANCE EVALUATION (Mid Term, End Sem Exam)

Latches

Topic Objective	Mapping with CO
To understand basics of sequential circuits.	CO3
To have a basic understanding of latches.	CO3

Latches

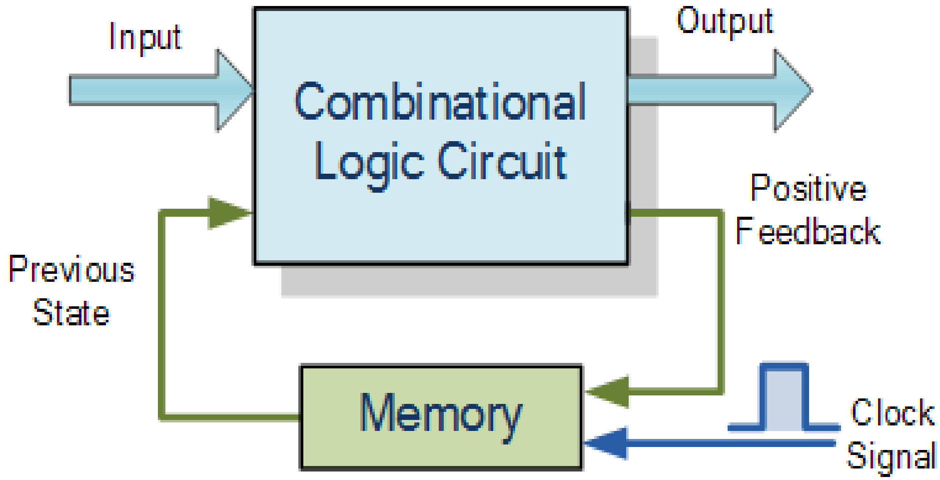
Prerequisite:

- Basic knowledge of logic gates.
- Knowledge of combinational circuits.

Introduction

Sequential Logic Representation

- The word “Sequential” means that things happen in a “sequence”, one after another and in Sequential Logic circuits, the actual clock signal determines when things will happen next.



Introduction

- It consists of a combinational circuit to which memory elements are connected to form a feedback path.
- The memory elements are devices capable of storing binary information within them. The binary information stored in the memory elements at any given time defines the state of the sequential circuit.
- The sequential circuit receives binary information from external inputs. These inputs, together with the present state of the memory elements, determine the binary value at the output terminals.
- Flip-flops, Latches and Counters and which themselves can be made by simply connecting together universal NAND Gates and/or NOR Gates in a particular combinational way to produce the required sequential circuit.

Introduction

- There are two main types of sequential circuits. Their classification depends on the timing of their signals.
- A synchronous sequential circuit is a system whose behaviour can be defined from the knowledge of its signals at discrete instants of time.
- The behaviour of an asynchronous sequential circuit depends upon the order in which its input signals change and can be affected at any instant of time.
- The memory elements commonly used in asynchronous sequential circuits are time-delay devices.
- The basic memory elements are latches and flip-flops. Latches are level sensitive and flip-flops are edge sensitive.

Latches

- A Latch is a special type of logical circuit.
- The latches have low and high two stable states.
- A latch has a feedback path, so information can be retained by the device. Therefore latches can be memory devices, and can store one bit of data for as long as the device is powered.
- The latches can be constructed from two NAND gates or two NOR gates.

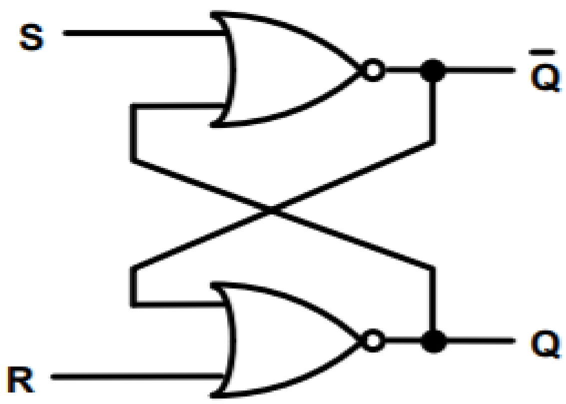
<u>Types of Latches:</u>

- SR Latch.
- D Latch.
- J-K Latch.
- T Latch.

SR Latch

SR Latch using NOR Gate:

- SR latch stands for set/reset latch.



S	R	Q_{n+1}	$\bar{Q}_{n+1}$	Operation
0	0	Q_n	$\bar{Q}_n$	No change
0	1	0	1	Reset
1	0	1	0	Set
1	1	X	X	Invalid

- The cross-coupled connection from the output of one gate to the input of the other gate constitutes a feedback path.
- Each latch has two outputs, Q and *Q', and two inputs, set and reset.*

SR Latch

Operation:

- If S = 1 and R = 0, Q becomes 1. Let us explain how.
- NOR gate always gives output 0 when at least one of the inputs is 1.
- So when S is applied as 1 the output of gate G2 i.e. is 0 irrespective of the condition of second input Q to the gate.
- Now is the input of gate G1 so both the inputs of G1 become 0 as R is already 0. So, the output of G1 is now or 1.
- So whatever may be the previous condition of Q, it always becomes Q = 1 and Q' = 0 when S = 1 and R = 0. This is called the SET condition of the latch.

SR Latch

- If S = 0 and R = 1, Q becomes 0. Let us explain how.
- As we already said, a NOR gate always gives output 0 when at least one of the inputs is 1.
- So when R is applied as 1, the output of gate G1 i.e. Q is 0 irrespective of the condition of the second input to the gate.
- So, whatever may be the previous condition of Q, it always becomes 0 this 0 is then fed back to the input of gate G2. As here S is already 0, both inputs of G2 are 0. Hence the output of G2 i.e. will be 1. So, Q = 0 and Q' = 1 when, S = 0 and R = 1. This is called the RESET condition of the latch.

SR Latch

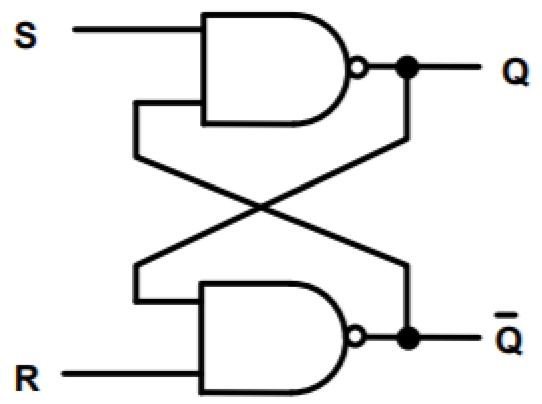
- If S = 0 and also R = 0, Q remains the same as it was.
- First suppose Q is previously 1.
- Now the inputs of G2 are 0 and 1 as S=0 and Q=1. So output of G2 is 0.
- Now both inputs of G1 are 0 as R=0 and Q' =0. So the output of G1 is 1.
- Now suppose Q is previously 0.
- Now both inputs of G2 are 0 as S = 0 and Q = 0. So the output of G2 is 1.
- Now the inputs of G1 are 0 and 1 as R=0 and Q= 1. So the output of G1 is 0.
- So it is proved that Q remains the same as it is when S = 0 and also R = 0 in SR latch of flip flop.

SR Latch

- If S = 1 and also R = 1, the condition of Q is totally unpredictable. Let us explain how.
- First suppose Q is previously 1.
- Now both inputs of G2 are 1 as S = 1 and Q = 1. So output of G2 is 0.
- Now the inputs of G1 are 1 and 0 as R = 1 and Q' = 0. So the output of G1 is 0. That means Q is changed.
- Now Q is 0. So inputs of G2 are 1 and 0 as S = 1 and Q = 0. So the output of G2 is 0. That means is unchanged.
- Now the inputs of G1 are 1 and 0 as R = 1 and Q' = 0. So the output of G1 is 0. That means Q is unchanged.
- So, when both S and R are 1, it becomes unpredictable whether the value of output Q will be changed or unchanged. This condition of SR latch normally avoided. As the latch is SET when S = 1(HIGH), the latch is called Active High SR Latch.

SR Latch

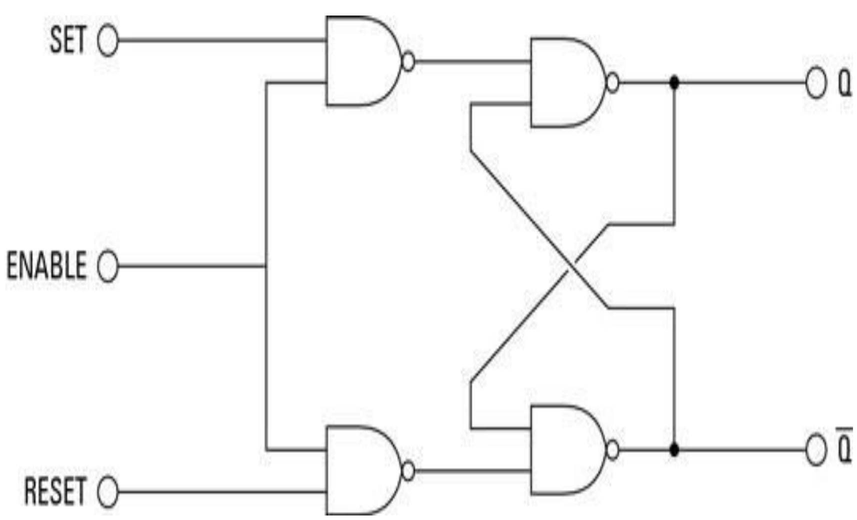
SR Latch using NAND Gate:



S	R	Q_{n+1}	$\bar{Q}_{n+1}$	Operation
0	0	X	X	Invalid
0	1	1	0	Set
1	0	0	1	Reset
1	1	Q_n	$\bar{Q}_n$	No change

Gated SR Latch

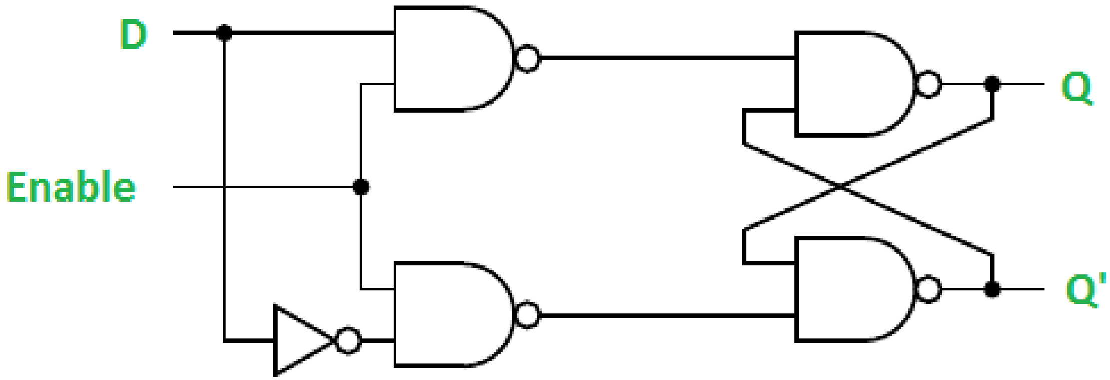
- A gated SR latch (or clocked SR Latch) can only change its output state when there is an enabling signal along with required inputs. For this reason it is also known as a **synchronous SR latch**
- In other words, the latch is active when ENABLE signal is HIGH and it is inactive when ENABLE signal is LOW.



E	**S**	**R**	$\mathbf{Q_{n+1}}$	$\mathbf{\bar{Q}_{n+1}}$	**Operation**
0	X	X	Q_n	$\bar{Q}_n$	No Change
1	0	0	Q_n	$\bar{Q}_n$	No Change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	X	X	Invalid

Gated D Latch

- There is one drawback of SR Latch. That is the next state value can't be predicted when both the inputs S & R are one. So, we can overcome this difficulty by D Latch. It is also called as Data Latch. The **circuit diagram** of D Latch is shown in the following figure.



E	D	Q_{n+1}	$\bar{Q}_{n+1}$
0	X	Q_n	$\bar{Q}_n$
1	0	0	1
1	1	1	0

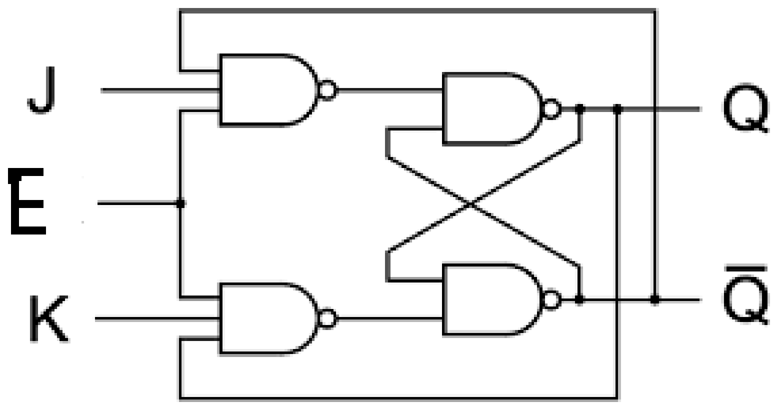
Gated JK Latch

- The basic S-R NAND circuit has many advantages and uses in sequential logic circuits but it suffers from two basic switching problems.

  1.the Set = 1 and Reset = 1 condition (S = R = 0) must always be avoided

  2. if Set or Reset change state while the enable (EN) input is high the correct latching action may not occur

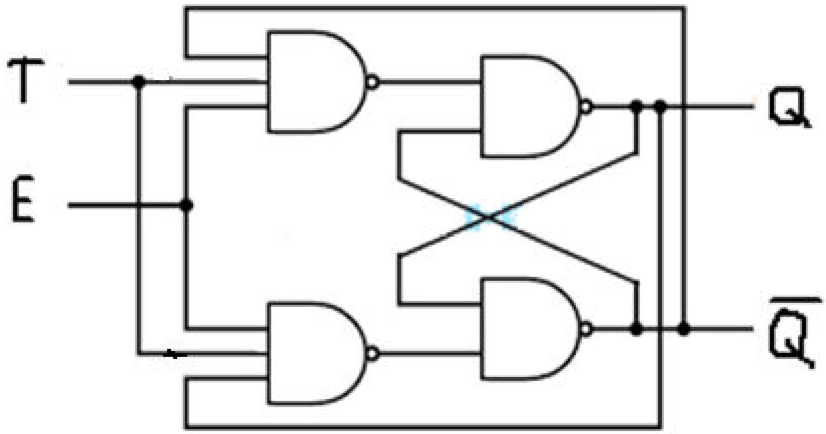
- Then to overcome these two fundamental design problems with the SR flip-flop design, the **JK flip Flop** was developed.



E	J	K	Q_{n+1}	$\bar{Q}_{n+1}$	Operation
0	X	X	Q_n	$\bar{Q}_n$	No Change
1	0	0	Q_n	$\bar{Q}_n$	No change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	$\bar{Q}_n$	Q_n	Toggle

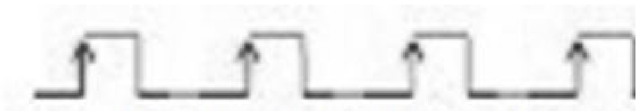
Gated T Latch

- The **T latch** can be formed whenever the JK latch inputs are shorted. The function of T Latch will be like this when the input of the latch is high, and then the output will be toggled.



E	T	Q_{n+1}	$\bar{Q}_{n+1}$	Operation
0	X	Q_n	$\bar{Q}_n$	No Change
1	0	Q_n	$\bar{Q}_n$	No Change
1	1	$\bar{Q}_n$	Q_n	Toggle

Difference between Level Triggering & Edge Triggering:

Level Triggering	Edge Triggering
In level triggering the circuit will become active when the gating pulse is on a particular level.	In edge triggering the circuit becomes active at negative or positive edge of the clock signal.
An event occurs during the high voltage level or low voltage level.	An event occurs at the rising edge or falling edge.
Latches are level triggered.	Filp-flops are edge triggered.
Asynchronous	Synchronous
	

Recap

- **Sequential circuits** consists of a combinational circuit to which memory elements are connected to form a feedback path.
- The memory elements are devices capable of storing binary information within them. The binary information stored in the memory elements at any given time defines the state of the sequential circuit.
- A latch has a feedback path, so information can be retained by the device. Therefore latches can be memory devices, and can store one bit of data for as long as the device is powered.

<u>Types of Latches:</u>

- SR Latch.
- D Latch.
- J-K Latch.
- T Latch.

Daily Quiz

- What do you understand by sequential circuit?
- Differentiate between combinational and sequential circuits.
- Draw & explain NAND SR latch.
- Draw & explain NOR SR latch.
- What is the use of enable signal in latch?

MCQ

- The truth table for an S-R latch has how many VALID entries?
  a) 1
  b) 2
  c) 3
  d) 4
- The logic circuits whose outputs at any instant of time depends only on the present input but also on the past outputs are called
  a) Combinational circuits
  b) Sequential circuits
  c) Latches
  d) Flip-flops
- How many types of sequential circuits are?
  a) 2 c) 4
  b) 3 d) 5
- The sequential circuit is also called ___________
  a) Flip-flop
  b) Latch
  c) Strobe
  d) Adder

Video Link

- https://nptel.ac.in/courses/117/106/117106086/
- https://www.youtube.com/watch?v=jm0PGDSSBkI&ab_channel=IITKharagpurJuly2018
- https://www.youtube.com/watch?v=ibQBb5yEDlQ&ab_channel=nptelhrd

Old Questions

- Differentiate between combinational and sequential circuits.
- Differentiate between level triggering and edge triggering?

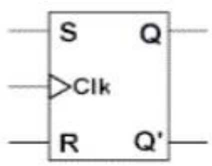
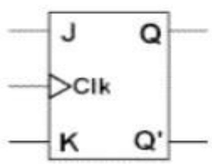
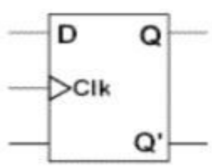
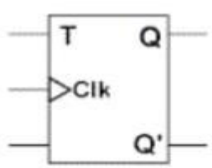
Recap of Previous Topic

- **Sequential circuits** consists of a combinational circuit to which memory elements are connected to form a feedback path.
- The memory elements are devices capable of storing binary information within them. The binary information stored in the memory elements at any given time defines the state of the sequential circuit.
- A latch has a feedback path, so information can be retained by the device. Therefore latches can be memory devices, and can store one bit of data for as long as the device is powered.

<u>Types of Latches:</u>

- SR Latch.
- D Latch.
- J-K Latch.
- T Latch.

Recap of Previous Topic

<table>
<tr><th>FLIP-FLOP NAME</th><th>FLIP-FLOP SYMBOL</th><th>CHARACTERISTIC TABLE</th><th>CHARACTERISTIC EQUATION</th><th>EXCITATION TABLE</th></tr>
<tr><td>SR</td><td>
</td><td><table><tr><th>S</th><th>R</th><th>Q(next)</th></tr><tr><td>0</td><td>0</td><td>Q</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>?</td></tr></table></td><td>Q(next) = S + R'Q
SR = 0</td><td><table><tr><th>Q</th><th>Q(next)</th><th>S</th><th>R</th></tr><tr><td>0</td><td>0</td><td>0</td><td>X</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>X</td><td>0</td></tr></table></td></tr>
<tr><td>JK</td><td>
</td><td><table><tr><th>J</th><th>K</th><th>Q(next)</th></tr><tr><td>0</td><td>0</td><td>Q</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>Q'</td></tr></table></td><td>Q(next) = JQ' + K'Q</td><td><table><tr><th>Q</th><th>Q(next)</th><th>J</th><th>K</th></tr><tr><td>0</td><td>0</td><td>0</td><td>X</td></tr><tr><td>0</td><td>1</td><td>1</td><td>X</td></tr><tr><td>1</td><td>0</td><td>X</td><td>1</td></tr><tr><td>1</td><td>1</td><td>X</td><td>0</td></tr></table></td></tr>
<tr><td>D</td><td>
</td><td><table><tr><th>D</th><th>Q(next)</th></tr><tr><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td></tr></table></td><td>Q(next) = D</td><td><table><tr><th>Q</th><th>Q(next)</th><th>D</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table></td></tr>
<tr><td>T</td><td>
</td><td><table><tr><th>T</th><th>Q(next)</th></tr><tr><td>0</td><td>Q</td></tr><tr><td>1</td><td>Q'</td></tr></table></td><td>Q(next) = TQ' + T'Q</td><td><table><tr><th>Q</th><th>Q(next)</th><th>T</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table></td></tr>
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Flip flops & Their Conversion

Topic Objective	Mapping with CO
To have a basic understanding of flip flops.	CO3
To understand flipflop conversion.	CO3

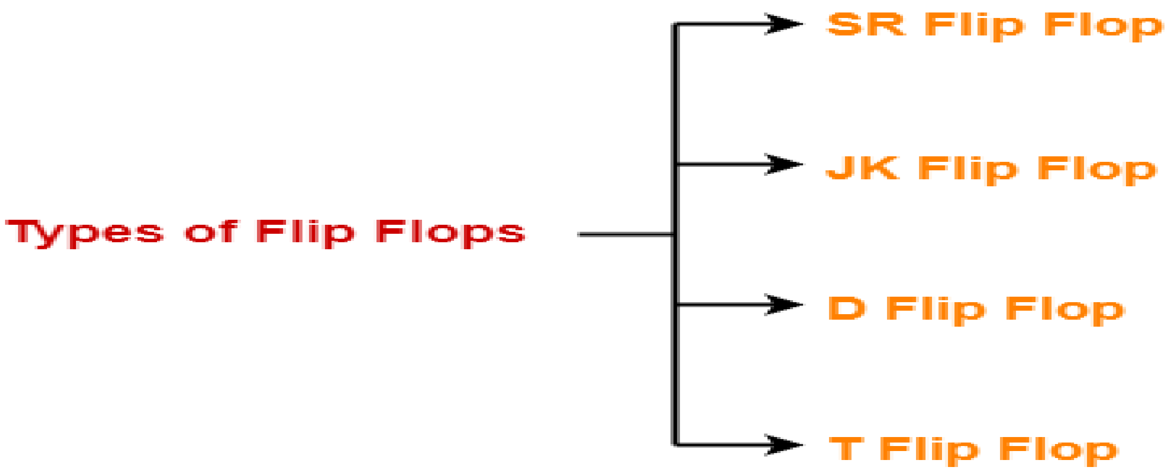
Flip flops & Their Conversion

Prerequisite:

- Basic knowledge of logic gates.
- Basic knowledge of latches.
- Knowledge of combinational circuits.

Flip Flop

- A Flip Flop is a memory element that is capable of storing one bit of information.
- It is also called as Bistable Multivibrator since it has two stable states either 0 or 1.
- There are following 4 basic types of flip flops-



SR Flip Flop

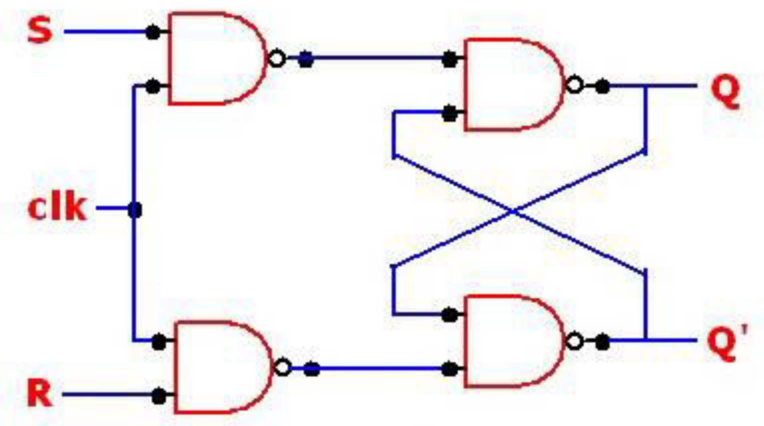
Construction of SR Flip Flop By Using NAND Latch-

This method of constructing SR Flip Flop uses-

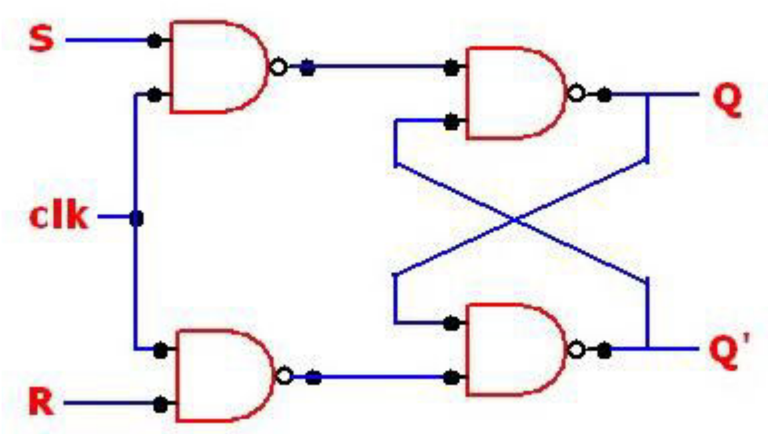
- NAND latch
- Two NAND gates

Logic Circuit-

- The logic circuit for SR Flip Flop constructed using NAND latch is as shown below:



Truth Table of SR Flip-flop:

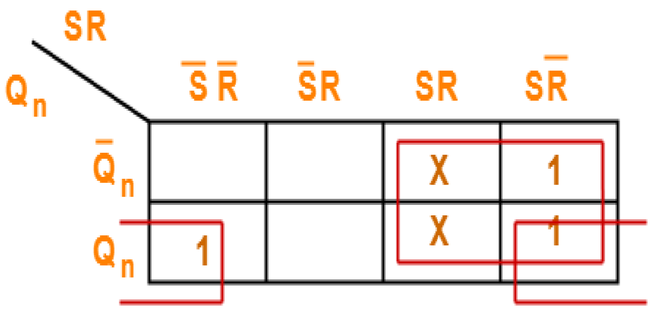


CLK	**S**	**R**	**Q_{n+1}**	**$\bar{Q}_{n+1}$**	**Operation**
1	0	0	Q_n	$\bar{Q}_n$	No Change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	X	X	Invalid

S R Flip Flop

- **Characteristic Table :**

Q_n	S	R	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	X
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	X



K Map

- Characteristic Equation of SR Flip-flop.

$$Q_{n+1} = S + Q_n \bar{R}$$

S R Flip Flop

- **Excitation Table** : For a given combination of present state Q_n and next state Q_{n+1}, excitation table tell the inputs required.
- The excitation table of any flip flop is drawn using its characteristic table.

Q_n	Q_{n+1}	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

SR Flip-Flop

Drawbacks of SR Flip Flop:

- The one major disadvantage of the S-R flip flop is that in the condition when the clock is triggered the inputs become high which is an undesirable condition because it causes invalid input ,the condition in which you can't predict the output.
- So, in short we can say that the outputs in S-R flip flop are undefined in that condition.
- JK flip flop is a refined & improved version of SR Flip Flop that has been introduced to solve the problem of indeterminate state that occurs in SR flip flop when both the inputs are 1.
- Input J behaves like input S of SR flip flop which was meant to set the flip flop.
- Input K behaves like input R of SR flip flop which was meant to reset the flip flop.

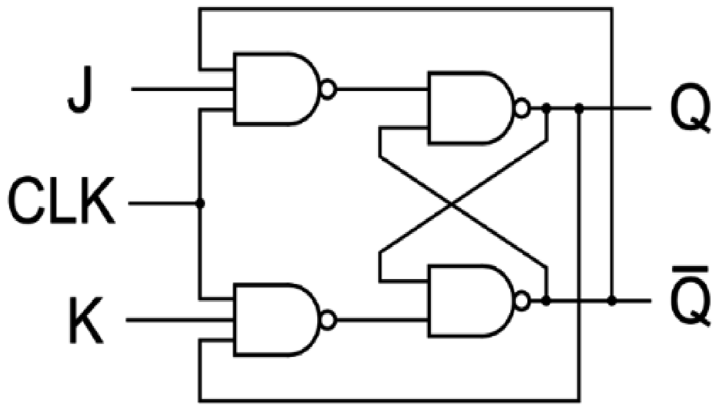
JK Flip Flop

Construction of JK Flip Flop By Using SR Flip Flop Constructed From NAND Latch-

- This method of constructing JK Flip Flop uses-
- SR Flip Flop constructed from NAND latch
- Two other connections

Logic Circuit-

- The logic circuit for JK Flip Flop constructed using SR Flip Flop constructed from NAND latch is as shown below:



CLK	J	K	Q_{n+1}	$\bar{Q}_{n+1}$	Operation
0	X	X	Q_n	$\bar{Q}_n$	No Change
1	0	0	Q_n	$\bar{Q}_n$	No change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	$\bar{Q}_n$	Q_n	Toggle

JK Flip Flop

Truth Table

- The truth table for JK Flip Flop is as shown below

INPUTS			OUTPUTS
Q_n	J	K	Q_{n+1} (Next State)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

K Map

$$Q_{n+1} = \bar{Q}_n J + Q_n \bar{K}$$

JK Flip Flop

Excitation Table-

- For a given combination of present state Q_n and next state Q_{n+1}, excitation table tell the inputs required.
- The excitation table of any flip flop is drawn using its truth table.

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

JK Flip Flop

Differences between J K Flip Flop and S R Flip Flop

- Both JK flip flop and SR flip flop are functionally same.
- The only difference between them is-
- In JK flip flop, indeterminate state does not occur.
- In JK flip flop, instead of indeterminate state, the present state toggles.
- In other words, the present state gets inverted when both the inputs are 1.

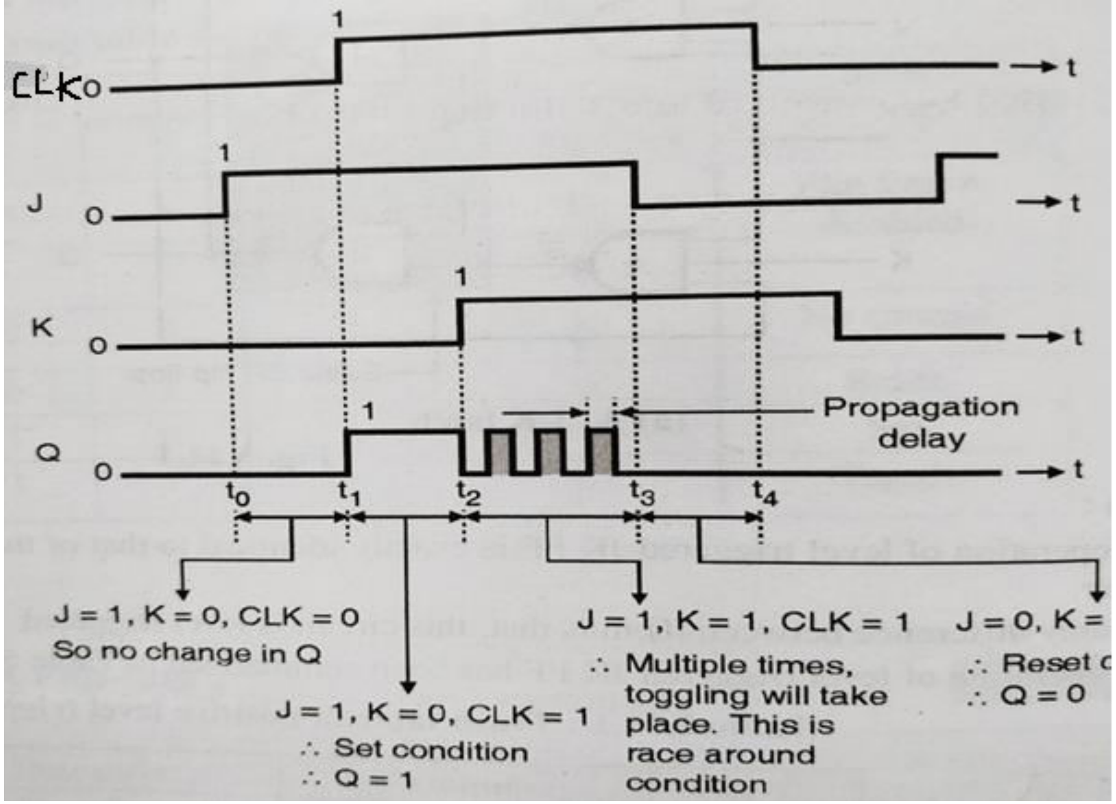
JK Flip Flop

Drawbacks of JK Flip Flop (Race around condition)

- The main drawback of the JK flip flop is the race around condition.
- It happens when both the input is 1.
- In race around condition output toggles more than one time.
- If that happens it will be very hard to predict the state of the flip flop.
- Assume present state is 1 and we are applying J=1 and K=1. what will happen the output toggles next state should be 0.
- But what happens in real scenario the output will not ended up getting 0 it will continues to toggle 010101010101010 it will go like that.

JK Flip Flop

- **Race Around Condition In JK Flip-flop** – For J-K flip-flop, if J=K=1, and if CLK=1 for a long period of time, then Q output will toggle as long as CLK is high, which makes the output of the flip-flop unstable or uncertain. This problem is called race around condition in J-K flip-flop.



JK Flip Flop

There are three methods to eliminate race around condition as described below:

- Increasing the delay of flip-flop
  - The propagation delay (delta t) should be made greater than the duration of the clock pulse (T). But it is not a good solution as increasing the delay will decrease the speed of the system.
- Use of edge-triggered flip-flop
  - If the clock is High for a time interval less than the propagation delay of the flip flop then racing around condition can be eliminated. This is done by using the edge-triggered flip flop rather than using the level-triggered flip-flop.
- Use of master-slave JK flip-flop
  - If the flip flop is made to toggle over one clock period then racing around condition can be eliminated. This is done by using Master-Slave JK flip-flop.

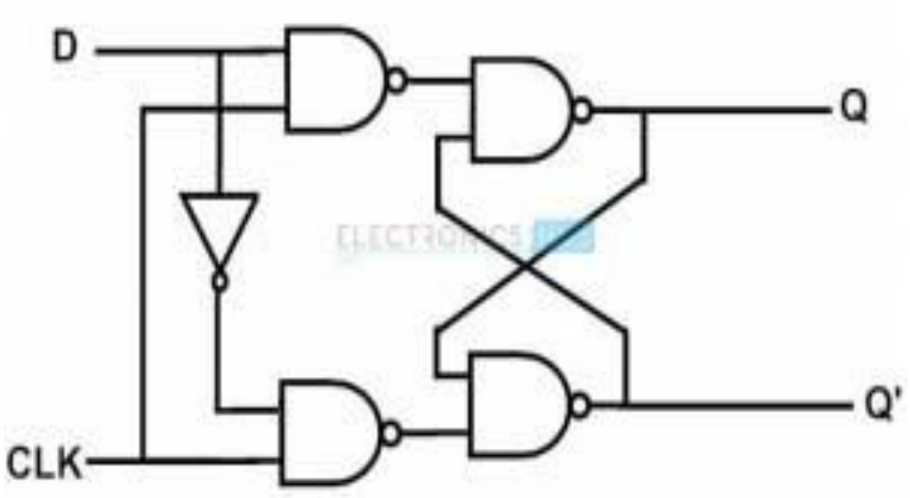
D Flip Flop

- The D stands for "data"; this flip-flop stores the value that is on the data line.
- It can be thought of as a basic memory cell.
- A D flip-flop can be made from a set/reset flip-flop by tying the set to the reset through an inverter.
- One of the salient features of a D-type flip-flop is its ability to "latch" and store and remember data.
- This property is used in creating a delay in progress of the data in the circuit used.
- There are several applications in which a D-type flip-flop is used, such as in frequency dividers and data latches.

D Flip Flop

Logic Circuit:

- The circuit diagram of D flip – flop is shown in below figure.



CLK	D	Q	Q'
↓	X	Q_{PREV}	Q'_{PREV}
↑	1	1	0
↑	0	0	1

D Flip Flop

- Characteristic table :

Q_n	D_n	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

Q_n \ D_n	0	1
0	0	1
1	0	1

K-Map

$$\boxed{Q_{n+1} = D_n}$$

Characteristic Equation

Excitation Table :

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

T Flip Flop

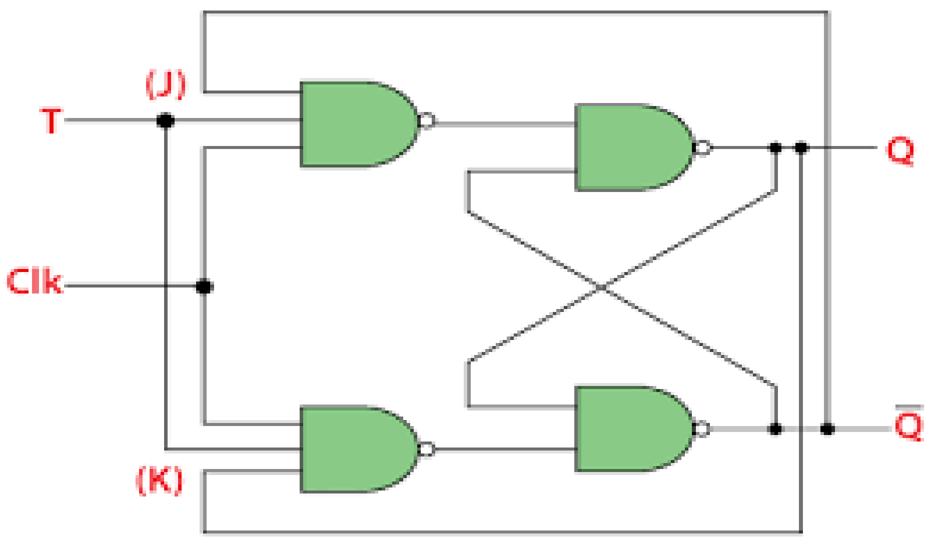
- The T or "toggle" flip-flop changes its output on each clock edge, giving an output which is half the frequency of the signal to the T input.
- It is useful for constructing binary counters, frequency dividers, and general binary addition devices.
- It can be made from a J-K flip-flop by tying both of its inputs high.

Construction

- We can construct a T flip – flop by connecting AND gates as input to the NOR gate SR latch.
- These AND gate inputs are fed back with the present state output Q and its complement Q’ to each AND gate.
- A toggle input (T) is connected in common to both the AND gates as an input.

T Flip Flop

Logic Diagram :



CLK	T	Q_{n+1}	$\bar{Q}_{n+1}$	Operation
0	X	Q_n	$\bar{Q}_n$	No Change
1	0	Q_n	$\bar{Q}_n$	No Change
1	1	$\bar{Q}_n$	Q_n	Toggle

T Flip Flop

- **Characteristic Equation**

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Q_p \ T	0	1
0	0	$\boxed{1}$
1	$\boxed{1}$	0

$$Q_{n+1} = \bar{T}\, Q_n + T\, \bar{Q}_n$$

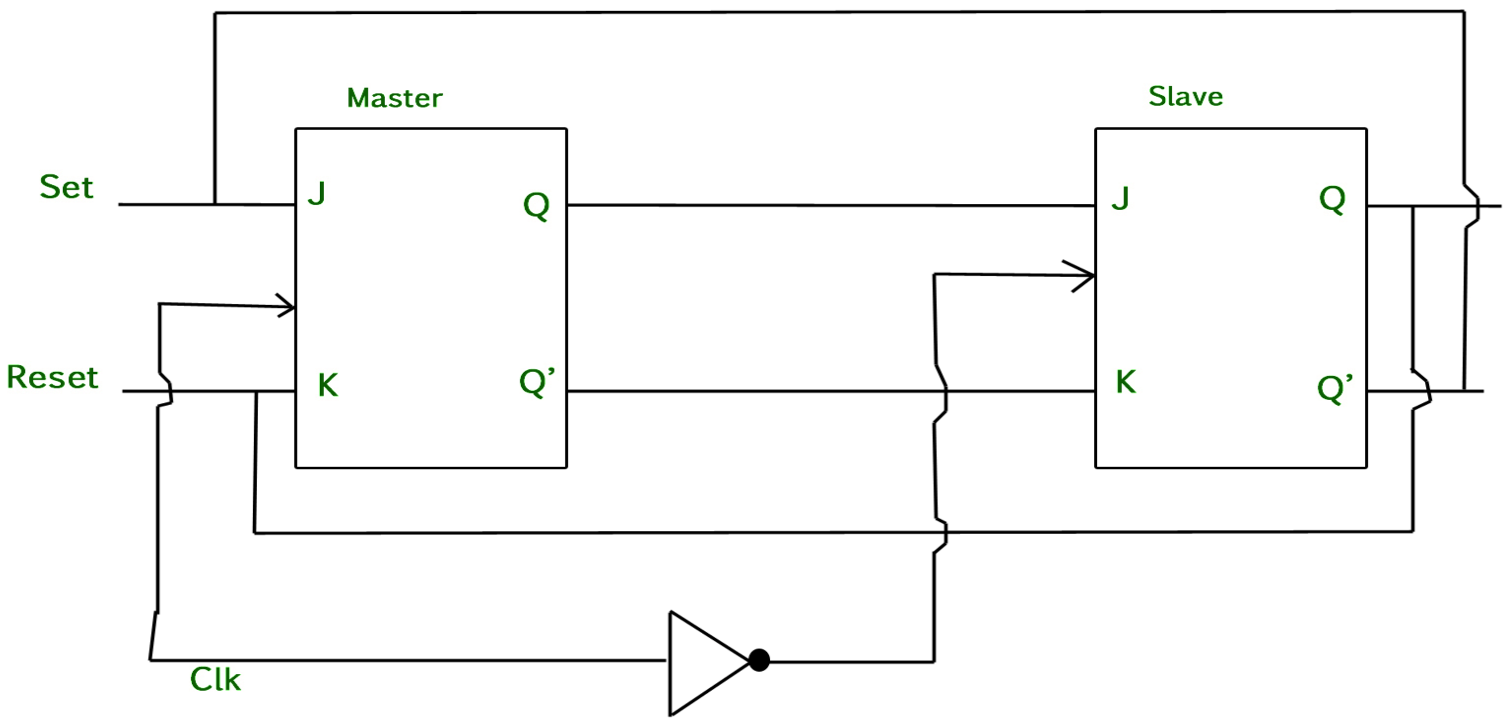
- **Excitation Table**

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Master Slave J K Flip Flop

- The Master-Slave Flip-Flop is basically a combination of two JK flip-flops connected together in a series configuration.
- Out of these, one acts as the “master” and the other as a “slave”.
- The output from the master flip flop is connected to the two inputs of the slave flip flop whose output is feedback to inputs of the master flip flop.
- In addition to these two flip-flops, the circuit also includes an **inverter**.
- The inverter is connected to clock pulse in such a way that the inverted clock pulse is given to the slave flip-flop.
- In other words if CLK=0 for a master flip-flop, then CLK=1 for a slave flip-flop and if CLK=1 for master flip flop then it becomes 0 for slave flip flop.

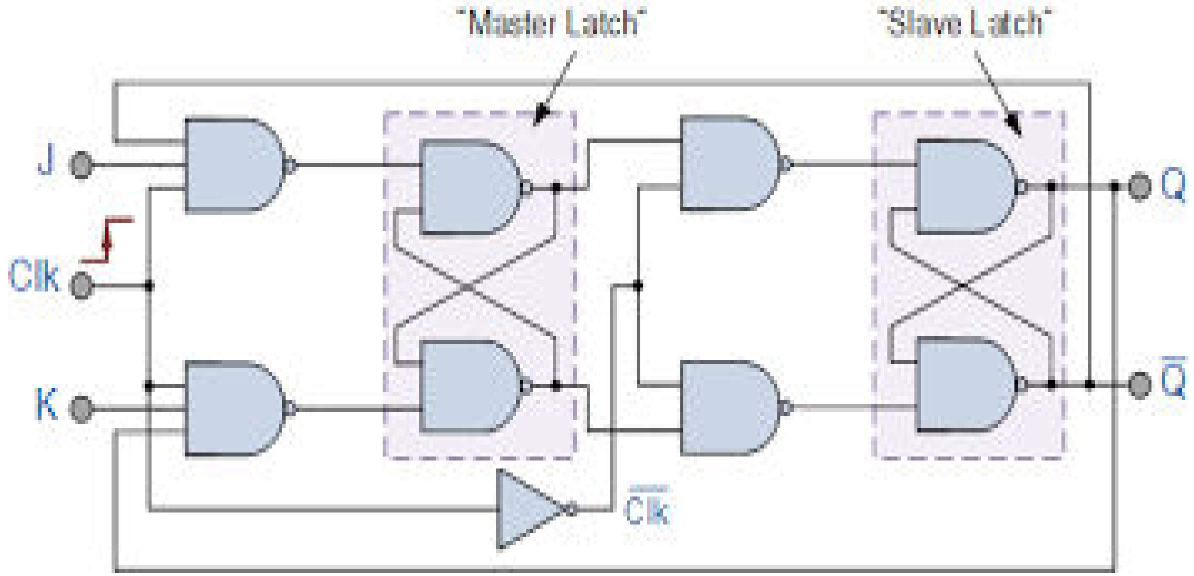
Master Slave J K Flip Flop

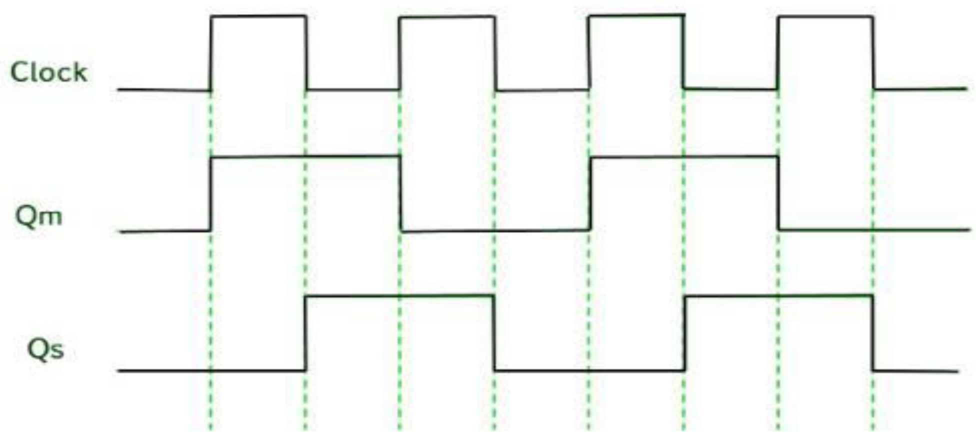


Master-slave JK Flip-Flop

Master Slave J K Flip Flop

- Timing diagram for master slave flip-flop :





Daily Quiz

- Differentiate between latches & flipflops.
- For the clocked SR flip-flop write the state table, draw the state diagram and the state equation.
- What are the different types of flipflops?
- Explain Master slave flipflop.
- Explain race around condition.

MCQ

1. When both inputs of a J-K flip-flop cycle, the output will ____________

a) Be invalid
b) Change
c) Not change
d) Toggle

2. Which of the following is correct for a gated D-type flip-flop?
a) The Q output is either SET or RESET as soon as the D input goes HIGH or LOW
b) The output complement follows the input when enabled
c) Only one of the inputs can be HIGH at a time
d) The output toggles if one of the inputs is held HIGH

3. A basic S-R flip-flop can be constructed by cross-coupling of which basic logic gates?
a) AND or OR gates
b) XOR or XNOR gates
c) NOR or NAND gates
d) AND or NOR gates

Old Questions

- What is difference between flip flop and latches?
- What is race around condition?
- For the clocked JK flip-flop write the state table, draw the state diagram and the state equation.
- What are the different types of flipflops?

NIET Greater Noida

Flip Flop

Latches	Flip Flops
Latches are building blocks of sequential circuits and these can be built from logic gates	Flip flops are also building blocks oof sequential circuits. But, these can be built from the latches.
Latch continuously checks its inputs and changes its output correspondingly.	Flip flop continuously checks its inputs and changes its output correspondingly only at times determined by clocking signal
The latch is sensitive to the duration of the pulse and can send or receive the data when the switch is on	Flipflop is sensitive to a signal change. They can transfer data only at the single instant and data cannot be changed until next signal change. Flip flops are used as a register.
It is based on the enable function input	It works on the basis of clock pulses
It is a level triggered, it means that the output of the present state and input of the next state depends on the level that is binary input 1 or 0.	It is an edge triggered, it means that the output and the next state input changes when there is a change in clock pulse whether it may a +ve or -ve clock pulse.

Conversion of flip-flops

We can convert one flip-flop into the remaining three flip-flops by including some additional logic. So, there will be total of twelve **flip-flop conversions**.

Follow these **steps** for converting one flip-flop to the other.

- Write characteristic table of desired flip-flop.
- Write the excitation table of given flip-flop.
- Using the excitation table of given flip-flop and given inputs by taking present state and next state of desired flip-flop.
- Simplify the logic expression using k-map for excitation inputs of given flip-flops.
- Draw a circuit using the above expression.

Conversion of flip-flops

Eg. Covert JK flip-flop to T flip-flop.

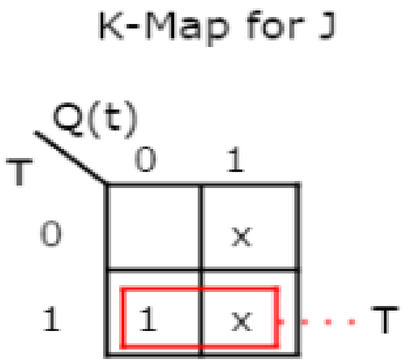
Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

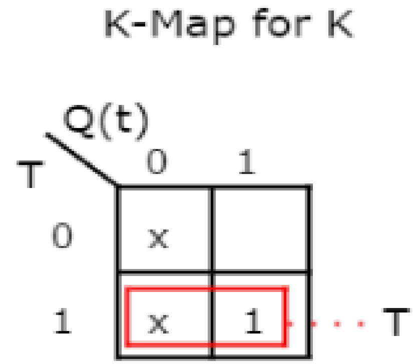
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Using the above excitation table find inputs J & K by taking present state and next state of T flip flop.

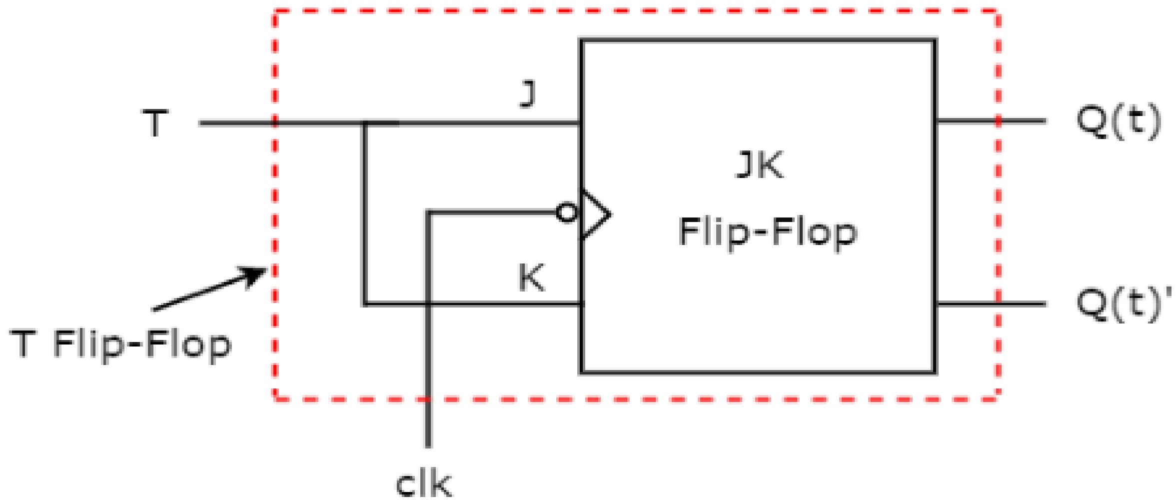
T	Q_n	Q_{n+1}	J	K
0	0	0	0	X
0	1	1	X	0
1	0	1	1	X
1	1	0	X	1

Conversion of flip-flops





So, we got, J = T & K = T after simplifying. The **circuit diagram** of T flip-flop is shown in the following figure.



Conversion of flip-flops

Eg. Covert T flip-flop to D flip-flop.

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Using the above excitation table find inputs T by taking present state and next state of D flip flop.

Q_n	D	Q_{n+1}	T
0	0	0	0
0	1	1	1
1	0	0	1
1	1	1	0

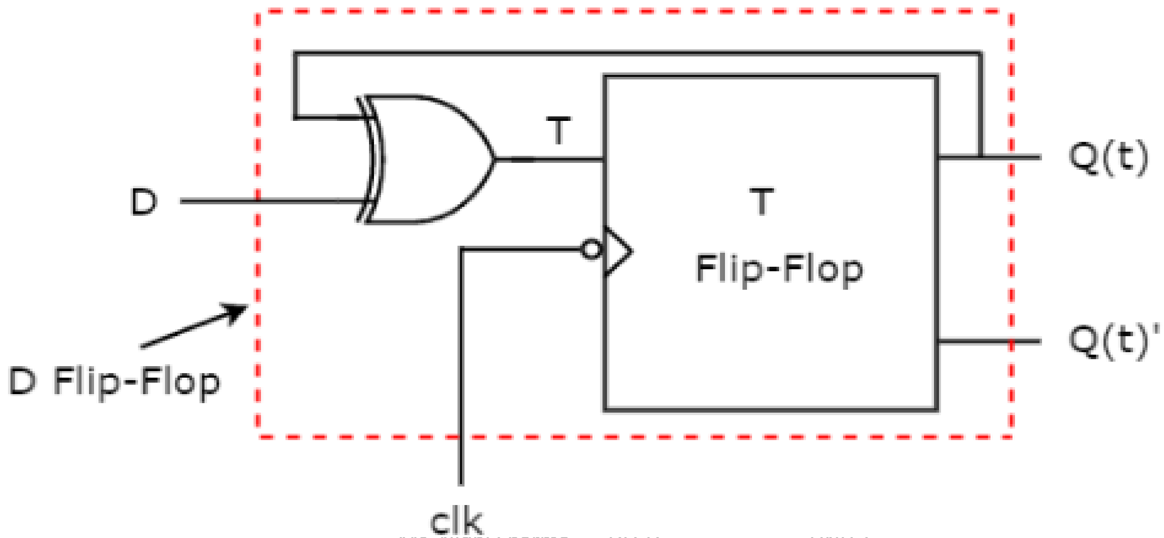
Conversion of flip-flops

Eg. Covert T flip-flop to D flip-flop.

$Q_n \backslash D$	0	1
0	0 [0]	1 [1]
1	1 [2]	0 [3]

$$T = D\overline{Q}_n + \overline{D}Q_n$$
$$= D \oplus Q_n$$

So, we require a two input Exclusive-OR gate along with T flip-flop. The **circuit diagram** of D flip-flop is shown in the following figure.



Video Link

- https://nptel.ac.in/courses/117/106/117106086/
- https://www.youtube.com/watch?v=2ecMG_OciLo&ab_channel=nptelhrdnptelhrd
- https://www.youtube.com/watch?v=2ecMG_OciLo&ab_channel=nptelhrdnptelhrd

Daily Quiz

- Differentiate between latches & flipflops.
- Write and explain steps of flip flop conversion.
- What are the different types of flipflops?
- Explain Master slave flipflop.

Video Link

- https://nptel.ac.in/courses/117/106/117106086/
- https://www.youtube.com/watch?v=2ecMG_OciLo&ab_channel=nptelhrdnptelhrd
- https://www.youtube.com/watch?v=2ecMG_OciLo&ab_channel=nptelhrdnptelhrd

MCQ

1. To design a synchronous sequential circuit with 9 states how many flip flops are required?

a) 4 c) 5

b) 9 d) 3

2. Following flip flop is used to eliminate race around condition:

a) JK flip flop
b) Master slave JK flip flop
c) SR flip flop
d) T flip flop

3. The flip flop is only activated by:

a) Positive edge triggering
b) Negative edge triggering
c) Either positive or negative edge triggering

Old Questions

- Realize

i. A JK flip flop using SP flip flop.

ii. A SR using NAND gates and explain its operation.

Weekly Assignment

- What is race around condition? How to eliminate race around condition?
- Draw and explain master slave flip flop.
- Realize D flip flop using T flip flop.
- Realize a T flip flop using SR flip flop.

Recap of Previous Topic

- A Flip Flop is a memory element that is capable of storing one bit of information.
- It is also called as Bistable Multivibrator since it has two stable states either 0 or 1.
- There are following 4 basic types of flip flops- SR, JK, T, D.
- The main drawback of the JK flip flop is the race around condition.
- It happens when both the input is 1.
- In race around condition output toggles more than one time.
- Master slave flip flop is used to eliminate this condition.

Counters

Topic Objective	Mapping with CO
To design asynchronous and synchronous counter.	CO3

Counters

Prerequisite:

- Basic knowledge of designing of synchronous sequential circuits.

Counters

- Counter is a sequential circuit. A digital circuit which is used for a counting pulses is known counter. Counter is the widest application of flip-flops. It is a group of flip-flops with a clock signal applied. Counters are of two types depending upon clock pulse applied.
  - Asynchronous or ripple counters.
  - Synchronous counters
- In **Asynchronous Counter** is also known as Ripple Counter, different flip flops are triggered with different clock, not simultaneously. While in **Synchronous Counter**, all flip flops are triggered with same clock simultaneously and Synchronous Counter is faster than asynchronous counter in operation.

Counters

Synchronous counter

- In synchronous counter, all flip flops are triggered with same clock simultaneously.
- Synchronous Counter is faster than asynchronous counter in operation.
- Synchronous Counter does not produce any decoding errors.
- Synchronous Counter is also called Parallel Counter.
- Synchronous Counter designing as well implementation are complex due to increasing the number of states.
- Synchronous Counter will operate in any desired count sequence.
- Synchronous Counter examples are: Ring counter, Johnson counter.
- In synchronous counter delay is less.

Asynchronous counter

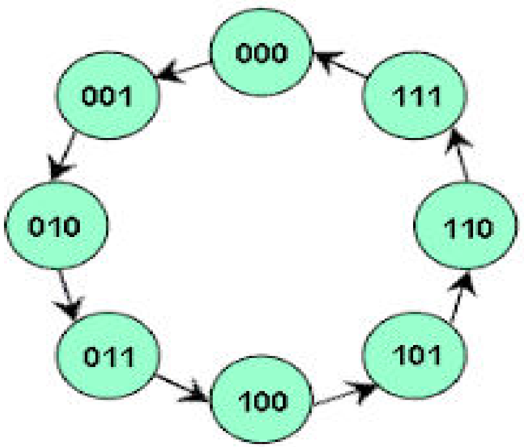
- In asynchronous counter, different flip flops are triggered with different clock, not simultaneously.
- Asynchronous Counter is slower than synchronous counter in operation.
- Asynchronous Counter produces decoding error.
- Asynchronous Counter is also called Serial Counter.
- Asynchronous Counter designing as well as implementation is very easy.
- Asynchronous Counter will operate only in fixed count sequence (UP/DOWN).
- Asynchronous counter examples are: Ripple UP counter, Ripple DOWN counter.
- In asynchronous counter, there is high propagation delay.

Ripple Counter

3 bit or MOD 8 Ripple Counter

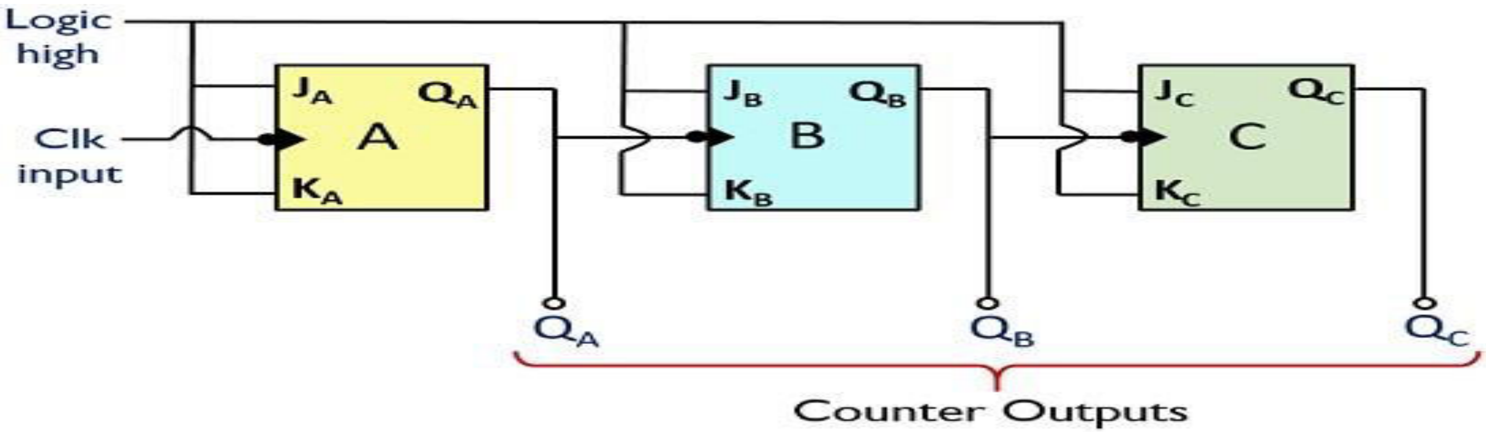
- In asynchronous counter we don't use universal clock, only first flip flop is driven by main clock and the clock input of rest of the following flip flop is driven by output of previous flip flops.
- $N \le 2^n$, where N is no of states and n is no of flip-flops.

N = 8 so no of flip flops is 3.



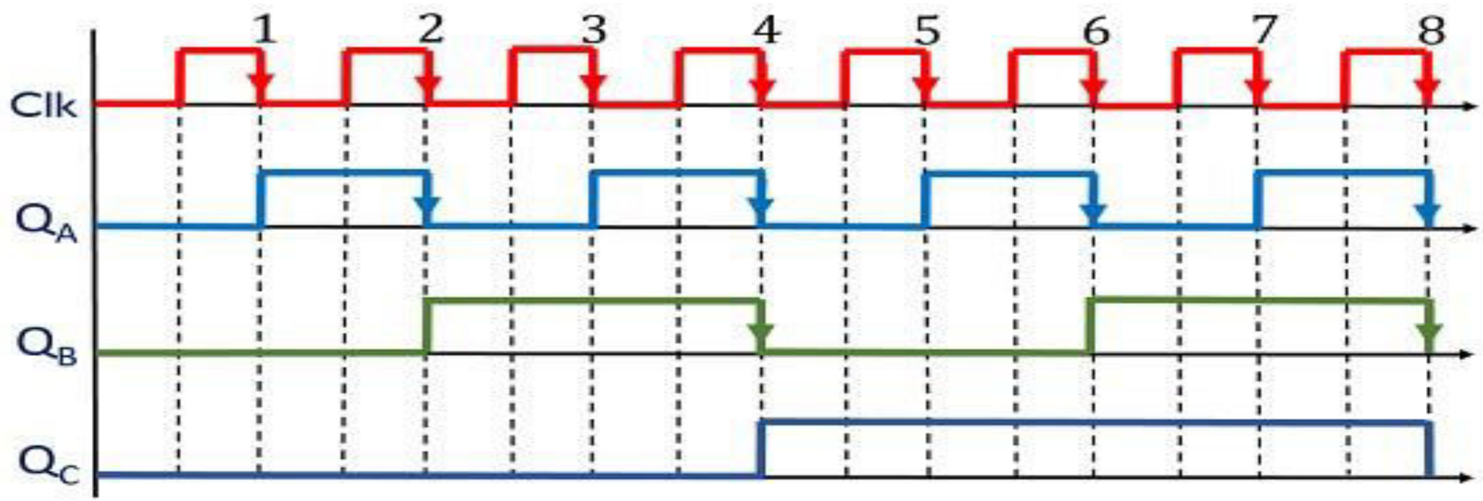
States	Q_C	Q_B	Q_A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Ripple Counter



Circuit Diagram of 3-bit Asynchronous Counter

Electronics Coach



Timing Diagram of 3-bit Asynchronous Counter

Electronics Coach

Ripple Counter

4 bit down Ripple Counter

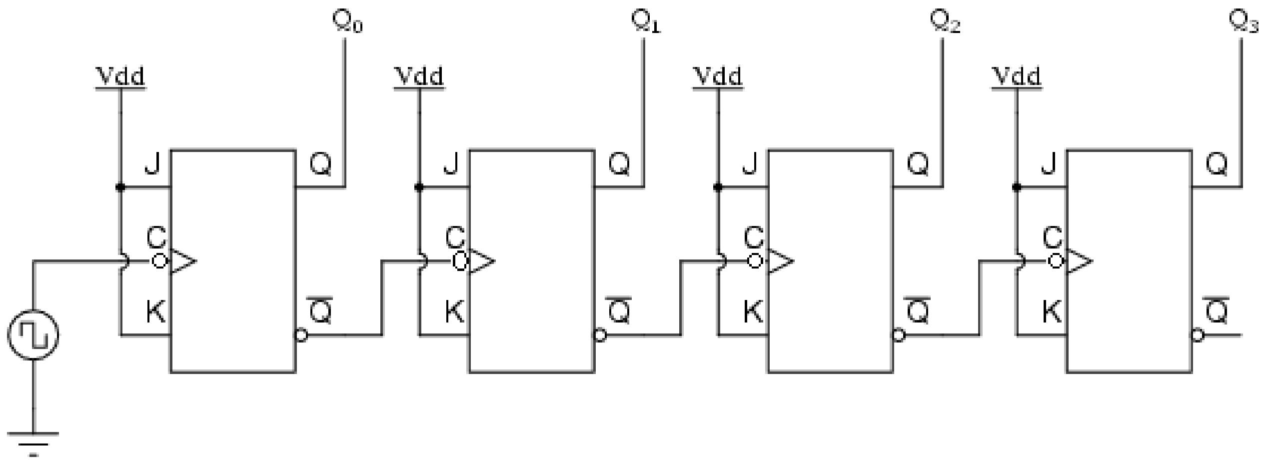
- $N \leq 2^n$, where N is no of states and n is no of flip-flops.

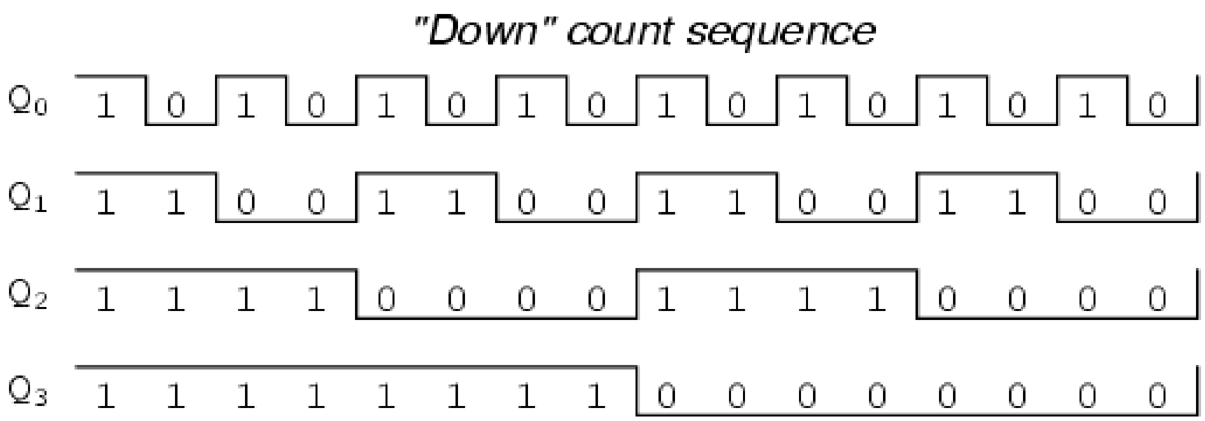
  no of flip flops is 3 the states at which the counter counts is 16.

CK	Q_3	Q_2	Q_1	Q_0
0	1	1	1	1
1	1	1	1	0
2	1	1	0	1
3	1	1	0	0
4	1	0	1	1
5	1	0	1	0
6	1	0	0	1
7	1	0	0	0
8	0	1	1	1
9	0	1	1	0
10	0	1	0	1
11	0	1	0	0
12	0	0	1	1
13	0	0	1	0
14	0	0	0	1
15	0	0	0	0

Ripple Counter

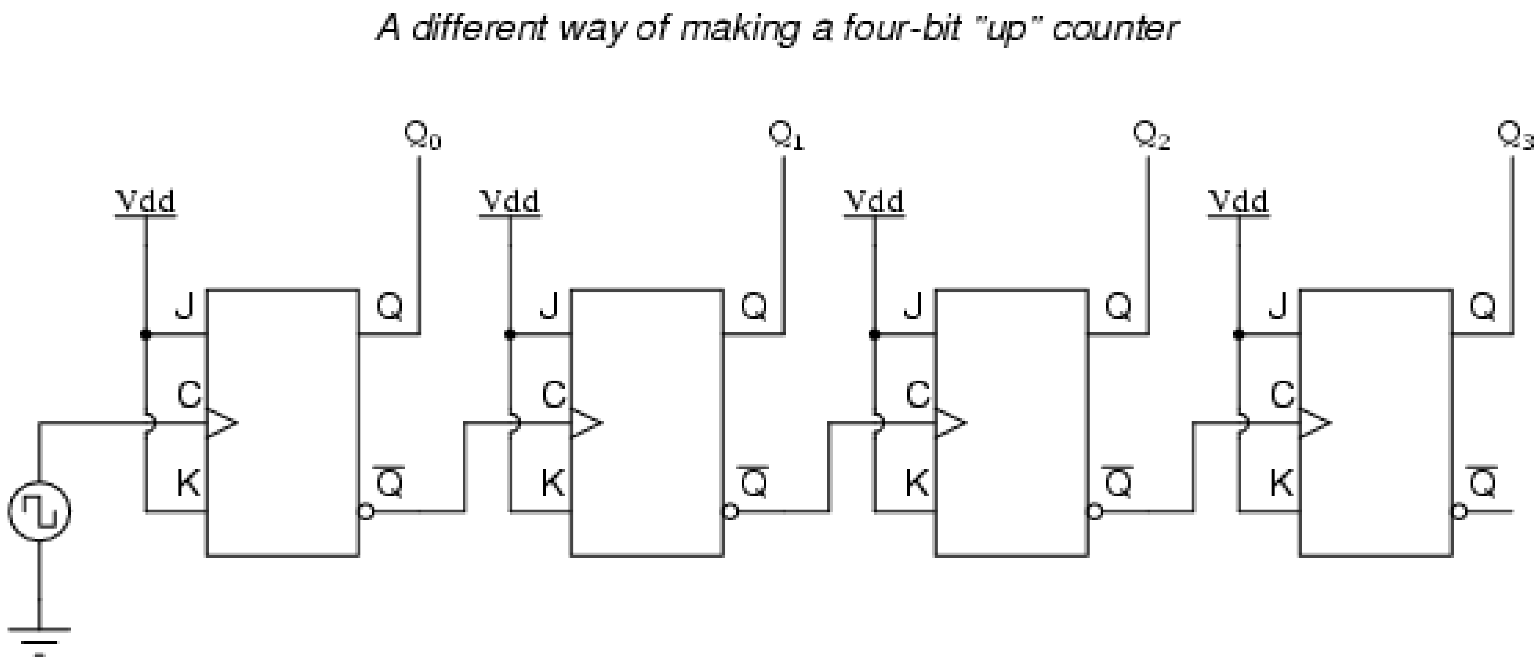
4 bit down Ripple Counter





Ripple Counter

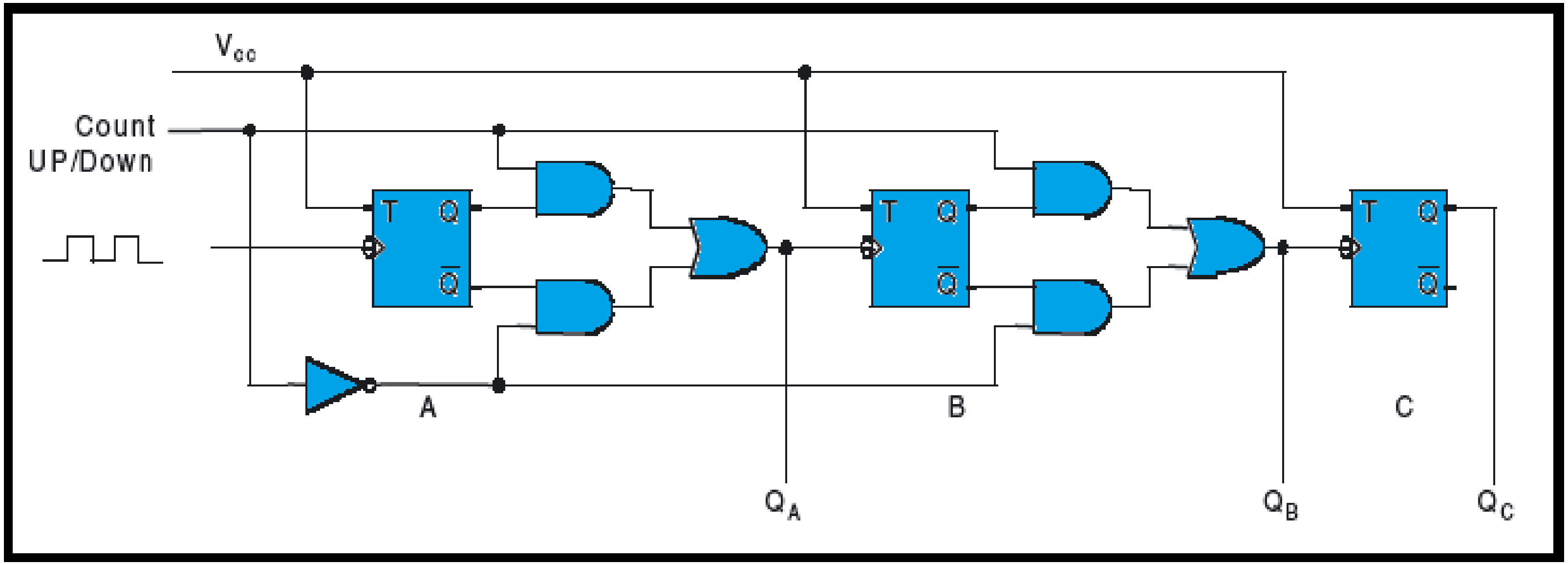
4 bit up counter using positive clock edge :



UP/DOWN Counter

- Both Synchronous and Asynchronous counters are capable of counting "Up" or counting "Down", but their is another more "Universal" type of counter that can count in both directions either Up or Down depending on the state of their input control pin and these are known as **Bidirectional Counters**.
- *Bidirectional counters*, also known as Up/Down counters, are capable of counting in either direction through any given count sequence and they can be reversed at any point within their count sequence by using an additional control input as shown below.

UP/DOWN Counter



COUNT-UP Mode				COUNT-DOWN Mode			
States	Q_C	Q_B	Q_A	States	Q_C	Q_B	Q_A
0	0	0	0	7	1	1	1
1	0	0	1	6	1	1	0
2	0	1	0	5	1	0	1
3	0	1	1	4	1	0	0
4	1	0	0	3	0	1	1
5	1	0	1	2	0	1	0
6	1	1	0	1	0	0	1
7	1	1	1	0	0	0	0

Synchronous Counter

Synchronous counters :

Counter is clocked such that all the flip-flops are clocked simultaneously, so that all the flip-flops change their output state at a same time. So the speed of operation is increased.

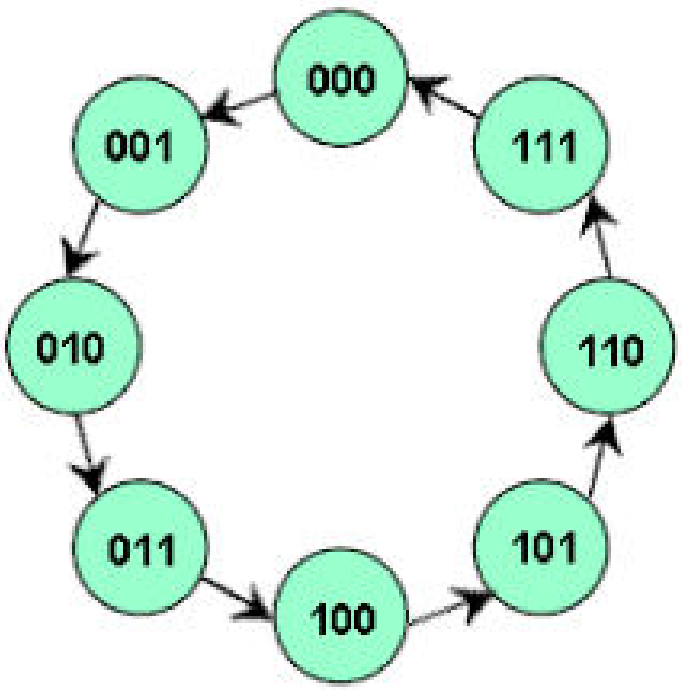
Synchronous counter Design

1. Find the no flip-flops required
2. Write count sequence in tabular form
3. Draw excitation table for flip-flop inputs
4. Prepare k-map for each flip-flop inputs
5. Connect the circuit using flip-flops and other logical gates.

Synchronous Counter

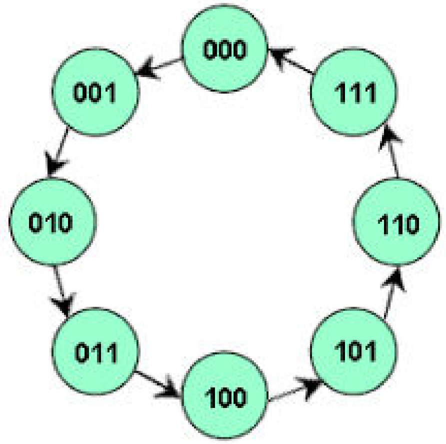
Example: Design a 3 bit synchronous counter using T flip-flops.

Solution: For 3 bit counter state diagram is



Synchronous Counter

- Now from the state diagram draw the state table:

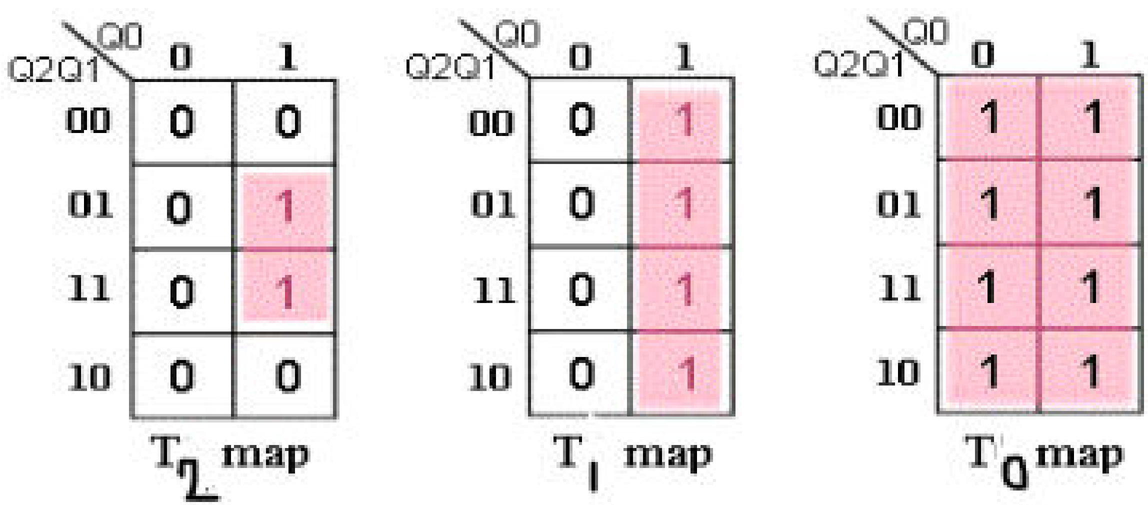


Output State Transitions		Flip-flop inputs
Present State $Q_2\ Q_1\ Q_0$	Next State $Q_2\ Q_1\ Q_0$	$T_2\ T_1\ T_0$
0 0 0	0 0 1	0 0 1
0 0 1	0 1 0	0 1 1
0 1 0	0 1 1	0 0 1
0 1 1	1 0 0	1 1 1
1 0 0	1 0 1	0 0 1
1 0 1	1 1 0	0 1 1
1 1 0	1 1 1	0 0 1
1 1 1	0 0 0	1 1 1

Synchronous Counter

- Next step is to transfer the flip-flop input functions to Karnaugh maps to derive a simplified Boolean expressions

Output State Transitions		Flip-flop inputs
Present State $Q_2\ Q_1\ Q_0$	Next State $Q_2\ Q_1\ Q_0$	$T_2\ T_1\ T_0$
0 0 0	0 0 1	0 0 1
0 0 1	0 1 0	0 1 1
0 1 0	0 1 1	0 0 1
0 1 1	1 0 0	1 1 1
1 0 0	1 0 1	0 0 1
1 0 1	1 1 0	0 1 1
1 1 0	1 1 1	0 0 1
1 1 1	0 0 0	1 1 1



Synchronous Counter

- The boolean expressions are obtained from K Map

Q2Q1 \ Q0	0	1
00	0	0
01	0	1
11	0	1
10	0	0

T_2 map

Q2Q1 \ Q0	0	1
00	0	1
01	0	1
11	0	1
10	0	1

T_1 map

Q2Q1 \ Q0	0	1
00	1	1
01	1	1
11	1	1
10	1	1

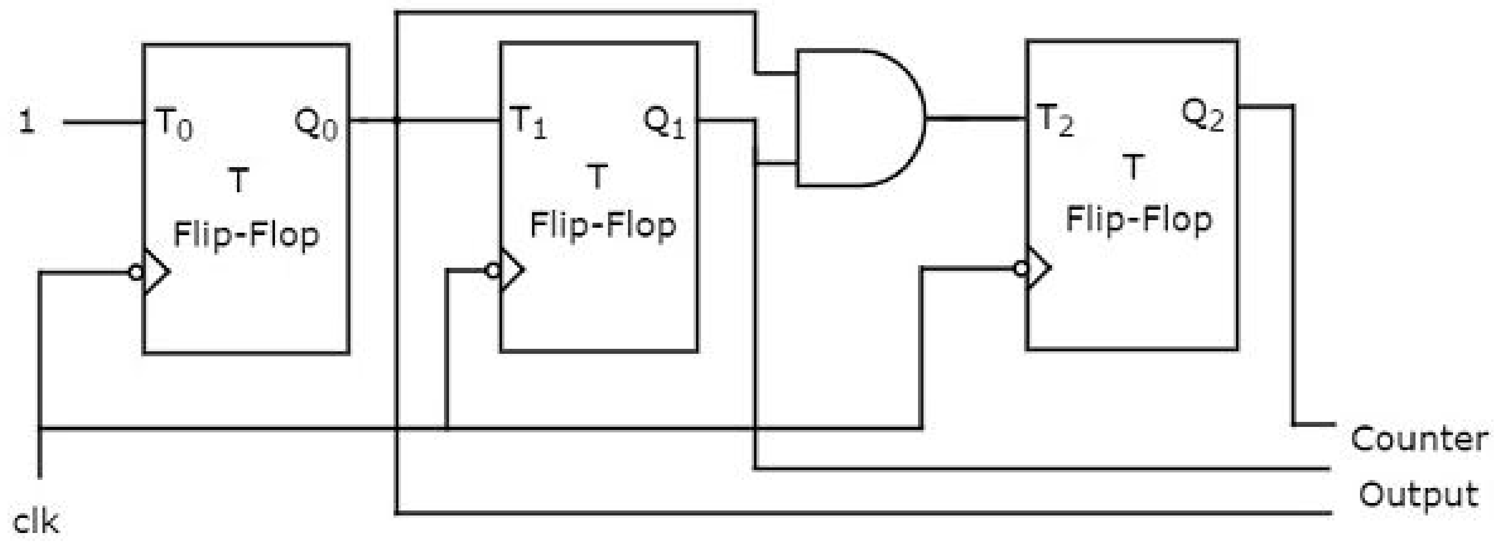
T_0 map

$T_0 = 1;$ $T_1 = Q_0;$ $T_2 = Q_1 \cdot Q_0$

Synchronous Counter

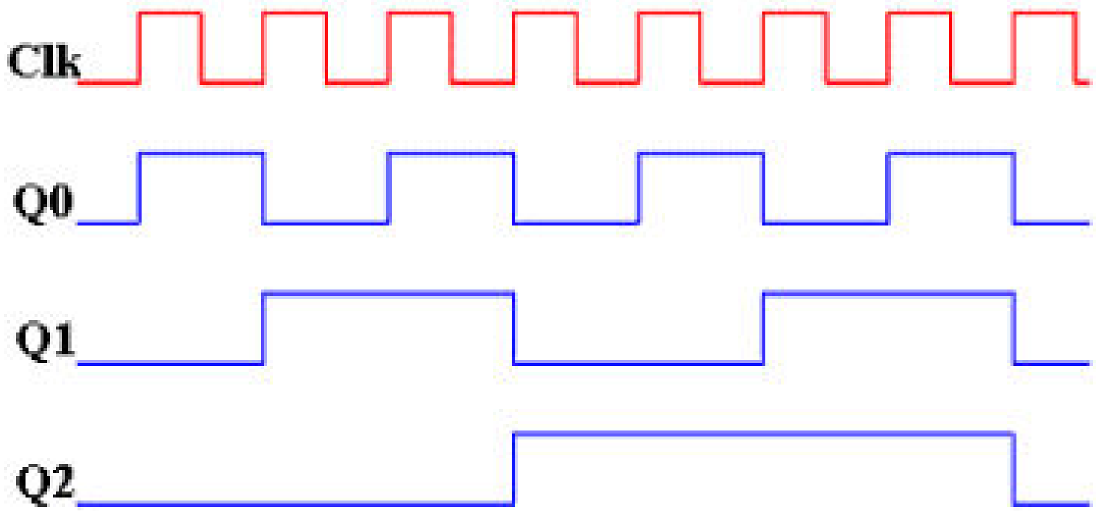
- From the boolean expressions circuit diagram can be drawn:

$$T_0 = 1; \qquad T_1 = Q_0; \qquad T_2 = Q_1 \cdot Q_0$$

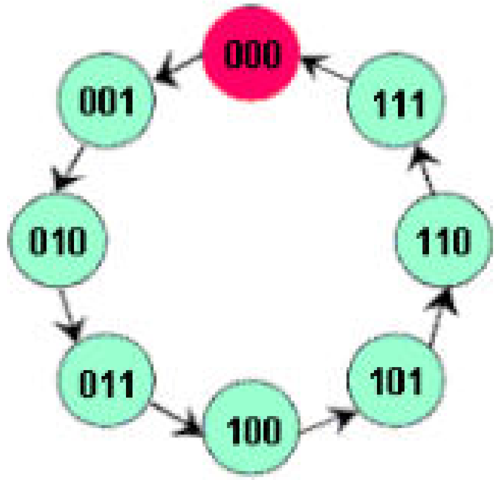


Synchronous Counter

- Timing diagrams:



Timing Diagram

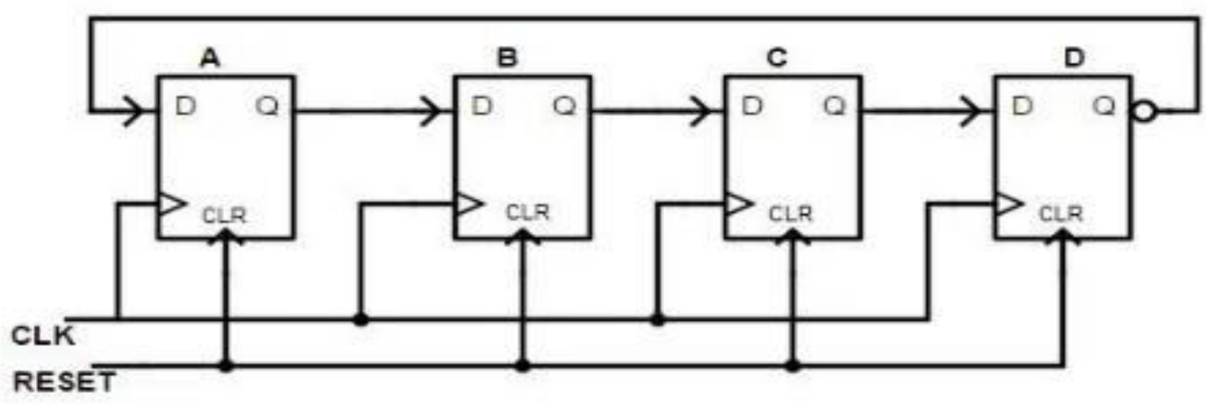


State Transition

Ring Counters

- A ring counter has one of its outputs connect back to the input. It is thus making a ring. There are two types of ring counters.
- Straight ring counter – The non-inverting output (Q) of the last flip-flop is connected to the first flip-flop.
- Johnson ring counter/Twisted ring counter – The inverting output of the last flip-flop is connected to the first flip-flop.

Ring Counters



4 bit ring counter

QA	QB	QC	QD
1	0	0	0
0	1	0	0
0	0	1	0
0	0	0	1

Ring Counters

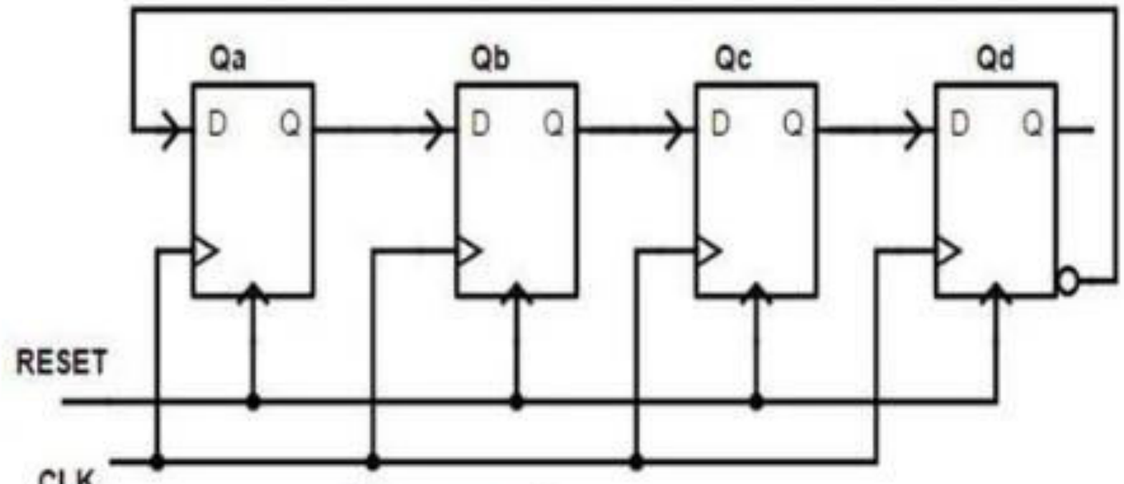
Advantages and disadvantages of a ring counter:

- A small advantage of a ring counter is that it has an automatically decoded output. However, ring counters have a major disadvantage because they need to be initialized. A number needs to be loaded to the ring counter before the start of the counting process. We had not seen this with any other counter yet. Another disadvantage is that only N states are present compared to the states of the binary counters.

Johnson Counters

Johnson Counters:

- In *Johnson ring counter* the inverted output of the last flip-flop is connected to the input of the first flip-flop. The only difference between the straight ring counter and the Johnson counter is that in the Johnson counter the inverted output of the last flip-flop (as opposed to the non-inverted output in the straight ring counter) is connected as the input to the first flip-flop. Johnson counter is also called the **twisted-ring counter or switch-tail ring counter.**



Johnson counter

Johnson Counters

Truth Table of Johnson ring counter

Qa	Qb	Qc	Qd
0	0	0	0
1	0	0	0
1	1	0	0
1	1	1	0
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1

- The truth table starts from 0000. This means that it is self-defaulting.
- The Johnson counter does not need any input. Moreover, a Johnson counter has more states than a straight ring counter. A binary counter has states, a straight ring counter has N states, and a Johnson ring counter has 2N states.

Johnson Counters

Advantages / Disadvantages of Johnson Counter

Advantages

- More outputs as compared to ring counter.
- It has same number of flip flop but it can count twice the number of states the ring counter can count.
- It only needs half the number of flip-flops compared to the standard ring counter for the same MOD
- **Disadvantages**
- Only 8 of the 15 states are being used.
- It doesn’t count in a binary sequence.

Recap

- Counter is a sequential circuit. A digital circuit which is used for a counting pulses is known counter. Counter is the widest application of flip-flops. It is a group of flip-flops with a clock signal applied. Counters are of two types depending upon clock pulse applied.
  - Asynchronous or ripple counters.
  - Synchronous counters
- In **Asynchronous Counter** is also known as Ripple Counter, different flip flops are triggered with different clock, not simultaneously. While in **Synchronous Counter**, all flip flops are triggered with same clock simultaneously and Synchronous Counter is faster than asynchronous counter in operation
- In *Johnson ring counter* the inverted output of the last flip-flop is connected to the input of the first flip-flop.
- Ring counters are basically a type of counter in which the output of the most significant bit is fed back as an input to the least significant bit.

Video Links

- https://www.youtube.com/watch?v=32v8s0R0qIk&ab_channel=TutorialsPoint%28India%29Ltd.TutorialsPoint%28India%29Ltd.Verified
- https://nptel.ac.in/courses/117/106/117106086/

Daily Quiz

- To design a synchronous counter with 9 states how many flip flops are required?

a) 4 c) 5

b) 9 d) 3

- In a 4-bit Johnson counter sequence, there are a total of how many states or bit patterns?
  a) 1
  b) 3
  c) 4
  d) 8
- What do you understand by ring counter?
- If a 10-bit ring counter has an initial state 1101000000, what is the state after the second clock pulse?
  a) 1101000000
  b) 0011010000
  c) 1100000000
  d) 0000000000

Old Questions

- What are the differences between synchronous and asynchronous counter?
- Design a 4 bit synchronous counter using D flip flop.
- Design MOD 3 UP/DOWN synchronous counter.
- Explain 4bit Johnson counter with circuit diagram and waveforms.

Shift Registers

Topic Objective	Mapping with CO
To Explain shift registers.	CO3

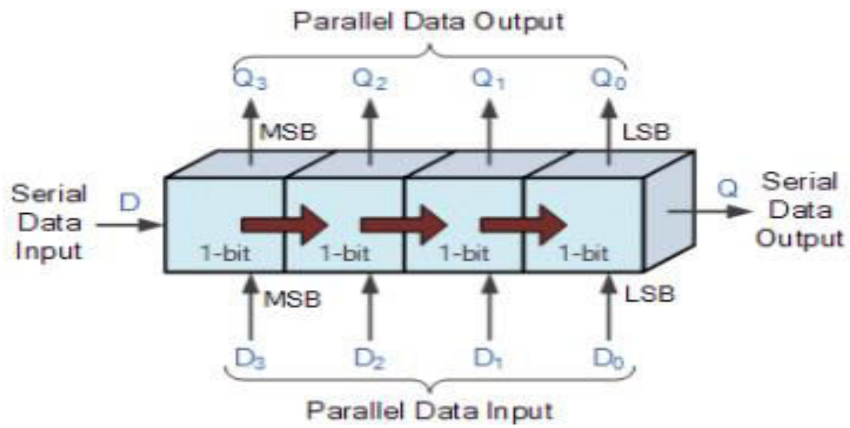
Shift Register

Prerequisite:

- To have a basic understanding of Flip flops.

Shift Register

- Shift Registers are sequential logic circuits, capable of storage and transfer of data.
- This sequential device loads the data present on its inputs and then moves or "shifts" it to its output once every clock cycle, hence the name **Shift Register**.
- A *shift register* basically consists of several single bit "D-Type Data Latches", one for each data bit, either a logic "0" or a "1", connected together in a serial type chain arrangement so that the output from one data latch becomes the input of the next latch and so on.



Shift Register

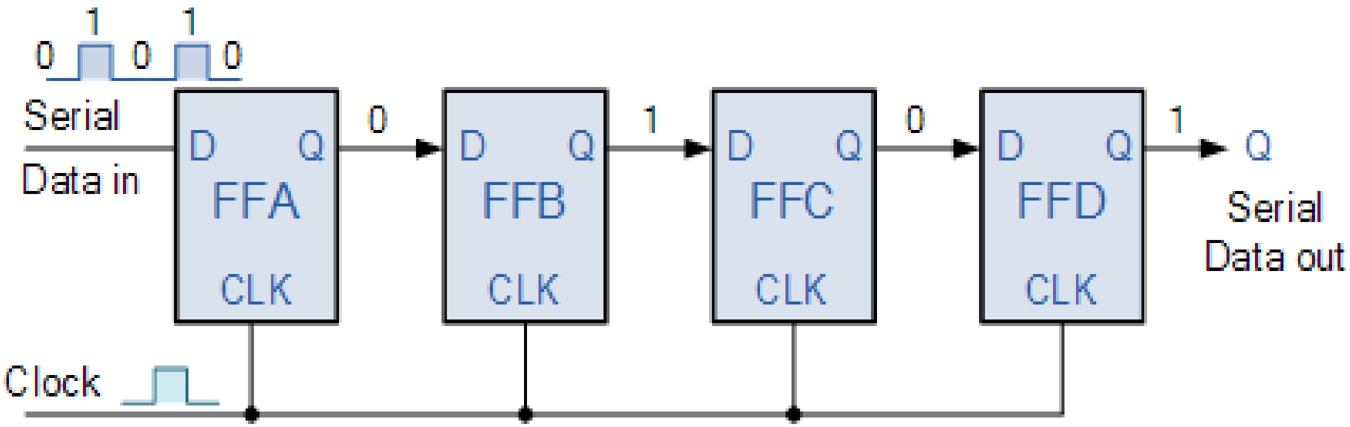
Types of Shift Registers

Generally, shift registers operate in one of four different modes with the basic movement of data through a shift register being:

- **Serial-in to Parallel-out (SIPO)** - the register is loaded with serial data, one bit at a time, with the stored data being available at the output in parallel form.
- **Serial-in to Serial-out (SISO)** - the data is shifted serially “IN” and “OUT” of the register, one bit at a time in either a left or right direction under clock control.
- **Parallel-in to Serial-out (PISO)** - the parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.
- **Parallel-in to Parallel-out (PIPO)** - the parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse.

Serial in - Serial out Shift Registers

- The SISO shift register is one of the simplest of the four configurations as it has only three connections, the serial input (SI) which determines what enters the left hand flip-flop, the serial output (SO) which is taken from the output of the right hand flip-flop and the sequencing clock signal (Clk). The logic circuit diagram below shows a generalized serial-in serial-out shift register.



Serial in - Serial out Shift Registers

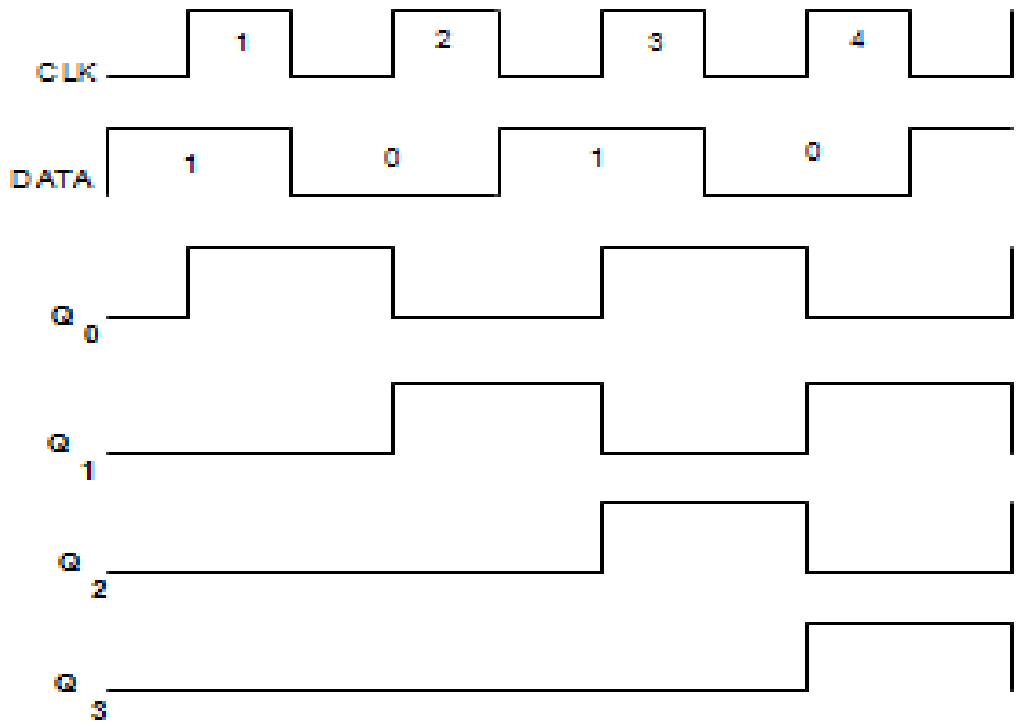
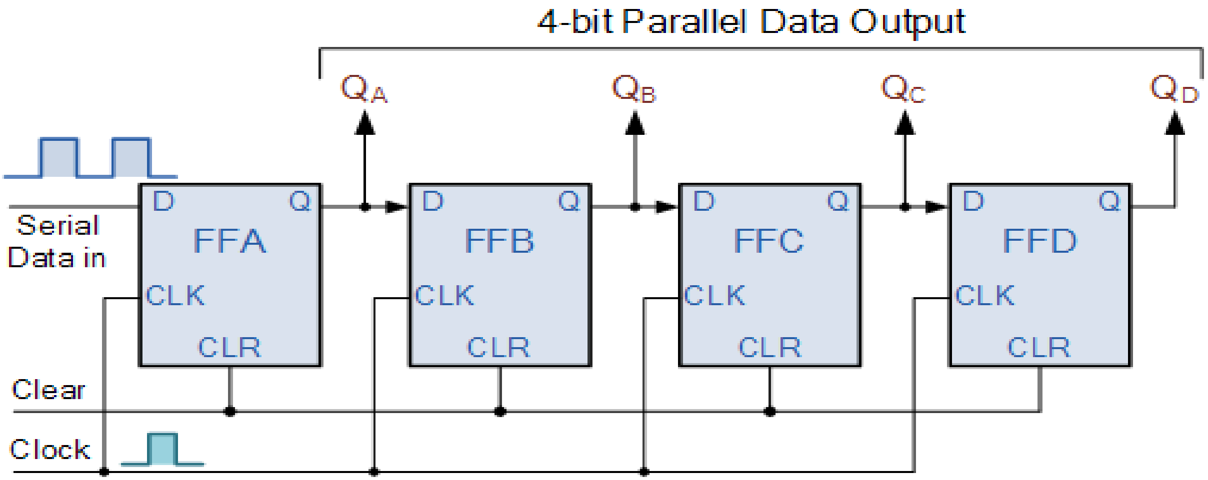


Fig.(b) Output Waveforms of 4-bit Serial-in Serial-out Register

Serial in – Parallel out Shift Register

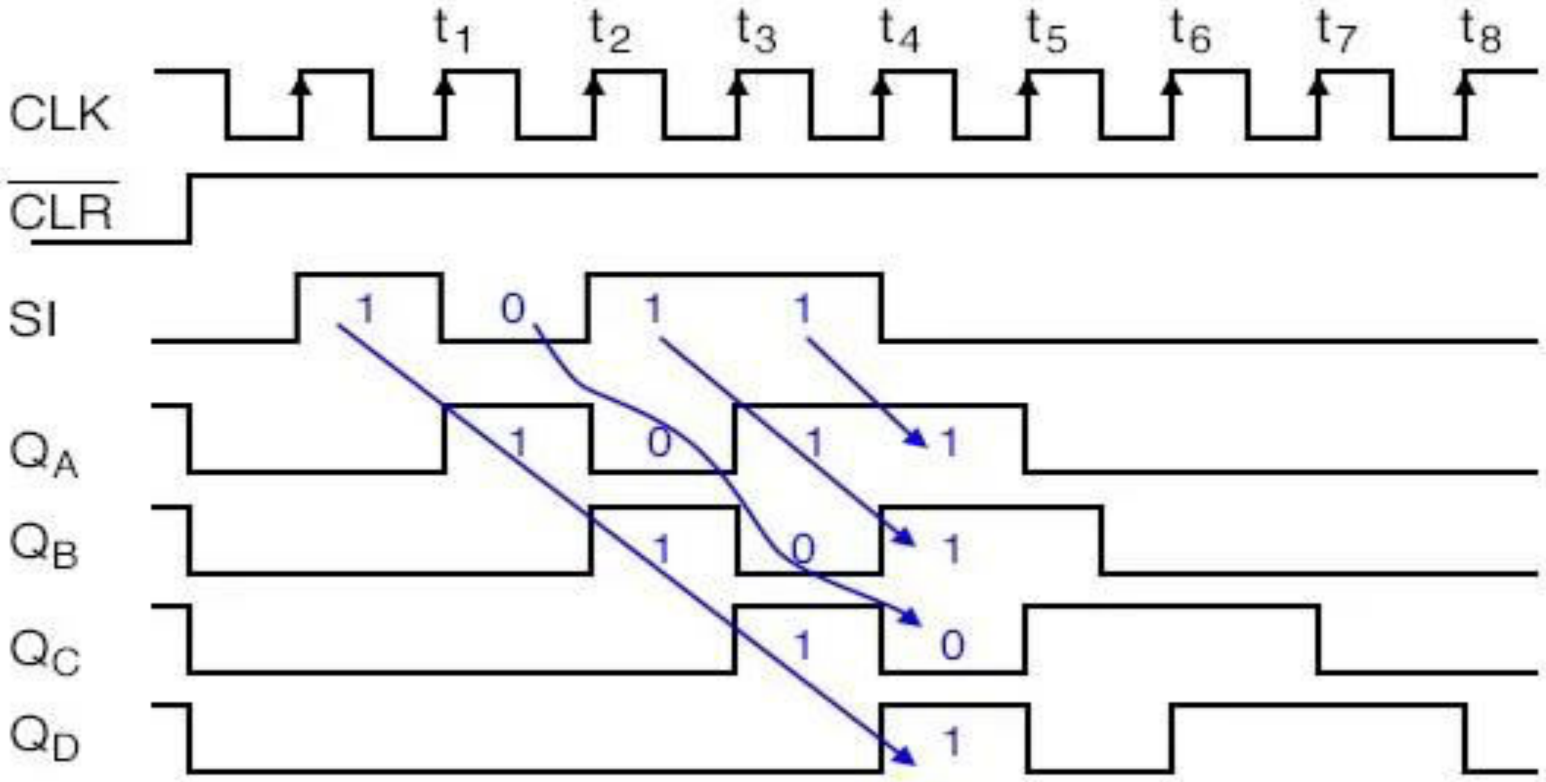
- These types of shift registers are used for the conversion of data from serial to parallel.
- A 4-bits serial in – Parallel out shift register is illustrated in the Image below.



- Lets assume that all the flip-flops (FFA to FFD) have just been RESET (CLEAR input) and that all the outputs Q_A to Q_D are at logic level “0” ie, no parallel data output.

Shift Register

The serial data **1011** pattern presented at the **SI** input. This data is synchronized with the clock **CLK**.

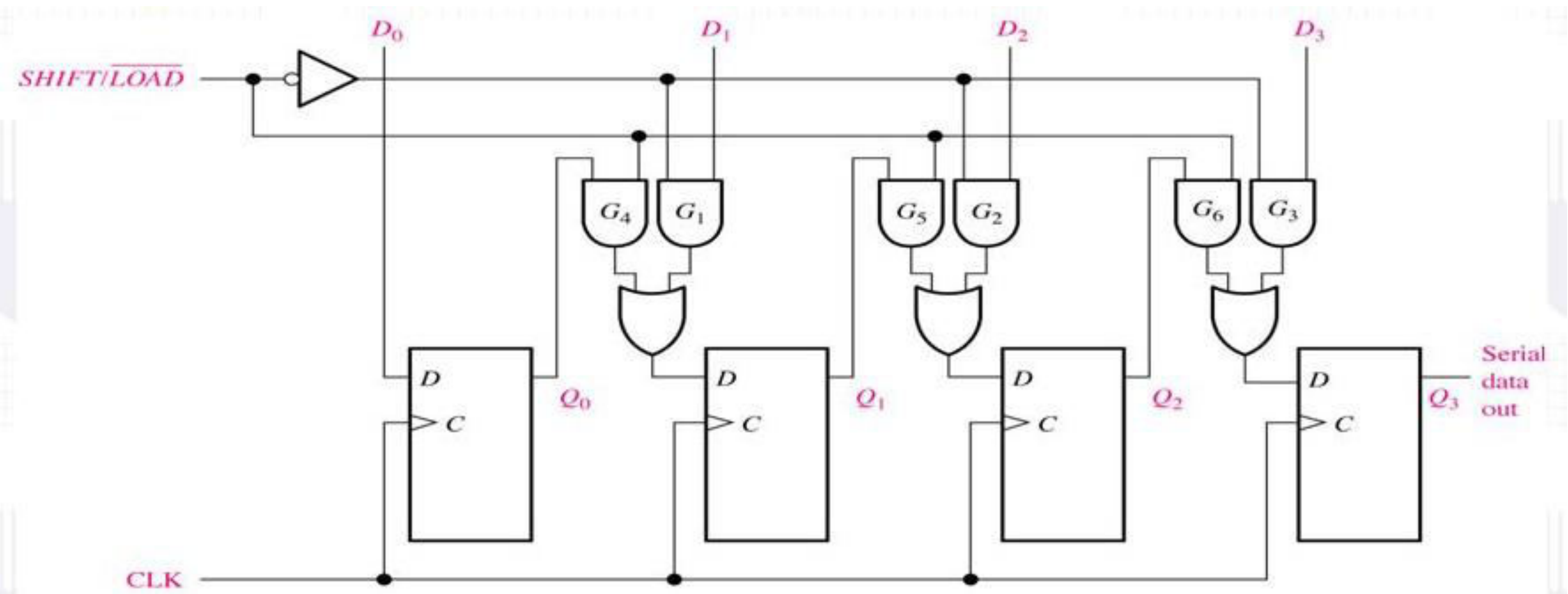


Serial-in/ parallel-out shift register waveforms

Shift Register

Parallel in – Serial out Shift Register

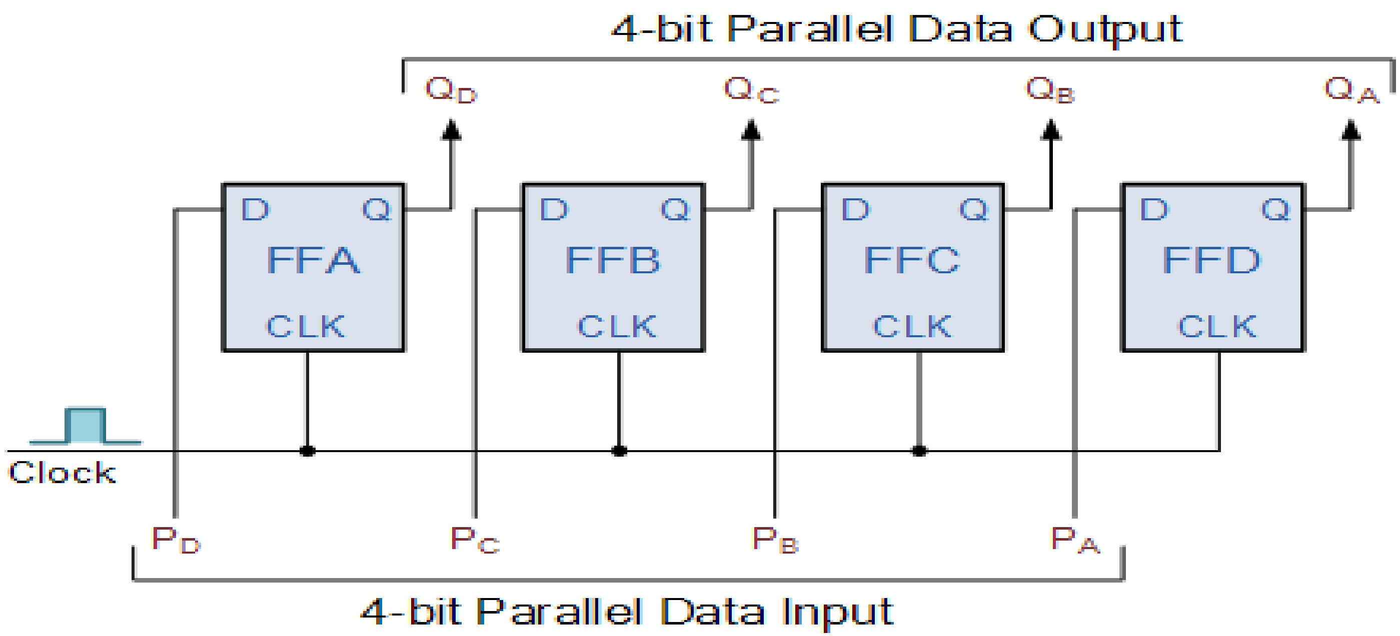
- For this type of shift register, the data is supplied in parallel.
- As this type of shift register converts parallel data, such as an 8-bit data word into serial format, it can be used to multiplex many different input lines into a single serial DATA stream which can be sent directly to a computer or transmitted over a communications line



Shift Register

Parallel in – Parallel out shift register

- For parallel in – parallel out shift register, the output data across the parallel outputs appear simultaneously as the input data is fed in.

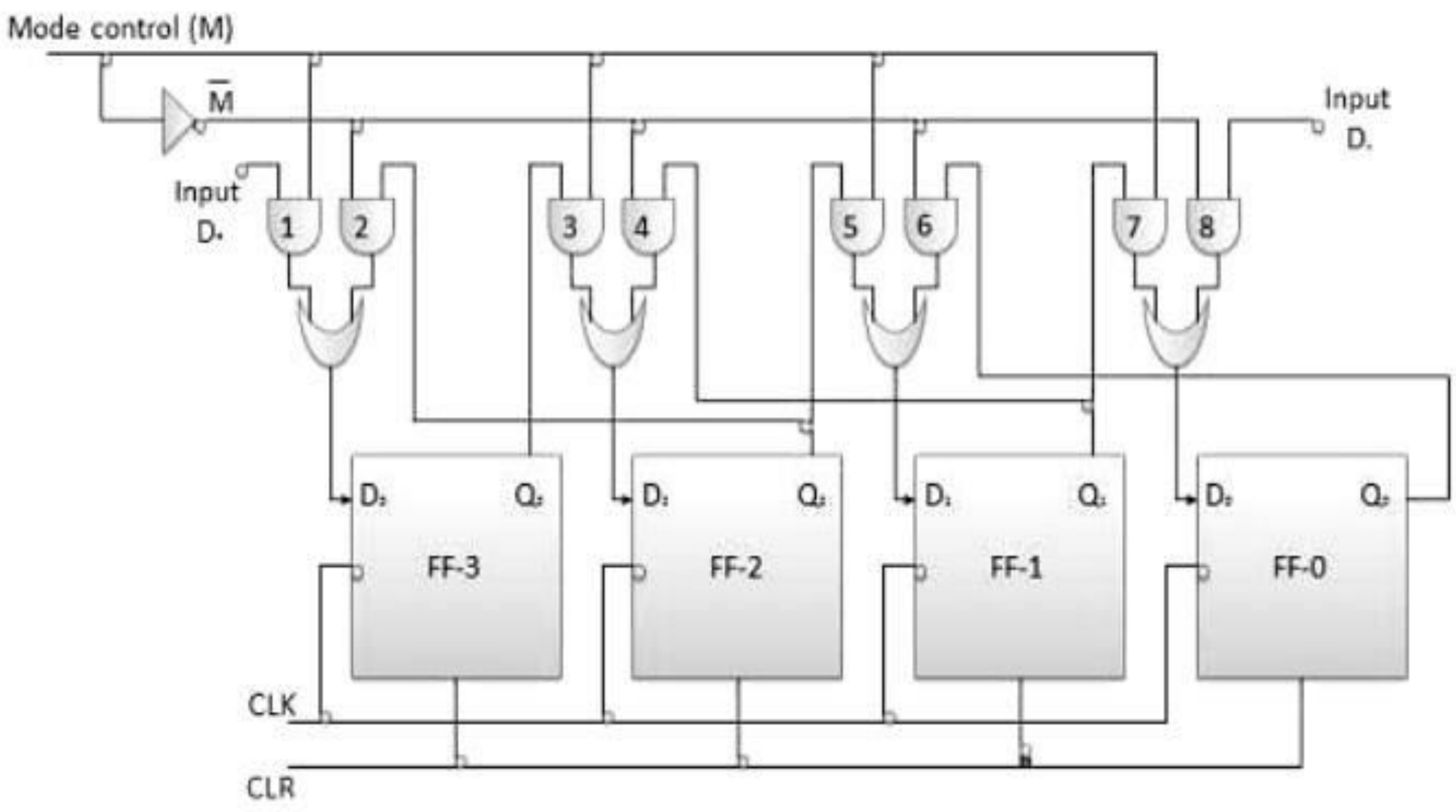


Shift Register

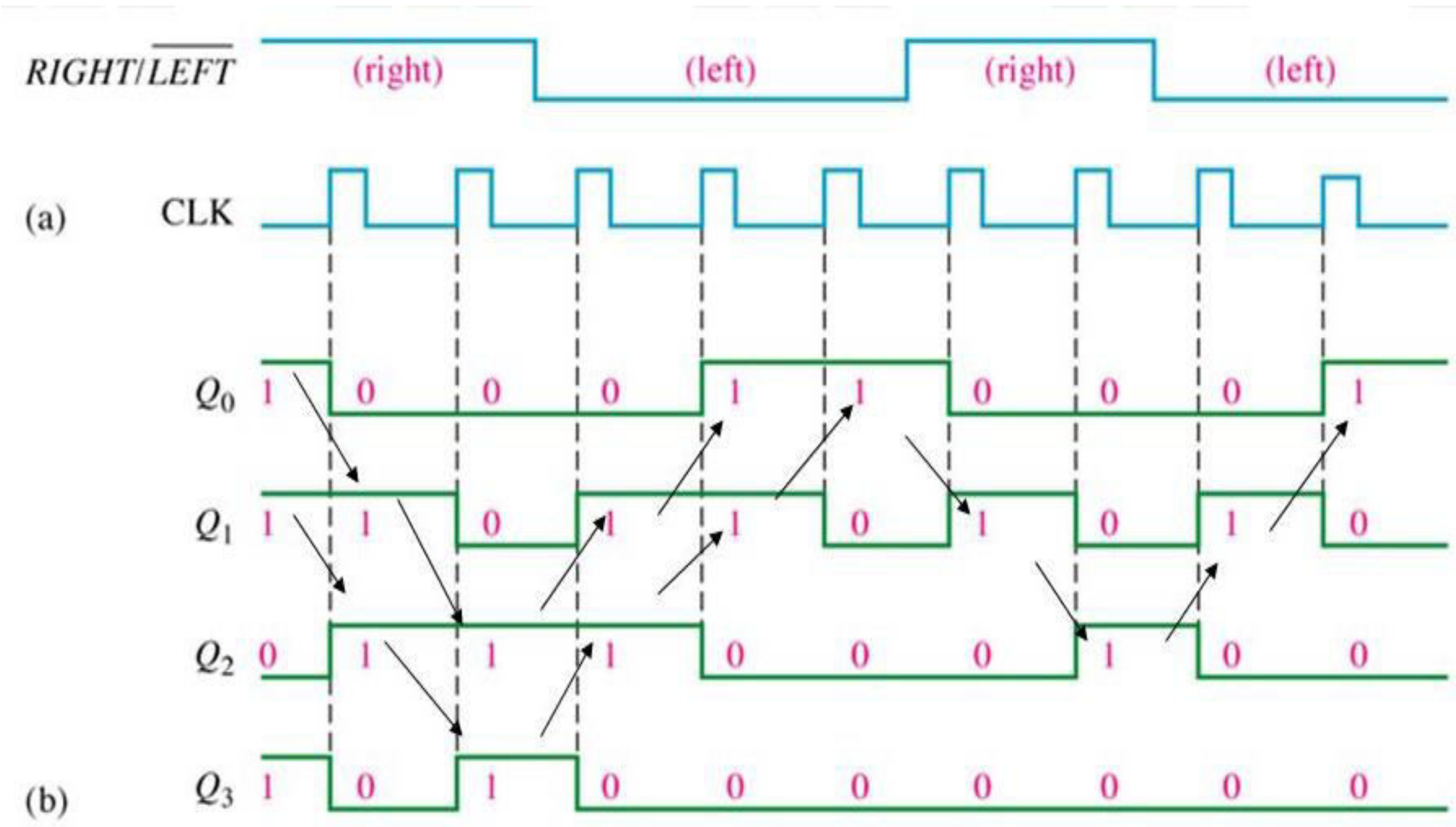
Bidirectional Shift Registers

- If we shift a binary number to the left by one position, it is equivalent to multiplying the number by 2 and if we shift a binary number to the right by one position, it is equivalent to dividing the number by 2.To perform these operations we need a register which can shift the data in either direction.
- Bidirectional shift registers are the registers which are capable of shifting the data either right or left depending on the mode selected. If the mode selected is 1(high), the data will be shifted towards the right direction and if the mode selected is 0(low), the data will be shifted towards the left direction.
- In right shift operations, the binary data is divided by two. If this operation is reversed, the binary data gets multiplied by two.
- A couple of NAND gates are configured as OR gates and are used to control the direction of shift, either right or left.

Shift Register



Shift Register



Universal shift register

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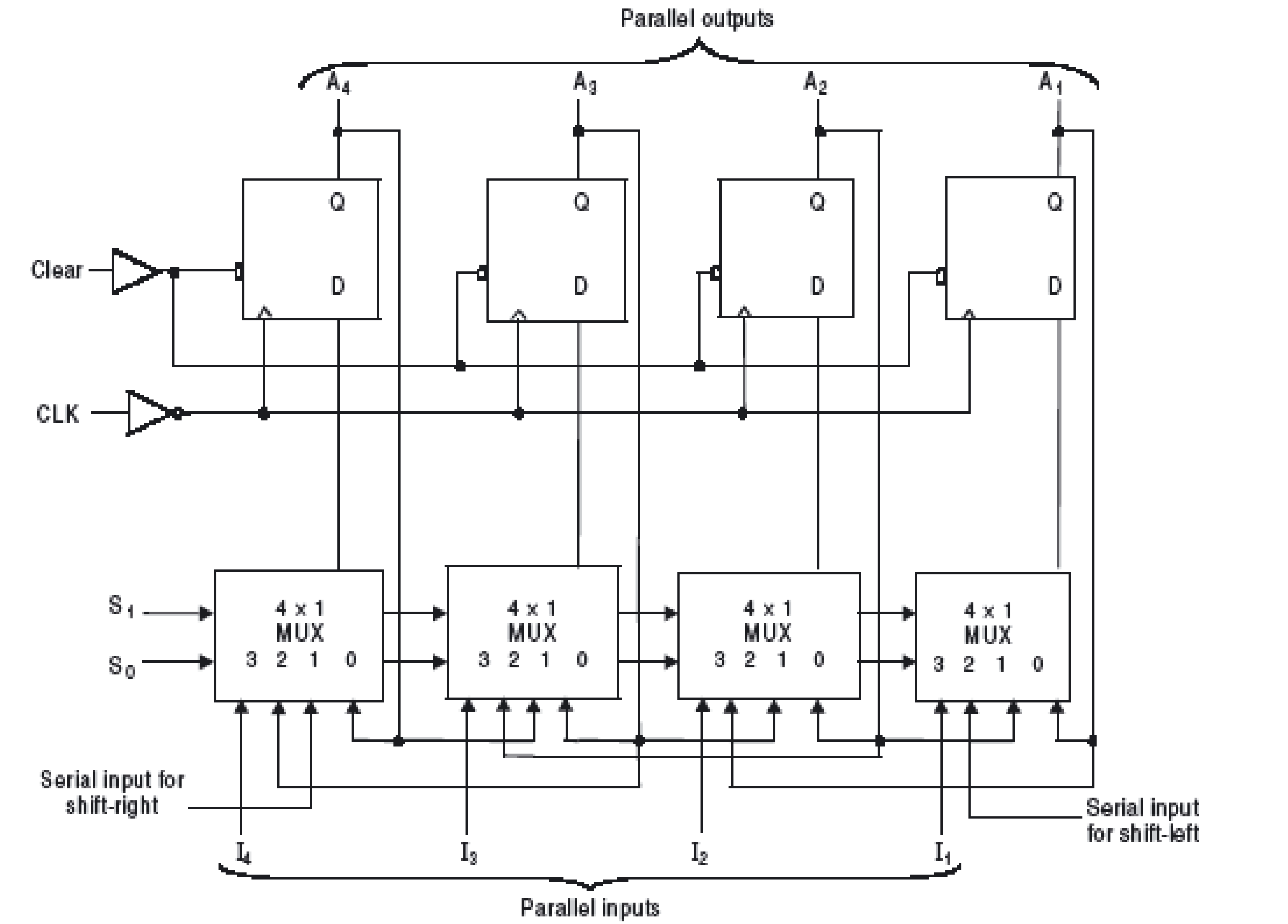

4-bit universal shift register.

Recap

- Shift Registers are sequential logic circuits, capable of storage and transfer of data.
- A *shift register* basically consists of several single bit "D-Type Data Latches", one for each data bit, either a logic "0" or a "1", connected together in a serial type chain arrangement so that the output from one data latch becomes the input of the next latch and so on.

Types of Shift Registers

Generally, shift registers operate in one of four different modes with the basic movement of data through a shift register being:

- Serial-in to Parallel-out (SIPO)
- Serial-in to Serial-out (SISO)
- Parallel-in to Serial-out (PISO)
- Parallel-in to Parallel-out (PIPO)

Daily Quiz

- A bidirectional 4-bit shift register is storing the nibble 1110. Its input is LOW. The nibble 0111 is waiting to be entered on the serial data-input line. After two clock pulses, the shift register is storing

a) 1110
b) 0111
c) 1000
d) 1001

- In a parallel in/parallel out shift register, D0 = 1, D1 = 1, D2 = 1, and D3 = 0. After three clock pulses, the data outputs are ________

a) 1110
b) 0001
c) 1100
d) 1000

- The group of bits 10110111 is serially shifted (right-most bit first) into an 8-bit parallel output shift register with an initial state 11110000. After two clock pulses, the register contains ______________
  a) 10111000
  b) 10110111
  c) 11110000
  d) 11111100

Old Questions

- What are the differences between synchronous and asynchronous counter?
- What do you mean by shift register? What is need of shift register? Draw & explain bidirectional shift register.
- Draw & explain universal shift register.

Weekly Assignment

- What are the differences between synchronous and asynchronous counter?
- Design **MOD-5** ring counter & **MOD -5** Johnson counter.
- What do you mean by shift register? What is need of shift register? Draw & explain bidirectional shift register.
- Design MOD-5 asynchronous counter.
- Design MOD 3 UP/DOWN synchronous counter.
- Explain 4bit Johnson counter with circuit diagram and waveforms. 10
- Design a 4 bit synchronous counter using D flip flop.

Video Link

- https://www.youtube.com/watch?v=Iecj9xmIfXM&ab_channel=nptelhrd
- https://nptel.ac.in/courses/117/106/117106086/

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Thank You