Noida Institute of Engineering and Technology, Greater Noida

Microprocessor

(ACSE0405)

Unit: 5

Programmable peripheral ICs and 8086 microprocessor

B.Tech 4th Semester

Khushboo
Assistant Professor
ECE

Faculty Introduction

I received my Master of Technology from VIT Chennai and Bachelor of Technology from UPTU, Lucknow. I have worked as Software Developer in Cognizant Technology Solutions, Kolkata. Presently I am working as an Assistant Professor in Electronics & Communication Engineering department of Noida Institute of Engineering & Technology, Greater Noida, India. My research interest includes Antennas, IoT and Embedded System.

Evaluation Scheme

Sl. No.	Subject Codes	Subject Name	Periods			Evaluation Scheme				End Semester		Total	Credit
			L	T	P	CT	TA	TOTAL	PS	TE	PE		
1	AAS0402	Engineering Mathematics-IV	3	1	0	30	20	50		100		150	4
2	AASL0401	Technical Communication	2	1	0	30	20	50		100		150	3
3	ACSE0405	Microprocessor	3	0	0	30	20	50		100		150	3
4	ACSE0403A	Operating Systems	3	0	0	30	20	50		100		150	3
5	ACSE0404	Theory of Automata and Formal Languages	3	0	0	30	20	50		100		150	3
6	ACSE0401	Design and Analysis of Algorithm	3	1	0	30	20	50		100		150	4
7	ACSE0455	Microprocessor Lab	0	0	2				25		25	50	1
8	ACSE0453A	Operating Systems Lab	0	0	2				25		25	50	1
9	ACSE0451	Design and Analysis of Algorithm Lab	0	0	2				25		25	50	1
10	ACSE0459	Mini Project using Open Technology	0	0	2				50			50	1
11	ANC0402 / ANC0401	Environmental Science*/ Cyber Security*(Non Credit)	2	0	0	30	20	50		50		100	0
12		MOOCs** (For B.Tech. Hons. Degree)											
		GRAND TOTAL										**1100**	**24**

Subject Syllabus

UNIT-I	8085 Microprocessor	8 Hours
Introduction to Microprocessor, Microprocessor evolutionandtypes, Microprocessorarchitectureand its operation, Logic devices for interfacing,Pin diagram and internal architecture of 8085 Microprocessor,Example of an 8085 based computer, Instructionanddataflow,timerandtimingdiagram,interruptandmachinecycle, Addressingmodes.		
UNIT-II	**8085 Instructions and Programming Techniques**	**8 Hours**
Instructionsets,InstructionClassification:datatransfer operations, arithmeticoperations,logicaloperations,branchingoperations,machinecontrolandassemblerdirectives, writing assembly language programs, Programming techniques: looping, counting and indexing		
UNIT-III	**Code Conversion and BCD Arithmetic**	**8 Hours**
Counter and time delays, Illustrative program: Hexadecimal counter, zero-to-nine, (module ten) counter, generating pulse waveforms, Stack, Subroutine, Restart, Conditional call and return instructions, Advance subroutine concepts, Program: BCD-to-Binary conversion, Binary-to-BCD conversion, BCD-to-Seven segment code converter, Binary-to-ASCII and ASCII-to-Binary code conversion, BCD Addition, BCD Subtraction, Introduction to Advance instructions and Application, Multiplication		
UNIT-IV	**Interfacing of I/O devices**	**8 Hours**
Basic interfacing concepts,Memoryinterfacing,Interfacing output displays, Interfacing input devices, Memory mapped I/O,Interfacing keyboard and seven segment displays, The 8085 Interrupts, 8085 vector interrupts,8259 programmable interrupt controller,		
UNIT-V	**Programmable Peripheral IC's and 8086 Microprocessor**	**8 Hours**
Peripheral Devices: 8255 programmable peripheral interface,8253/8254 programmable timer/counter, 8237 DMA Controller, 8251 USART and RS232C.Introduction to 8086 microprocessors: Architecture of 8086 (Pin diagram, Functional block diagram, register organization), Addressing Modes		

Branch Wise Application

- Digital electronics is the basic building for every system while in IOT we are using Sensors and Microprocessor and microcontroller.
- Microcontrollers use network interfaces to interact with other devices locally and to push the data to the IoT application for any analysis.

Course Objective

- To teach the fundamental concepts of logic systems and various logic circuit optimization techniques.
- Understand techniques for the designing of combinational & sequential circuits.
- The objective of this course is to understand basic concepts of Microprocessor based systems and able to do programming in Assembly Language of 8085. They will be able to learn and program Peripheral IC's.

Course Outcome

At the end of this course students will able to:

- Apply a basic concept of digital fundamentals to Microprocessor based personal computer system.
- Analyze a detailed s/w & h/w structure of the Microprocessor.
- Illustrate how the different peripherals (8085/8086) are interfaced with Microprocessor.
- Analyze the properties of Microprocessors (8085/8086)
- Evaluate the data transfer information through serial & parallel ports.

Program Outcomes

- **Program Outcomes** are narrow statements that describe what the students are expected to know and would be able to do upon the graduation.

- These relate to the skills, knowledge, and behavior that students acquire through the programmed.

1. Engineering knowledge
2. Problem analysis
3. Design/development of solutions
4. Conduct investigations of complex problems
5. Modern tool usage
6. The engineer and society
7. Environment and sustainability
8. Ethics
9. Individual and team work
10. Communication
11. Project management and finance
12. Life-long learning

CO-PO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
1	3	2	-	-	-	-	-	-	-	-	-	2
2	3	3	2	-	-	-	-	-	-	-	-	2
3	2	3	2	2	-	-	-	-	-	-	-	2
4	3	3	3	2	-	-	-	-	-	-	-	2
5	3	2	1	-	-	-	-	-	-	-	-	2
AVERAGE	2.8	2.6	2	2	-	-	-	-	-	-	-	2

End Semester Question Paper Template

B.Tech (Semester III Theory Examination 2021-22)			**Total Marks : 100**
Note: Attempt all sections. If require any missing data, then choose suitably. **Time: 3 hours**			
Section A			
1. Attempt all questions in brief.		2 X 10 = 20	
Q. No.	Question	Marks	CO
a. to j		2	
Section B			
2. Attempt any three of the following		3 X 10 = 30	
Q. No.	Question	Marks	CO
a to e		10	
Section C			
Question no. 3,4,5,6,7. Attempt any one of the following		1 X 10 = 10	
a		10	
b		10	

Prerequisite

- Understanding of Digital Logic Design
- Knowledge of Analog Electronics

Prerequisites

- Boolean Algebra is used to analyze and simplify the digital (logic) circuits.
- It uses only the binary numbers i.e. 0 and 1.
- It is also called as **Binary Algebra** or **logical Algebra**.
- Binary logic consists of binary variables and a set of logical operations.
- Here variable having two and only two distinct possible values: 1 and 0.
- There are three basic logical operations: AND, OR, and NOT.

Recap

Data transfer operations

Ex.

a) MOV
b) MVI
c) LXI
d) LDA
e) STA
f) LDAX
g) STAX
h) XCHG
i) LHLD
j) SHLD

SOURCE	DESTINATION
Register	Register
Memory	Register
Register	Memory
Register(ACC)	I/O device
I/O device	Register(ACC)
Data	Register

Recap

Arithmetic operations

Ex:

Addition : ADD, ADI, ADC, ACI, DAD

Subtraction: SUB, SUI, SBB, SBI

Increment: INR, INX

Decrement: DCR, DCX

Logical operations

Ex:

a) AND
b) OR
c) XOR
d) CMA
e) CMP
f) CMC
g) STC
h) Rotate: RLC, RAL, RRC, RAR

Brief Introduction about Subject

Digital electronics **deals with the electronic manipulation of numbers**, or with the manipulation of varying quantities by means of numbers. Because it is convenient to do so, today's digital systems deal only with the numbers 'zero' and 'one', because they can be represented easily by 'off and 'on' within a circuit.

The microprocessor is useful in very intensive processes. It only contains a CPU (central processing unit) but there are many other parts needed to work with the CPU to complete a process. These all other parts are connected externally.

Microprocessors are not made for a specific task as well as they are useful where tasks are complex and tricky like the development of software, games, and other applications that require high memory and where input and output are not defined.

Video link: https://youtu.be/DBTna2ydmC0

Unit Content

- Course Objective
- Unit Objective
- Course Outcome
- Co and Po Mapping
- Topic Objective
- Prerequisite
- Features and Pin description of Intel 8086 Microprocessor
- Architecture of Intel 8086 Microprocessor
- Addressing Modes
- 8237 DMA Controller
- 8255 Programmable Peripheral Interface
- 8253 Programmable Interrupt Timer
- 8259 Programmable Interrupt Controller
- Communication Protocols
- Daily quiz & MCQs
- Old Question Papers
- Recap
- Video Links
- Weekly Assignments
- References

Topic Objective and its Mapping with CO

Name of Topic	Objective of Topic	Mapping with CO
8255 Programmable Peripheral Interface	Students will be able to outline the features and Architecture of 8255 Programmable Peripheral Interface	CO5

8255 programmable peripheral interface

Introduction

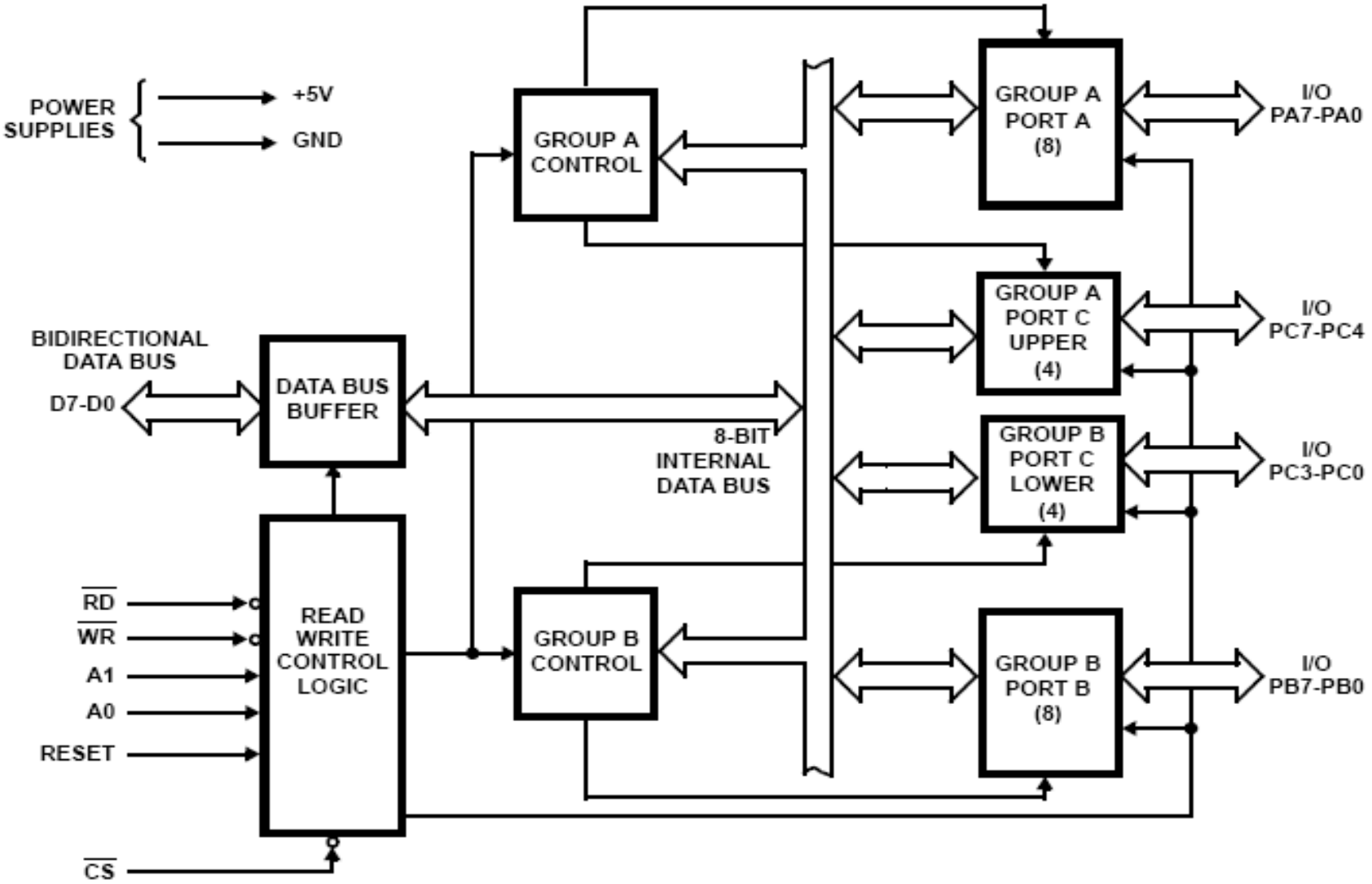
- The 8255 PPI is a programmable peripheral interface device.
- It contains 3 I/O ports (Port A, Port B & Port C) which can be programmed in different modes.
- To program the function to all three I/O ports, it contains a register called as control registers. The control register defines the function of each I/O port and in which mode they should operate.

8255 programmable peripheral interface

8255 PPI Functional Block Diagram

- It contains the following blocks
- Data bus buffer
- Read/Write control logic
- Group A and Group B control
- Port A and Port B
- Port C

8255 PPI Block Diagram



8255 programmable peripheral interface

Function of pins

Data bus(D0-D7):

- These are 8-bit bi-directional buses, connected to 8085 data bus for transferring data.

$\overline{CS}$:

- This is Active Low signal. When it is low, then data is transfer from 8085.

$\overline{RD}$:

- This is Active Low signal, when it is Low read operation will be start.

$\overline{WR}$:

This is Active Low signal, when it is Low Write operation will be start.

Address (A0-A1):

- This is used to select the ports.

8255 programmable peripheral interface

Function of pins

A1	A0	Select
0	0	PA
0	1	PB
1	0	PC
1	1	Control reg.

8255 programmable peripheral interface

Function of pins

RESET: This is used to reset the device. That means clear control registers.

PA0-PA7: It is the 8-bit bi-directional I/O pins used to send the data to peripheral or to receive the data from peripheral.

PB0-PB7: Similar to PA

PC0-PC7:This is also 8-bit bidirectional I/O pins. These lines are divided into two groups.

- PC0 to PC3(Lower Groups)
- PC4 to PC7 (Higher groups)

These two groups working in separately using 4 data's.

8255 programmable peripheral interface

Data Bus buffer:

- It is a 8-bit bidirectional Data bus.
- Used to interface between 8255 data bus with system bus.
- The internal data bus and Outer pins D0-D7 pins are connected in internally.
- The direction of data buffer is decided by Read/Control Logic.

Read/Write Control Logic:

- This is getting the input signals from control bus and Address bus.
- Control signal are RD and WR.
- Address signals are A0,A1,and CS.
- 8255 operation is enabled or disabled by CS.

8255 programmable peripheral interface

Group A and Group B control:

- Group A and B get the Control Signal from CPU and send the command to the individual control blocks.
- Group A send the control signal to port A and Port C (Upper) PC7-PC4.
- Group B send the control signal to port B and Port C (Lower) PC3-PC0.

PORT A:

- This is a 8-bit buffered I/O latch.
- It can be programmed by mode 0, mode 1, mode 2 .

PORT B:

- This is a 8-bit buffer I/O latch.
- It can be programmed by mode 0 and mode 1.

8255 programmable peripheral interface

PORT C:

- This is a 8-bit Unlatched buffer Input and an Output latch.
- It is splitted into two parts.
- It can be programmed by bit set/reset operation.

8255 PPI Operation Modes

Operation modes:

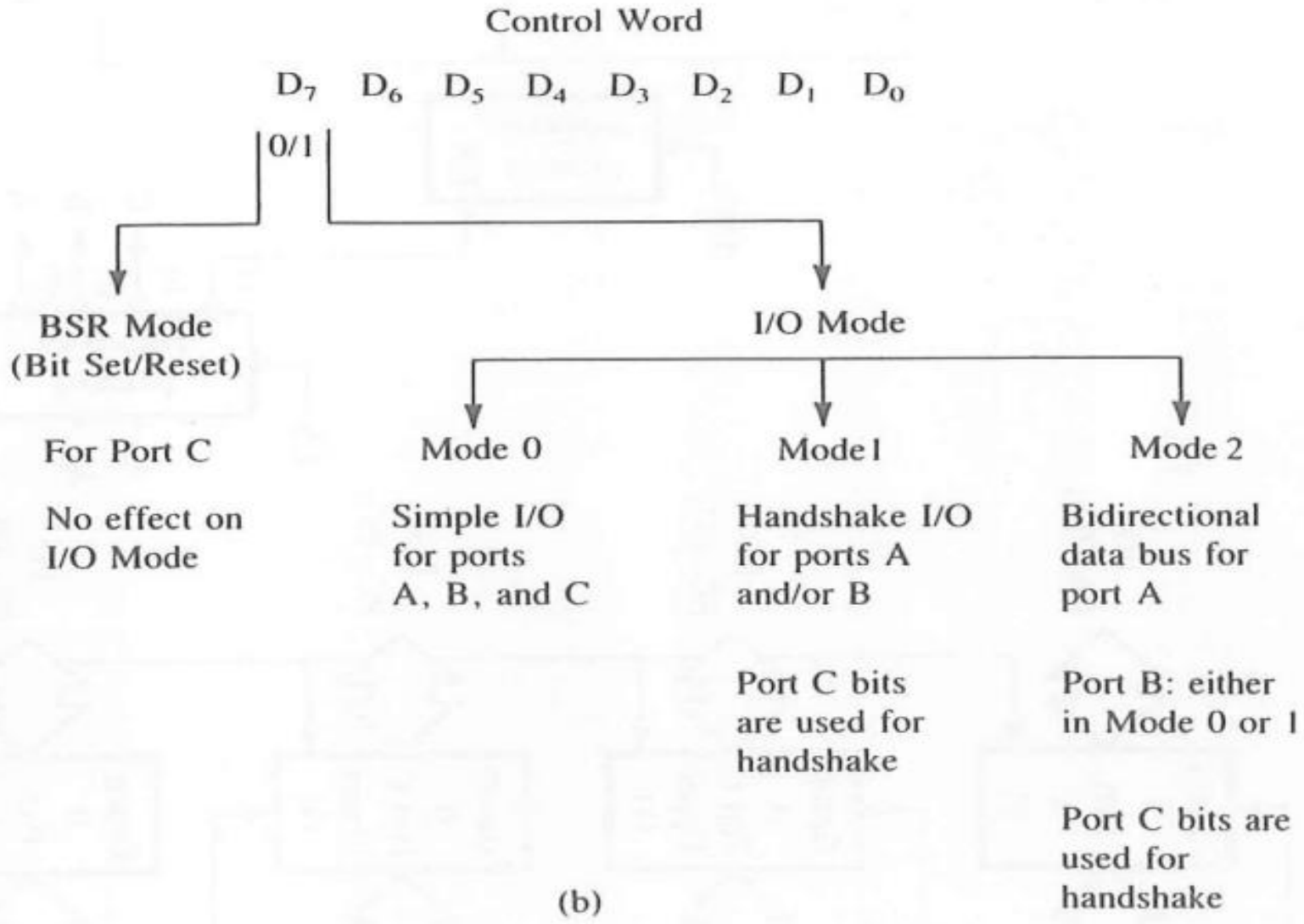
1. BIT SET/RESET MODE
2. I/O MODES
   - Mode 0
   - Mode 1
   - Mode 2

BIT SET/RESET MODE:

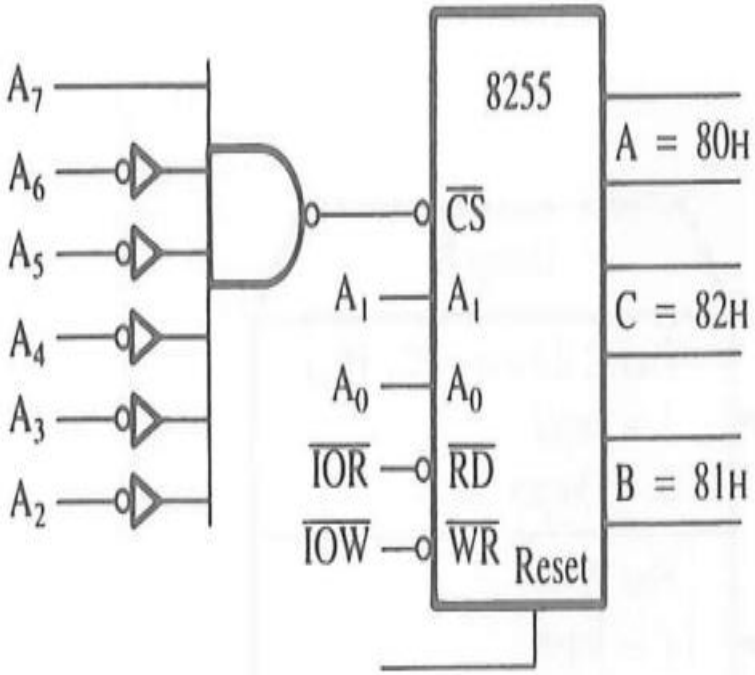
- The PORT C can be Set or Reset by sending OUT instruction to the CONTROL registers.

8255 PPI Operation Modes

8255A Modes:



8255 PPI Operation Modes



(a)

$\overline{CS}$		Hex Address	Port
A_7 A_6 A_5 A_4 A_3 A_2	A_1 A_0		
1 0 0 0 0 0	0 0	= 80H	A
	0 1	= 81H	B
	1 0	= 82H	C
	1 1	= 83H	Control Register

(b)

FIGURE 15.3
8255A Chip Select Logic (a) and I/O Port Addresses (b)

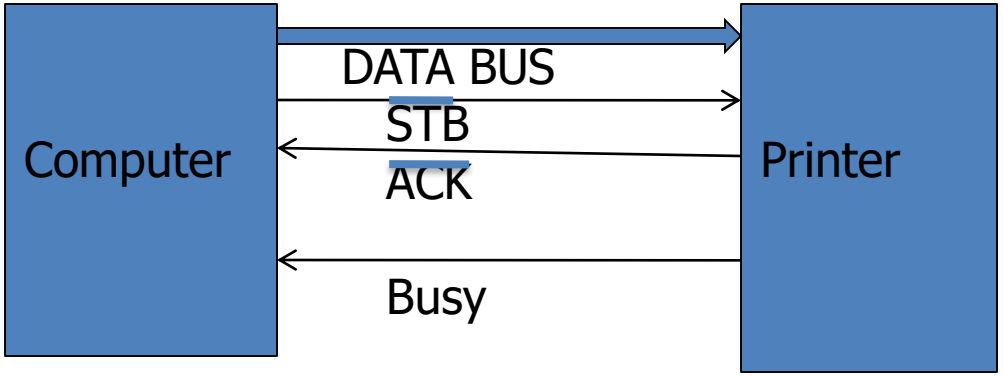
8255 programmable peripheral interface

I/O MODES:

- MODE 0 (Simple input / Output)
  - In this mode , port A, port B and port C is used as individually (Simply).
  - Features:
    - Outputs are latched , Inputs are buffered not latched.
    - Ports do not have Handshake or interrupt capability.

MODE 1 :(Input/output with Hand shake)

- In this mode, input or output is transferred by hand shaking Signals.



8255 programmable peripheral interface

MODE 2:bi-directional I/O data transfer:

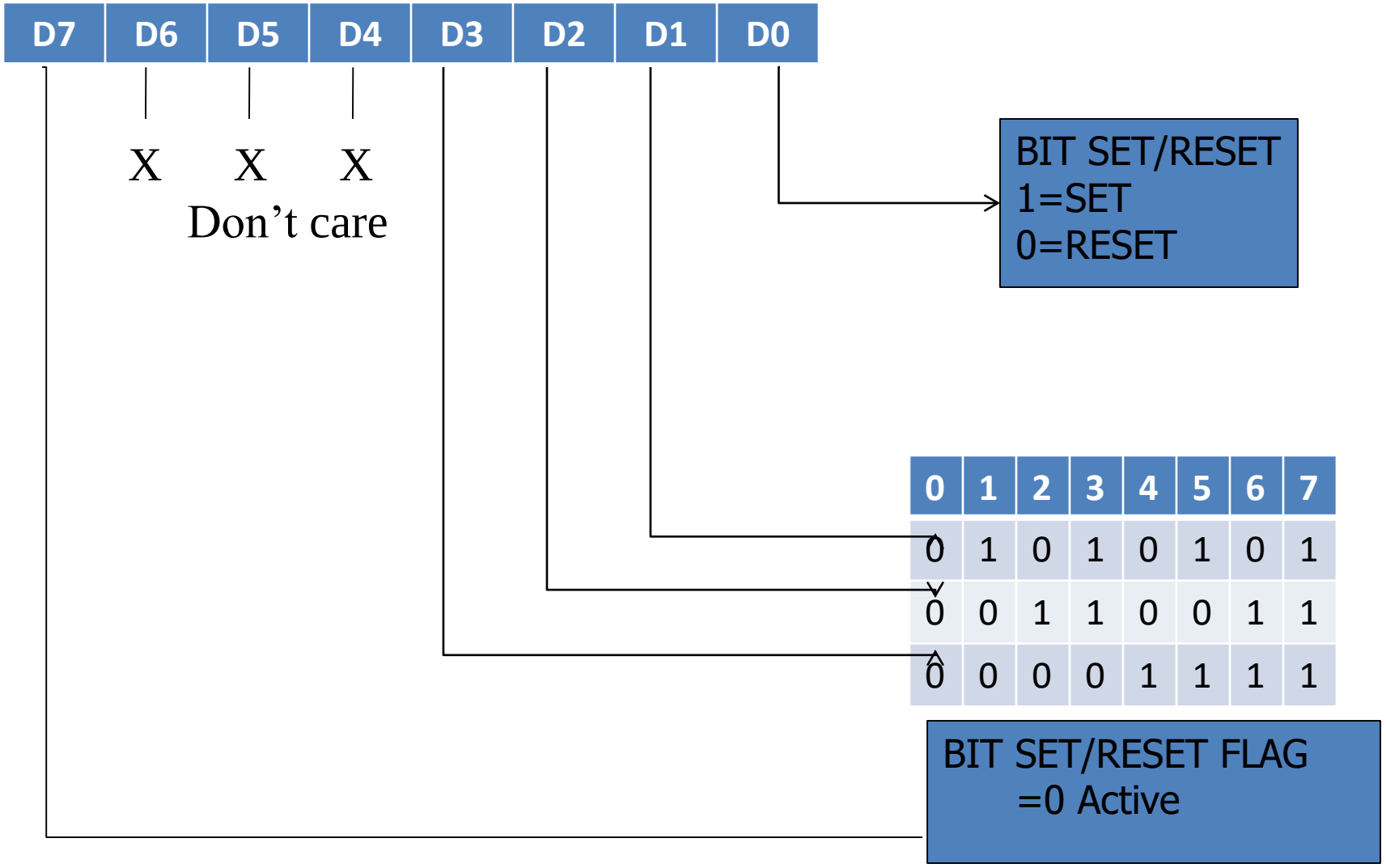
- This mode allows bidirectional data transfer over a single 8-bit data bus using handshake signals.
- This feature is possible only in Group A.
- Port A is working as 8-bit bidirectional.
- PC3-PC7 is used for handshaking purpose.
- The data is sent by CPU through this port , when the peripheral request it.

CONTROL WORD FORMATS:

- In the INPUT mode , When RESET is High all 24 pins (3-ports) be a input mode.
- This condition is maintained even after RESET goes low.
- This can be avoid by writing single control word to the control registers , when required.

8255 PPI Control Word Format- BSR Mode

BIT SET/RESET MODE:



8255 PPI Control Word Format- BSR Mode

BIT SET/RESET MODE:

- This is bit set/reset control word format.
- PC0-PC7 is set or reset as per the status of D0.
- A BSR word is written for each bit.

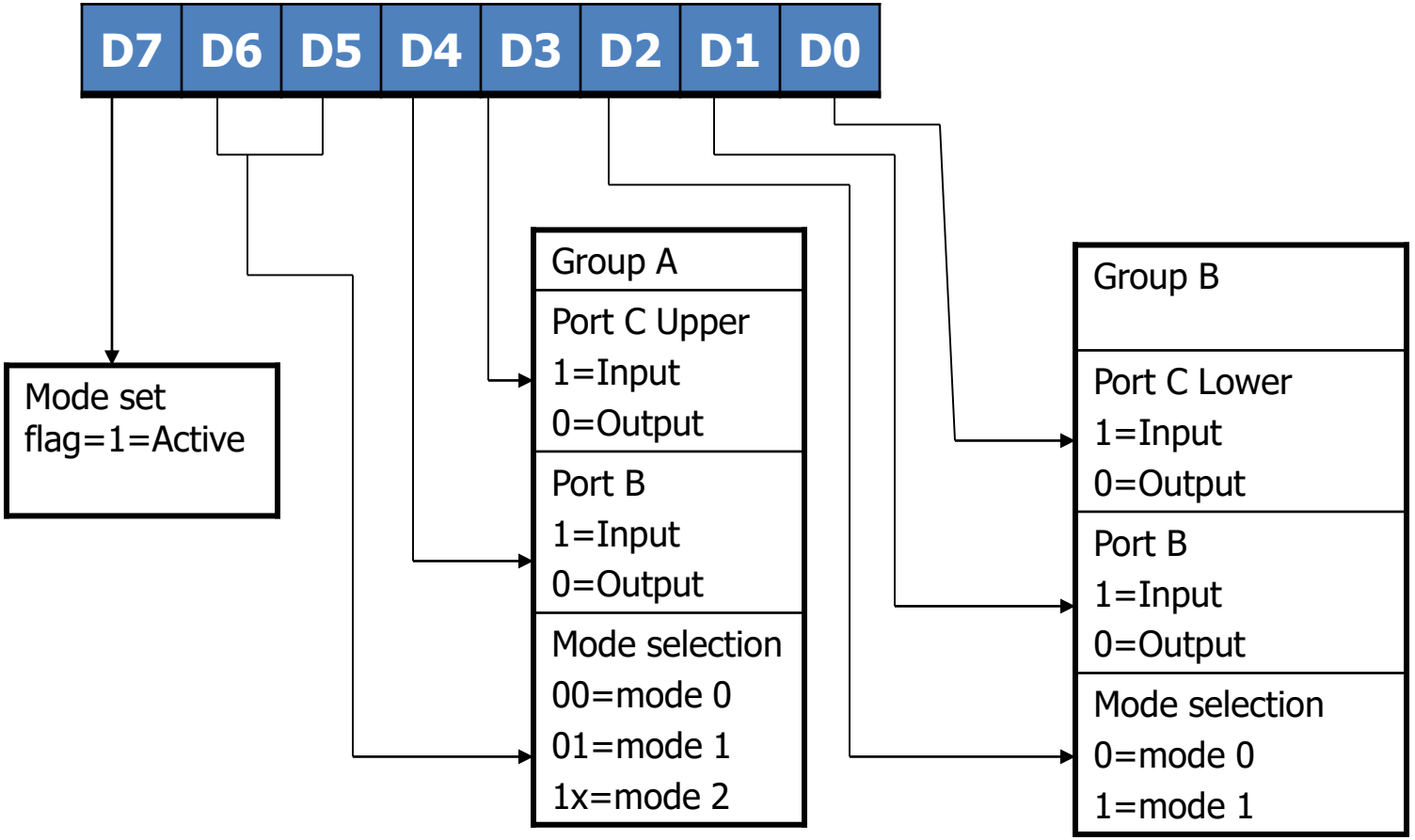
Example:

- PC3 is Set then control register will be 0XXX0111.
- PC4 is Reset then control register will be 0XXX01000.
- X is a don’t care.

8255 PPI Control Word Format- I/O Mode

I/O MODE:

- The mode format for I/O as shown in figure.



8255 programmable peripheral interface

BIT SET/RESET MODE:

- The control word for both mode is same.
- Bit D7 is used for specifying whether word loaded in to Bit set/reset mode or Mode definition word.
- D7=1=Mode definition mode.
- D7=0=Bit set/Reset mode.

Quiz

- How many pins does the 8255 PPI IC contains?

a) 24

b) 20

c) 32

d) 40

- In which mode do all the Ports of the 8255 PPI work as Input-Output units for data transfer?

a) BSR mode

b) Mode 0 of I/O mode

c) Mode 1 of I/O mode

d) Mode 2 of I/O mode

Quiz

- Which of the following pins are responsible for handling the on the Read Write control logic unit of the 8255 PPI?

a) CS'

b) RD'

c) WR'

d) ALL of the above

- In which of the following modes is the 8255 PPI capable of transferring data while handshaking with the interfaced device?

a) BSR mode

b) Mode 0 of I/O mode

c) Mode 1 of I/O mode

d) Mode 2 of I/O mode

Quiz

- What is the size of internal bus of the 8255 PPI?

a) 16 bits

b) 12 bits

c) 8 bits

d) None of the above

- Which port of the 8255 PPI is capable of performing the handshaking function with the interfaced devices?

a) Port A

b) Port B

c) Port C

d) All of the above

Quiz

- In which of the following modes of the 8255 PPI, only port C is taken into consideration?

a) BSR mode

b) Mode 0 of I/O mode

c) Mode 1 of I/O mode

d) Mode 2 of I/O mod

- In mode 2 of I/O mode, which of the following ports are capable of transferring the data in both the directions?

a) Port A

b) Port B

c) Port C

d) All of the above

YouTube & NPTEL Video Links

YouTube/other Video Links

- https://www.youtube.com/watch?v=3RfqkVyvnnc

Recap

- Features of 8255 PPI
- Pin description and ports of PPI
- Modes of PPI and its working

Topic Objective and its Mapping with CO

Name of Topic	Objective of Topic	Mapping with CO
8253/8254 Programmable Timer/Counter	Students will be able to outline the Architecture and operation of 8253/8254 Programmable Timer/Counter	CO5

8253/8254 Programmable Interval Timer/Counter

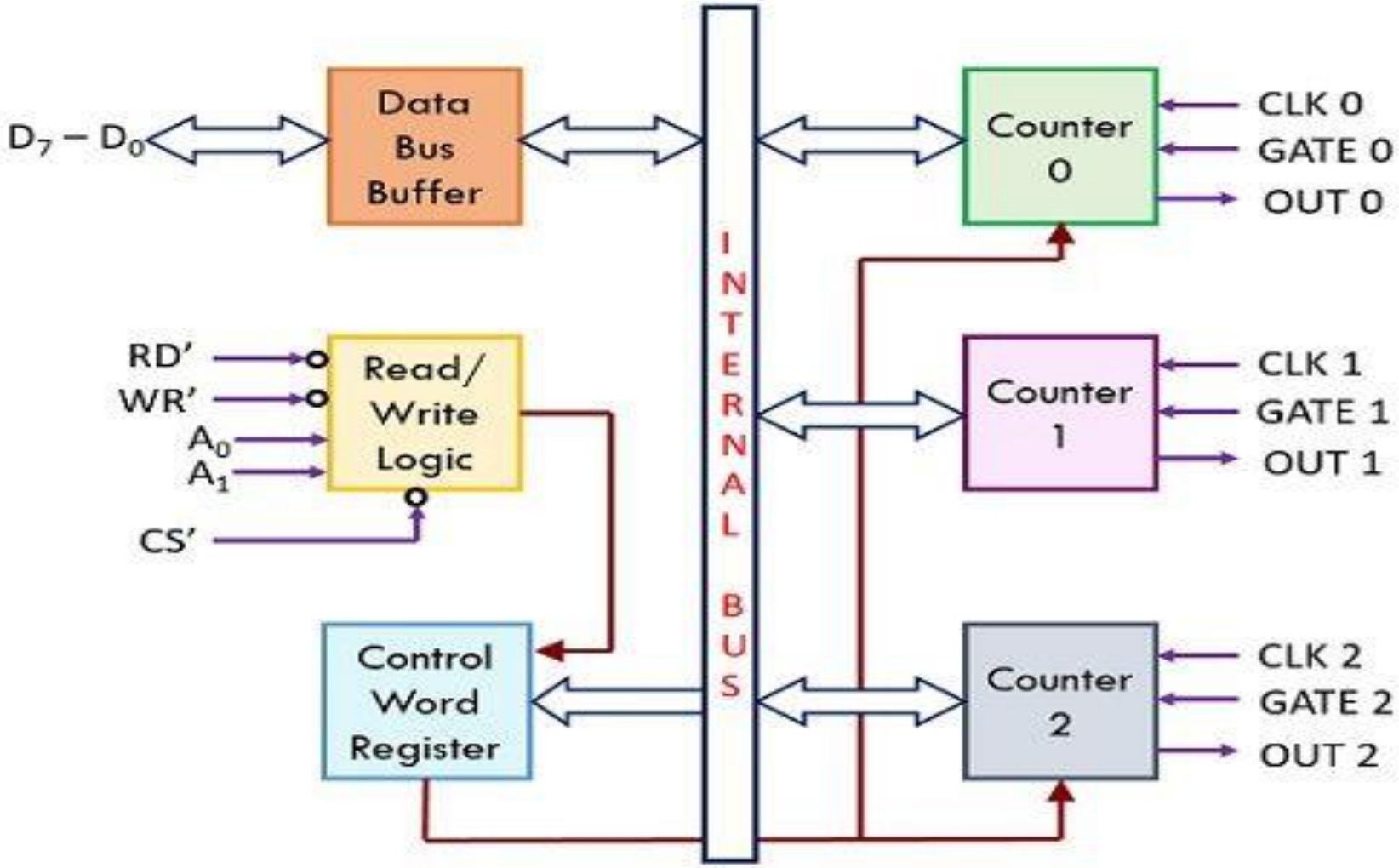
- **Intel 8254** is a **programmable interval timer** designed by intel is a programmable external timer device built with an aim to resolve the time control issues that occur in between various processes occurring within the microprocessor.
- Intel 8254 is an external timer that maintains the timing of the processor operations.
- In order to communicate with the processor, it has a total of 8 data lines.
- There are overall 24 pin signals in which it operates and the power supply provided to it is **+5V**.

8253/8254 Programmable Interval Timer/Counter

Features-

1. Three Independent 16-Bit Counters,
2. Clock input upto 10 MHz,
3. Status Read-Back Command,
4. Six Programmable Counter Modes,
5. Binary or BCD Counting,
6. Single +5V Supply,
7. Superset of PIT-8253

8253/8254 Programmable Interval Timer/Counter



Functional Block Diagram of 8254 Timer

8253/8254programmable timer/counter

Internal Blocks of Counter

- The Control Word Register is not part of the Counter itself, but its contents determine how the Counter operates.
- The status register, when latched, contains the current contents of the Control Word Register and status of the output and null count flag.

8254 Programming

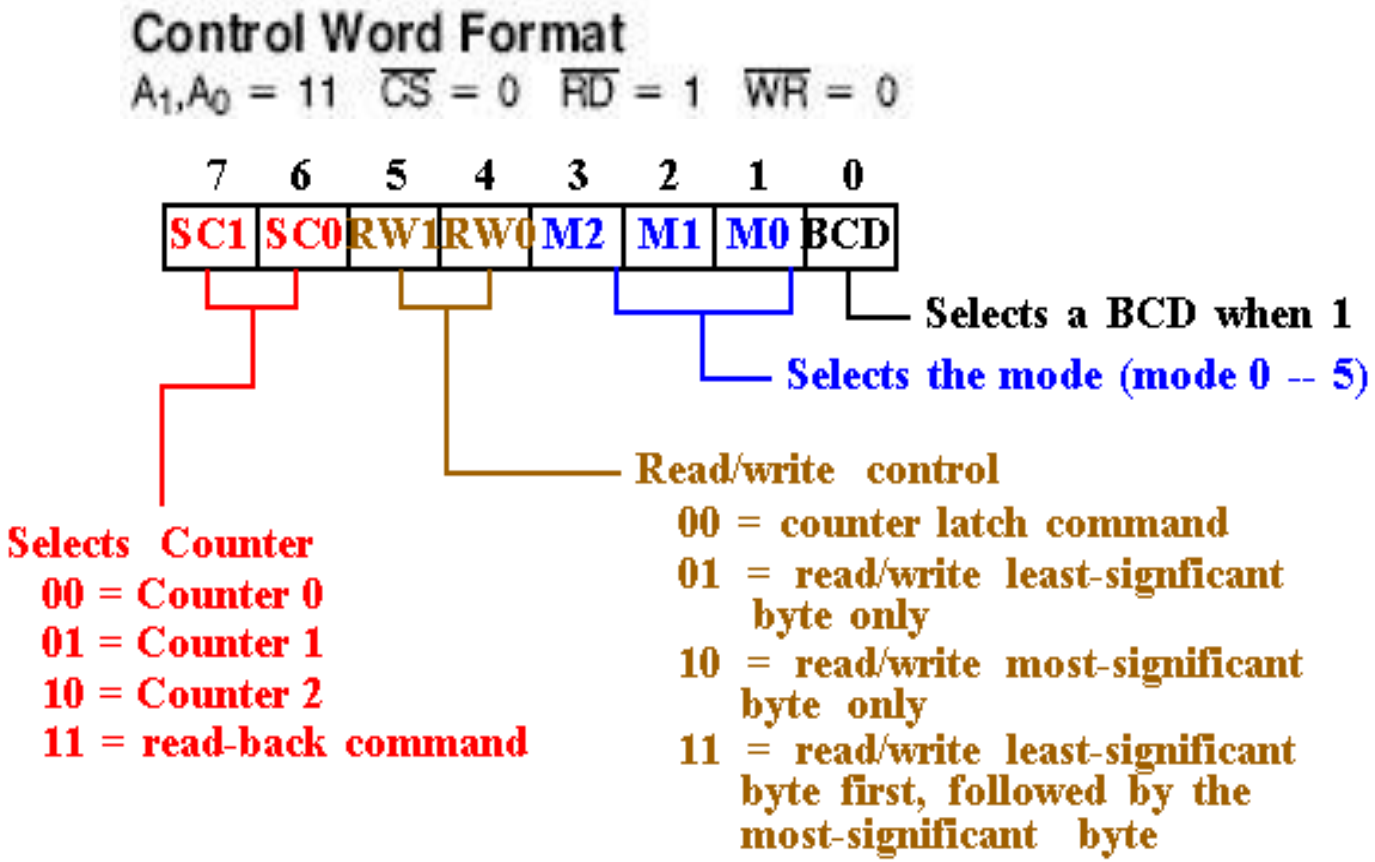
- Each counter is individually programmed by writing a control word, followed by the initial count.
- The control word allows the programmer to select the counter, mode of operation, binary or BCD count and type of operation (read/write).

8253/8254programmable timer/counter

A_1	A_0	Device Selected
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Register

8253/8254programmable timer/counter

Control Word format



8253/8254programmable timer/counter

WRITE Operation

- Control Word to Control register
- Initial count must follow the count format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

$$\overline{CS} = 0 \quad \overline{RD} = 1 \quad \overline{WR} = 0$$

READ Operation

- Three Possible Methods to read counters
  - Simple Read Operation,
  - Counter Latch Command,
  - Read Back Command.

$$\overline{CS} = 0 \ , \ \overline{RD} = 0 \ , \ \overline{WR} = 1$$

8253/8254programmable timer/counter

Modes of 8254

Six Different Modes

- Mode 0: Interrupt On Terminal Count
- Mode 1: Hardware Retriggerable One-shot
- Mode 2: Rate Generator
- Mode 3: Square Wave Mode
- Mode 4: Software Triggered Strobe
- Mode 5: Hardware Triggered Strobe (Retriggerable)

Applications of 8254

- Real time clock
- Event-counter
- Digital one-shot
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

Quiz

- Which of the following uses N-MOS technology?

A. 8253
B. 8254
C. 8255
D. 8256

- It is a tri-state, bi-directional, 8-bit buffer, which is used to interface the 8253 to the system data bus.

A. A. Read/Write Logic
B. B. Data Bus Buffer
C. C. system data bus
D. D. System Buffer

Quiz

- 8253 can be operated in _____ Modes?

A. 3
B. 4
C. 5
D. 6

- Which mode can be used as a mono stable multi-vibrator?

A. Mode 0
B. Mode 1
C. Mode 2
D. Mode 3

- Which mode generates a strobe in response to an externally generated signal?

A. Mode 3
B. Mode 4
C. Mode 5
D. Mode 6

Quiz

- Which mode generates a strobe in response to an externally generated signal?

A. Mode 3
B. Mode 4
C. Mode 5
D. Mode 6

- It is a tri-state, bi-directional, 8-bit buffer, which is used to interface the 8253 to the system data bus.

A. Read/Write Logic
B. Data Bus Buffer
C. System data bus
D. System Buffer

Recap

- Features of PIT
- Block diagram and Operation of PIT
- Modes Operation of PIT

Topic Objective and its Mapping with CO

Name of Topic	Objective of Topic	Mapping with CO
Introduction to 8237 DMA Controller	The objective of the student is to Introduce with 8237 DMA Controller	CO5

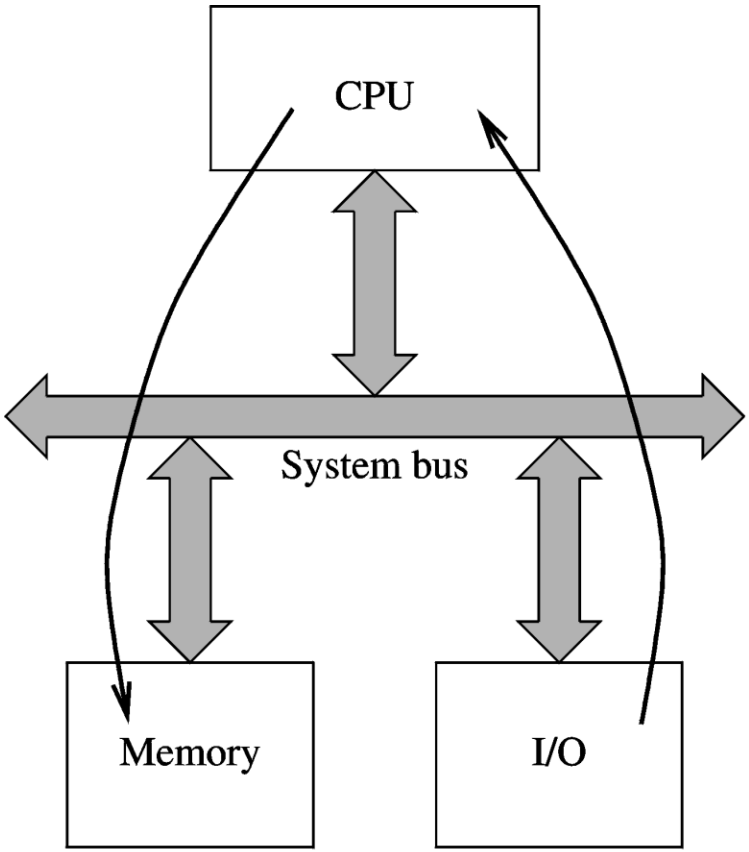
8237 DMA Controller

DMA

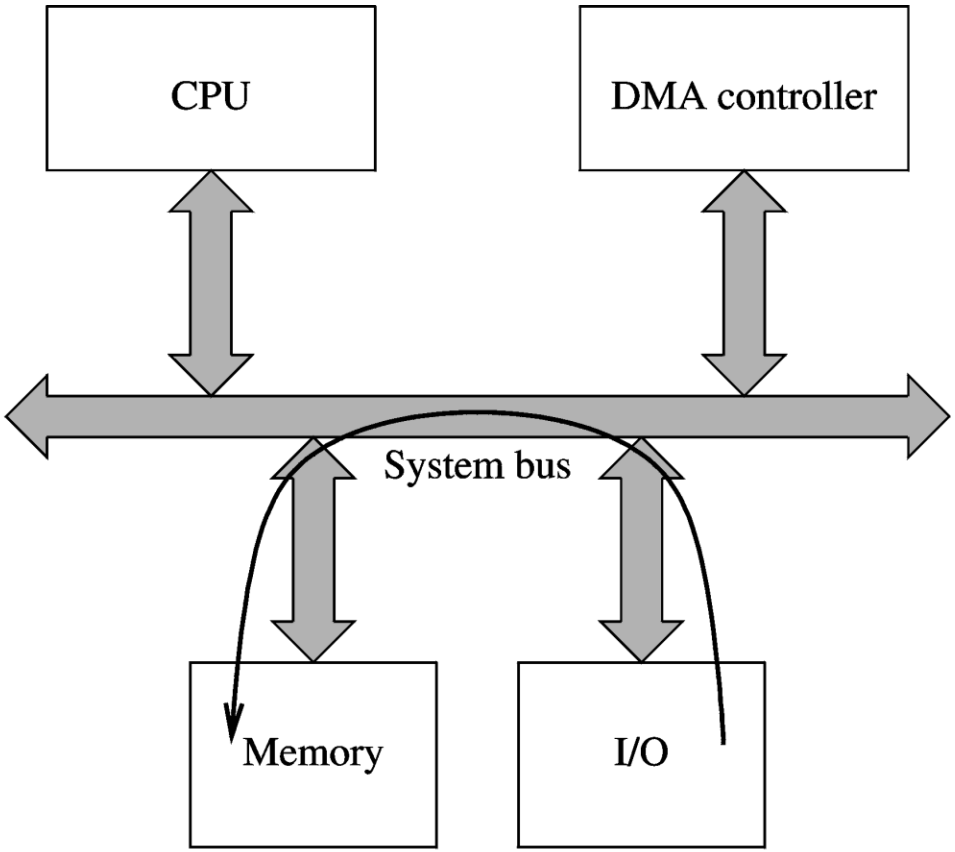
- The DMA I/O technique provides direct access to the memory while the microprocessor is temporarily disabled.
- In memory-memory or memory-peripherals communication, the processor is a "middleman" which is not really needed.
- Used with HOLD & HLDA signals.
- DMA requires another processor - The DMA Controller or DMAC- to generate the memory and I/O addresses.

8237 DMA Controller

I/O Data Transfer



(a) Programmed I/O transfer



(b) DMA transfer

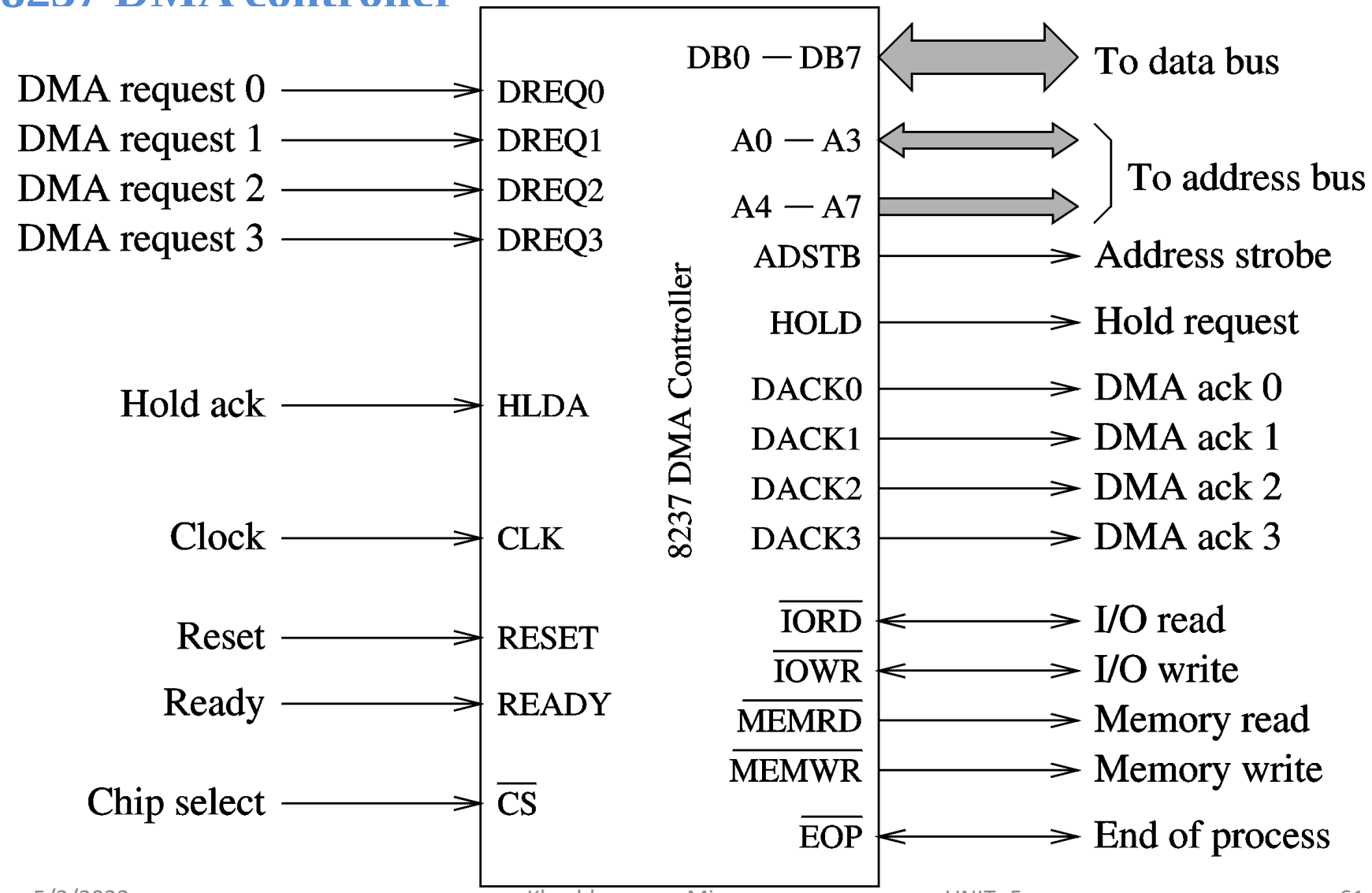
8237 DMA Controller

BASIC DMA TERMINOLOGY

- ***DMA channel***: system pathway used by a device to transfer information directly to and from memory. There are usually 8 in a computer system
- ***DMA controller***: dedicated hardware used for controlling the DMA operation
- ***Single-cycle mode****:* DMA data transfer is done one byte at a time
- ***Burst-mode****:* DMA transfer is finished when all data has been moved

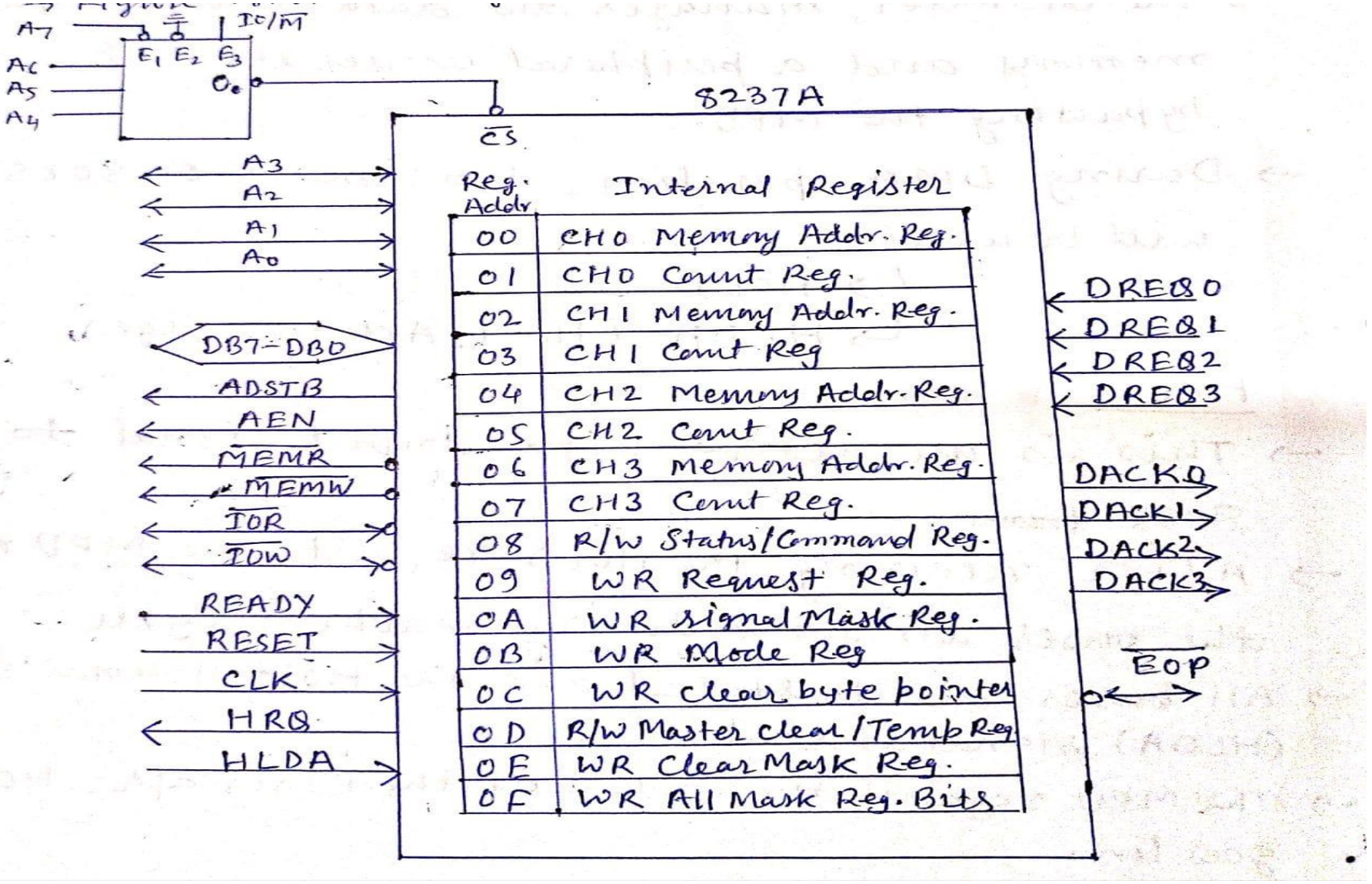
8237 DMA Controller

8237 DMA controller



8237 DMA Controller

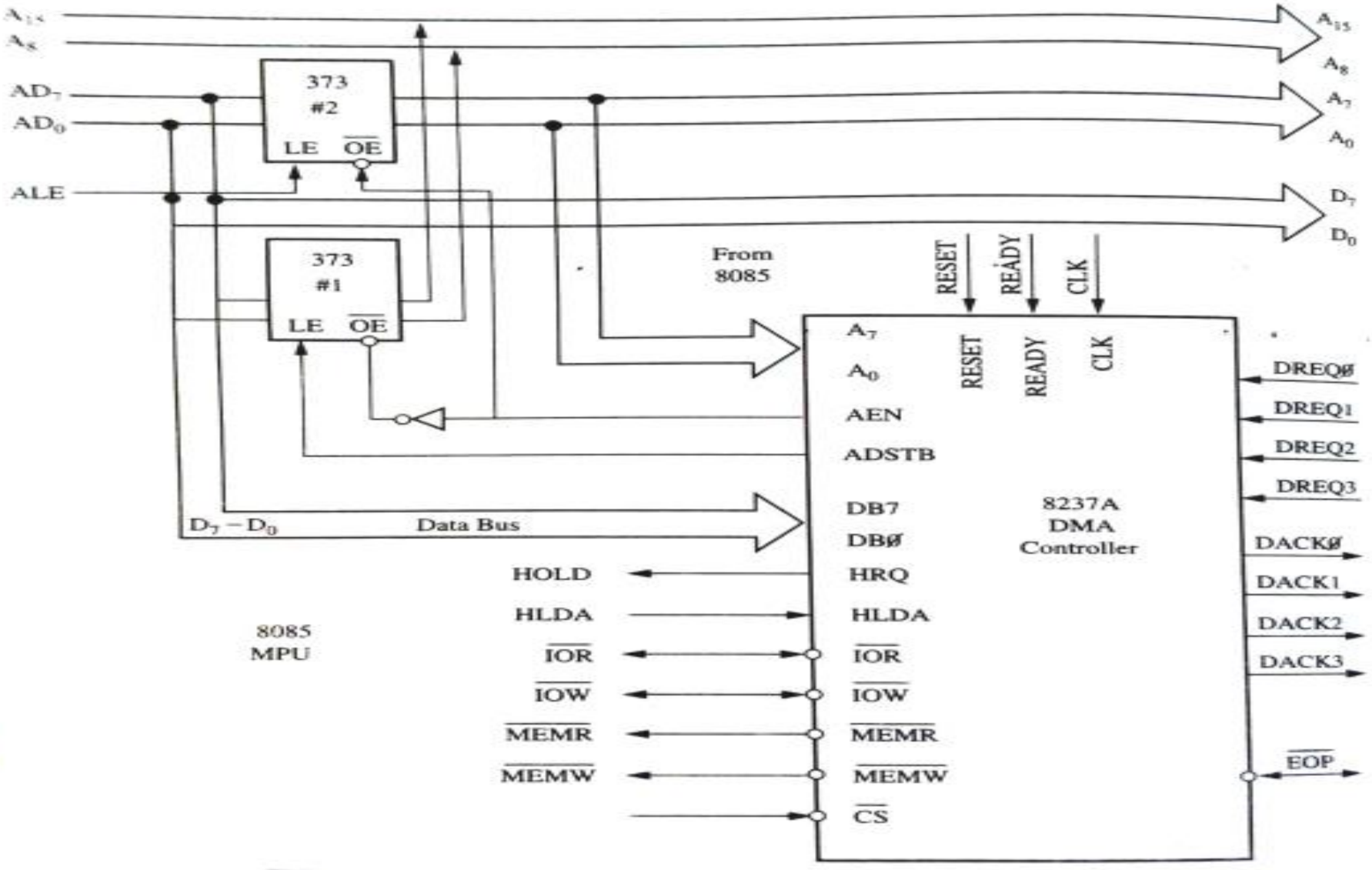
8237 DMA controller with internal registers



Reg. Addr	Internal Register
00	CH0 Memory Addr. Reg.
01	CH0 Count Reg.
02	CH1 Memory Addr. Reg.
03	CH1 Count Reg
04	CH2 Memory Addr. Reg.
05	CH2 Count Reg.
06	CH3 Memory Addr. Reg.
07	CH3 Count Reg.
08	R/W Status/Command Reg.
09	WR Request Reg.
0A	WR Signal Mask Reg.
0B	WR Mode Reg
0C	WR clear byte pointer
0D	R/W Master clear/Temp Reg
0E	WR Clear Mask Reg.
0F	WR All Mask Reg. Bits

8237 DMA Controller

Interfacing 8237A DMA controller with 8085



8237 DMA Controller

Description

It containing Five main Blocks.

- Data bus buffer
- Read/Control logic
- Control logic block
- Priority resolver
- DMA channels.

8237 DMA Controller

Description

DATA BUS BUFFER:

- It contains tristate ,8 bit bi-directional buffer. **Slave mode** ,it transfer data between microprocessor and internal data bus. **Master mode** ,the outputs A8-A15 bits of memory address on data lines (Unidirectional).

READ/CONTROL LOGIC:

- It control all internal Read/Write operation. **Slave mode**, it accepts address bits and control signal from microprocessor. **Master mode** ,it generate address bits and control signal.

8237 DMA Controller

Description

Control logic block:

- It contains ,
  - Control logic
  - Mode set register and
  - Status Register.

CONTROL LOGIC:

- **Master mode**, It control the sequence of DMA operation during all DMA cycles.
- It generates address and control signals.
- It increments 16 bit address and decrement 14 bit counter registers.
- It activate a HRQ signal on DMA channel Request.
- **Slave mode,** it is disabled.

8237 DMA Controller

D0-D7:

- It is a bidirectional ,tri state ,Buffered ,Multiplexed data (D0-D7)and (A8-A15).
- In the slave mode it is a bidirectional (Data is moving).
- In the Master mode it is a unidirectional (Address is moving).

IOR:

- It is active low ,tristate ,buffered ,Bidirectional lines.
- In the slave mode it function as a input line. IOR signal is generated by microprocessor to read the contents 8237 registers.
- In the master mode it function as a output line. IOR signal is generated by 8237 during write cycle

8237 DMA Controller

IOW:

- It is active low ,tristate ,buffered ,Bidirectional control lines.
- In the slave mode it function as a input line.
- IOR signal is generated by microprocessor to write the contents 8237 registers.
- In the master mode it function as a output line.
- IOR signal is generated by 8237 during read cycle.

CLK:

- It is the input line ,connected with TTL clock generator.
- This signal is ignored in slave mode.

8237 DMA Controller

RESET:

- Used to clear mode set registers and status registers.

A0-A3:

- These are the tristate, buffer, bidirectional address lines.
- In slave mode ,these lines are used as address inputs lines and internally decoded to access the internal registers.
- In master mode, these lines are used as address outputs lines,A0-A3 bits of memory address on the lines.

CS:

- It is active low, Chip select input line.
- In the slave mode, it is used to select the chip.
- In the master mode, it is ignored.

8237 DMA Controller

A4-A7:

- These are the tristate, buffer, output address lines.
- **In slave mode** ,these lines are used as address input lines.
- **In master mode**, these lines are used as address outputs lines,A0-A3 bits of memory address on the lines.

READY:

- It is a asynchronous input line.
- In master mode, When ready is high it receives the signal.
- When ready is low, it adds wait state between S1 and S3
- In slave mode, this signal is ignored.

HRQ:

- It is used to receiving the hold request signal from the output device.

8237 DMA Controller

HLDA:

- It is acknowledgment signal from microprocessor.

MEMR:

- It is active low ,tristate ,Buffered control output line.
- In slave mode, it is tristated.
- In master mode ,it activated during DMA read cycle.

MEMW:

- It is active low ,tristate ,Buffered control input line.
- In slave mode, it is tristated.
- In master mode ,it activated during DMA write cycle.

8237 DMA Controller

AEN (Address enable):

- It is a control output line.
- In master mode ,it is high
- In slave mode ,it is low
- Used it isolate the system address ,data ,and control lines.

ADSTB: (Address Strobe)

- It is a control output line.
- Used to split data and address line.
- It is working in master mode only.
- In slave mode it is ignore.

8237 DMA Controller

TC (Terminal Count):

- It is a status of output line.
- It is **activated in master mode only.**
- It is high ,it selected the peripheral.
- It is low ,it free and looking for a new peripheral.

MARK:

- It is a **modulo 128 MARK output line**.
- It is activated in master mode only.
- It goes high ,**after transferring every 128 bytes of data block.**

8237 DMA Controller

DRQ0-DRQ3 (DMA Request):

- These are the asynchronous peripheral request input signal.
- **The request signals is generated by external peripheral device.**

DACK0-DACK3:

- These are the active low DMA acknowledge output lines.
- Low level indicate that, peripheral is selected for giving the information (DMA cycle).
- In **master mode it is used for chip select.**

Quiz

- The block of 8237 that decodes the various commands given to the 8237 by the CPU is

a) timing and control block

b) program command control block

c) priority block

d) none of the mentioned

- The priority between the DMA channels requesting the services can be resolved by

a) timing and control block

b) program command control block

c) priority block

d) none of the mentioned

Quiz

- In direct memory access mode, the data transfer takes place

A. Directly

B. Indirectly

C. Both

D. None of these

- The register that holds the data byte transfers to be carried out is

a) current word register

b) current address register

c) base address register

d) command register

Quiz

- In 8257 (DMA), each of the four channels has

a) a pair of two 8-bit registers

b) a pair of two 16-bit registers

c) one 16-bit register

d) one 8-bit register

- The common register(s) for all the four channels of 8257 is

a) DMA address register

b) Terminal count register

c) Mode set register and status register

d) None of the mentioned

Recap

- Basics of DMA controller
- The technique of priority resolver
- The concept of DMA interfacing

Assignment

1. Illustrate any five important features of DMA controller.
2. What do you mean by Master and Slave mode ?
3. Discuss the modes of DMA operation.
4. What is the use of HOLD and HLDA in DMA data transfer?
5. Explain about Read/Write logic of DMA controller.

YouTube & NPTEL Video Links

YouTube/other Video Links

- https://www.youtube.com/watch?v=CSkN0wj0zZU

Prerequisite

- Understanding of 8086 Pin Description
- Knowledge of features of 8086 Microprocessor
- Basic function of gates

Topic Objective and its Mapping with CO

Name of Topic	Objective of Topic	Mapping with CO
Communication Protocols	Students will be able to outline the Communication Protocol such as USART and RS232C	CO5

8251 USART and RS232C

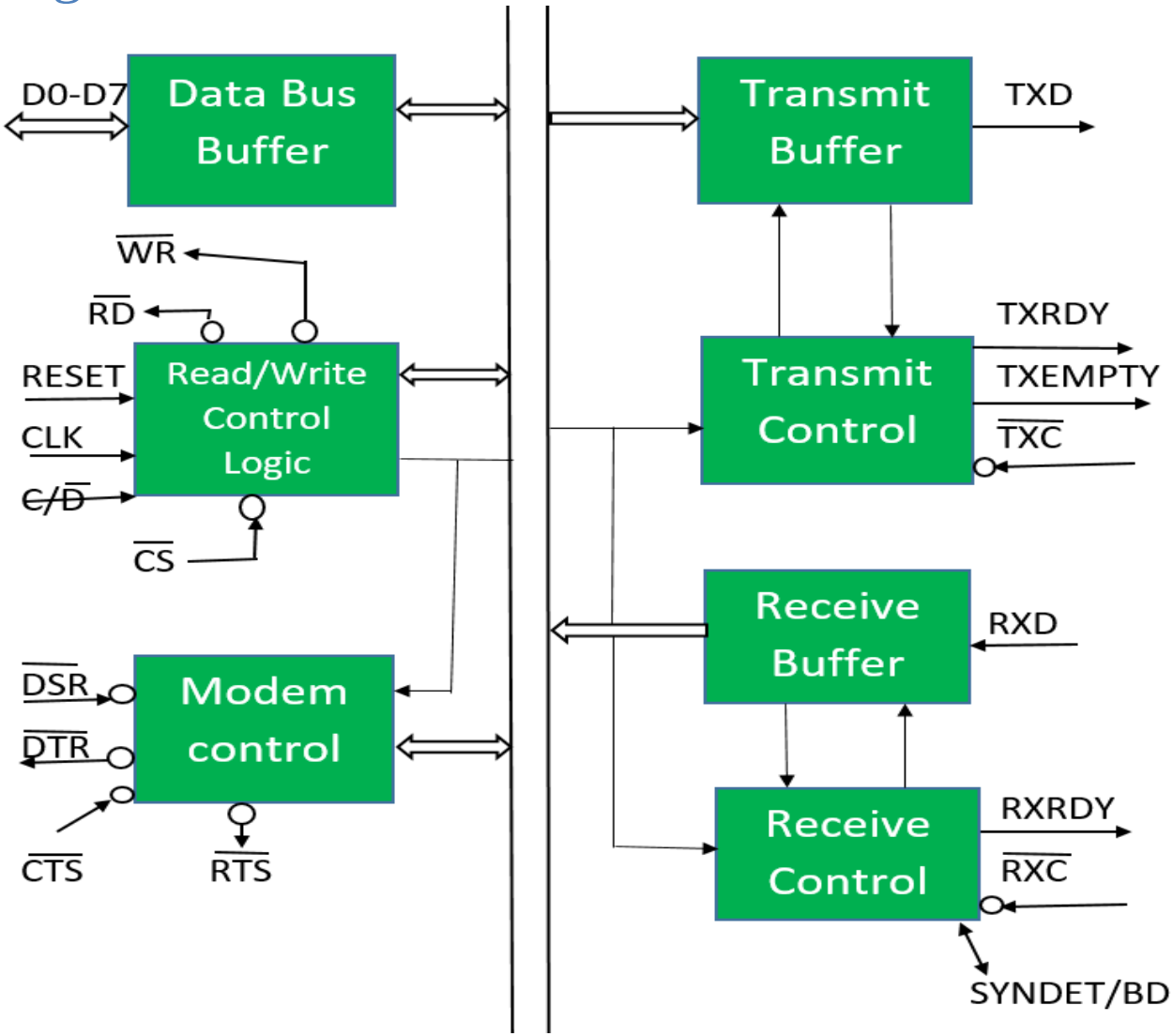
8251 USART

- 8251 universal synchronous asynchronous receiver transmitter (USART) acts as a mediator between microprocessor and peripheral to transmit serial data into parallel form and vice versa.

1. It takes data serially from peripheral (outside devices) and converts into parallel data.
2. After converting the data into parallel form, it transmits it to the CPU.
3. Similarly, it receives parallel data from microprocessor and converts it into serial form.
4. After converting data into serial form, it transmits it to outside device (peripheral).

8251 USART and RS232C

Block Diagram of 8251 USART



8251 USART and RS232C

Block Diagram of 8251 USART

Data bus buffer –

- This block helps in interfacing the internal data bus of 8251 to the system data bus.
- The data transmission is possible between 8251 and CPU by the data bus buffer block.

Read/Write control logic –

- It is a control block for overall device.
- It controls the overall working by selecting the operation to be done.
- In this way, this unit selects one of the three registers- data buffer register, control register, status register.
- The operation selection depends upon input signals as:

8251 USART and RS232C

Block Diagram of 8251 USART

Read/Write control logic –

$\overline{CS}$	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	Operation
1	X	X	X	Invalid
0	0	0	1	data CPU< ----- 8251
0	0	1	0	data CPU ----- > 8251
0	1	0	1	Status word CPU < ----------8251
0	1	1	0	Control word CPU---------- > 8251

8251 USART and RS232C

Block Diagram of 8251 USART

Modem control (modulator/demodulator) –

- A device converts analog signals to digital signals and vice-versa and helps the computers to communicate over telephone lines or cable wires.
- The following are active-low pins of Modem.

DSR: Data Set Ready signal is an input signal.

DTR: Data terminal Ready is an output signal.

CTS: It is an input signal which controls the data transmit circuit.

RTS: It is an output signal which is used to set the status RTS.

Transmit buffer –

- This block is used for parallel to serial converter that receives a parallel byte for conversion into serial signal and further transmission onto the common channel.

TXD: It is an output signal, if its value is one, means transmitter will transmit the data.

8251 USART and RS232C

Block Diagram of 8251 USART

Transmit control –

- This block is used to control the data transmission with the help of following pins:
  - **TXRDY:** It means transmitter is ready to transmit data character.
  - **TXEMPTY:** An output signal which indicates that TXEMPTY pin has transmitted all the data characters and transmitter is empty now.
  - **TXC:** An active-low input pin which controls the data transmission rate of transmitted data.

Receive buffer –

This block acts as a buffer for the received data.

RXD: An input signal which receives the data.

8251 USART and RS232C

Block Diagram of 8251 USART

Receive control –

This block controls the receiving data.

RXRDY: An input signal indicates that it is ready to receive the data.

RXC: An active-low input signal which controls the data transmission rate of received data.

SYNDET/BD: An input or output terminal. External synchronous mode-input terminal and asynchronous mode-output terminal.

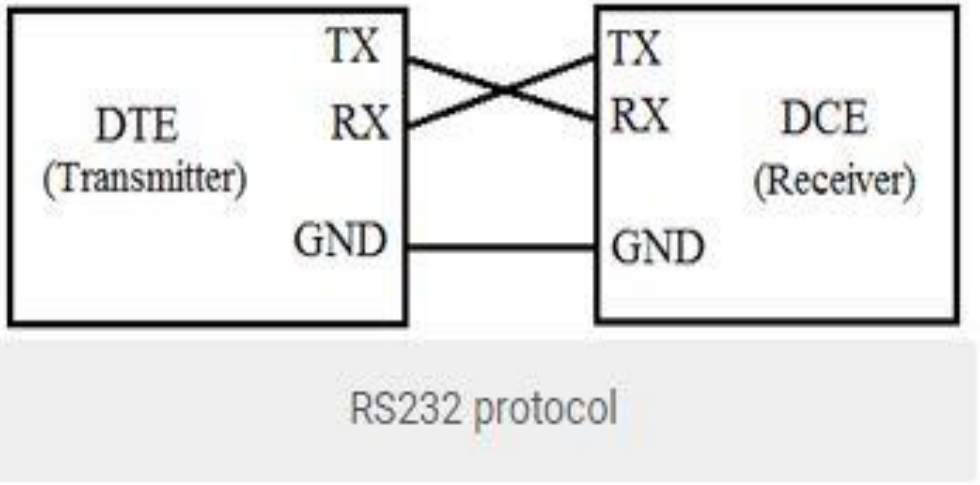
8251 USART and RS232C

RS232C

- **RS232C "Recommended Standard 232C"** is the recent version of Standard 25 pin whereas, **RS232D** which is of 22 pins.
- In new PC's male D-type which is of 9 pins.
- **RS232 is a standard protocol used for serial communication, it is used for connecting computer and its peripheral devices to allow serial data exchange between them.**
- As it obtains the voltage for the path used for the data exchange between the devices.
- It is used in serial communication up to 50 feet with the rate of 1.492kbps.
- As EIA defines, the RS232 is used for connecting Data Transmission Equipment (DTE) and Data Communication Equipment (DCE).

8251 USART and RS232C

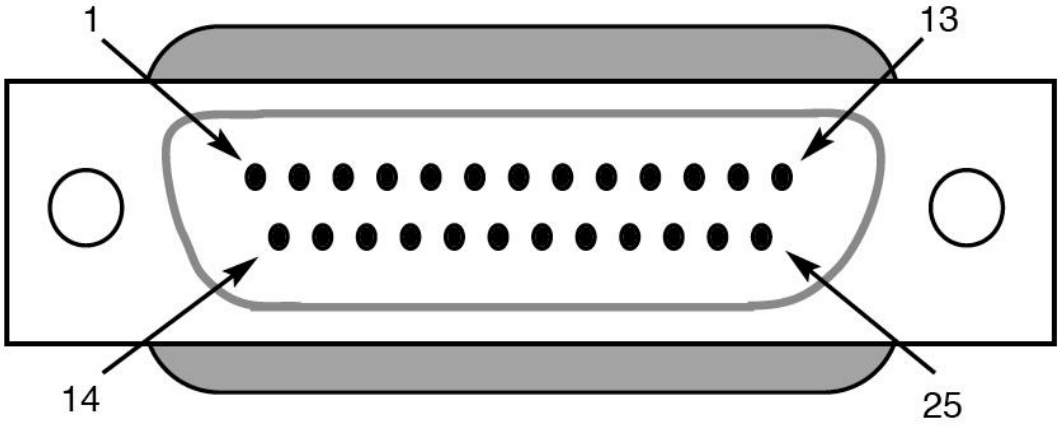
Data communication classification



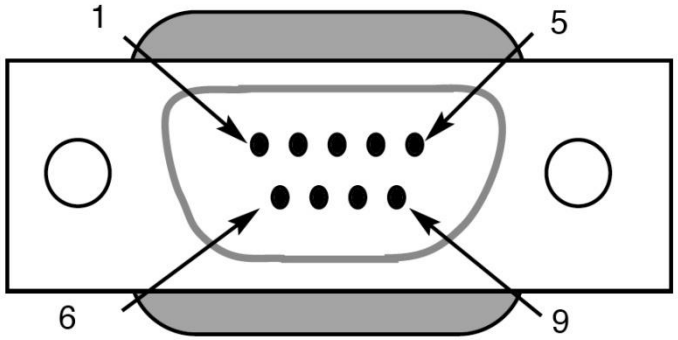
- DTE (data terminal equipment)
- DCE (data communication equipment)
- DTE - terminals and computers that send and receive data
- DCE - communication equipment responsible for transferring the data
  - simplest connection between a PC and microcontroller requires a minimum of three pins, TxD, RxD, and ground

8251 USART and RS232C

RS232 Connector DB-25



DB-9 9-Pin Connector



Quiz

- What is the protocol used by USART?

a) RS232
b) RS232C
c) RS485
d) RS422

- USART provides a synchronous mode that is not in UART?

a) True
b) False

- Which of the following needs a clock?

a) Only Asynchronous
b) Only synchronous
c) Both synchronous and Asynchronous
d) Sometimes Synchronous

Quiz

- Which of the following is not a mode of data transmission?
  a) simplex
  b) duplex
  c) semi duplex
  d) half duplex

- In 8251A, the pin that controls the rate at which the character is to be transmitted is

a) TXC(active low)
b) TXC(active high)
c) TXD(active low)
d) RXC(active low)

Quiz

- TXD(Transmitted Data Output) pin carries serial stream of the transmitted data bits along with

a) start bit
b) stop bit
c) parity bit
d) all of the mentioned

- The disadvantage of RS-232C is

a) limited speed of communication
b) high-voltage level signaling
c) big-size communication adapters
d) all of the mentioned

Quiz

- Which of the following can be used for long distance communication?

a) RS 232
b) SPI
c) I2C
d) Parallel Port

- Which lines are utilized during the enable state of hardware flow control in DTE and DCE devices of RS232 ?

a) a. CD & IR
b) b. DSR & DTR
c) c. RTS & CTS
d) d. None of the above

Quiz

- The USB supports the signaling rate of

a) full-speed USB 1.0 at rate of 12 Mbps

b) high-speed USB 2.0 at rate of 480 Mbps

c) super-speed USB 3.0 at rate of 596 Mbps

d) all of the mentioned

- The bit packet that commands the device either to receive data or transmit data in transmission of USB asynchronous communication is

a) Handshake packet

b) Token packet

c) PRE packet

d) Data packet

Recap

- USART features
- Working of USART
- Features of RS232 Protocol
- RS232 Operation

YouTube & NPTEL Video Links

YouTube/other Video Links

- https://nptel.ac.in/courses/108/103/108103157/
- https://onlinecourses.nptel.ac.in/noc20_ee11/preview
- https://www.youtube.com/watch?v=3RfqkVyvnnc
- https://www.youtube.com/watch?v=CSkN0wj0zZU

Topic Objective and its Mapping with CO

Name of Topic	Objective of Topic	Mapping with CO
Features and Pin Description of Intel 8086 Microprocessor	Students will be able to outline the features and pin description of Intel 8086 Microprocessor	CO5

Architecture of 8086

Features of 8086

- It is a 16-bit μp.
- 8086 has a 20 bit address bus can access up to 2^20 memory locations (1 MB).
- It can support up to 64K I/O ports.
- It provides 14, 16 -bit registers.
- Word size is 16 bits and double word size is 4 bytes.
- It has multiplexed address and data bus AD0- AD15 and A16 – A19.
- 8086 is designed to operate in two modes, Minimum and Maximum.
- It can prefetches up to 6 instruction bytes from memory and queues them in order to speed up instruction execution

Architecture of 8086

Features of 8086

- It requires +5V power supply.
- A 40 pin dual in line package.
- Address ranges from 00000H to FFFFFH

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Architecture of 8086

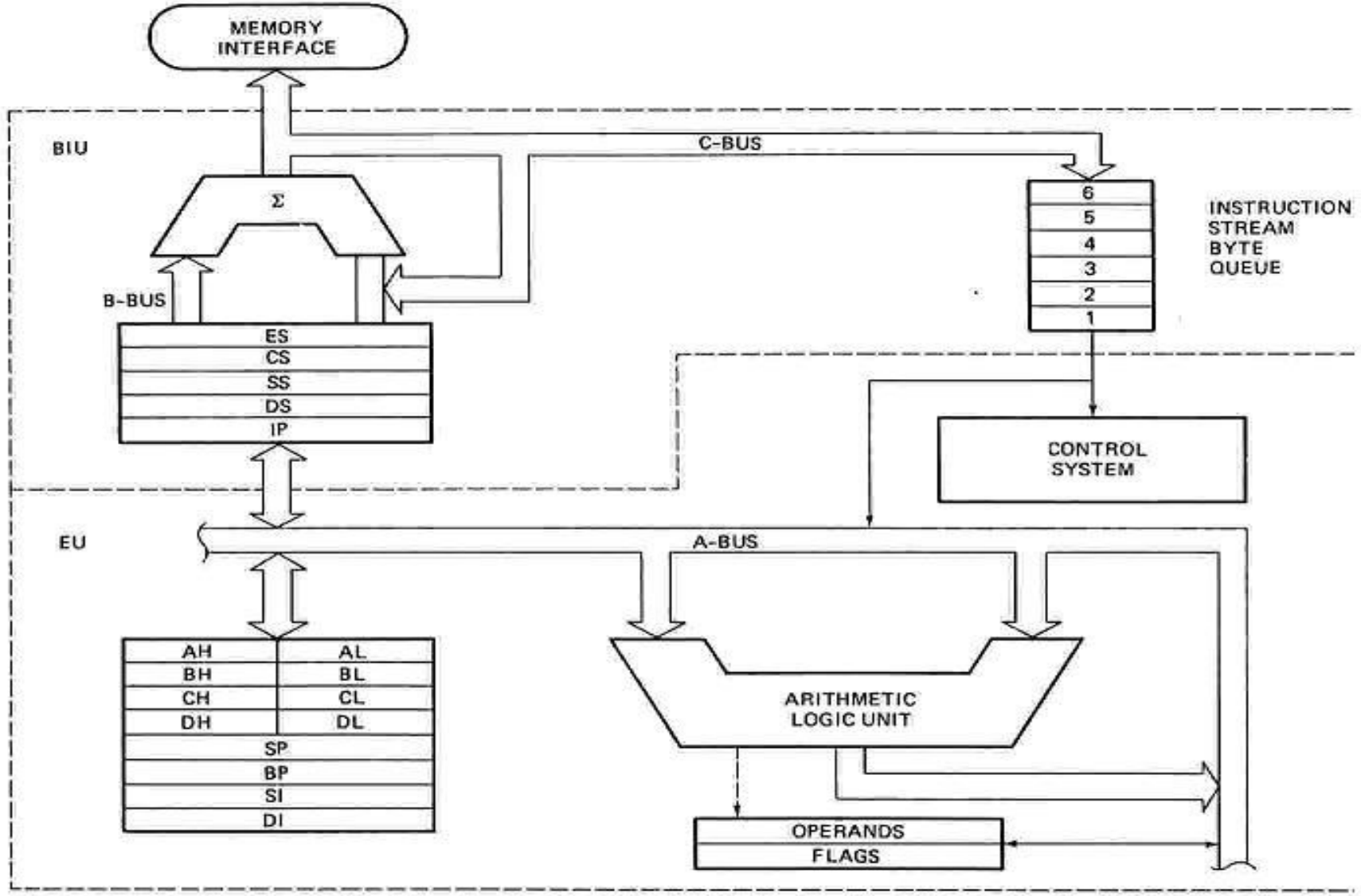


FIGURE 8086 internal block diagram. (*Intel Corp.*)

Architecture of 8086

Functional Block Description

- 8086 has two blocks BIU and EU.
- The BIU handles all transactions of data and addresses on the buses for EU.
- The BIU performs all bus operations such as instruction fetching, reading and writing operands for memory and calculating the addresses of the memory operands. The instruction bytes are transferred to the instruction queue.
- EU executes instructions from the instruction system byte queue.

Architecture of 8086

Functional Block Description

- BIU contains Instruction queue, Segment registers, Instruction pointer, Address adder.

- EU contains Control circuitry, Instruction decoder, ALU, Pointer and Index register, Flag register.

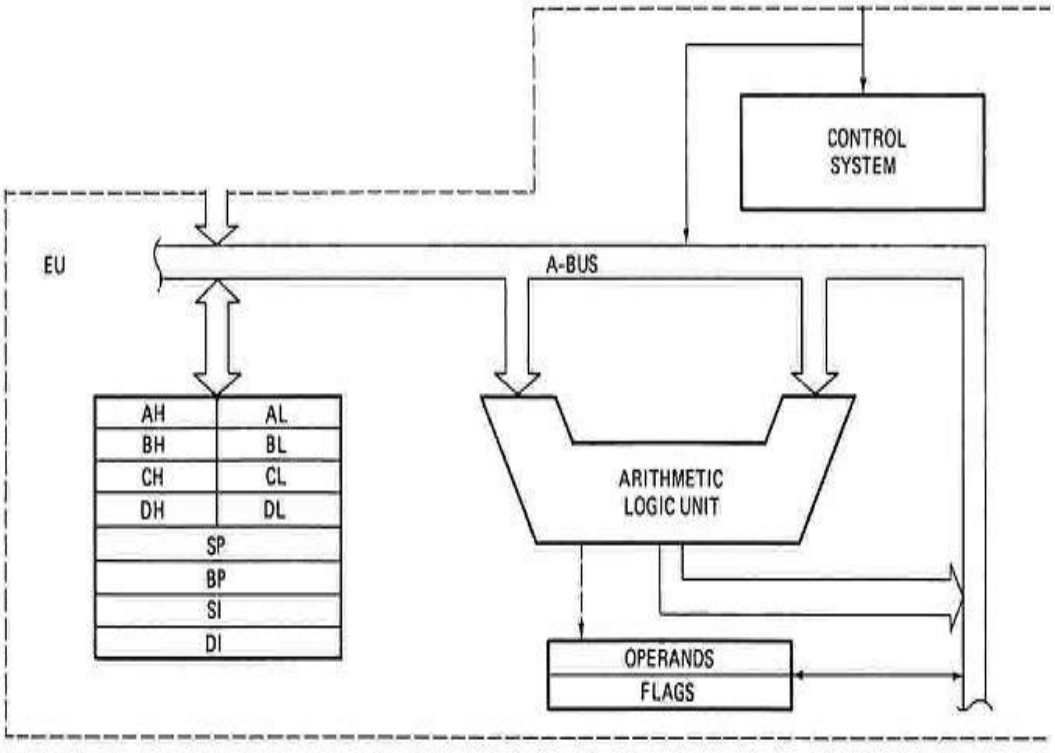
Architecture of 8086

EXECUTION UNIT

- Decodes instructions fetched by the BIU
- Generate control signals,
- Executes instructions.

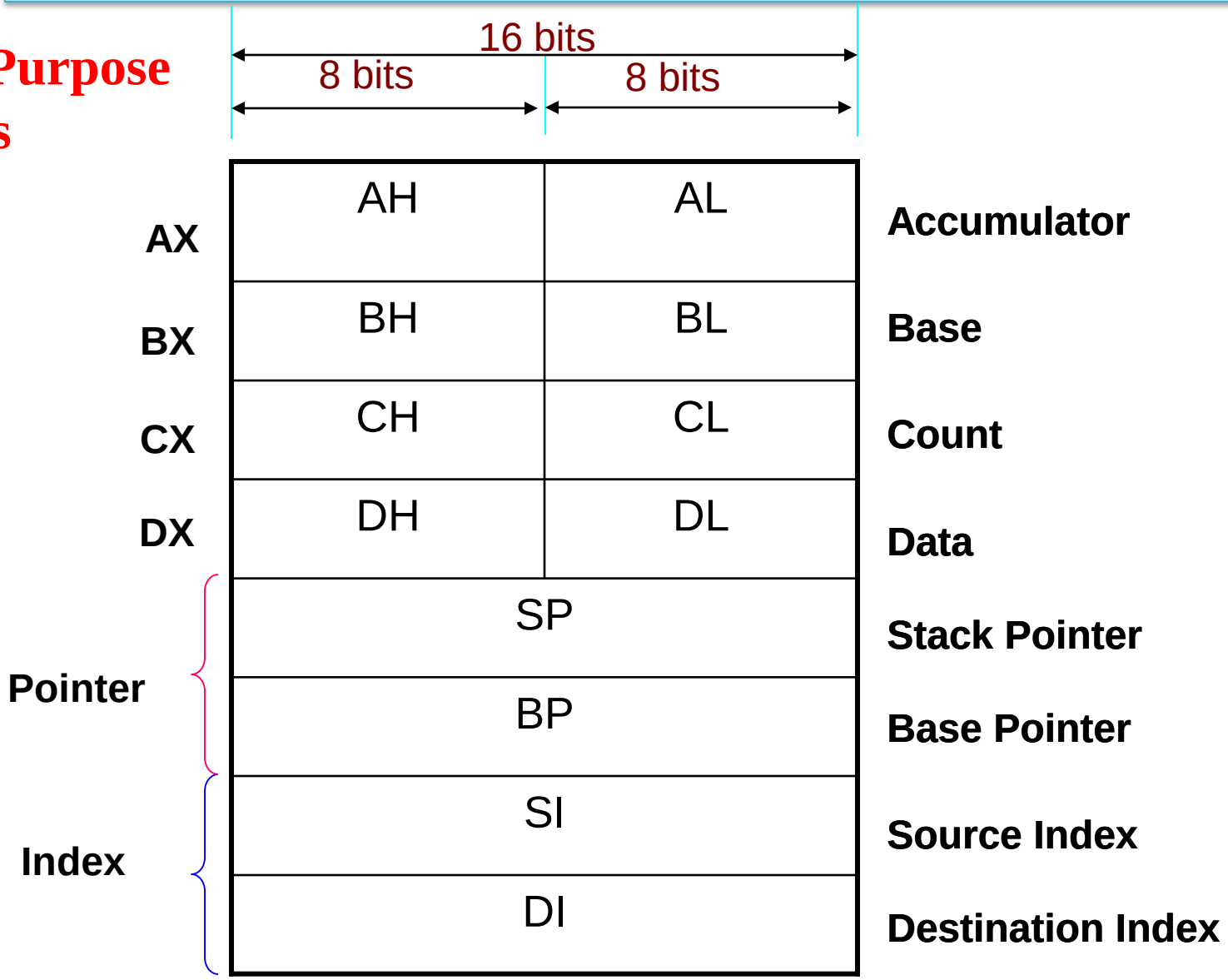
The main parts are:

- Control Circuitry
- Instruction decoder
- ALU



Architecture of 8086

General Purpose Registers



Architecture of 8086

Register	Purpose
AX	Word multiply, word divide, word I /O
AL	Byte multiply, byte divide, byte I/O, decimal arithmetic
AH	Byte multiply, byte divide
BX	Store address information
CX	String operation, loops
CL	Variable shift and rotate
DX	Word multiply, word divide, indirect I/O (Used to hold I/O address during I/O instructions. If the result is more than 16-bits, the lower order 16-bits are stored in accumulator and higher order 16-bits are stored in DX register)

Architecture of 8086

Pointer And Index Registers

- Used to keep offset addresses.
- Used in various forms of memory addressing.
- In the case of SP and BP the default reference to form a physical address is the Stack Segment (SS-will be discussed under the BIU)
- The index registers (SI & DI) and the BX generally default to the Data segment register (DS).
- SP: Stack pointer
  - Used with SS to access the stack segment
- BP: Base Pointer
  - Primarily used to access data on the stack
  - Can be used to access data in other segments

Architecture of 8086

Pointer And Index Registers

- SI: Source Index register

  – is required for some string operations

  – When string operations are performed, the SI register points to memory locations in the data segment which is addressed by the DS register. Thus, SI is associated with the DS in string operations.

- DI: Destination Index register

  – is also required for some string operations.

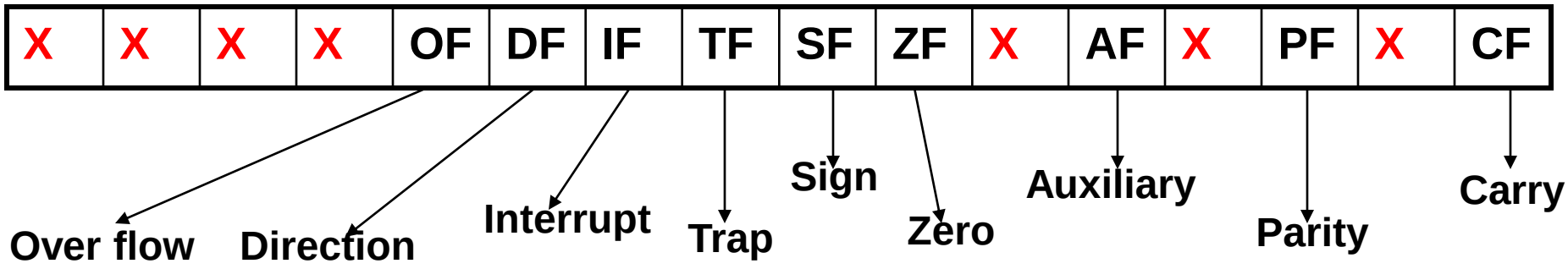
  – When string operations are performed, the DI register points to memory locations in the data segment which is addressed by the ES register. Thus, DI is associated with the ES in string operations.

- The SI and the DI registers may also be used to access data stored in arrays

Architecture of 8086

EXECUTION UNIT – Flag Register

- A flag is a flip flop which indicates some conditions produced by the execution of an instruction or controls certain operations of the EU .
- In 8086 The EU contains
  - a 16 bit flag register
  - 9 of the 16 are active flags and remaining 7 are undefined.
  - 6 flags indicates some conditions- status flags
  - 3 flags –control Flags



X - Unused

Architecture of 8086

EXECUTION UNIT – Flag Register

Flag	Purpose
Carry (CF)	Holds the carry after addition or the borrow after subtraction. Also indicates some error conditions, as dictated by some programs and procedures .
Parity (PF)	PF=0;odd parity, PF=1;even parity.
Auxiliary (AF)	Holds the carry (half – carry) after addition or borrow after subtraction between bit positions 3 and 4 of the result (for example, in BCD addition or subtraction.)
Zero (ZF)	Shows the result of the arithmetic or logic operation. Z=1; result is zero. Z=0; The result is 0
Sign (SF)	Holds the sign of the result after an arithmetic/logic instruction execution. S=1; negative, S=0

Architecture of 8086

EXECUTION UNIT – Flag Register

Flag	Purpose
Trap (TF)	A control flag. Enables the trapping through an on-chip debugging feature.
Interrupt (IF)	A control flag. Controls the operation of the INTR (interrupt request) I=0; INTR pin disabled. I=1; INTR pin enabled.
Direction (DF)	A control flag. It selects either the increment or decrement mode for DI and /or SI registers during the string instructions.
Overflow (OF)	Overflow occurs when signed numbers are added or subtracted. An overflow indicates the result has exceeded the capacity of the Machine

Architecture of 8086

Example

If register AL = 7Fh and the instruction ADD AL,1 is executed then what is the status of flag?

AL = 80h

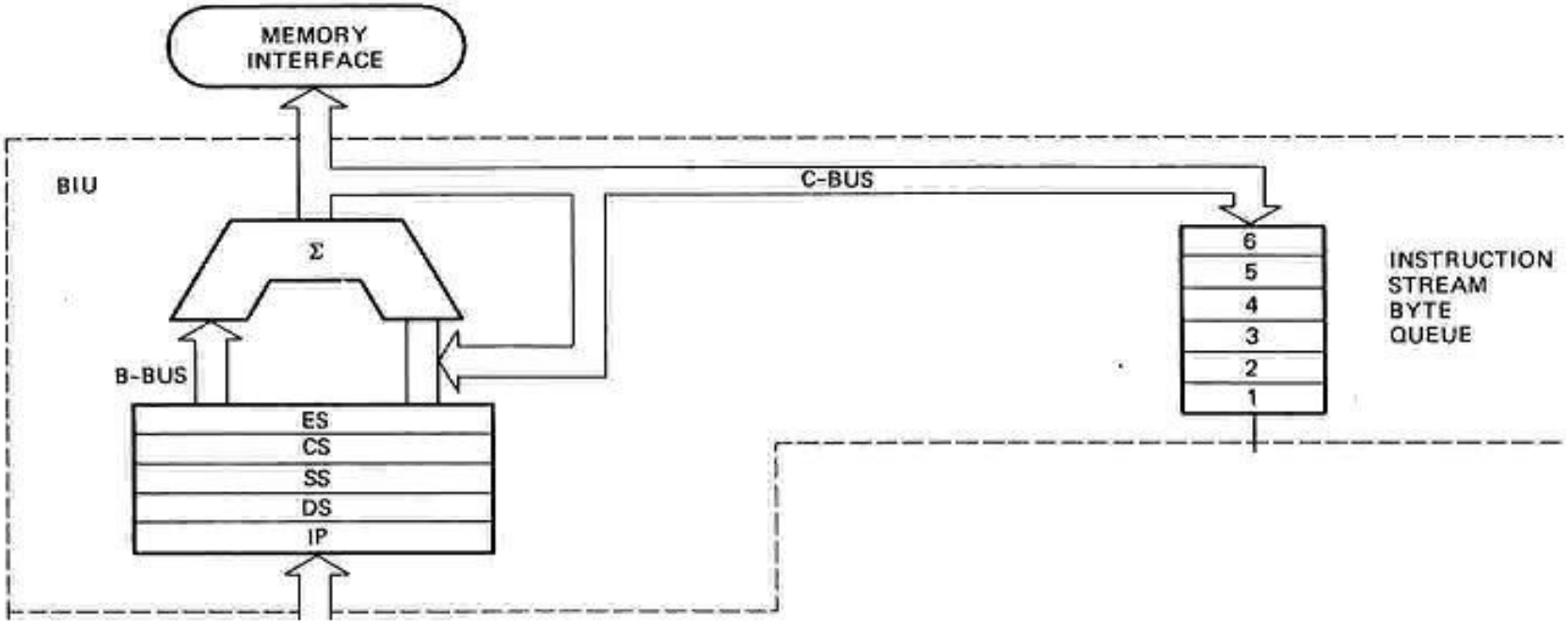
CF = 0; there is no carry out of bit 7
PF = 0; 80h has an odd number of ones
AF = 1; there is a carry out of bit 3 into bit 4
ZF = 0; the result is not zero
SF = 1; bit seven is one
OF = 1; the sign bit has changed

Architecture of 8086

BUS INTERFACE UNIT (BIU)

Contains:

- 6-byte Instruction Queue (Q)
- The Segment Registers (CS, DS, ES, SS).
- The Instruction Pointer (IP).
- The Address Summing block (Σ)



Architecture of 8086

THE QUEUE (Q)

- The BIU uses a mechanism known as an instruction stream queue to implement a pipeline architecture.

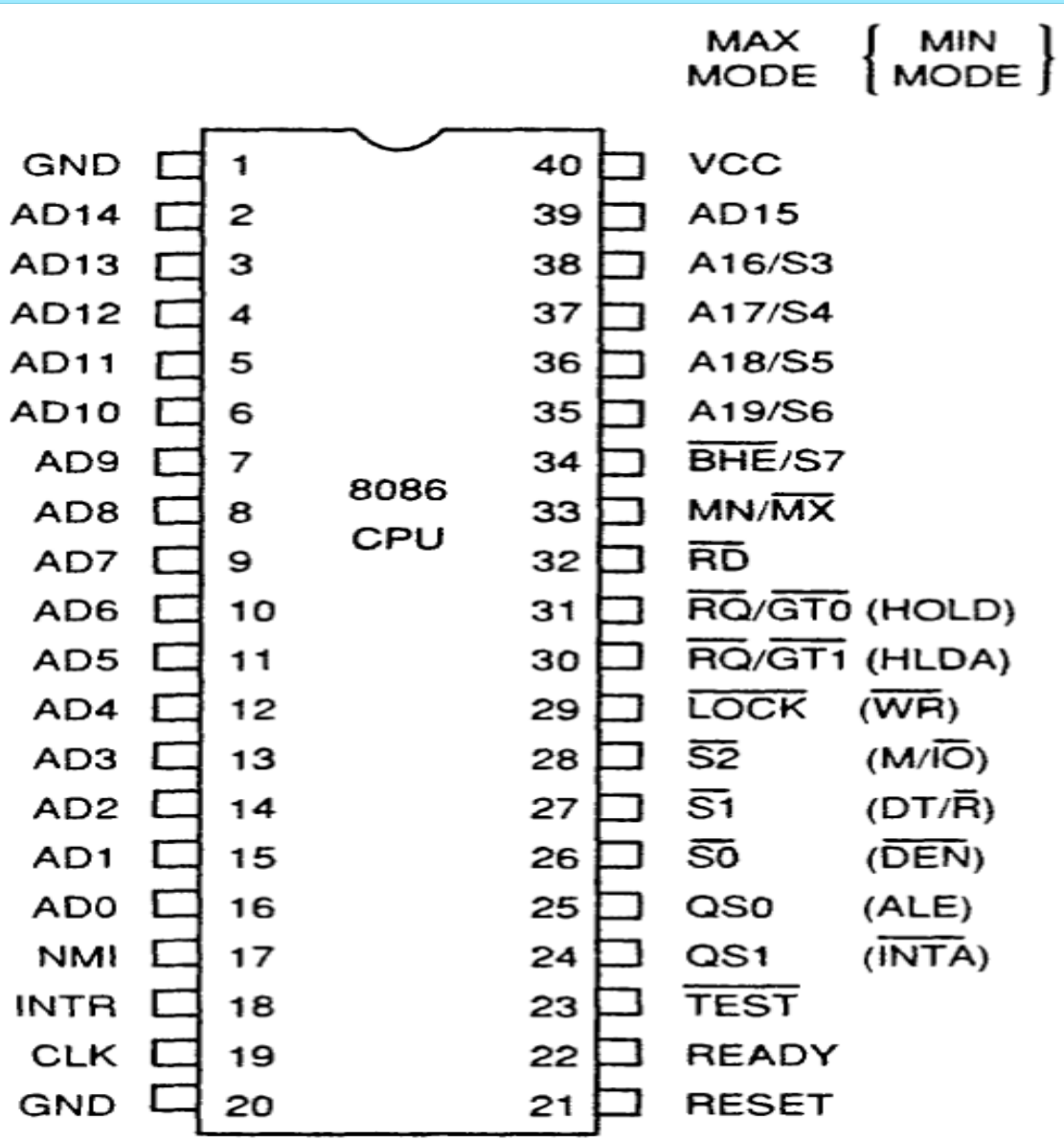
- This queue permits pre-fetch of up to 6 bytes of instruction code.
- Whenever the queue of the BIU is not full, it has room for at least two more bytes and at the same time the EU is not requesting it to read or write operands from memory, the BIU is free to look ahead in the program by pre-fetching the next sequential instruction.

Architecture of 8086

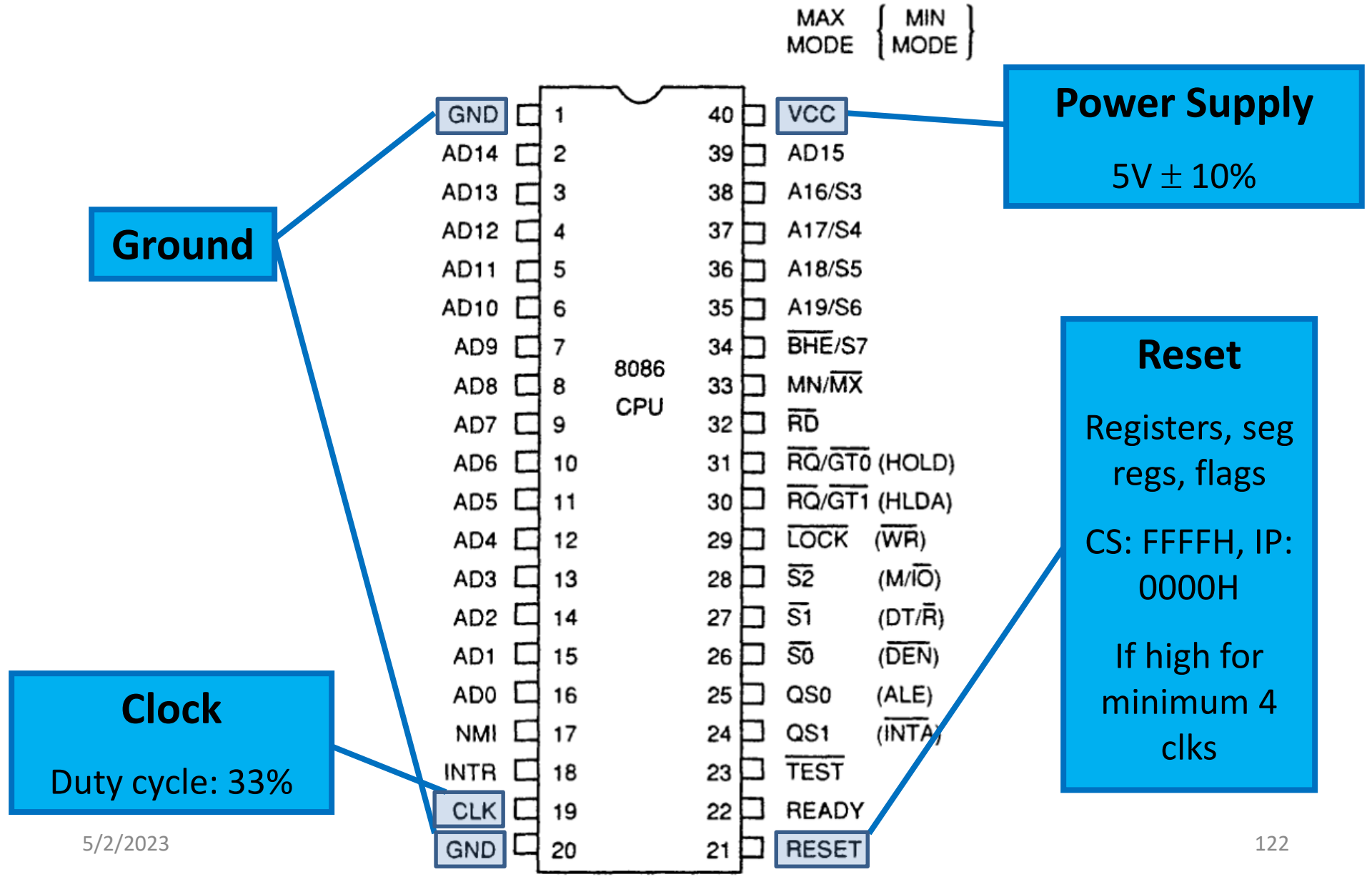
Instruction pointer

- IP - the instruction pointer:
    1. Always points to next instruction to be executed
    2. Offset address relative to CS
- IP register always works together with CS segment register and it points to currently executing instruction

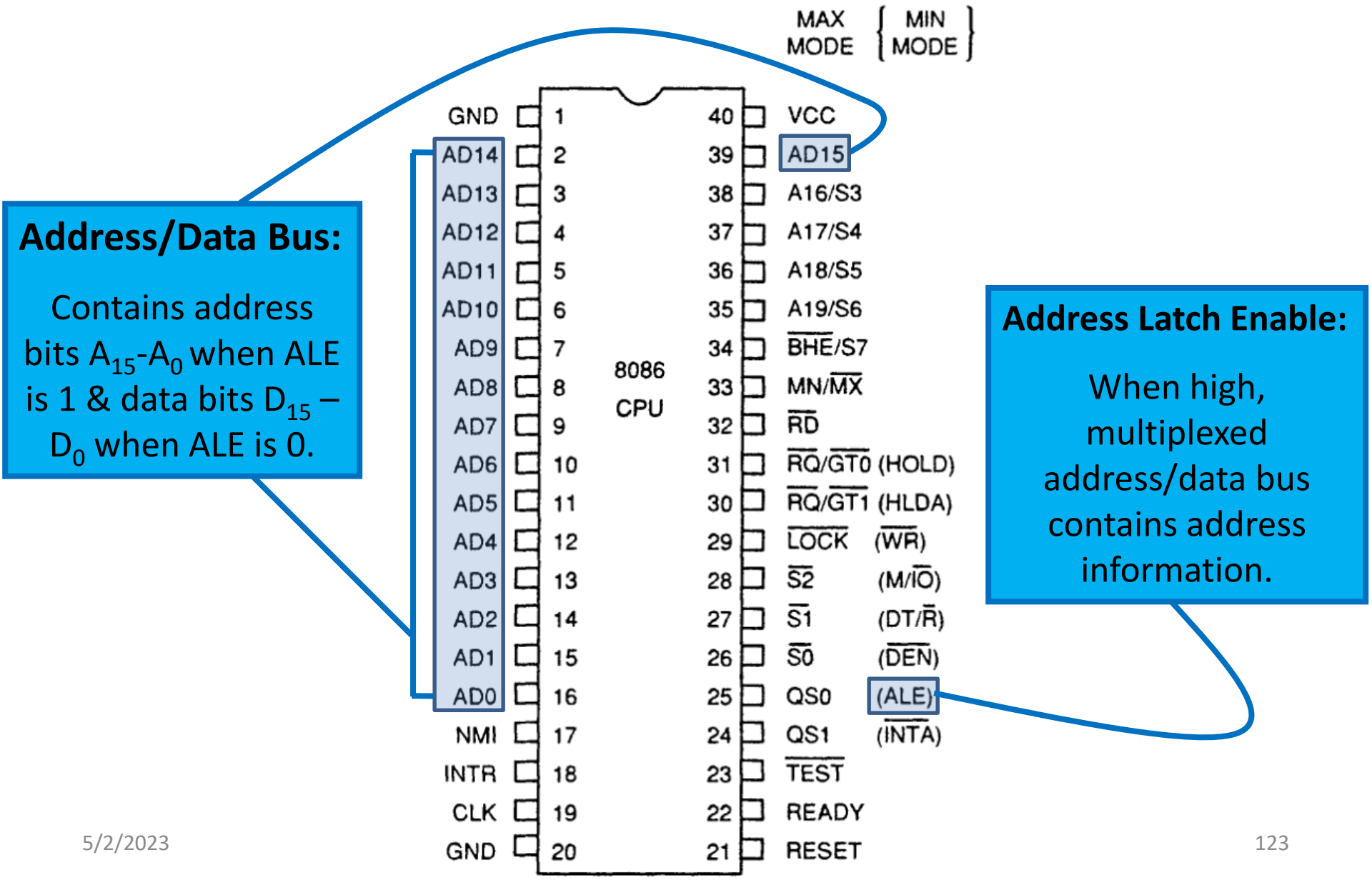
Pin Description of 8086



Pin Description of 8086



Pin Description of 8086



Address/Data Bus:

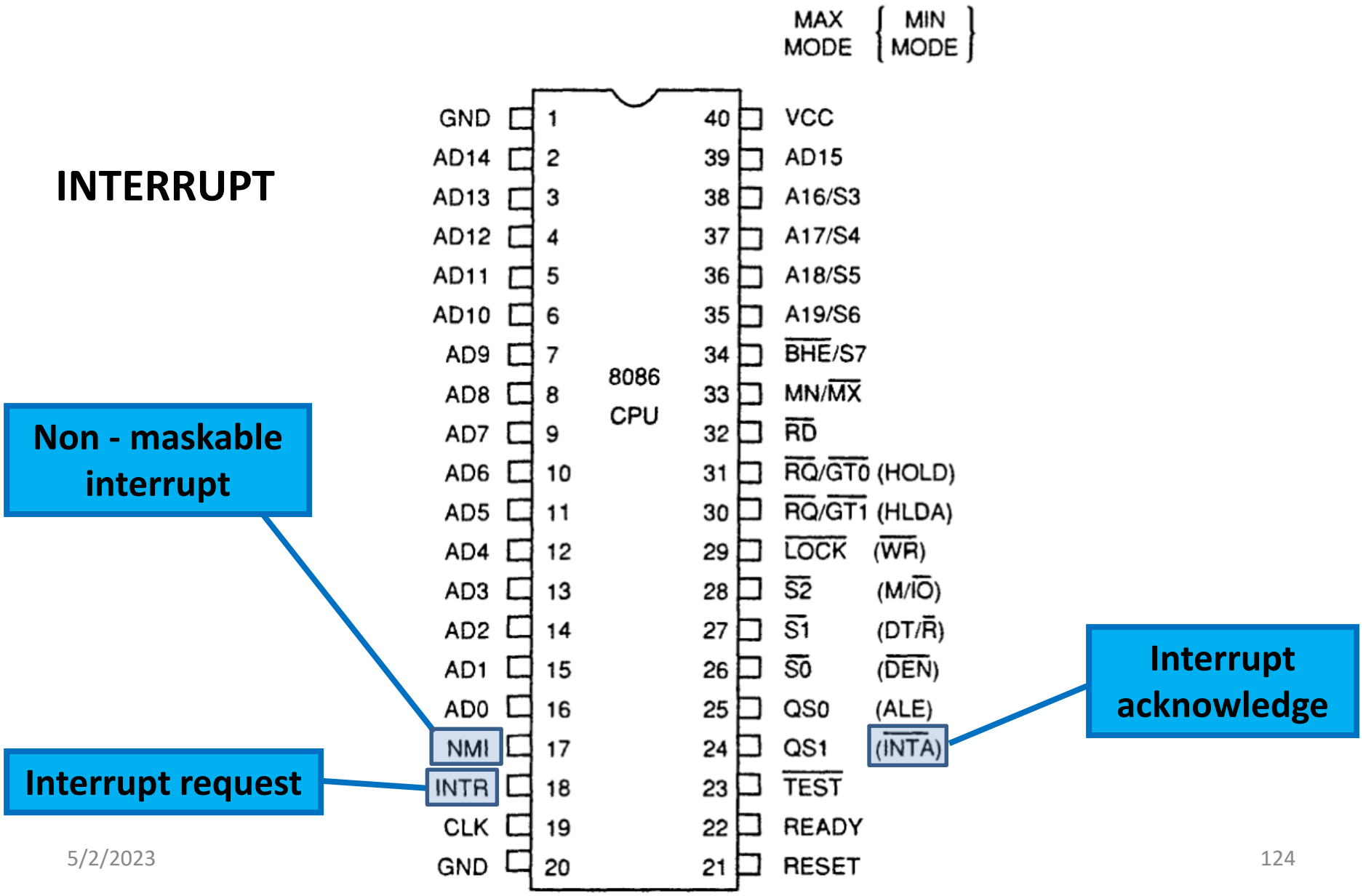
Contains address bits A_{15}-A_0 when ALE is 1 & data bits D_{15} – D_0 when ALE is 0.

Address Latch Enable:

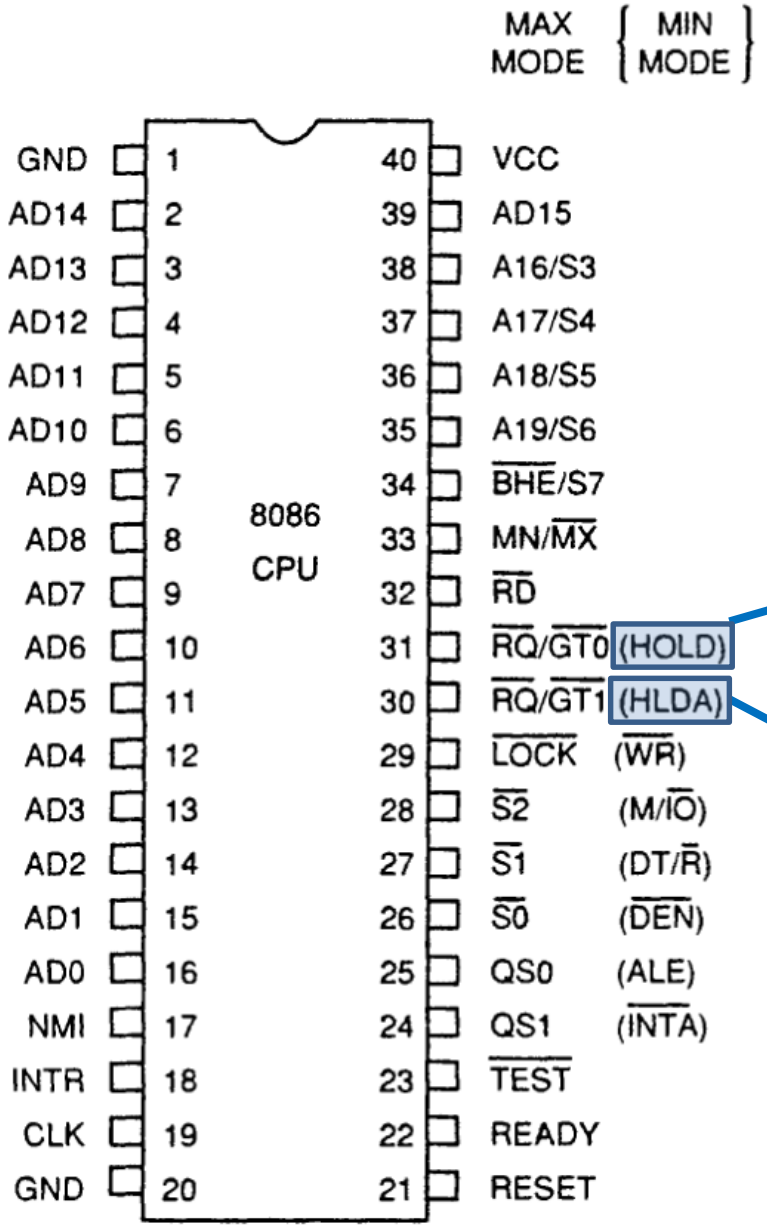
When high, multiplexed address/data bus contains address information.

Pin Description of 8086

INTERRUPT



Pin Description of 8086



Direct Memory Access

Hold

Hold acknowledge

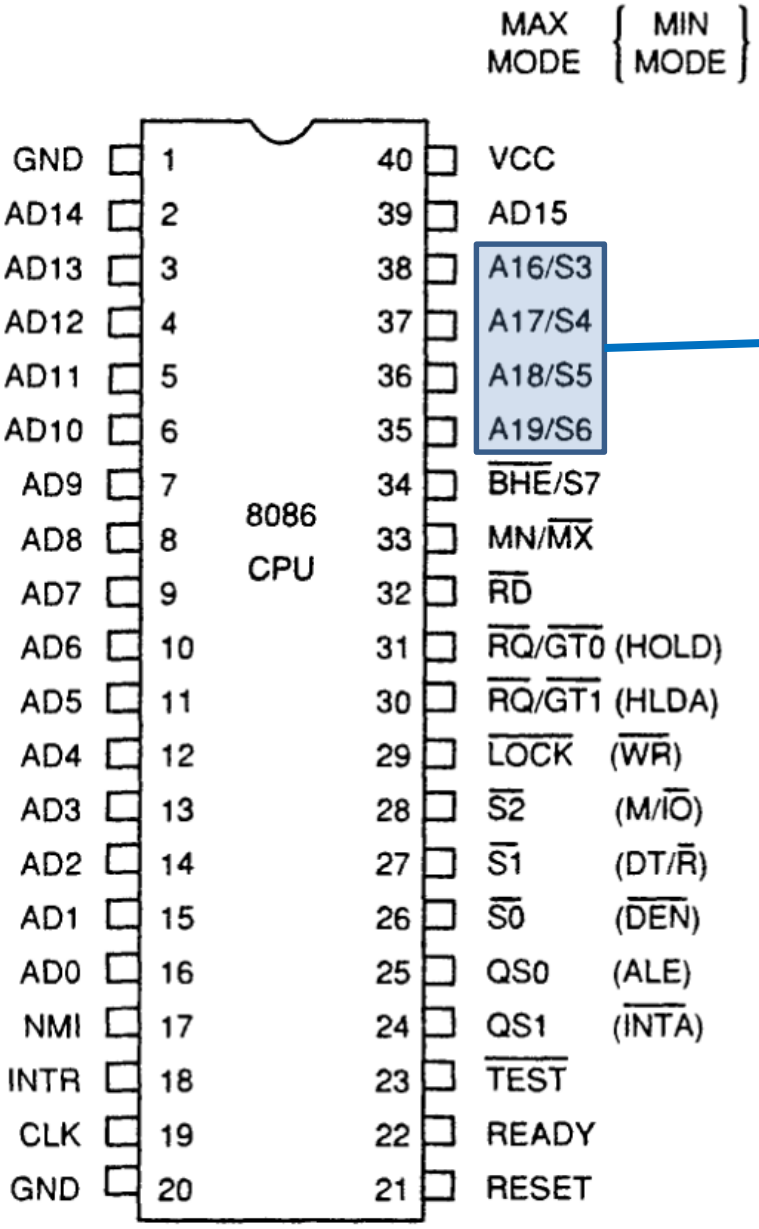
Pin Description of 8086

S6: Logic 0.

S5: Indicates condition of IF flag bits.

S4-S3: Indicate which segment is accessed during current bus cycle:

S4	S3	*Function*
0	0	Extra segment
0	1	Stack segment
1	0	Code or no segment
1	1	Data segment



Address/Status Bus

Address bits A_{19} – A_{16} & Status bits S_6 – S_3

Pin Description of 8086

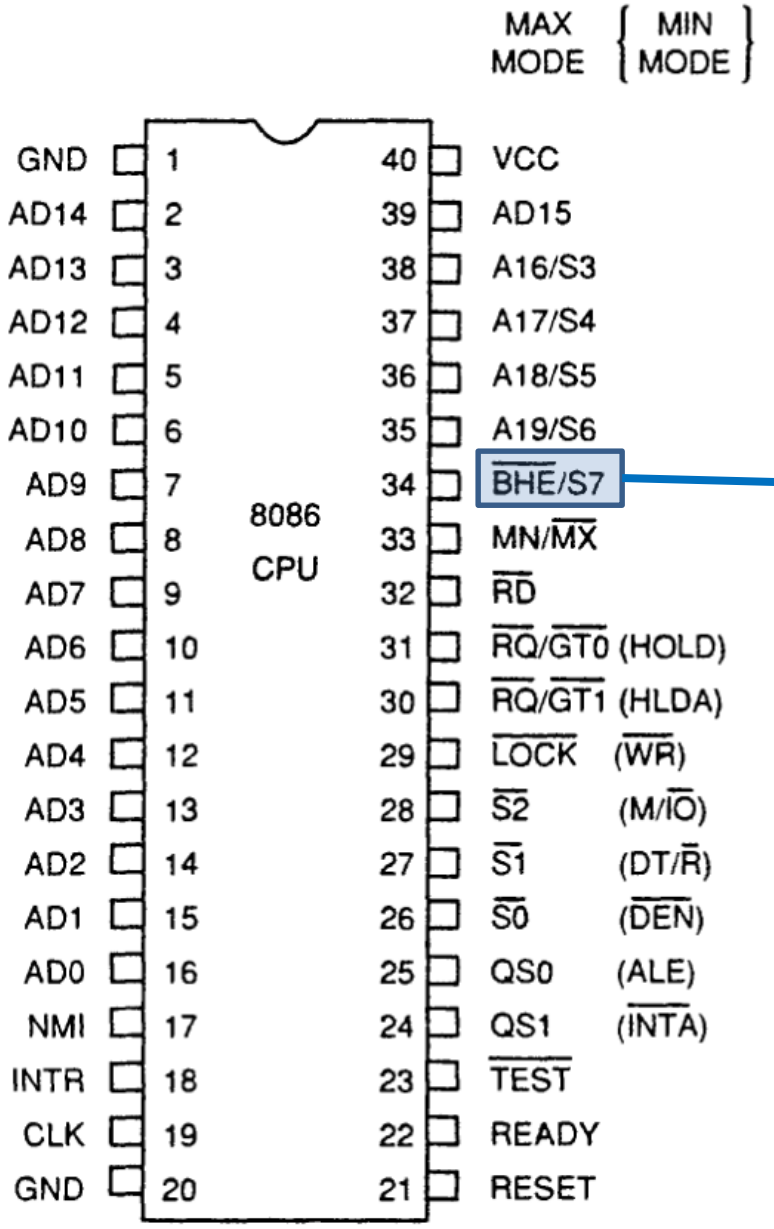
BHE#, A_0:

0,0: Whole word (16-bits)

0,1: High byte to/from odd address

1,0: Low byte to/from even address

1,1: No selection

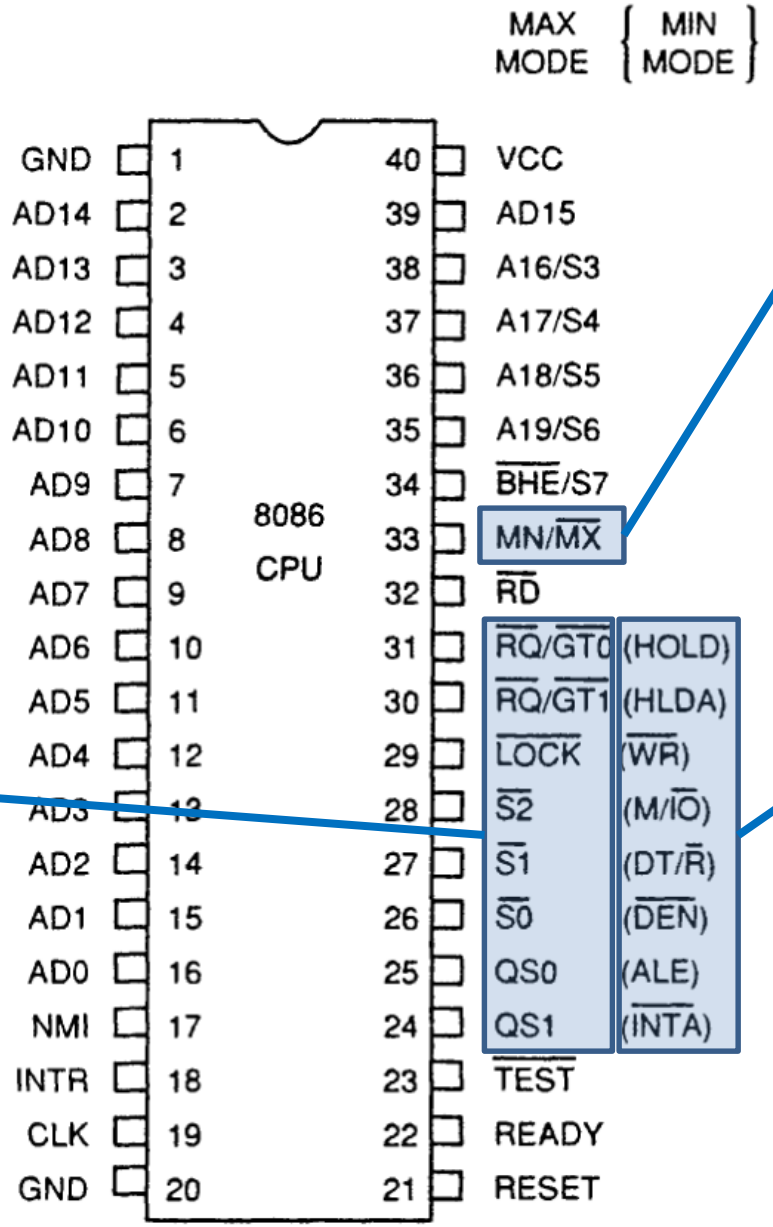


Bus High Enable/S7

Enables most significant data bits $D_{15} – D_8$ during read or write operation.

S_7: Always 1.

Pin Description of 8086



Min/Max mode

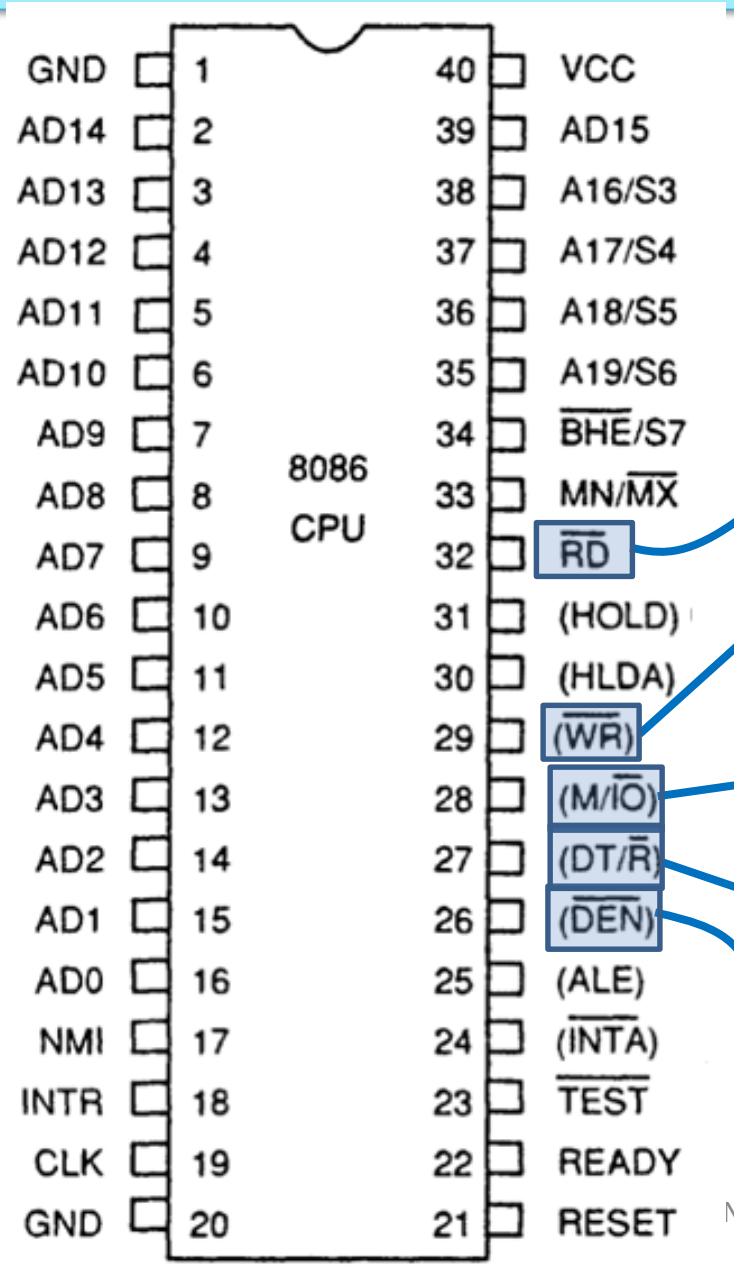
Minimum Mode: +5V

Maximum Mode: 0V

Minimum Mode Pins

Maximum Mode Pins

Pin Description of 8086



Read Signal

Write Signal

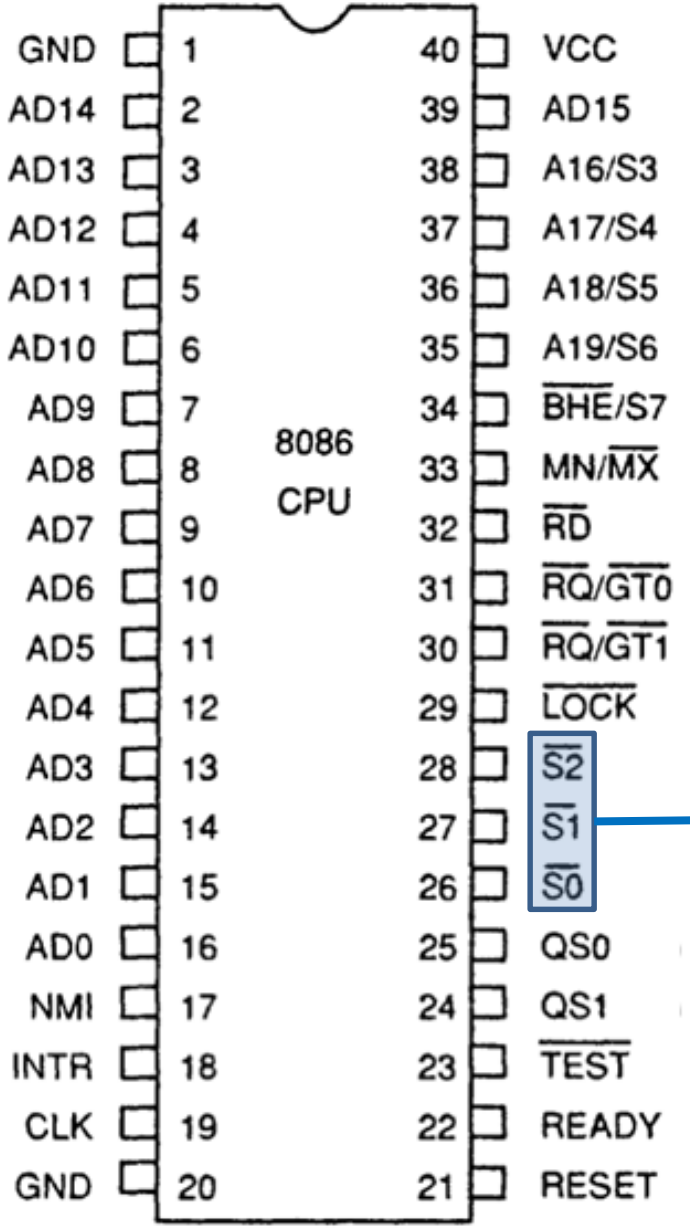
Memory or I/0

Data Transmit/Receive

Data Bus Enable

129

Pin Description of 8086



S2 S1 S0

000: INTA
001: read I/O port
010: write I/O port
011: halt
100: code access
101: read memory
110: write memory
111: passive state

Status Signal

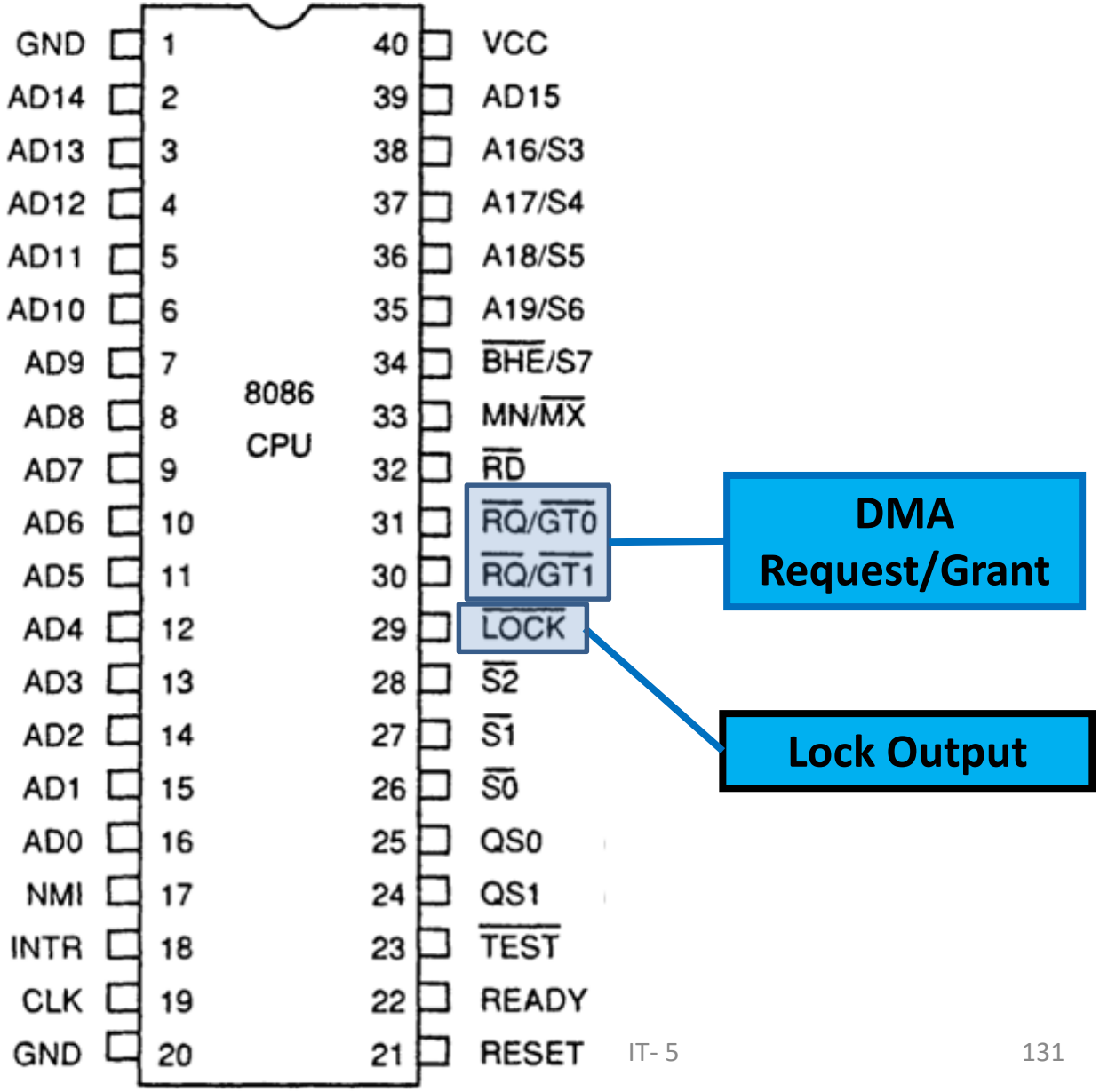
Inputs to 8288 to generate eliminated signals due to max mode.

Pin Description of 8086

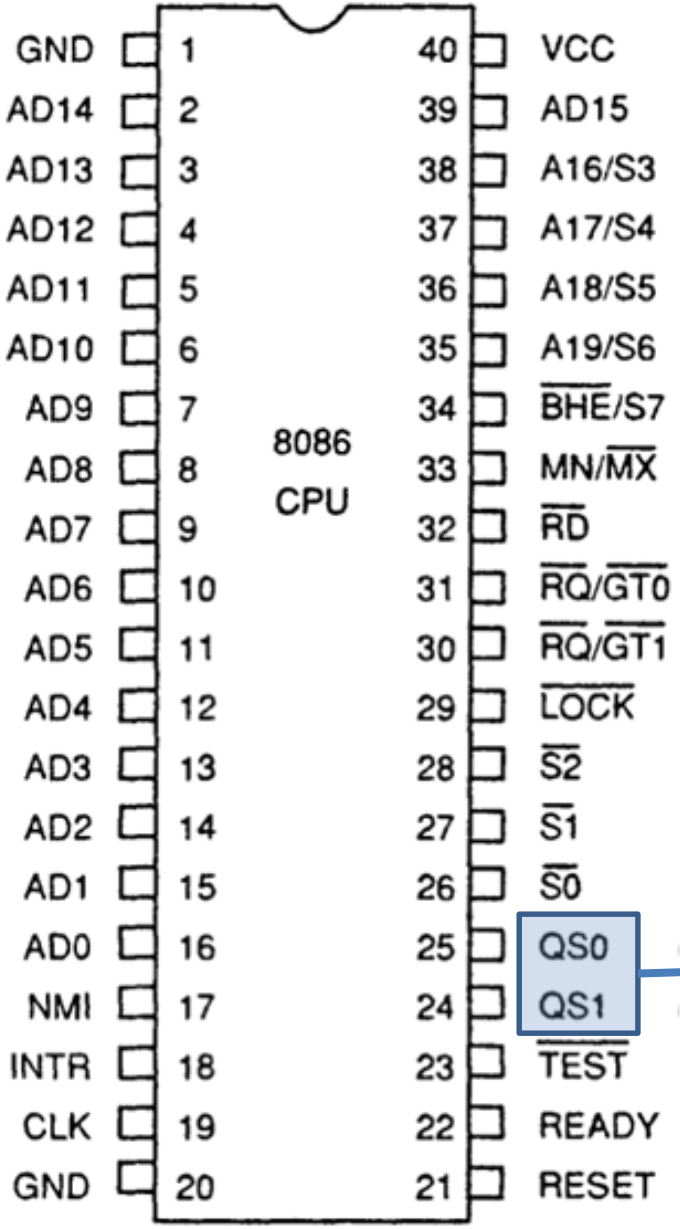
Lock Output

Used to lock peripherals off the system

Activated by using the LOCK: prefix on any instruction



Pin Description of 8086



QS1 QS0

00: Queue is idle

01: First byte of opcode

10: Queue is empty

11: Subsequent byte of opcode

Queue Status

Used by numeric coprocessor (8087)

Quiz

- In 8086 Microprocessor LOCK is a _____mode signal.
  A. Maximum
  B. Minimum
  C. Both
  D. None
- 8086 can access up to?
  A. 512KB
  B. 1Mb
  C. 2Mb
  D. 256KB
- 8086 has _____ address bus.
  A. 16-bit
  B. 18-bit
  C. 20-bit
  D. 24-bit

Quiz

- 8086 Microprocessor supports _____ modes of operation.

A. 2
B. 3
C. 4
D. 5

- Multiprocessor environment can work in _____

A. 16-bit
B. 18-bit
C. 20-bit
D. 24-bit

- ALE stand for _____

A. Address Level Enable
B. Address latch Enable
C. Add Latch Enable
D. None of these

Quiz

- 8086 Microprocessor is a _____bit processor.

A. 8

B. 4

C. 16

D. 32

- Multiprocessor environment can work in _____

A. Maximum mode

B. Minimum mode

C. Both

D. None

Assignment

1. Illustrate five features of Intel 8086 Microprocessor.
2. What are the functions of following pins:

- LOCK
- ALE
- RD’
- HOLD

3. Elaborate the statement that Intel 8086 is a 16 bit microprocessor.
4. What is the significance of clock pin?
5. Differentiate between Intel 8085 microprocessor and Intel 8086 microprocessor

YouTube & NPTEL Video Links

YouTube/other Video Links

- https://nptel.ac.in/courses/108/103/108103157/

Recap

- Features of Intel 8085 Microprocessor
- Pin Description of Intel 8085 Microprocessor
- Minimum and Maximum mode pins

Quiz

- Which flag is set to 1 when the result of arithmetic or logical operation is zero else it is set to 0?

A. Binary bit

B. Zero flag

C. Sign flag

D. Overflow flag

- Which flag represents the result when the system capacity is exceeded?

A. Carry flag
B. Auxiliary flag
C. Trap flag
D. Overflow flag

Quiz

- Which flag is set to 1 when the result of arithmetic or logical operation is negative else it is set to 0?

A. Carry Flag
B. Overflow Flag
C. Sign Flag
D. None

- The work of Execution Unit

A. Encoding
B. Decoding
C. Processing
D. Calculation

Quiz

- It is an edge triggered input, which causes an interrupt request to the microprocessor.

A. NMI

B. INTR

C. INTA

D. ALE

- Pipelining is possible with

A. Intel 8085 Microprocessor

B. Intel 8086 Microprocessor

C. Both

D. None

YouTube & NPTEL Video Links

YouTube/other Video Links

- https://onlinecourses.nptel.ac.in/noc20_ee11/preview

Topic Objective and its Mapping with CO

Name of Topic	Objective of Topic	Mapping with CO
Introduction to Addressing modes of Intel 8086 Microprocessor	Introduce with the Addressing modes of Intel 8086 Microprocessor	CO5

Prerequisite

- Understanding of Pin Description of Intel 8086 Microprocessor
- Knowledge of Architecture of Intel 8086 Microprocessor

Addressing modes

- Addressing modes help us to understand the types of operands and the way they are accessed while executing an instruction.
  1. Immediate addressing mode
  2. Direct addressing mode
  3. Register addressing mode
  4. Register Indirect addressing mode
  5. Indexed addressing mode
  6. Register Relative addressing mode
  7. Based Index addressing mode
  8. Relative Based Indexed addressing mode
  9. Intra segment Direct addressing mode
  10. Intra segment Indirect addressing mode
  11. Inter segment Direct addressing mode
  12. Inter segment Indirect addressing mode
  13. Implicit addressing mode

Addressing modes

Immediate Addressing Mode

- The source operand is a constant
- can be used to load information to any registers except the segment registers and flag registers (can be done indirectly)
- operands come immediately after the opcode
- EXP: MOV AX,2550H
  MOV CX,625
  MOV BL,40H
- How about MOV DS, 0123H ? (page 42)

Addressing modes

Direct Addressing Mode

- The data is in memory
- The address of the operand is provided in the instruction directly
- The address is the offset address
- The physical address can be calculated using the content in the DS register
- Exp1: MOV DL,[2400]
- Exp2: MOV AL,99H
  MOV [3518],AL

Addressing modes

Register Addressing Mode

- Registers are used to hold the data
- Memory is not accessed (hence is fast)
- Source and destination registers must match in size
- Exp:

```
MOV BX,DX
MOV ES,AX
ADD AL,BH
MOV CL,AX  (error)
```

Addressing modes

Register Indirect Addressing Mode

- The address of the memory location is in a register (SI, DI, or BX only)
- The physical address is calculated using the content of DS
- EXP: MOV CL,[SI]
  MOV [DI],AH
  MOV [SI],AX ; little endian is applied

Addressing modes

Indexed addressing mode

- In this addressing mode, offset of the operand is stored in one of the index registers. DS is the default segment for index register SI and DI.

  Example:

  MOV AX,[SI]

  Effective Address = 10H * DS + [SI]

Addressing modes

Register Relative addressing mode

- In this mode, the data is available at an effective address formed by adding an 8-bit or 16-bit displacement with the content of any one of the registers BX, BP, SI and DI in the default (either DS or ES) segment.

MOV AX, 50H[BX]

Effective Address = 10H * DS + 50H + [BX]

Addressing modes

Base plus index / Based indexed addressing mode

- In this mode the effective address is formed by adding content of a base register (any one of BX or BP) to the content of an index register (SI or DI). Default segment register DS.

MOV AX, [BX] [SI]

Effective Address = 10H * DS + [BX] + [SI]

Addressing modes

Relative Based indexed addressing mode

- In the effective address is formed by adding an 8 or 16-bit displacement with sum of contents of any one of the base registers (BX or BP) and any one of the index registers, in a default segment.

MOV AX, 50H [BX] [SI]

Effective Address = 10H * DS + 50H + [BX] + [SI]

Addressing modes

Intra segment Direct addressing mode

- If the location to which control is to be transferred in the same segment, it is called intra segment mode.
- If address to which the control is to be transferred appears directly in the instruction as a displacement value, it is what called as intra segment direct mode.

Effective Address = 8 bit / 16 bit displacement + Current content of IP

Addressing modes

Intra segment In Direct addressing mode

- In this mode, the displacement to which the control is to be transferred, is in the same segment in which the control transfer instruction lies, but it passes to the instruction indirectly.

  Example: JMP [BX]

Addressing modes

Inter segment Direct addressing mode

- In this mode, the address to which the control is to be transferred, is in different segment.
- CS & IP of the destination address are specified directly in the instructions.

Example: JMP 5000H : 2000H

Addressing modes

Inter segment In Direct addressing mode

- In this mode, the address to which the control is to be transferred, is in different segment & it is passed to the instruction directly.

  Example: JMP [2000H]

Addressing modes

Implicit addressing mode

- Instructions using this mode have no operands.
- The instruction itself will specify the data to be operated by the instruction.

  Example: CLC, STD

Quiz

- The instruction, MOV AX, 0005H belongs to the address mode

a) register

b) direct

c) immediate

d) register relative

- The instruction, MOV AX, 1234H is an example of

a) register addressing mode

b) direct addressing mode

c) immediate addressing mode

d) based indexed addressing mode

- The instruction, MOV AX, [2500H] is an example of

a) immediate addressing mode

b) direct addressing mode

c) indirect addressing mode

d) register addressing mode

Quiz

- The instruction, MVI BX, 1105H belongs to the address mode

a) register

b) direct

c) immediate

d) register relative

- The instruction, MOV CX, 1A24H is an example of

a) register addressing mode

b) direct addressing mode

c) immediate addressing mode

d) based indexed addressing mode

- The instruction, MOV BX, [2533H] is an example of

a) immediate addressing mode

b) direct addressing mode

c) indirect addressing mode

d) register addressing mode

YouTube & NPTEL Video Links

YouTube/other Video Links

- https://www.youtube.com/watch?v=3RfqkVyvnnc

Recap

Learnt about the various addressing modes

i. Register Addressing Mode
ii. Immediate Addressing Mode
iii. Direct Addressing Mode
iv. Register Indirect Addressing Mode
v. Based Addressing Mode
vi. Indexed Addressing Mode
vii. Direct I/O Addressing Mode
viii. Indirect I/O Addressing Mode
ix. Relative Addressing Mode
x. Implicit/Implied Addressing Mode

Weekly Assignment

1. State any five important features of 8086 Microprocessor.
2. What do you mean by pipelining?
3. What is the importance of Bus request and Bus grant signals?
4. Illustrate the following pins: Test, Ready, MN/MX.
5. What is the need of Multiplexing in 8086?
6. List the advantage of Queue in 8086 architecture?
7. Elaborate flags of Intel 8086 Microprocessor.
8. Discuss about Execution Unit and Bus Interface Unit in detail.
9. Differentiate between 8085 and 8086 Microprocessor.
10. Discuss control unit of 8086 Microprocessor in detail.

MCQ s

- The instruction, MOV BX, 0234H is an example of

a) register addressing mode

b) direct addressing mode

c) immediate addressing mode

d) based indexed addressing mode

- Which flag is set to 1 when the result of arithmetic or logical operation is zero else it is set to 0?

A. Binary bit

B. Zero flag

C. Sign flag

D. Overflow flag

MCQ

- The block of 8237 that decodes the various commands given to the 8237 by the CPU is

a) timing and control block

b) program command control block

c) priority block

d) none of the mentioned

- The priority between the DMA channels requesting the services can be resolved by

a) timing and control block

b) program command control block

c) priority block

d) none of the mentioned

- The register that holds the data byte transfers to be carried out is

a) current word register

b) current address register

c) base address register

d) command register

Quiz

- Which flag is set to 1 when the result of arithmetic or logical operation is zero else it is set to 0?

A. Binary bit

B. Zero flag

C. Sign flag

D. Overflow flag

- Which flag represents the result when the system capacity is exceeded?

A. Carry flag
B. Auxiliary flag
C. Trap flag
D. Overflow flag

- It is an edge triggered input, which causes an interrupt request to the microprocessor.

A. NMI
B. INTR
C. INTA
D. ALE

MCQ

- 8086 Microprocessor supports _____ modes of operation.
  A. 2
  B. 3
  C. 4
  D. 5
- 8086 can access up to?
  A. 512KB
  B. 1Mb
  C. 2Mb
  D. 256KB
- 8086 has ___ address bus.
  A. 16-bit
  B. 18-bit
  C. 20-bit
  D. 24-bit

MCQ

- Which of the following is correct about 8086 microprocessor?
  a) **Intel's first x86 processor**
  b) Motorola's first x86 processor
  c) STMICROELECTRONICS's first x86 processor
  d) NanoXplore x86 processor

Old Question Papers

1. Discuss the use of PUSH and POP Instructions in subroutines.
2. Explain the architecture of Intel 8086 microprocessor in detail
3. Discuss the various addressing modes of Intel 8086 microprocessor .
4. What is the function of PC and SP in assembly language programming?
5. Discuss about MN/MX, Test', RD' and ALE signals.
6. Specify the handshake signals and their functions of port A of the 8255A is set up as an output port in Mode 1.
7. Port A of 8255A is set up in Mode 1, and the status word is read as 18H. Is there an error in the sttus word?
8. Explain how 8237 DMA controller transfers 64K bytes of data per channel with eight address lines.
9. Specify the conditions to start the timer 8254.
10. Design a five- minute clock (timer) using the 8254 and the interrupt technique. Display minutes and seconds.
11. Set up 8254 as a square-wave generator with a 1 ms period, if the input frequency to 8254 is 1MHz.
12. Specify bit of a control word for 8255, which differentiates between I/O mode and BSR mode.

Glossary Questions

- The microprocessor is a programmable device that takes in numbers, performs on them arithmetic or logical operations according to the program stored in memory and then produces other numbers as a result. Microprocessor consists of:

– Control unit: control microprocessor operations.

– ALU: performs data processing function.

– Registers: provide storage internal to CPU.

– Interrupts

– Internal data bus

In addition to the arithmetic & logic circuits, the ALU includes the accumulator, which is part of every arithmetic & logic operation. Also, the ALU includes a temporary register used for holding data temporarily during the execution of the operation. This temporary register is not accessible by the programmer.

1. What are the functions of an accumulator?
2. List few applications of microprocessor-based system.
3. List the 16 – bit registers of 8086 microprocessor.
4. What is an operand and opcode?

Sessional Question Paper

Old Question Papers

B.TECH.

Theory Examination (Semester-VI) 2015-16

MICROCONTROLLER

Time : 3 Hours ***Max. Marks : 100***

Section-A

1. Attempt all parts. All parts carry equal marks. Write answer of each part in short. (2×10=20)

(a) What is the role of processor reset and system reset?

(b) Define the term RISC and CISC.

(c) Draw the PSW format of 8051 microcontroller & state various conditions of flags.

(d) Is it possible to write PSW register? In 8051, which register bank conflicts with the stack?

(e) How Embedded Microcontrollers are differing than Embedding Microprocessor?

(f) How will you assign Counter to count an external event?

1 (1) P.T.O.

(g) Compare microprocessors and microcontrollers.

(h) If you write to SBUF in serial mode 1, nothing is being transmitted. What may be the probable reason for this.

(i) What is the advantage of two or three level handling of interrupts?

Old Question Papers

Attempt any five questions from this section. (10×5=50)

(a) Is it possible to address 8051 individual bits? What are the addresses of bit addressable locations? How is bit addressing distinguished from the byte-wise addressing by the 8051 microcontroller? Explain.

(b) Generate a square wave with an ON time of 5 ms and on OFF time of 7ms on all pins of port0. Assume an XTAL of 22MHz.

(c) Enlist Draw generalized functional block diagram of a 8051 microcontroller specifying each block.

(d) A simple 8-bit analog-to-digital converter device, as shown, is to be interfaced to an 8051 microcomputer.

1 (2) P.T.O.

The READY line goes low when conversion data is available. The READY line should be used to interrupt the 8051 microcontroller.

Old Question Papers

ii. Write an assembly language program which will capture 250 data samples from the A/D converter and store this data in XDATA memory. The program is to be interrupt driven.

(e) Draw a simple block diagram for the transmitter section of an 8051 UART which supports 9-bit data transmission. Briefly explain the function of each block in your diagram.

(f) What does it mean when it is said that a given sensor has a linear output? Draw 8051 connection to ADC0848 and Temperature Sensor.

(g) Draw the architecture of 8096 microcontroller and compare with 8051 architecture

(h) Describe MC68HC11 microcontroller main Features with its Architecture.

Section-C

Attempt any two questions from this section. (15×2=30)

3. (i) Assume that XTAL=11.0592 MHz. What values do we need to load timer's registers if we want to have time delay of 2ms? Show the program for Timer 1 to create a pulse width of 2ms on P2.3.

(ii) Assume that bit P2.2 is used to control the outdoor light and bit P2.5 to control the light inside a building .Show how to turn on the outside light & turn off the inside one.

Expected Questions for University Exam

Q1) Explain the significance of HOLD and READY pin of 8086 microprocessor.

Q2) What is the function of PC and SP in assembly language programming?

Q3) Discuss the use of PUSH and POP Instructions in subroutines.

Q4) Explain the architecture of Intel 8086 microprocessor in detail

Q5) Discuss the various addressing modes of Intel 8086 microprocessor .

Summary

- Studied about features of Intel 8086 Microprocessor
- Studied about Pin description
- Learnt the Architecture of Intel 8086 Microprocessor
- Understood the concept of DMA Controller

References

1. Ramesh Gaonkar, “Microprocessor Architecture Programming and Applications with the 8085”, 5th Edition Penram International Publication , (India) Pvt. Ltd. 2009.
2. D.V. Hall : Microprocessors Interfacing , TMH, 2nd Edition, 2006.

Thank You