Printed page: 02Subject Code: ACSE0304/AMICSE0304/ACSEH0304

Roll No: | | | | | | | | | | | | |

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute)

Affiliated to Dr. A.P. J. Abdul Kalam Technical University, Uttar Pradesh, Lucknow

Course: B.Tech **Branch: CSE/CS/IT/M.Tech Integrated/Regional**

Semester: III[rd] **Sessional Examination: First**

Subject Name: Digital Logic and Circuit Design **Year- (2022-2023)**

Time: 1.15 Hours **Max. Marks:30**

General Instructions:

- *This Question paper consists of .....pages & .....questions. It comprisesthree Sections -A, B, &C. You are expected to answer them as directed.*
- *Section A–Q.No- 1 isof one 1 mark each &Q.No- 2 carries 2 mark each.*
- *Section B-Q. No- 3 carries5 marks each.*
- *Section C-Q.No-4 &5carries6markseach.Attempt any one parta orb*

		SECTION – A	[08Marks]	
1.	All questions are compulsory-		(4×1=4)	
	a.	Binary equivalent of gray code 101011 is: a. 110010 b. 101010 c. 110110 d. 110011	(1)	CO-1
	b.	The value of (011010101.110)2 in octal and hexadecimal are: a. (236.6)8 and (D5.B)16 b. (235.6)8 and (D5.C)16 c. (325.6)8 and (D5.C)16 d. (225.6)8 and (D5.C)16	(1)	CO-1
	c.	Excess-3 code of 739 is: a. 1010 0110 1100 b. 1101 1001 1000 c. 1101 0110 1100 d. 1010 1001 1000	(1)	CO-1
	d.	Determine the value of base x if (50)x=(203)4	(1)	CO-

		a. 6 b. 5 c. 7 d. 8		1
2.		**All questions are compulsory-**		(2×2=4)
	a.	$(347)_{10} = ()_2 = ()_8 = ()_{16} = ()_{BCD}$	(2)	CO-1
	b.	Given the two binary numbers X = 1010101 and Y = 1001011, perform the subtraction X-Y using 1's complements.	(2)	CO-1
		SECTION – B		[10Marks]
3.		**Answer any two of the following-**		(2×5=10)
	a.	Add in BCD 6710 and 431810.	(5)	CO-1
	b.	Simplify the expression using DEMORGAN'S THEOREM:[a(b+c)+a'b]'	(5)	CO-1
	c.	Receiver receives the hamming code 1111001, check whether the data received is correct if not, check the error and correct it.	(5)	CO-1
		SECTION – C		[12Marks]
4		**Answer any one of the following-**		(1×6=6)
	a.	What is cyclic Code? Prove that (110, 101, 011) is a cyclic code.	(6)	CO-1
	b.	Minimise the following function in POS minimal form using K-Maps: F(A, B, C, D) = M(6, 7, 8, 9) + d(10, 11, 12, 13, 14, 15)	(6)	CO-1
5.		**Answer any one of the following-**		(1×6=6)
	a.	Simplify the following Boolean functions using the Karnaugh map: $F(w,x,y,z)=\Sigma m(0,1,2,4,5,12,13,14)$ + don't care conditions $\Sigma d(6,8,9)$	(6)	CO-1
	b.	The solution to the quadratic equation k2 – 11k + 22 = 0 is k = 3 and k = 6. What is the base of number systems?	(6)	CO-1

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Course B.Tech **Branch:-CSE/CS/IT/M.Tech Integrated/Regional**

Semester:III[rd] **Sessional Examination: Second**

Subject Name: Digital Logic and Circuit Design Year- (2022 - 2023)

Time: 1.15Hours **Max. Marks:30**

General Instructions:

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- *Section C-Q.No-4 &5carries 6 markseach.Attempt any one part a orb*
-

SECTION – A [08Marks]

1. All questions are compulsory- (4×1=4)

a. In a 1:16 demultiplexer, the number of control inputs will be: (1) CO2

a) 3 b) 4
c) 5 d) 16

b. A decoder converts n inputs to _____ outputs. (1) CO2

a) n b) n^2
c) 2^n d) n^n

c. How many full adder are needed to implement 4 bit parallel adder: (1) CO2

a) 2 b) 3
c) 4 d)5

d. If A and B are the inputs of a half adder, the sum is given by _____ (1) CO2

a) A AND B b) A OR B
c) A XOR B d) A EX-NOR B

2. All questions are compulsory- (2×2=4)

a. Explain Applications of Multiplexer. (2) CO2

b. Define combinational logic. (2) CO2

SECTION – B **[10Marks]**

3. Answer any two of the following- **(2×5=10)**

a. Draw the truth table and circuit diagram of the 8 to 3 encoder. (5) CO2

b. Implement 3:8 decoder using 2:4 decoders. (5) CO2

c. Draw the logic diagram of full subtractor and explain its operation. (5) CO2

SECTION – C **[12Marks]**

4 Answer any one of the following- **(1×6=6)**

a. Implement the following Boolean function using 8:1 multiplexer (6) CO2

$F(A, B, C.D) = \Sigma m\,(0,1,2,5,7,8,9,14,15)$.

b. Draw a BCD adder and explain its working. (6) CO2

5. Answer any one of the following- **(1×6=6)**

a. Explain about 2-bit Magnitude Comparator. (6) CO2

b. Design the combinational circuit of 4 Bit Parallel Adder? (6) CO2