Clocks Basics in 10 Minutes or Less

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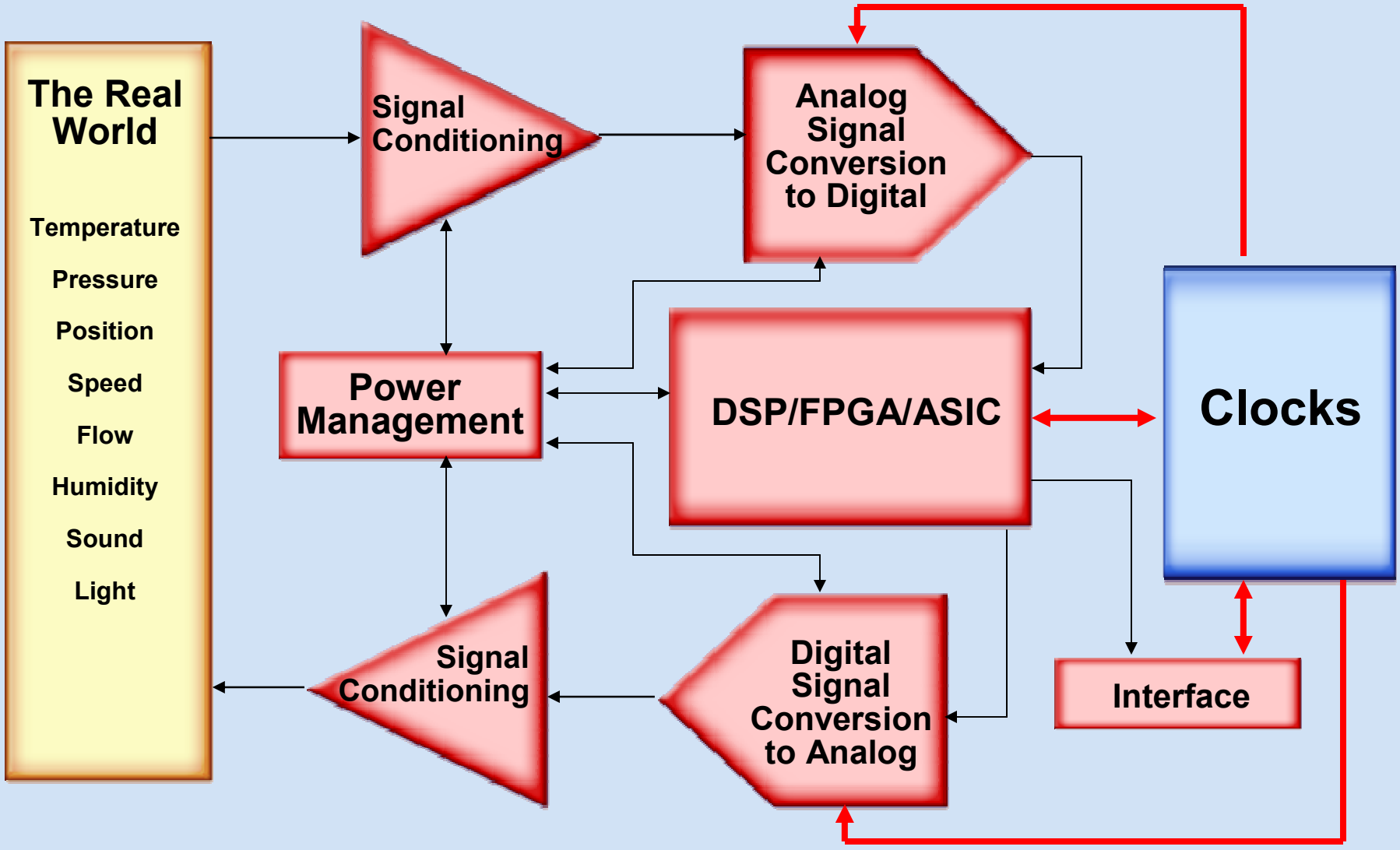
Presentation Overview

- Introduction to Clocks
- Clock Functions
- Clock Parameters
- Common Applications
- Summary

Clocks in the Signal Chain



Introduction to Clock

Every Electronic system needs some form of clocks!
Clocks provide the “pulse” in electronics.

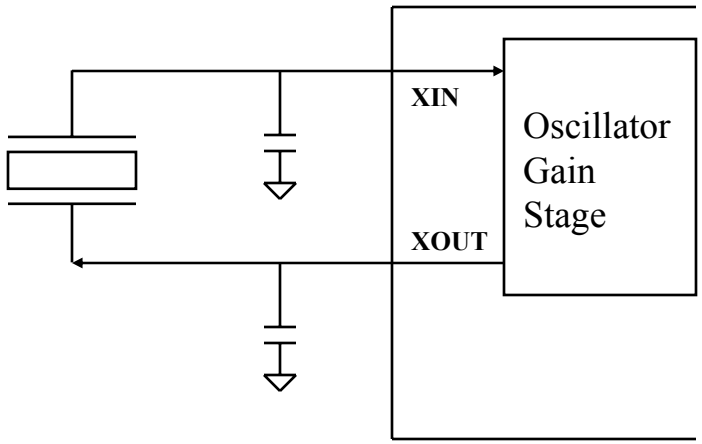
Clock signal regulates to flow of logic signals so that system can run an optimum speed

Introduction to Clocks

- What is a Clock?
  - A device that generates periodic signals for timing.
- What types of systems require a clock?
  - Any system that requires a reference to time for synchronization, command execution, and data transfer.
- How does the clock fit into the signal chain?
  - Clocks are connected to anything that processes a signal in the digital domain. Therefore, clocks are needed to connect the **DSP/FPGA/ASIC, Data Converters, and Interface components**.
- What role does the clock play in the system?
  - The clocking network provides the frequency inputs to the various devices within a system allowing them to perform their intended function.

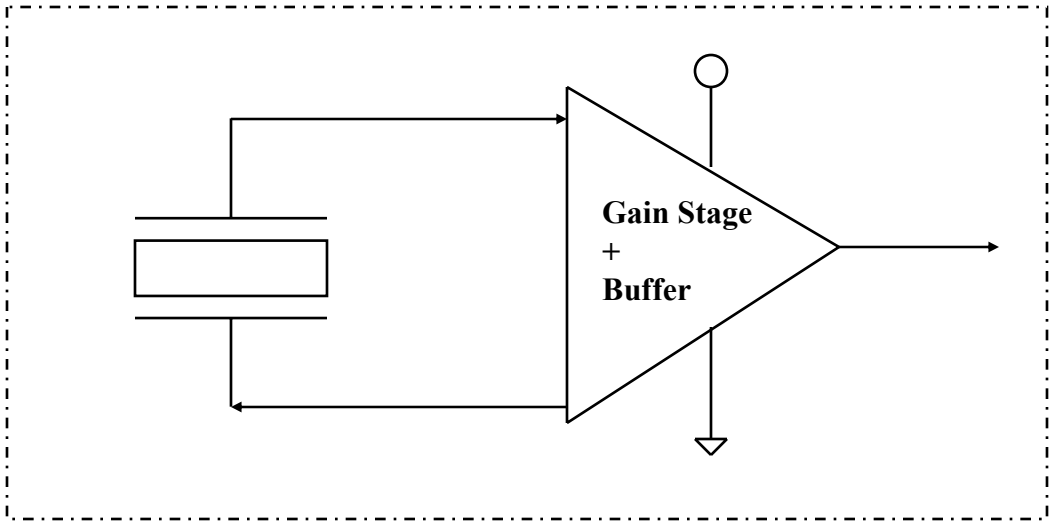
Crystal

Crystal—A crystal is the disk of quartz and the packaging around it. It is a passive circuit element which requires an oscillation circuit to produce a useful signal.

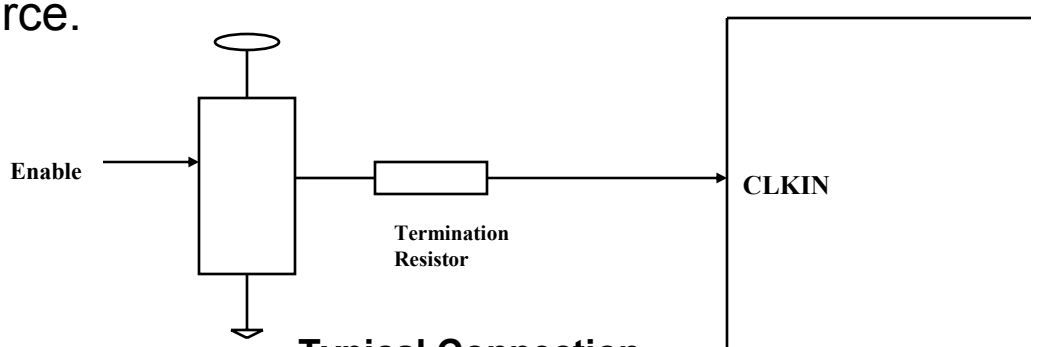


Typical Connection

Oscillator



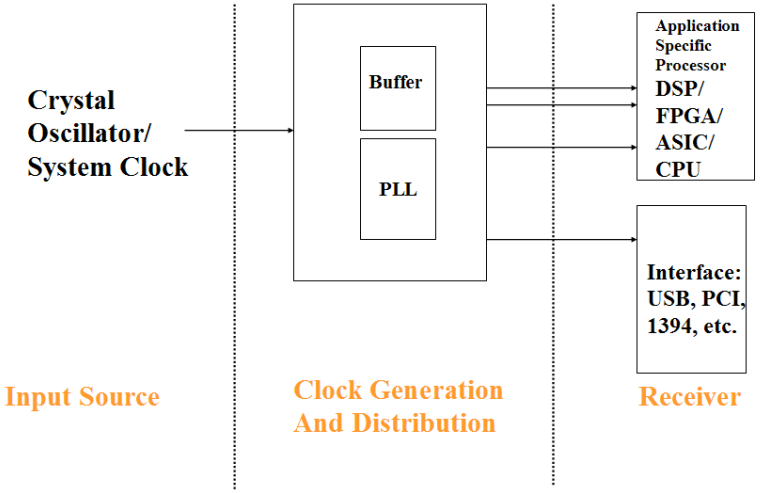
Oscillator—An oscillator includes the crystal and the oscillation circuit which Provides a signal with a logic level output. An oscillator is an independent clock source.

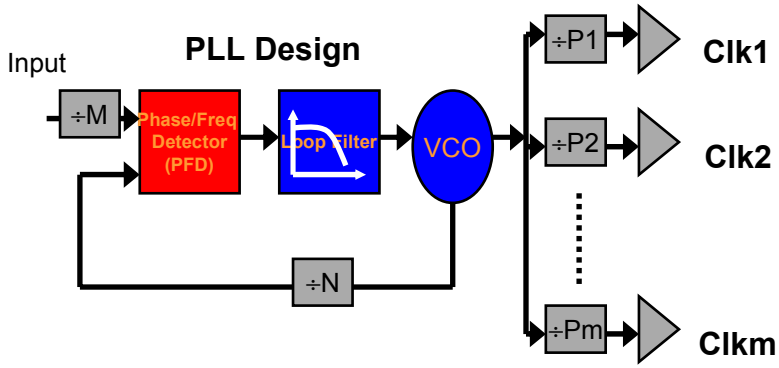


Typical Connection

How Does a Basic Clock Work?

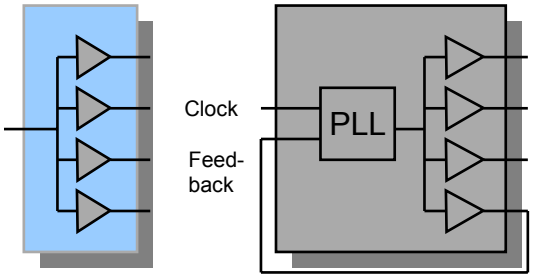
- A clock receives an input frequency from a source and either distributes that frequency or generates new frequencies to send as outputs to other devices within the system. This can either be done using Phases Locked Loop (PLL) or non-PLL based circuitry.
- Non-PLL clocks are used when the time delay between source and output, known as a propagation delay, is not important to the system.
- PLL Clocks are used when the system needs to minimize the propagation delay. It is able to do this by acting as a phase detector to keep an input clock in phase with an incoming frequency through the use of a feedback loop.
  - PLL's allow a clock to:
    - Eliminate propagation delay
    - Allows Phase Adjustments
    - Perform Integer or Fractional Multiplication
    - Make Duty Cycle Corrections
    - Remove noise from the reference clock with jitter cleaning.

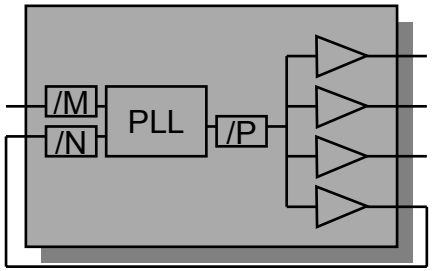


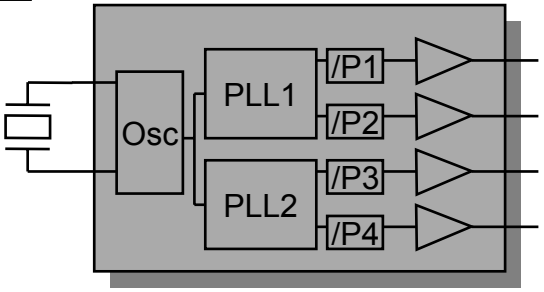


Clock Functions

- Fanout Buffers
- Multipliers/Dividers
- Synthesizers
- Jitter Cleaners

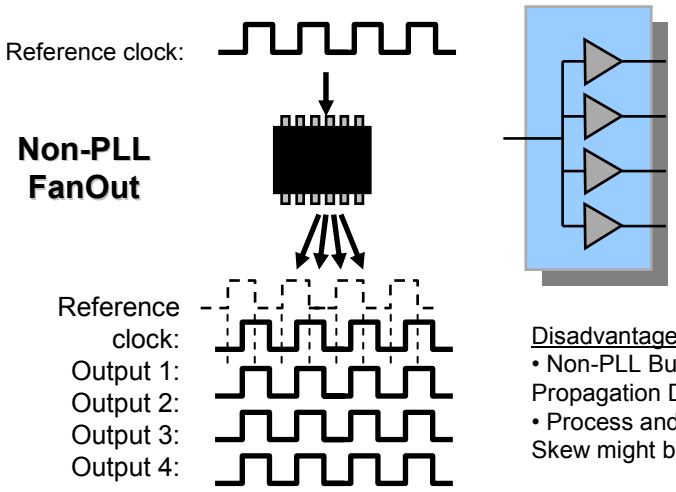




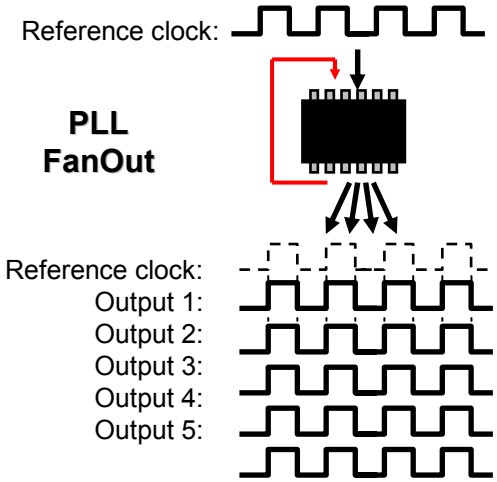


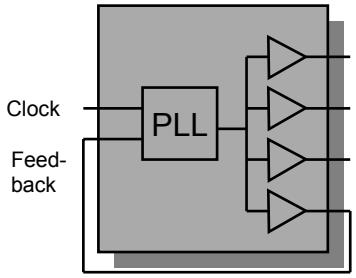
Fanout Buffers

Fanout Buffers are the most basic type of clock and they are used to distribute an input frequency to multiple outputs at the same frequency. These are typically used in low phase-noise clock distributions. Fanout Buffers can be either PLL or Non-PLL Based, depending on the system requirements.



Disadvantages:
- Non-PLL Buffer adds a Propagation Delay time
- Process and Part to Part Skew might be an issue





Multiplier/Divider

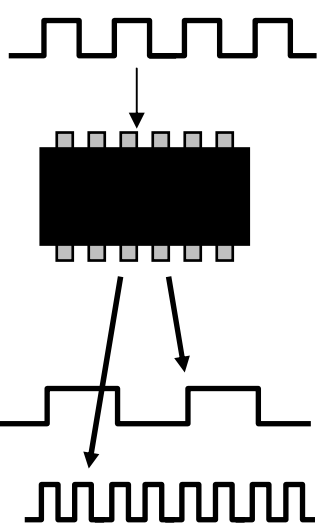
Multiplier / Divider: A Clock which is able to translate an input clock into an output clock with a higher (multiplier) or lower frequency (divider). A Divider Clock can be either PLL or Non-PLL based.

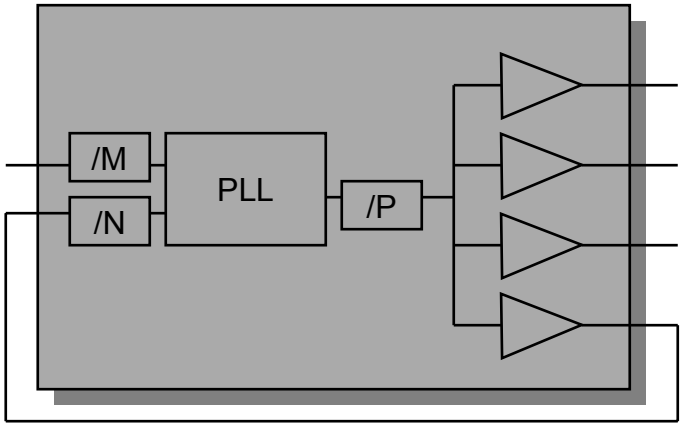
Reference clock (f_{clock}):

Clock Multiplying / Dividing

½ * f_{clock}

2 * f_{clock}



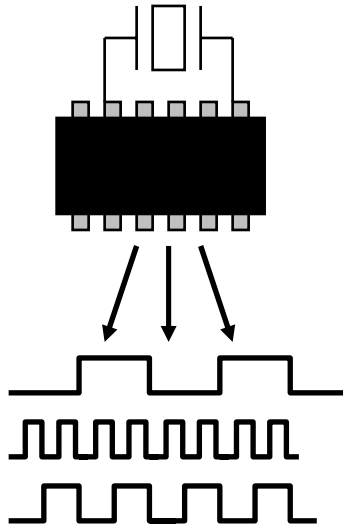


Synthesizer

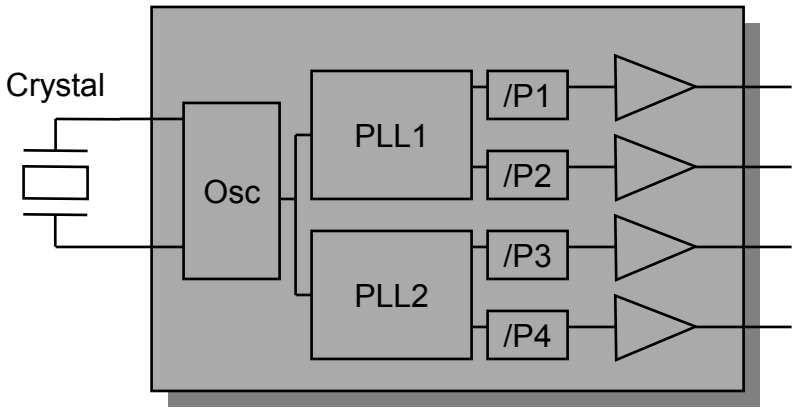
Synthesizer: A special kind of circuit that contains one or more PLLs. It receives a stimulus, usually a low frequency signal from a crystal, and generates multiple outputs with different (integer or fractional) frequencies.

Clock Synthesizers

Reference clock



f_{clock1}
f_{clock2}
f_{clock3}



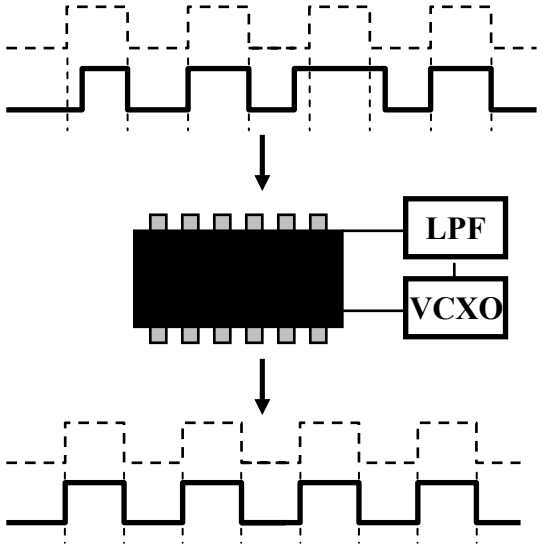
Jitter Cleaner

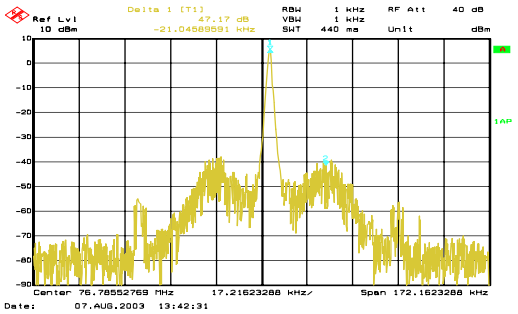
Jitter Cleaner: Any PLL-based clock that cleans the noises from the reference clock and provides a clean and synchronized signal for the receivers using an external VCO (VCXO) or internal VCO.

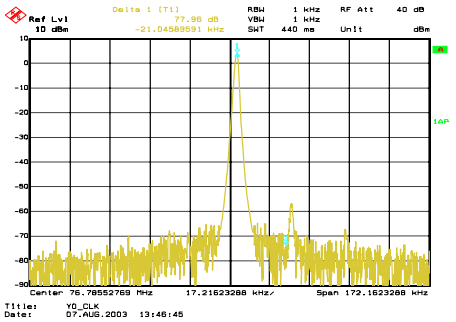
Ideal Input clock:
Real Input clock with Jitter:

Jitter Cleaning using a VCXO

Ideal Input clock:
Clean Clock:







Clock Parameters

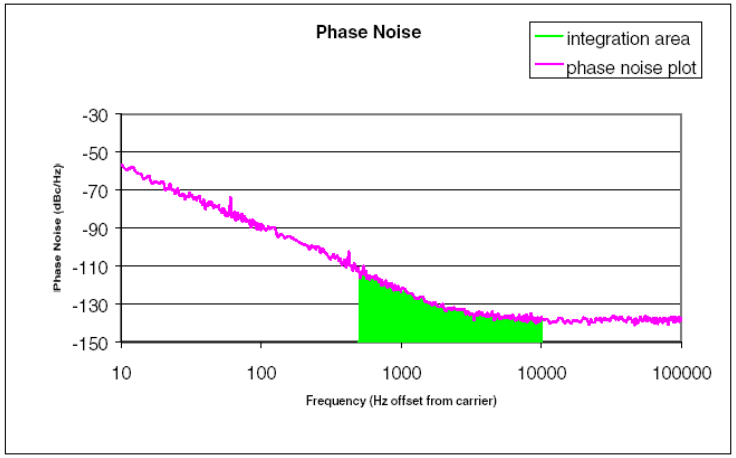
- What are the key characteristics of a clock?
  - Signaling Level (Pre-Defined by the Receivers in the System)
    - Single-Ended: LVCMOS,TTL, LVTTL – Up to ~250 MHz
    - Differential: LVDS, LVPECL, CML, PCI Express (HCSL), SSTL, HSTL - Up to 10+ GHz
  - Performance
    - Jitter: Common Range of <200 fs – 100 ps
    - Propagation Delay: Common Value of ~3 ns
    - Output Skew: Common Range of 100 – 500 ps
  - # of Outputs: Common Range of 1-24 Channels
  - # of Frequencies: Can be equal to # of channels
  - Input Voltage: Common Range of 1.2 – 5 V
  - Input Frequency
  - Output Frequencies

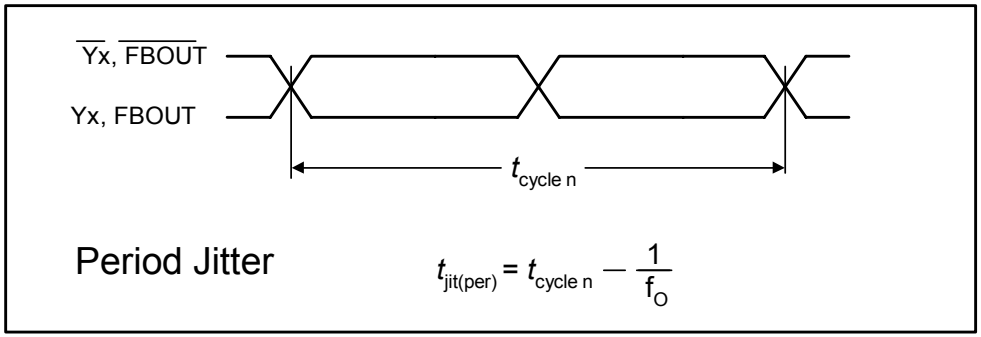
Jitter

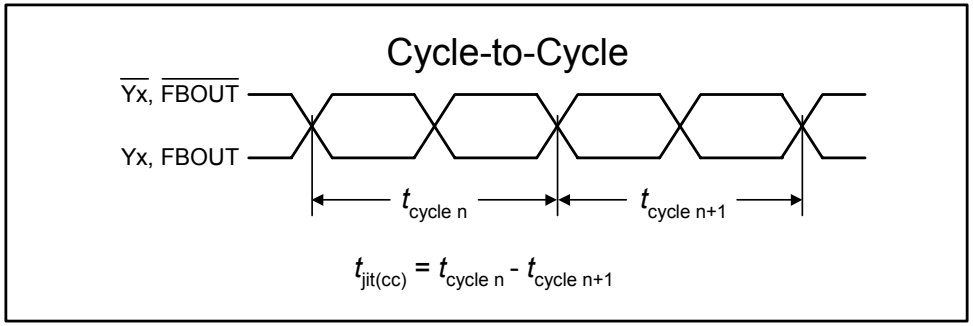
- Jitter is the most commonly used measure of the performance of a clock. It is defined as any signal edge deviation from ideal. There are three main types of jitter that are commonly considered. These are period, phase, and cycle-to-cycle. Common Jitter performance can range from < 200 fs to 100 ps.

- Period
  - The deviation in cycle time of a signal with respect to ideal period over a random sample of cycles. This is also referred to as short-term jitter.

- Cycle-to-Cycle
  - the variation in cycle time of a signal between consecutive cycles, over a random sample of successive cycle pairs. Also known as adjacent cycle jitter.





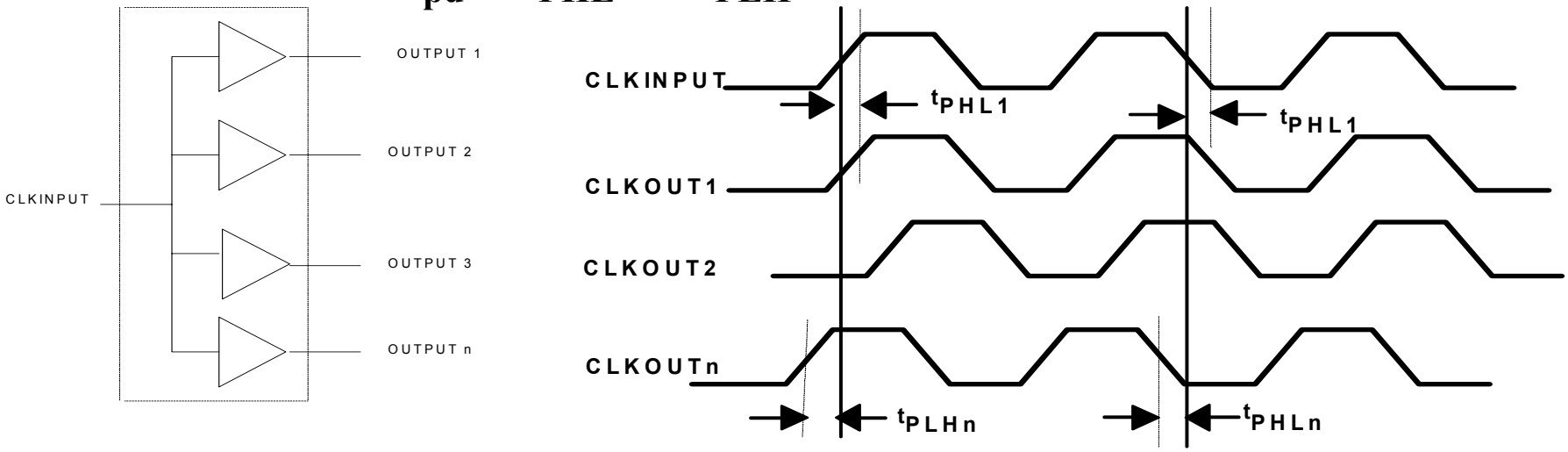


- Phase
  - The integrated value from phase noise plot in time over a specific band of frequencies. This is long term jitter.

Propagation Delay

Propagation delay time, t_{pd}: The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (High or Low) to the other defined level. It is common to have a propagation delay of ~3 ns.

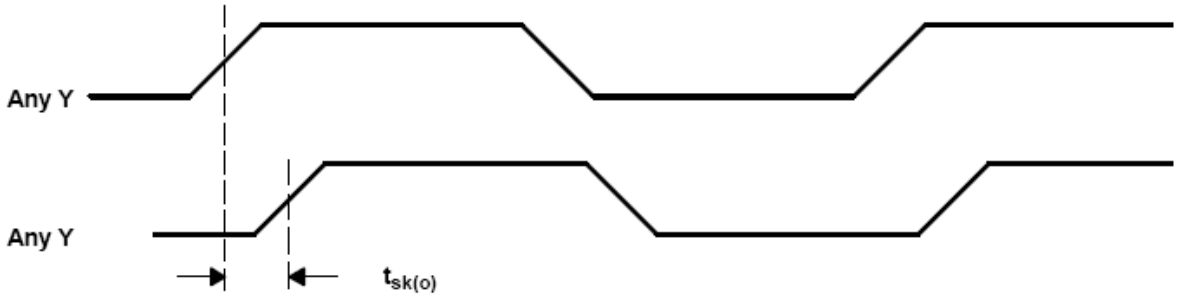
$$t_{pd} = t_{PHL} \text{ or } t_{PLH}$$



Propagation delays, t_{PLH} and t_{PHL}

Output Skew

Output Skew, $t_{sk(o)}$: The difference between any two propagation delay times when input switching causes multiple outputs switching. Common output skew can range anywhere from 100 ps to 500 ps.



Common Applications

- Communications
  - Very Low Jitter
  - High Performance Requirements
  - Generally differential inputs to support higher speeds
- Consumer
  - Frequency Accuracy (0 PPM translation Error)
  - Low Power
  - Different/Multiple Clock Frequencies
  - Medium Jitter Performance
  - Frequency Synchronization
  - Low Cost
  - Market on Time
- PC/Memory
  - JEDEC Standards
  - Medium Jitter Performance
  - Timing Performance
  - Support DDR/DDR2/DDR3 requirements.

Wireless Basestations

HDTV

Video Surveillance

Servers

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