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TITLE: Part 3

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Objective

The goal of this lab was to design a clocking system to be able to drive the ADC externally with a 555 Timer IC. Th design required a certain clock period and duty cycle which would intern complete the sampling required. A MATLAB script was used to determine the certain component values required for the design. Which then was verified through simulation and testing through physical hardware. Once done, the results will be used to compare against simulation and hardware verification and to the pervious design goals.

Circuit Diagrams

Schematic of external astable system clock on Multisim

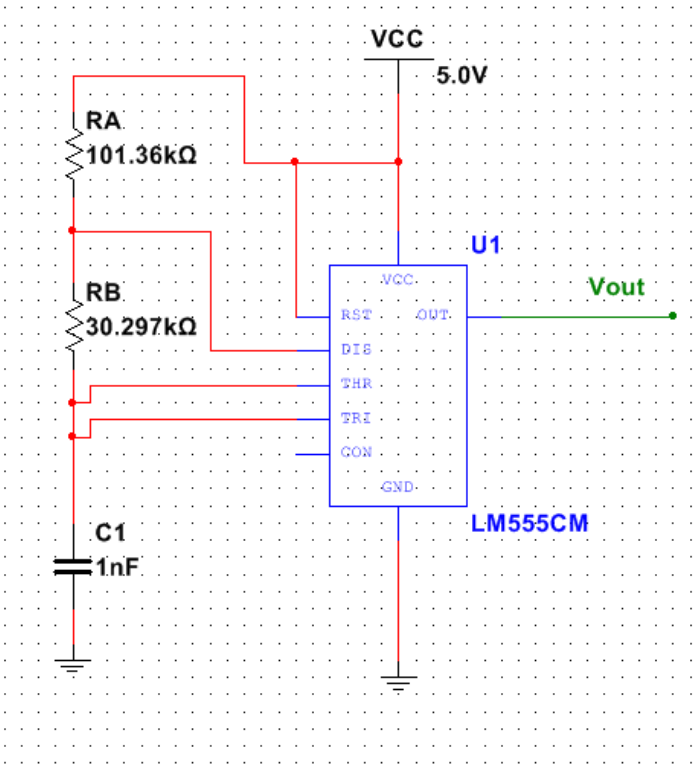

Figure 1: Schematic of LM555CM external clock

Results

Simulation

Graph showing Voltage (V) vs. Time (s) of Simulation Duty Cycle

Voltage (V)

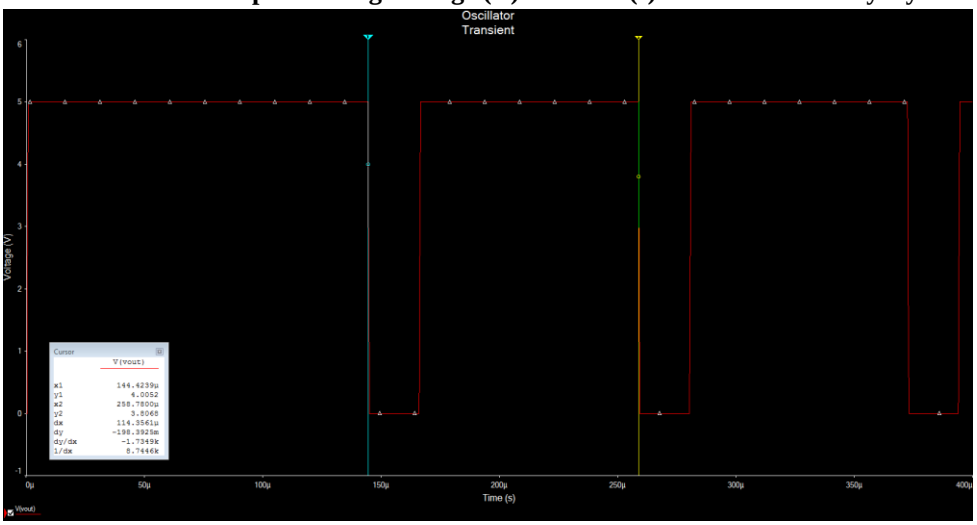

Figure 2: Duty Cycle of clock on Multisim

Time (µs)

Graph showing Voltage (V) vs. Time (s) of Simulation Off time

Voltage (V)

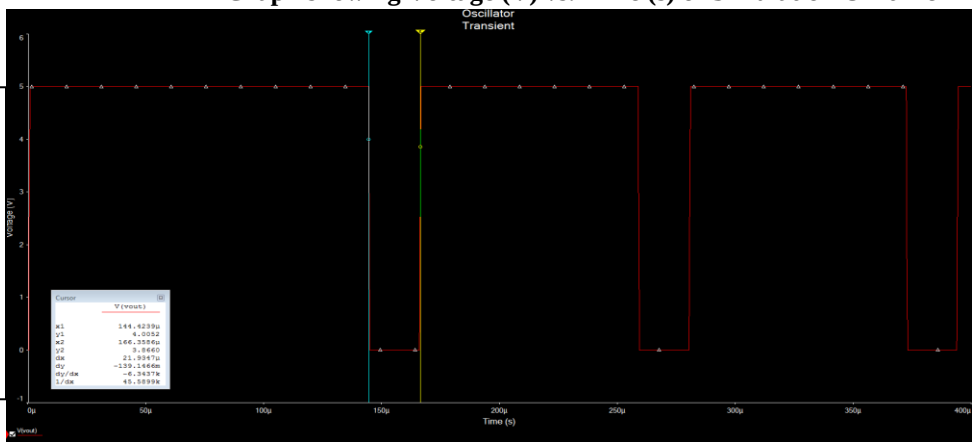

Figure 3: Off time of clock on Multisim

Time (µs)

Graph showing Voltage (V) vs. Time (s) of Simulation On time

Voltage (V)

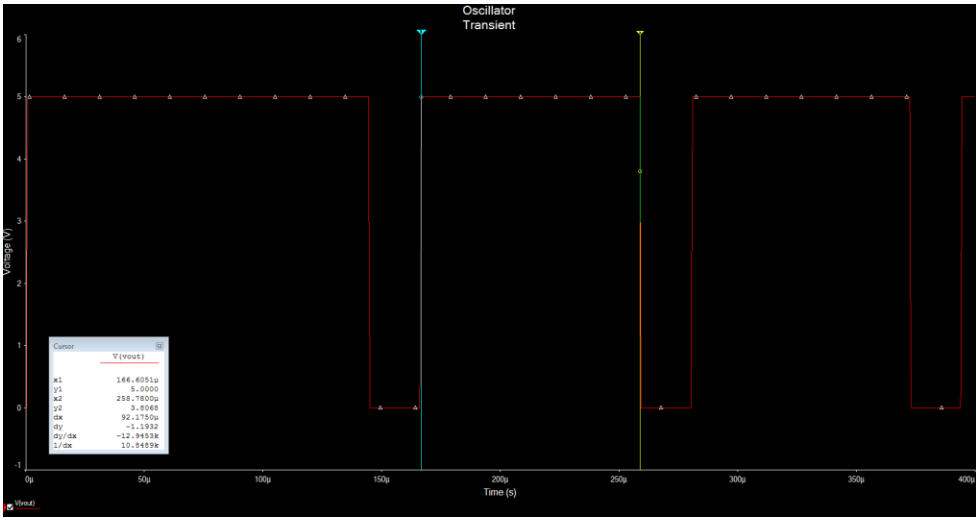

Figure 4: On time for clock on Multisim

Time (µs)

Graph showing Voltage (V) vs. Time (s) for discharge time

Voltage (V)

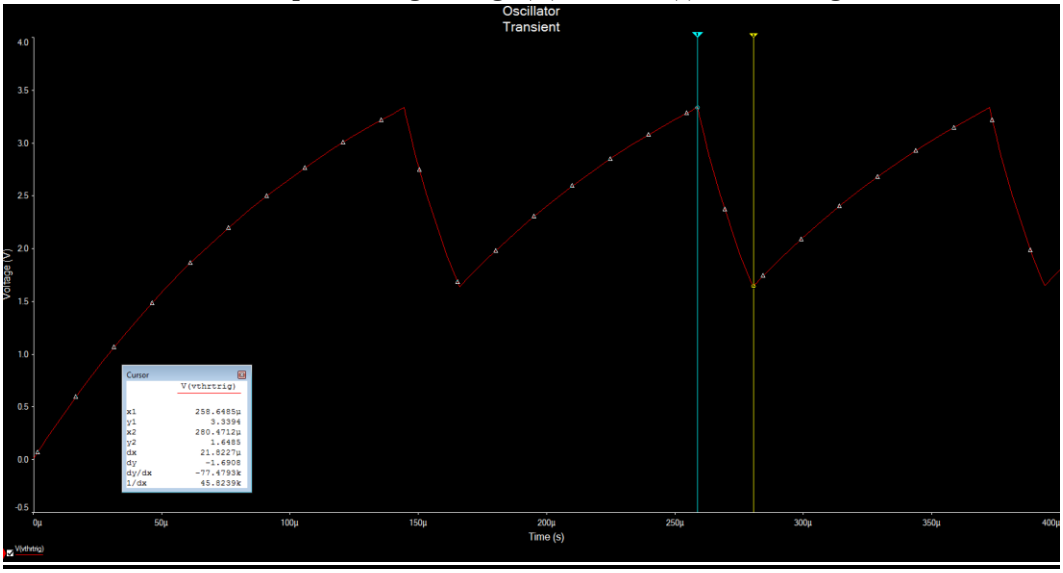

Figure 5: Discharge time in Multisim

Time (µs)

Graph showing Voltage (V) vs. Time (s) of Simulation Charge time

Voltage (V)

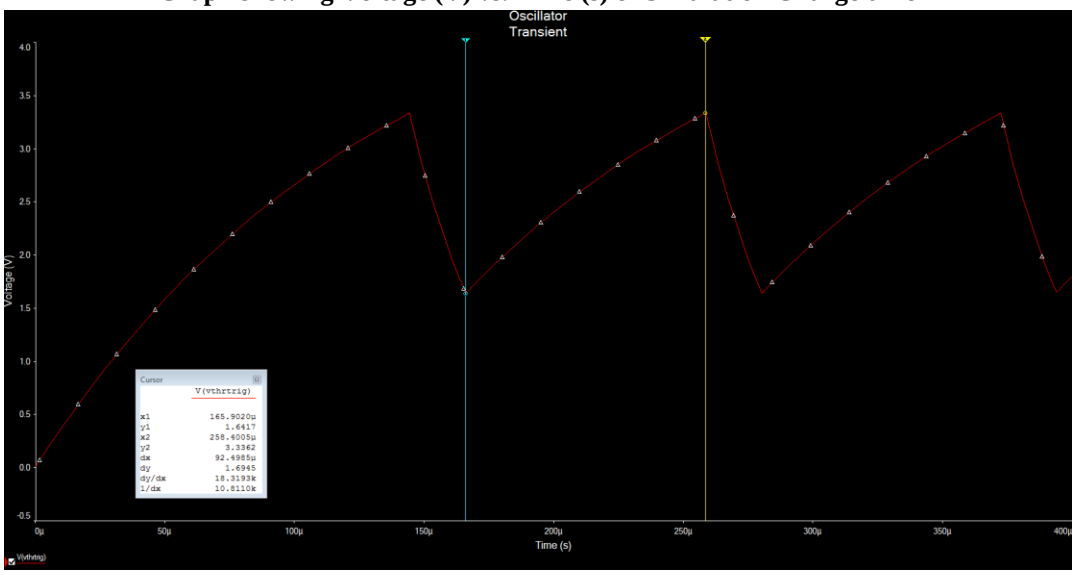

Figure 6: Charge time on Multisim

Time (µs)

Graph showing Voltage (V) vs. Time (s) of Simulation Trigger

Voltage (V)

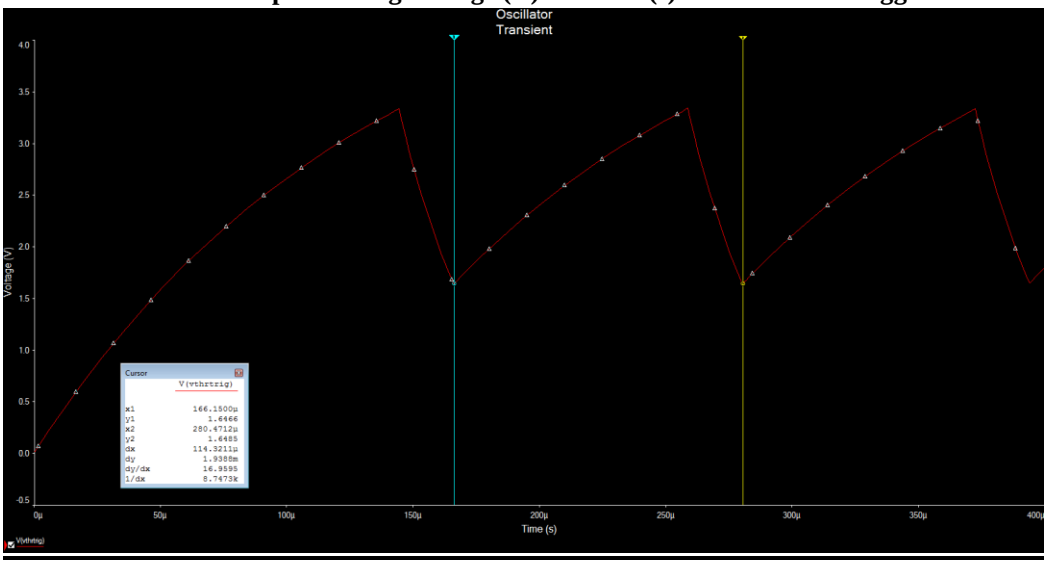

Figure 7: One clock cycle of Trigger waveform

Time (µs)

Hardware

Graph showing Voltage (V) vs. Time (s) of LM555 clock

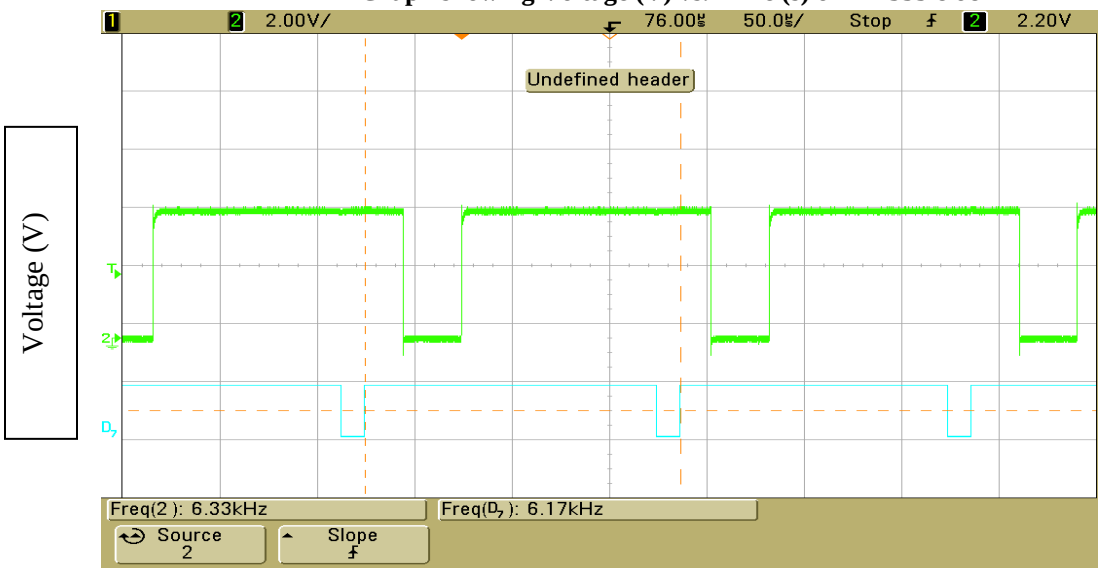

Figure 8: Waveform showing frequency

Time (µs)

Graph showing Voltage (V) vs. Time (s) of INTR

Voltage (V)

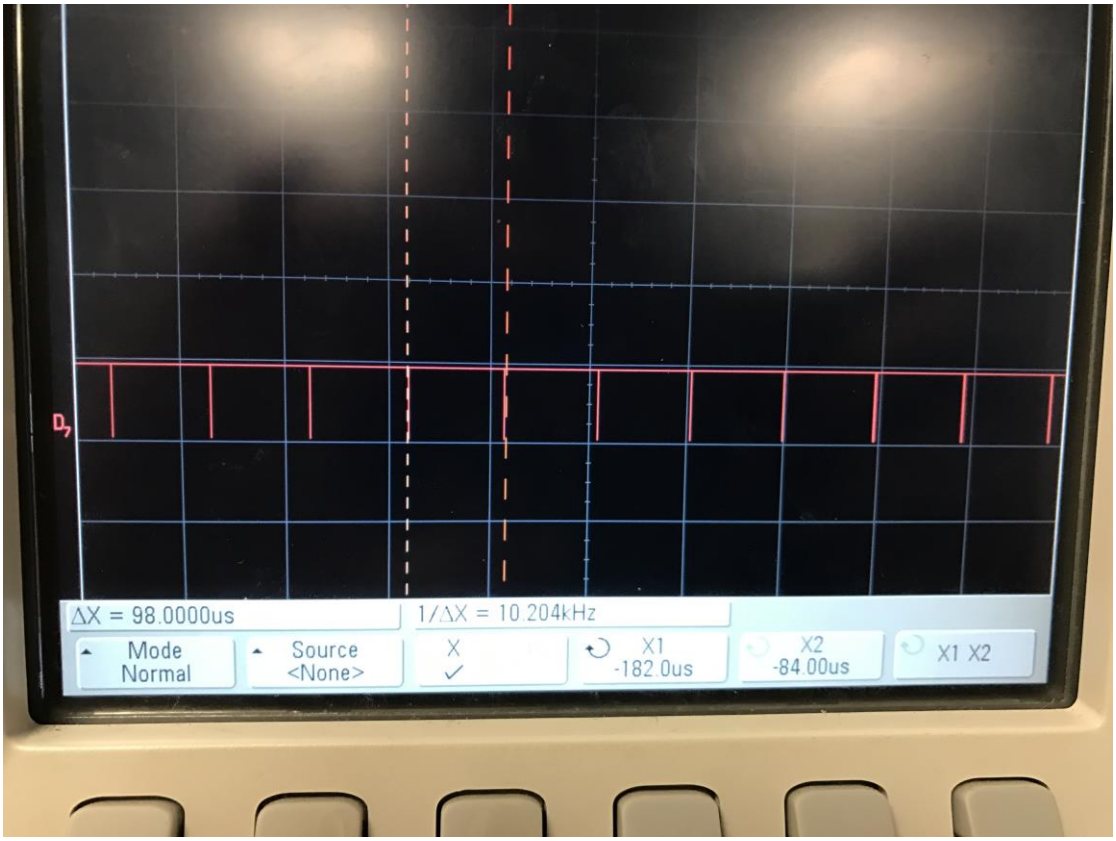

Figure 9: INTR Waveform of ADC

Time (µs)

Graph showing Voltage (V) vs. Time (s) of LM555 off time

Voltage (V)

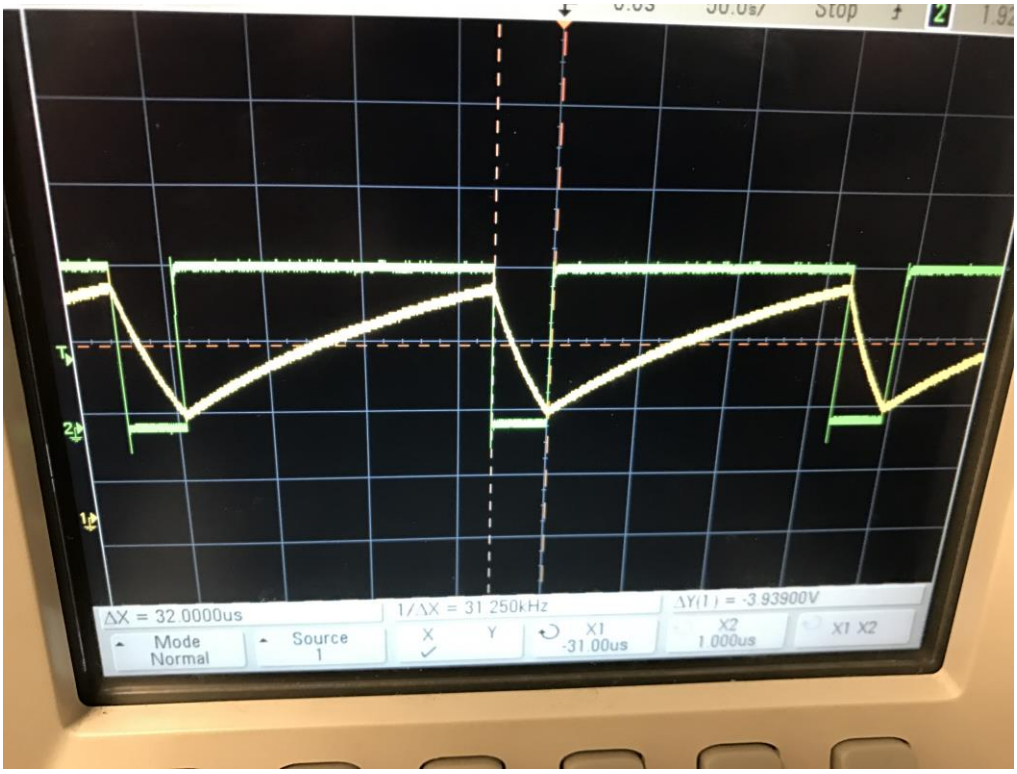

Figure 10: Off time of external system clock

Time (µs)

Graph showing Voltage (V) vs. Time (s) of LM555 on time

Voltage (V)

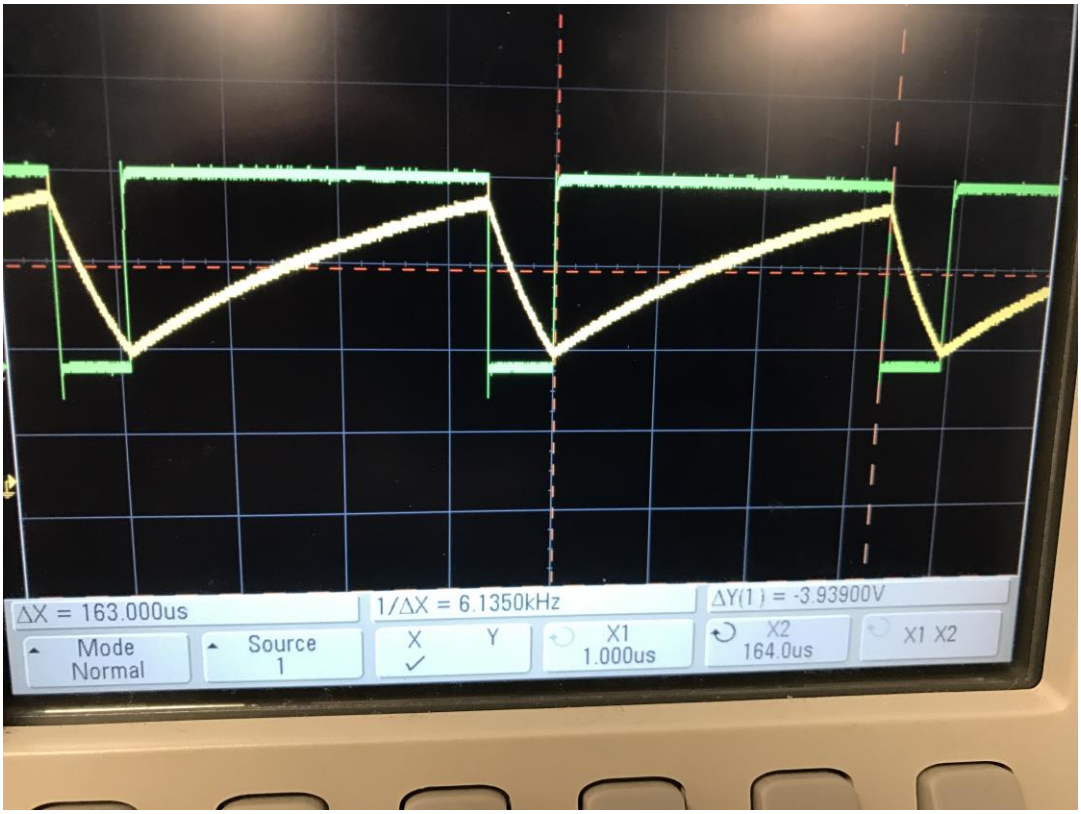

Figure 11: On time for system clock

Time (µs)

Table 1. Table showing component values used for the experiment

	Theoretical	Simulation	Hardware (Resistors in series to make total)				Percent Error
C (nF)	1	1	1.4	R_1	R_2	R_{total}	40.00%
R_A (kΩ)	101.36	101.36	N/A	99.615	0	99.615	1.72%
R_B (kΩ)	30.297	30.297		0.99	29.877	30.867	1.88%

Table 2. Table showing LM555 Clock parameter values

	Theoretical	Simulation	Hardware	Percent Error
Frequency (kHz)	8.91	8.7446	6.33	27.61%
On-Time (µs)	91.238	92.17	163	76.85%
Off-Time (µs)	20.996	21.937	32	45.87%
Charge Time (µs)	91.238	92.49	163	76.24%
Discharge Time (µs)	20.996	21.82	32	46.65%
Period	112.234	114.356	195	70.52%
Duty-Cycle (%)	81.29	80.59	83.58	3.71%

Explanation Of Results

The First part of the lab called for calculating the desired RA, RB, and C values needed to run the 555 Timing clock to drive the ADC. For our design a capacitor value of 1 nF and the desired time low for the design was chosen to be 120 ns. At first the time low was 120ns which should have produced a 99.98% duty cycle. But this lead to an issue during simulation where the oscillator would never reach 0V. In turn the design was changed and a time low was chosen to be 20 µs instead. The MATLAB script was used shown in Append A, showing the automation of this to find the other parameters RA and RB for the design. Equations 1 and 2 shown below, where used to find these values.

$$\text{Discharging Interval: } T_L = R_B C \ln(2) \quad \text{Eq 1.}$$

$$\text{Period of Oscillation: } T_H + T_L = (R_A + 2R_B)C \ln(2) \quad \text{Eq 2.}$$

As shown in Table 1 the parameter values, one thing to take away from this table is the large percentage error in the capacitor value, which was 40% error. This caused the other results to be off by that margin of error do to the lack of accurate capacitor value.

The Simulation was done with Multisim using the LM555CM and the resistors values chosen through the MATLAB script. The schematic of the circuit that was used can be seen in Figure 1. Figures 2 through Figures 8 show the plots obtained by conducting transient analysis on the circuit in Multisim. The results obtained from simulation were congruent with the theoretical values. In Table 2 the off time of the simulation was 21.937 µs and the on time was 92.17 µs. Also, Respectively the charging time and discharging time of the capacitor was 92.49 µs and 21.92 µs

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The frequency and duty cycle values obtained were 8.7446 kHz and 80.59% respectively. Studying the Trigger pin gave the charge, discharge, and period values of 21.82 µs, 114.356 µs and 92.49 µs respectively. The period, duty cycle, frequency was close to theoretical values. Additionally, charging and discharging times were also found using simulation. The plots obtained from this part were used as a basis for the hardware setup.

The parameters such as the resistor and capacitor values obtained from the MATLAB script were also used to set the period and duty cycle of the external clock, for the hardware

aspect. The clock itself was implemented using the LM555CN Timer . The period, frequency, duty cycle, charge time, discharge time were found from the waveform displayed on the scope by probing the output and the trigger pins of the Timer IC. The values were tabulated in Tables 1 and Table 2 can be seen from these tables, the on time, off time and period values obtained from the LM555CN clock s were 163µs, 32µs and 195 µs respectively. The frequency and duty cycle values obtained were 6.33 kHz and 83.58%. The trigger also yielded discharge, charge, and period values of 163µs, 32µs and 195 µs respectively. The error within the capacitor can be seen here which might have caused the numbers to be skewed with the simulation and theoretical values here.

Once the external clock was designed as per specifications, the ADC's WR, the Timer was now directly tied. Since the INTR and WR were no more tied it was imperative to ensure that INTR went low while the external clock was high. To see if this occurred, INTR and the external clock were connected to the Logic Analyzer and both waveforms were studied on the scope as seen in figure 8. A 10 kΩ potentiometer replaced the original set of resistors used in the previous lab. The potentiometer was tweaked to increase the frequency of the internal clock.

Throughout this lab our team overcame many issues with tolerances with in comments to equipment not functioning correctly. The above screen shots where not consistent because of the tool failing on us multiple times in order to get a accurate capture. But, in all we were able to construct a working clock to drive the ADC for the desired conditions.

Appendix

```
close all
clear all
clc

C = 1*10^(-9);

TL = 21*10^(-6);

RB = TL/(C*log(2))

RA = (9.126*10^(-5))/(C*log(2)) - RB

fprintf('RA is %f ohm\n', RA)
fprintf('RB is %f ohm\n', RB)
%Value outputs
% RB =
%    3.0297e+04
% RA =
%
%    1.0136e+05
```

Figure 12: Matlab Script