DREXEL UNIVERSITY
Electrical and Computer Engineering
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Electrical Engineering Laboratory IV, ECEL-304

TITLE: Part 5

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Objective

The objective of this lab was to build a counter circuit that will drive the addressable bit on the RAM. This will allow for reading the signal from the ADC into the RAM to store for playback. The counter circuit will be built using the three cascading 74LS590 8-bit counters to achieve the 17 bits needed for this design. Other external control mechanism will be designed in order to play and pause the counter for playback. The circuit will be both simulated and built with hardware to compare the thermotical and experimental results.

Results

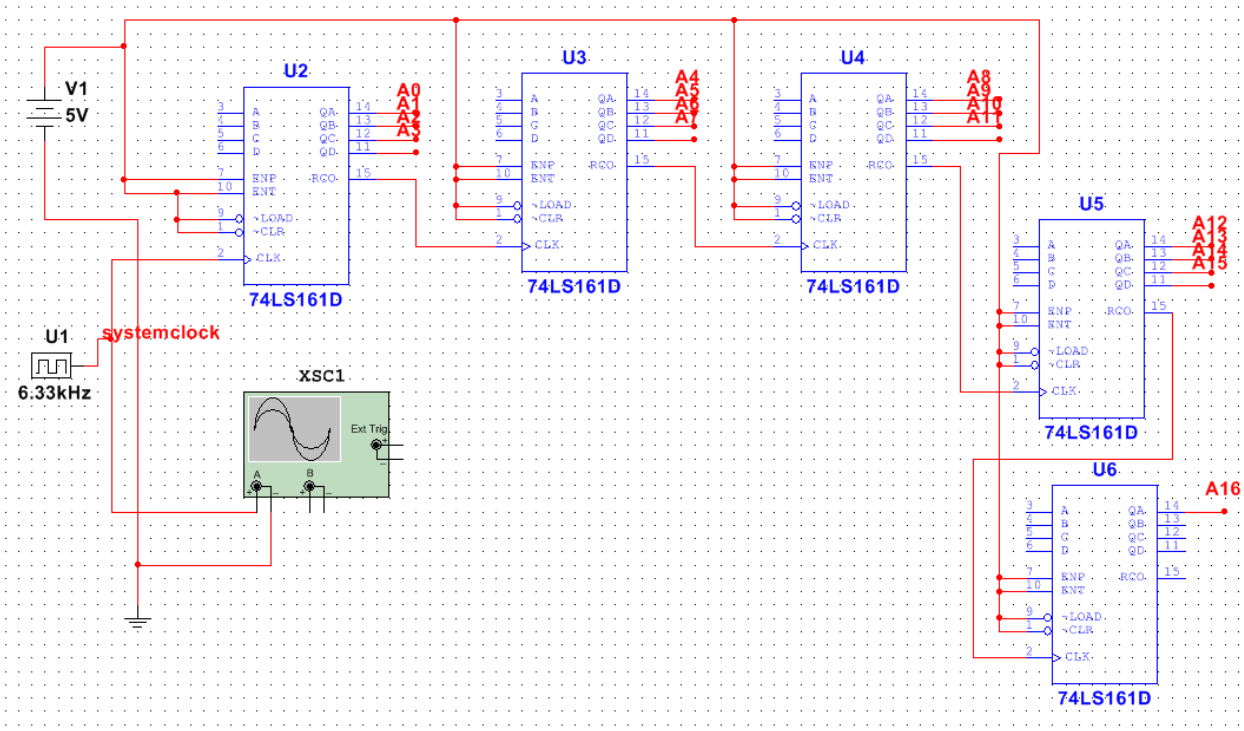

Figure 1:Schematic used in Multisim to achieve 17-bit counter

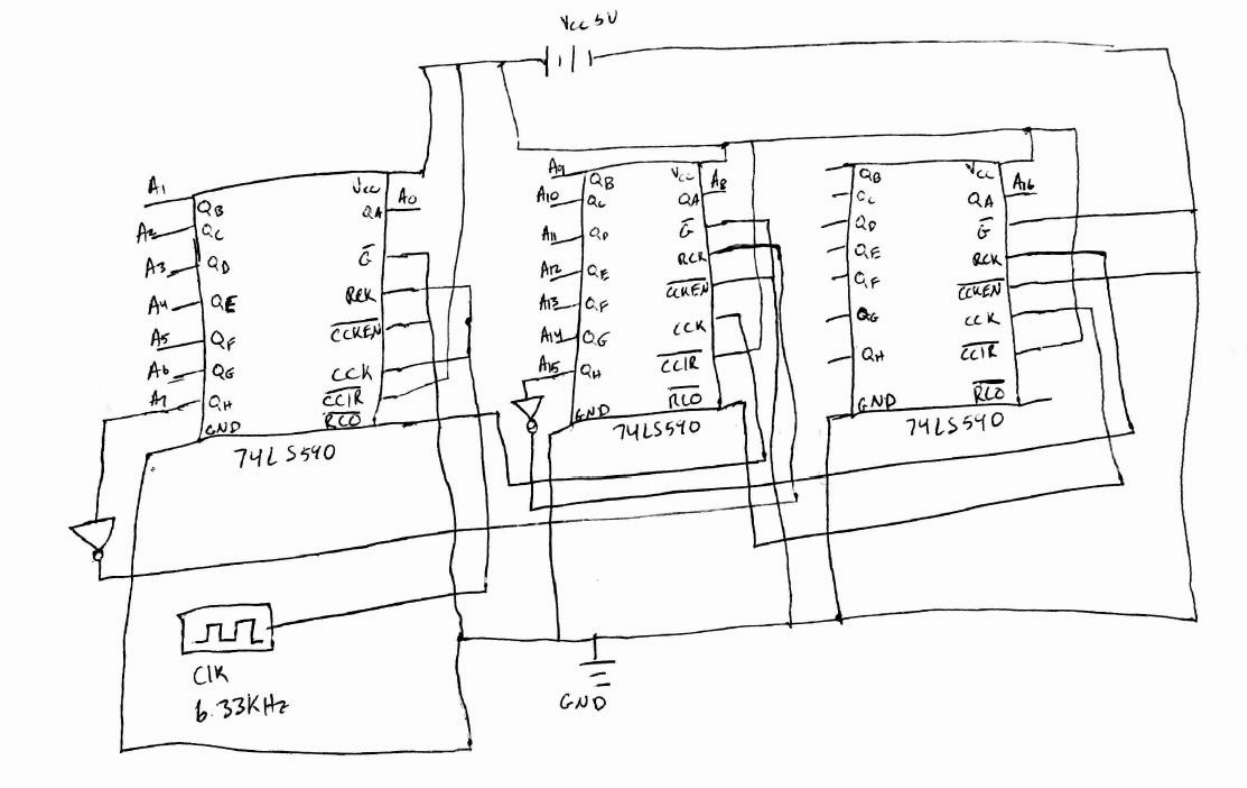

Figure 2:Schematic with 9bit counters to achieve 17-bit counter

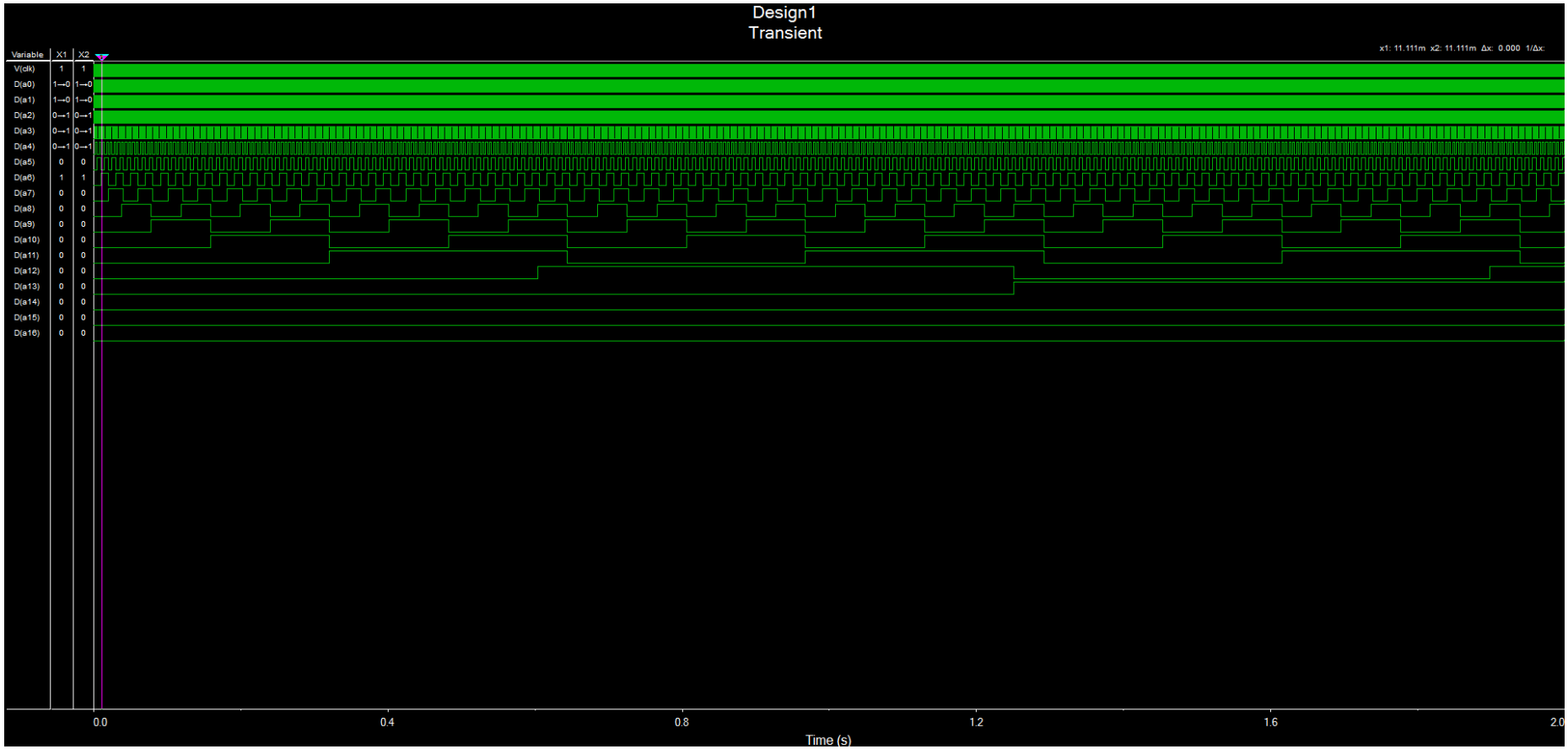

Figure 2: Multisim output of 17-bit Counter all bits

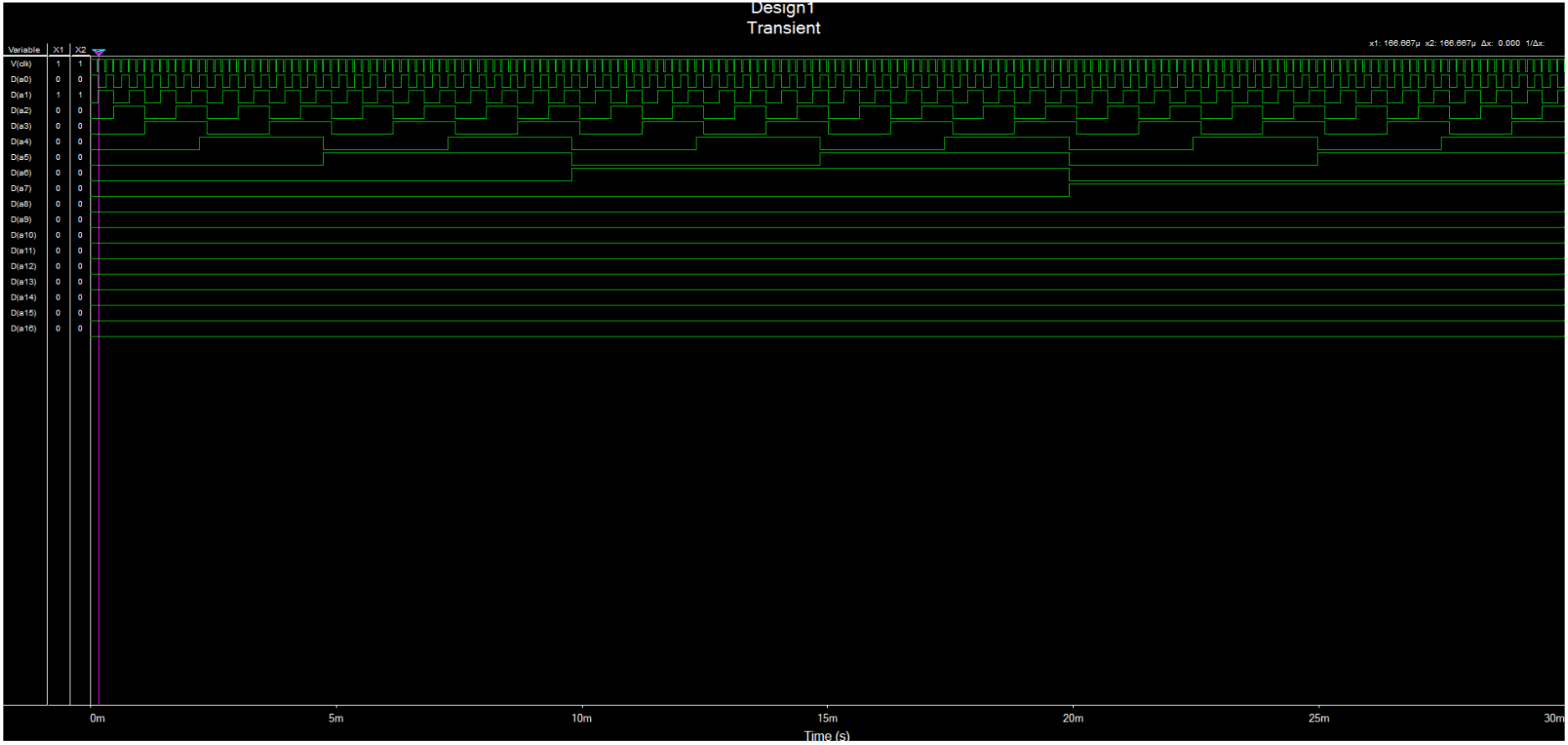

Figure 3: Multisim 17-bit counter bits 7 - 0

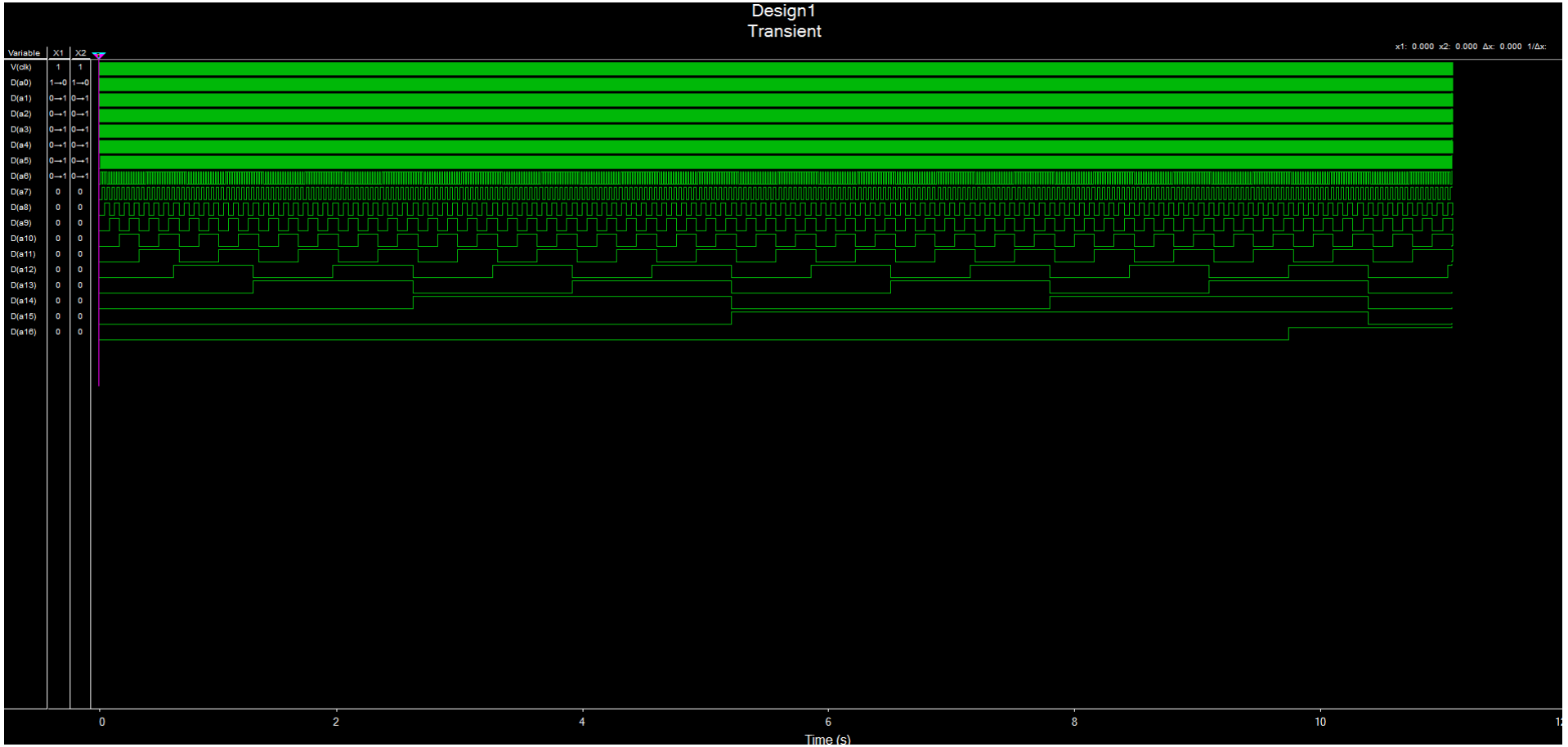

Figure 4: Multisim 17-bit Counter bits 16-8

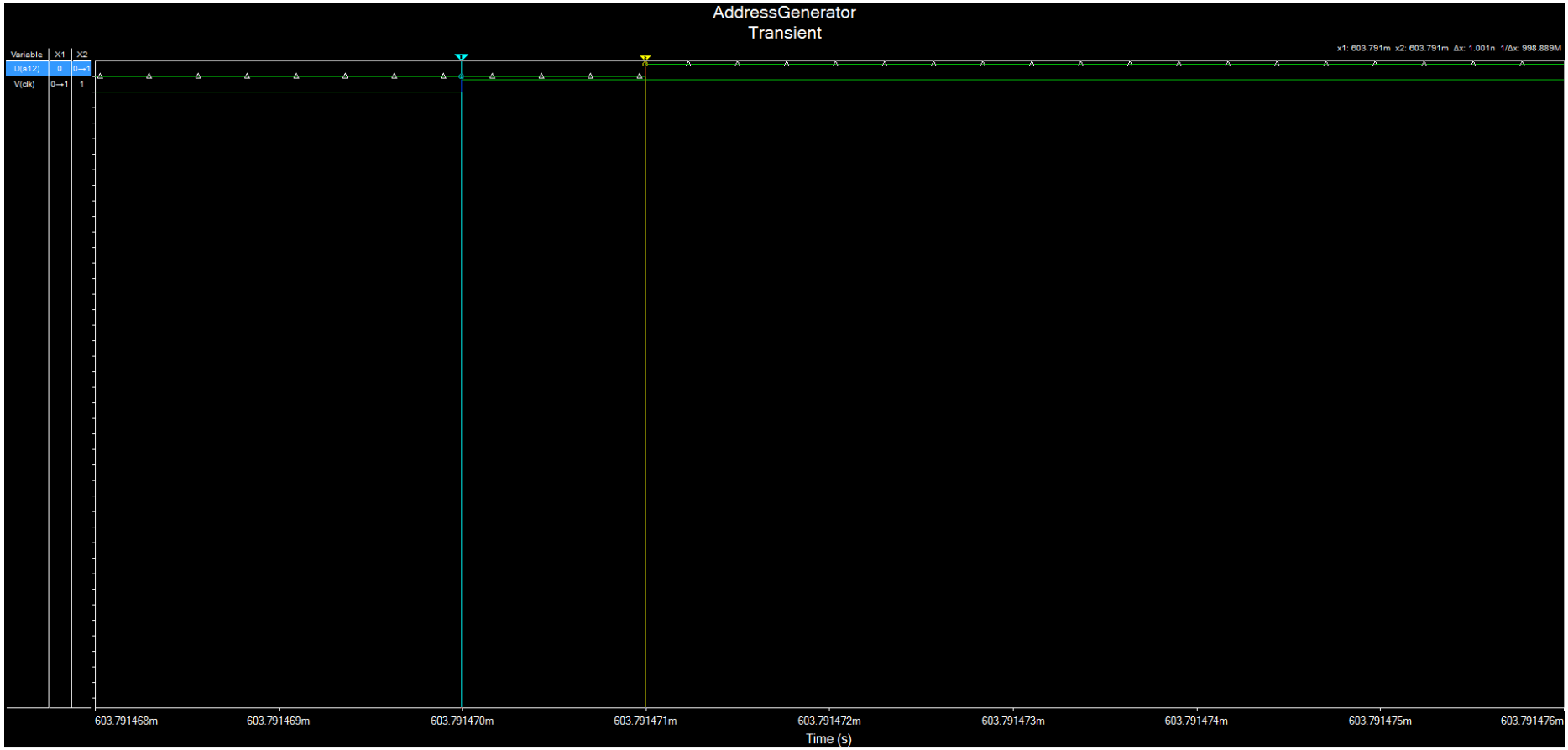

Figure 6: Multisim bit A12 Time high to low Delay, 1.001 ns

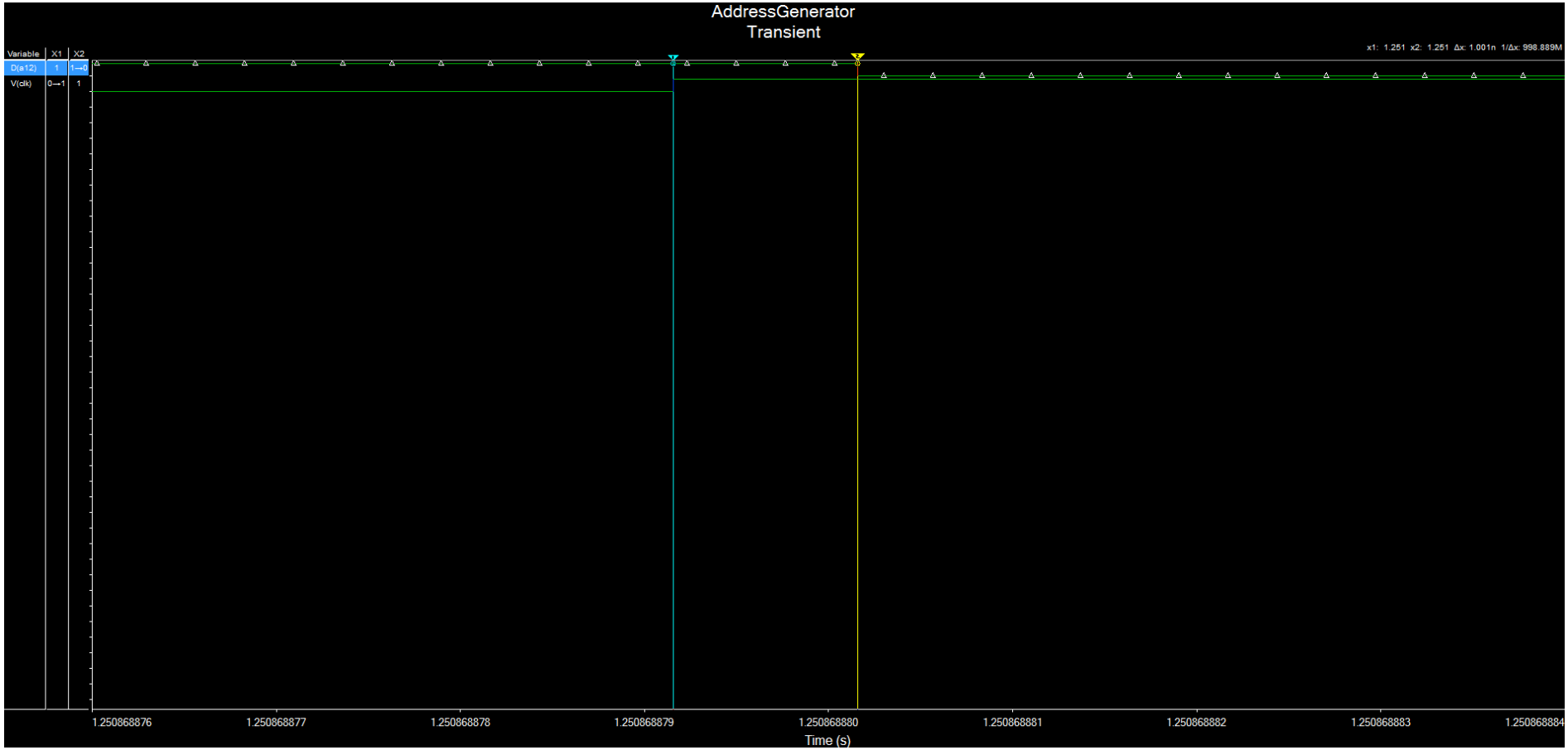

Figure 5: Multisim bit A12 Time high to low Delay, 1.001 ns

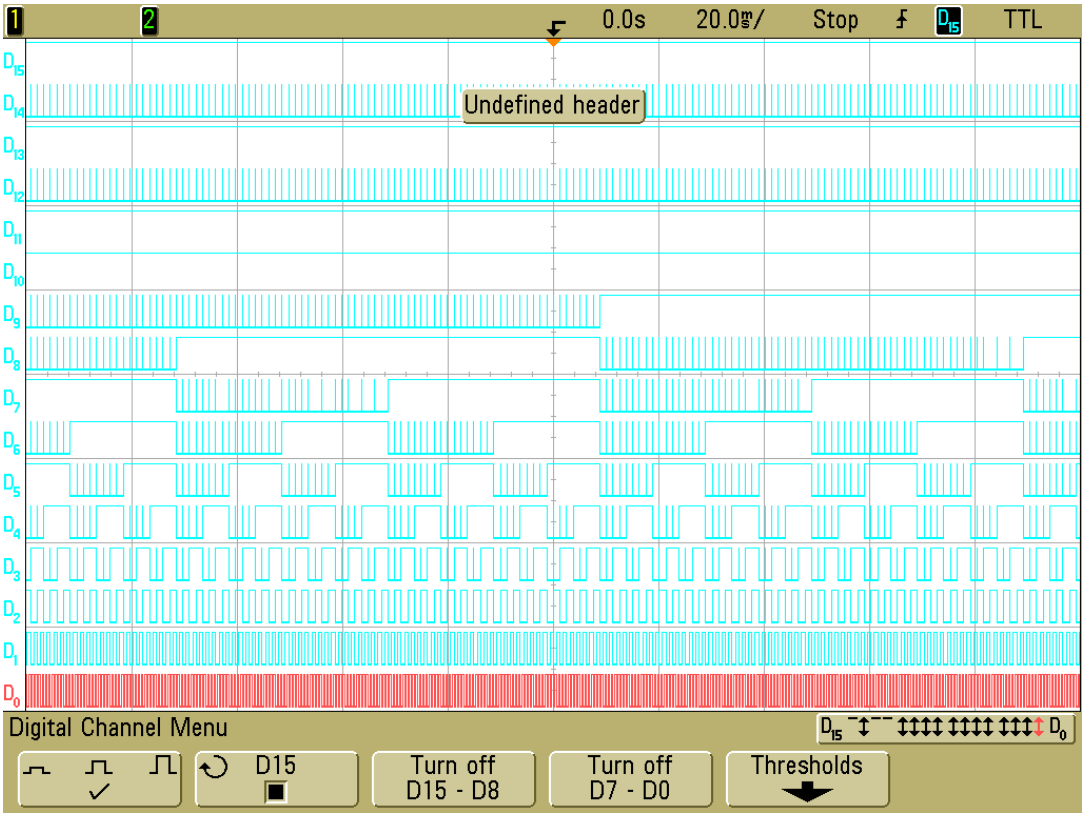

Figure 6: Output of 17-bit counter built on Data Acquisition Board

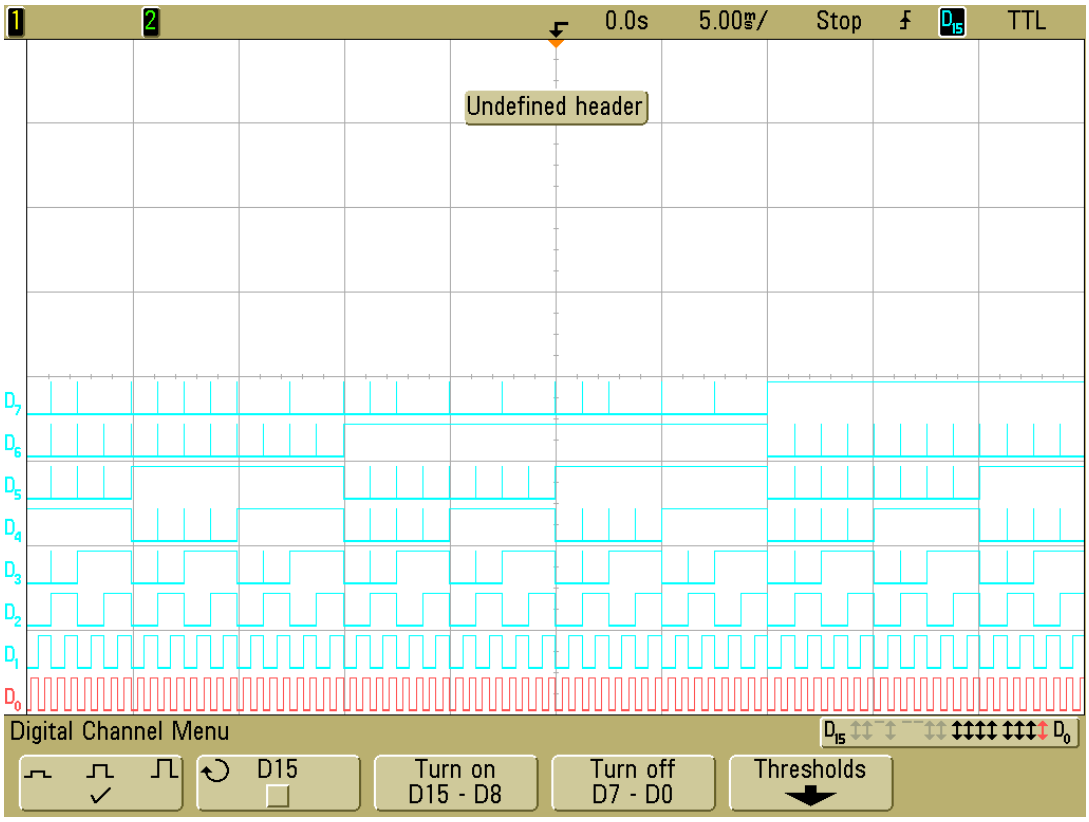

Figure 7: Output of 17-bit counter, bits 7 - 0

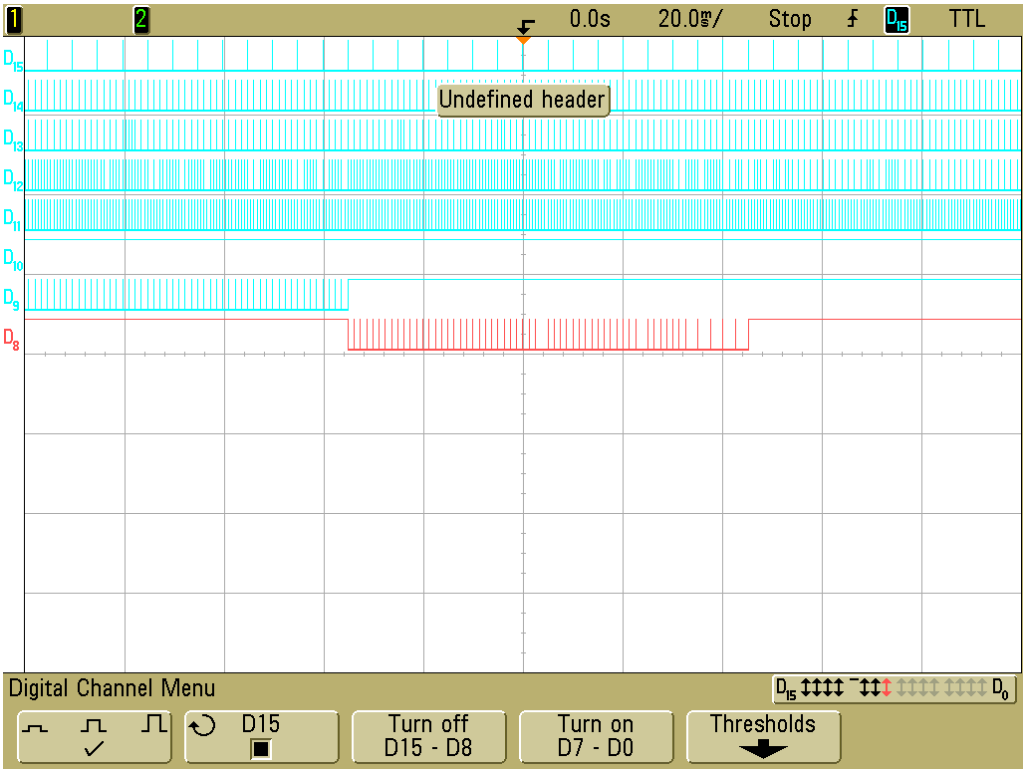

Figure 8: Output of 17 bit counter, bits 16 - 9

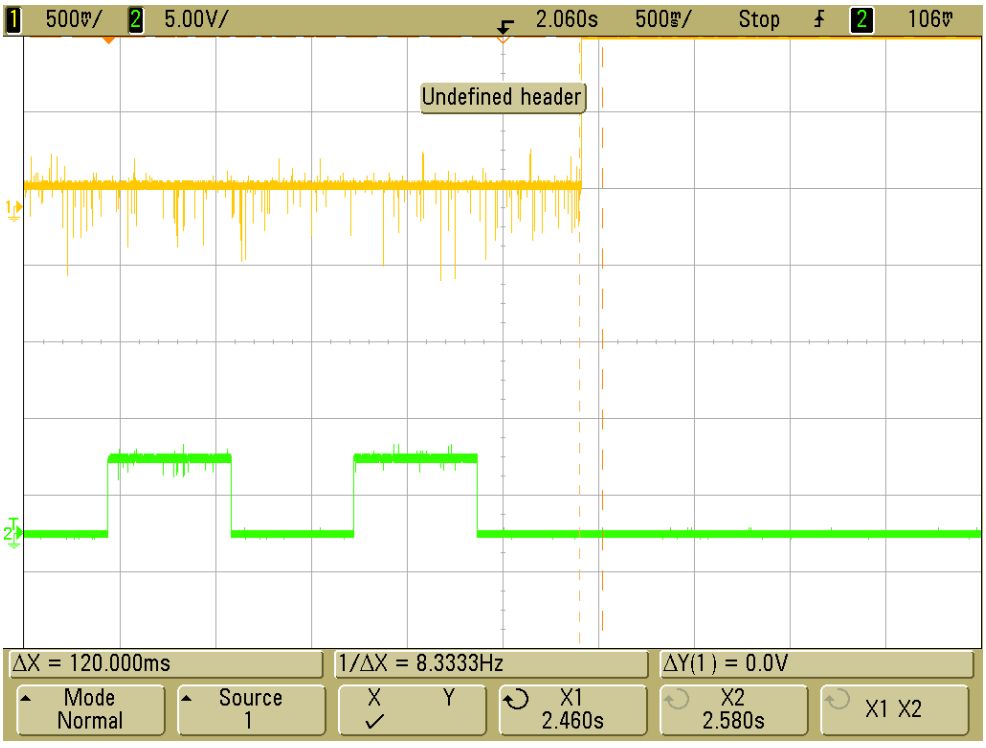

Figure 9:T_{LH} Delay of bit 12 of 17 - bit counter, 120 ms

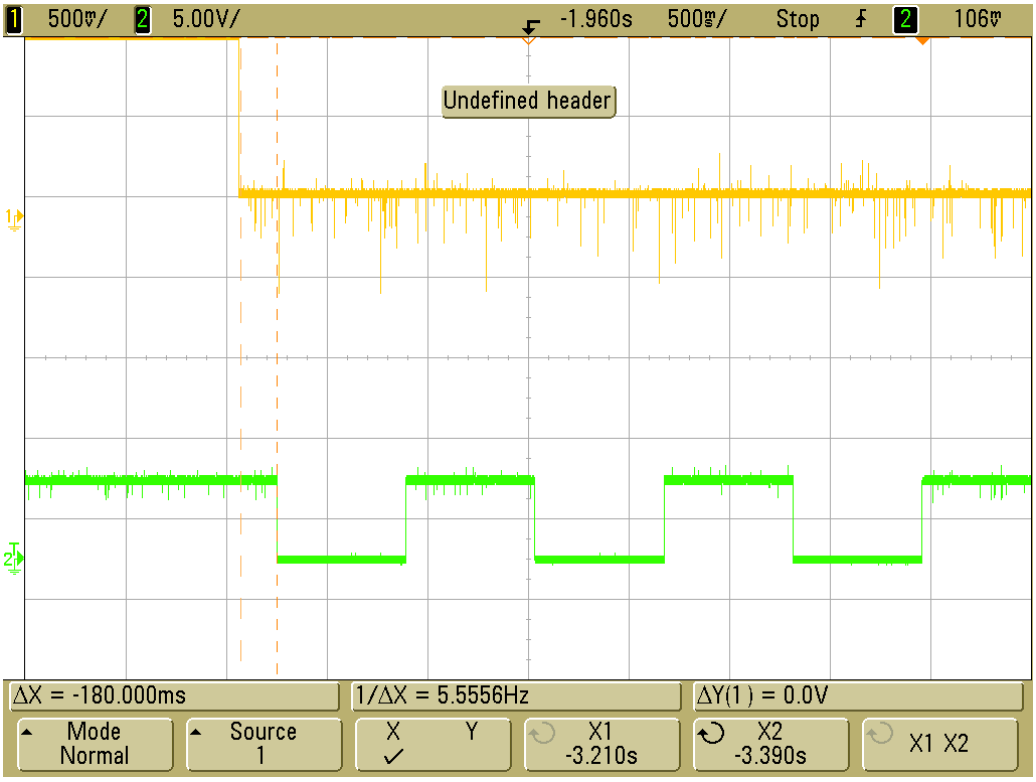

Figure 10: THL Delay of bit 12 of 17-bit counter, 180 ms

Table 1: Comparison of Propagation Delay of Simulation vs Hardware

Propagation Delay				
Bit Measured	Simulation T_{HL}	Simulation T_{LH}	Hardware T_{HL}	Hardware T_{LH}
A12	1.001 ns	1.001 ns	180 ms	120 ms

Explanation

In order to design the 17-bit cascading counter, three 74LS590 8 bit counters needed to be connected. This was achieved by routing the Ripple Carry Out pin (9) to the clock pin (11) of the next counter do to the design contracts a not gate from the first to the second and the second to the third counter needed to be connected to achieve correct count. In the simulation, this was not needed the 8-bit counter used in the hardware implementation was not available in Multisim. Figure 1 shows the 17-bit counter by using 74LS161 4-bit counters. Using the 6.33 kHz clocked used in the lab up until now.

The Multisim simulation is shown in Figures 3 through Figures 5. The simulation correctly shows the system counting, which proves that the memory addressing system will achieve the necessary addressing for the RAM. The simulation also allowed the measurement of the propagation delay of each signal being applied. The propagation delays of the 12^{th} bit was measured and can be seen in Figures 6,7 as seen in Table 1.

After the simulation was completed the hardware implementation was built. The hardware design with the 8-bit counter as mentioned before was accomplished by implementing a not gate before the next 8 bit counter starts counting in order to assure the counting of the bits our correct. Since the schematic for the 8-bit counter was not done Multisim Figure 2 shows the drawn schematic with the 8-bit counter. Figures 9 through 10 shows the results captured using the logic analyzer. Due to threshold issue the outputs seem to be reading some noise. This was fixed by applying a higher user threshold to the scope to 2.55 V which removed the noise from the output. The propagation delay was next measured on the same bit that was measured during the simulation bit 12 was also measured for the hardware implementation the measurement can be seen in Figures 11,12 and also shown in Table 1.

The last part of the lab asked to set up a control for the pause and playback system, allowing the counter to be manipulated. CCKEN (12) pin was wired to the output of the state machine to disable and enable the clock when the button was pressed. Using the SPDT button a reset was also wired to the RAM allowing the counting to be reset.

Table 1 compares the simulation and the theoretical propagation delays. Since there was different competes used between hardware and simulation the error margins will be off by a higher margin but the system operation was tested and verified. In all, the objective of the lab was achieved and the lab was a success.