





FIGURE 3.68 Example of CRC encoding.

FIGURE 3

Clock  
 0  
 1  
 2  
 3  
 4  
 5  
 6  
 7

$i(x) =$

The final step in the encoding procedure obtains the binary codeword  $b(x)$  by adding the remainder  $r(x)$  from  $x^{n-k}i(x)$ :

$$b(x) = x^{n-k}i(x) + r(x). \quad (3.53)$$

Because the divisor  $g(x)$  had degree  $n - k$ , the remainder  $r(x)$  can have maximum degree  $n - k - 1$  or lower. Therefore  $r(x)$  has at most  $n - k$  terms. In terms of the previously introduced register of length  $n$ ,  $r(x)$  will occupy the lower  $n - k$  positions. Recall that the upper  $k$  positions were occupied by the information bits. We thus see that this encoding process introduces a binary polynomial in which the  $k$  higher-order terms are the information bits and in which the  $n - k$  lower-order terms are the cyclic redundancy check bits. In the example in Figure 3.68, the division of  $x^3 i(x)$  by  $g(x)$  gives the remainder polynomial  $r(x) = x$ . The codeword polynomial is then  $x^6 + x^5 + x$ , which corresponds to the binary codeword  $(1, 1, 0, 0, 0, 1, 0)$ . Note how the first four positions contain the original four information bits and how the lower three positions contain the CRC bits.

In Figure 3.66 we showed that in normal division dividing 122 by 35 yields a quotient of 3 and a remainder of 17. This result implies that  $122 = 3(35) + 17$ . Note that by subtracting the remainder 17 from both sides, we obtain  $122 - 17 = 3(35)$  so that 122 - 17 is evenly divisible by 35. Similarly, the codeword polynomial  $b(x)$  is divisible by  $g(x)$  because

$$b(x) = x^{n-k}i(x) + r(x) = g(x)q(x) + r(x) + r(x) = g(x)q(x) \quad (3.54)$$

where we have used the fact that in modulo 2 arithmetic  $r(x) + r(x) = 0$ . Equation (3.54) implies that all codewords are multiples of the generator polynomial  $g(x)$ . This is the pattern that must be checked by the receiver. The receiver can check to see whether the pattern is satisfied by dividing the received polynomial by  $g(x)$ . If the remainder is nonzero, then an error has been detected.

The Euclidean Division algorithm can be implemented using a feedback shift-register circuit that implements division. The feedback taps in this circuit are determined by the coefficients of the generator polynomial. Figure 3.69 shows the division

The same division circuit.

The final remainder is the same as the remainder in step 3, corresponding to the quotient term and the example, contains a "1," a polynomial at any given of the register contains the same division

corresponds to the three columns in the highest order of the polynomial: the circuit for the generator

Table 3.7 gives the CRC-12 and the CRC-16 and used in the HDLC LAN standards as in ATM networks of these generators been used in the

### 3.9.5 Standards