Introduction to VLSI Design

ECE-C 471/ECE-C 571 — Syllabus
Fall 2016 — Lec: Monday 9:00-10:50am
Prof. Ioannis Savidis — Lab: Tuesday/Wednesday 9:00-10:50am

Course Information

Course Title:	Introduction to VLSI Design
Course Type:	Undergraduate/Graduate cross listing (CRN: 12058/13056)
Credits:	3 credits
Meeting Locations:	Lectures: Randell 121
	Laboratory: Bossone 605

Instructor and TA Information

Instructor:	Prof. Ioannis Savidis
Email:	isavidis@coe.drexel.edu
Office:	Bossone 610
Office Hours:	Tuesday, 11:00am-1:00pm or by appointment
Teaching Assistant:	Mr. Shazzad Hossain
Email:	md.shazzad.hossain@drexel.edu
Office:	Bossone 304
Office Hours:	Thursday, 10:00am-12:00pm
Teaching Assistant:	Mr. Vaibhav Venugopal Rao
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Office:	Bossone 333
Office Hours:	Friday, 10:00-12:00pm

Intended Audience

This course is intended for **senior-level ECE undergraduate students** and **graduate students**. The workload for graduate and undergraduate students will differ, and the two groups will be evaluated independently.

Prerequisites

Knowledge of digital logic design (**ECE 200**) and introductory electronics (**ECE-L 301-302**) is required. Previous exposure to transistors and semiconductor devices would be useful but not required. These introductory topics will be discussed in early stages of the course to provide the necessary technical background to all students from EE and CE.

Course Description

This is an introductory course in the field of *Very Large Scale Integration (VLSI) circuit and systems design*. An understanding of VLSI integrated circuits is achieved through circuit design and analysis. This course focuses exclusively on digital CMOS VLSI circuit and systems design, although some topics on mixed-signal circuits are also addressed.

The course begins with a review of CMOS transistor operation and semiconductor manufacturing processes. Logic design with CMOS transistors and circuit families is described. Specifically, layout, design rules, and circuit simulation is addressed as pertaining to custom VLSI design principles.

Learning Goals

By the end of the course, students will:

- Understand the basic concepts of modern VLSI circuit design by studying logic design, physical structures, and fabrication of semiconductor devices.
- Analyze and design static and dynamic CMOS digital circuits.
- Understand the functions and the properties of CMOS devices, combinational gates, and sequential circuits.
- Develop a thorough understanding of the static and dynamic characteristics (including delay, power, noise immunity, density) of various MOS based logic families (CMOS, pass transistor, domino).
- Optimize a digital circuit with respect to different quality metrics such as cost, speed, power dissipation, and reliability.
- Understand the interface between logic and electronics through analysis of electrical and design characteristics of transistors and gates for high-performance integrated circuits.
- Analyze the role of computer-aided design tools (SPICE and Cadence-Layout and simulation) in automating the design flow, resulting in increased productivity in VLSI systems design.
- Investigate the relationship between semiconductor technology, transistors and architecture, while addressing all levels of the hierarchy in the VLSI system design flow.
- Learn cooperative team building skills through homework and laboratories with the goal of applying design principles to minimize certain objective functions while meeting other design constraints for a functional circuit block.
- Develop skills for transistor-level analysis and design of simple and complex logic gates such as inverters, NOR, and NAND gates.
- Compare and contrast between different logic styles and tradeoffs to make informed decisions on when and where each logic style benefits (or impedes) overall circuit performance.
- Analyze the effect of interconnect parasitics on circuit performance.
- Understand important future trends in large-scale integrated circuit design, including manufacturing restrictions and barriers to device scaling.

Course Structure

Laboratory:	Once a week for 2 hours, eight (8) assignments
Exam(s):	Two (2) exams, one midterm and a final examination.
Homework(s):	Up to four (4) homework assignments.
Project(s):	*None*

This is a senior level undergraduate and graduate level class. The evaluation criteria is adjusted according to the academic level of the student. The evaluation process includes an analysis of the quality of individual work as well as participation in group projects (homework and lab) and lectures. The final grade will be calculated as follows:

Final exam	35%
Midterm exam	25%
Homework(s)	10%
Lab assignment(s)	30%
Total	*100%*

A mix of individual and student paired homework will be assigned. Homework assignments must be submitted at the beginning of class on the day they are due. Homework submitted more than three days late will not be graded. Late homework is penalized 15% per day until the third day (days are considered at noon). All requests for a re-grade must be submitted in writing within a week of the assignment being returned. No assignment will be re-graded after one week. Please let me know immediately if I incorrectly added your score.

The midterm exam is an individual, in-class exam tentatively scheduled for week 5 of the quarter. The final exam is also an *individual*, in-class exam tentatively scheduled for exam week. All exams must be taken at the scheduled time unless a previous arrangement (with a good reason) has been made with the instructor. Good reasons include medical conditions, family emergencies, and religious observation.

Note that this course is cross-listed as a graduate level course. Graduate and undergraduate course work *differs*, and students are evaluated *independently*. Graduate students are assigned more questions on the both homeworks and examinations.

The instructor and the TAs will provide feedback on any assignment submitted on time within two weeks after the submission deadline. For late submissions, feedback will be provided within two weeks from the date of submission. For laboratory work that was started (and worked on) during laboratory hours, immediate feedback will be provided by the laboratory instructor (TAs and/or instructor). There will be minimal to no feedback during the laboratory hours on laboratory assignments assigned during previous weeks. Feedback provided during laboratory sessions typically consists of corrections to student work and personal instruction. Feedback outside the laboratory hours typically includes a repeat of the instructions given during the laboratory session for the given laboratory assignment and resolving potential system errors (software problems, account problems, etc.), but not correction of errors in student work.

The Academic Policies set by the Drexel University Office of the Provost dictates the scale of letter grades as pertaining to grade point average (http://www.drexel.edu/provost/policies/grades.asp). The percentages used to assign these grades are listed below.

Letter	Grade Percentage
A+	97-100%
A	93-96.9%
A-	90-92.9%
B+	87-89.9%
B	83-86.9%
B-	80-82.9%
C+	77-79.9%
C	73-76.9%
C-	70-72.9%
D+	67-69.9%
D	63-66.9%
F	Below 63%

The instructor reserves the right to adjust the grade percentages (e.g. based on the distribution of grades) to accommodate non-standard (low or high) distributions.

Lectures

Lecture is a time for individual and group learning. Distractions during class reduce the overall quality of academic growth. Cell phone use is therefore prohibited during lecture. All cell phones must be placed in silent mode. You should not be talking, web-surfing, or texting on your phone during class. If you need to use your phone in any way, please leave the classroom.

Laptops are permitted during lecture for the explicit use of note taking or searching for additional information on a topic of discussion. Laptop use in class is a privilege. If the use of your laptop becomes a distraction to other students, laptops will be banned from use.

Class Website

We will use Drexel's **Blackboard Learn** course management website for this class. I will mail you important information regarding the class through this system. Please make sure you setup the system to forward BB/Learn emails to an account you check regularly. Homework, homework solutions, supplemental materials, etc. will be posted on the main course page.

If you want to email me or the TAs, please do so at the email addresses listed above. This is preferred to emailing us from within Blackboard Learn.

Attendance Policy

You are expected to attend each class punctually and remain for the entire class period. You need to inform the instructor in advance if you expect to miss a class or leave the course before the end of the semester. If you miss class your absence will be excused by the instructor only if a valid doctors certificate or other evidence is submitted. You remain responsible for the work associated with the class you missed, even if your absence has a valid reason.

A 5% reduction in a student's overall quarterly score will be assessed for every three days of unexcused absence. Please make sure to attend each class as a role call will be made at the beginning of each lecture period.

Class Withdrawal

A student may withdraw from the course at any time during the term, but before the deadline established in the University Academic Calendar. A discussion with the instructor is advised before a withdrawal is undertaken.

Academic Dishonesty

Cheating in any form is not tolerated, nor is assisting another person to cheat. The submission of any work by a student is taken as a guarantee that the thoughts and expressions in it are the students own except when properly credited to another. Violations of this principle include giving or receiving aid in an exam or where otherwise prohibited, fraud, plagiarism, the falsification or forgery of any record, and any other deceptive act in connection with academic work. Plagiarism is the representation of anothers words, ideas, programs, formulae, options or other products of work as ones own work from others, since it is often not possible to determine who the originator or the copier was. Such offense will result in a failing grade "F".

Textbook

The required textbook and additional reference textbooks are listed below. The additional textbooks provide additional information on VLSI design and are quite useful.

Required Textbook: N. Weste and D. M. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective,* Addison-Wesley, 4^{th} ed., 2011.

Additional Textbooks:
1. S. M. Kang, Y. Leblebici, and C. Kim, *CMOS Digital Integrated Circuits Analysis and Design,* McGraw-Hill Inc., 4^{th} ed., 2015.
2. R. J. Baker, *CMOS Circuit Design, Layout, and Simulation,* John Wiley & Sons, 3^{rd} ed., 2011.
3. J. M. Rabaey, A. Chandrakasan and B. Nikolic, *Digital Integrated Circuits*, Prentice Hall, 2^{nd} edition, 2003.
4. D. A. Hodges, H. G. Jackson, and R. A. Saleh, *Analysis and Design of Digital Integrated Circuits In Deep Submicron Technology,* McGraw-Hill Inc., 3^{rd} ed., 2004.

Laboratory

Weekly design and simulation assignments using Cadence CAD tools are completed. Specifically, the Cadence Virtuoso toolset is used for schematic capture, simulation, layout, and pre- and post-layout analysis. Students will use the Cadence Analog Artist environment for circuit simulation and analysis, and Diva/Assura for design rules checking (DRC) of layouts.

Weekly assignments will include:

- CMOS Inverter
- CMOS NAND and NOR gates
- CMOS XOR and MUX gates
- Registers: Latch and Flip-flop design
- Interconnect Analysis
- Data paths: Simple sequential circuits (i.e. 2-bit adder with storage)

Tentative Schedule

Week	Lecture	Chapter	Lab	Homework
1	Introduction to VLSI Systems	1		
2	MOS Transistor Theory	2	CMOS inverter design	HW#1
3	CMOS Processing Technology	3		
4	Combinational Circuit Design	9	Inverter Chain	HW#2
5	Delay	4	CMOS NAND and NOR	
6	Power	5	***(Midterm Exam)***	
7	Interconnect	6	CMOS XOR and MUX	HW#3
8	Robustness	7	The Wire	
9	Circuit Simulation	8	2-bit Adder	HW#4
10	Sequential Circuit Design	10	D Latch and D-FF	
11	Datapath Subsystems	11		
12	**Final Examination** (Date TBA)			

Academic Policies

The academic policies defined by the Office of the Provost are upheld for this course. The complete list of policies (academic and otherwise) can be found at the following url: http://www.drexel.edu/policies. Students should pay particular attention to the following policies:

Academic Integrity	http://www.drexel.edu/provost/policies/academic_dishonesty.asp
Course Drop Statement	http://www.drexel.edu/provost/policies/course_drop.asp
Disability Statement	http://www.drexel.edu/oed/disabilityResources/Overview/
Student Conduct and Community Standards	http://www.drexel.edu/studentaffairs/community_standards/studentHandbook/

Course Change Policy: The instructor reserves the right to change the course during the quarter at his discretion. All changes, if applicable, will be communicated to the students verbally during class or through Blackboard Learn Announcements. Every effort will be made to

1. Not change any course policy past the course withdrawal period.
2. Collect student feedback prior to implementing any course change.