

# Design Analysis and Simulation of 1 bit Arithmetic Logic Unit on different foundaries

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**Abstract—** In this paper an ALU has been designed and implemented using different foundaries like 45nm, 65nm and 90 nm. The performance of developed ALU has been analyzed and compared in terms of area and power using BSIM4 device model. The schematic of ALU circuit has been designed using DSCH 3.5 and its equivalent layout has been created using Microwind tool. It can be observed from simulation results that 45nm technology based ALU has shown area reduction ranging from 48 % to 75% with 65nm and 90nm technology and power reduction from 84% to 97.9% as compared with 65nm and 90nm based technologies.

**Index Terms**—ALU, delay, logic gate, power, Power dissipation.

## I. INTRODUCTION

The demand for increasing speed and low power dissipation elicits numerous research efforts with the increasing demand of handy devices driven by batteries. Advancement in VLSI technology has allowed following Moore's law [1] for doubling component density on a silicon chip after every three years. Though MOS transistors have been scaled down, augmented interconnections have limited circuit density on a chip. Microprocessors are essential to many of the products we use everyday such as radio, home appliances and of course, computers. Furthermore, the size of transistor is limited by hot-carrier phenomena and increase in electric field that lead to degradation of device performance and device lifetime [2]. Transistors are the main components of microprocessors. At their most vital level, transistors may seem very simple but their development actually required many years of meticulous research. Major challenge is microscopic issues as ultra high speed power dissipation and supply rail drop growing importance of interconnect noise, crosstalk reliability, manufacturing clock distribution. Low power also leads to smaller power supplies, less exclusive batteries, and enables products to be powered by signal lines (such as fire alarm wires) lowering the cost of the end result. The arithmetic logic unit (ALU) is the core of a CPU in a computer. The adder cell is the basic unit of an ALU. The constrictions the adder has to satisfy are area, power and speed requirements. Some of the conventional types of adders are ripple-carry adder, carry-lookahead adder, carry-skip adder and Manchester carry chain adder [3]. Macroscopic issues time to market design complexity (millions of gates) high levels of abstraction design for test reuse and IP portability.

## II.1 bit – ALU

The digital function that implements the micro-operations on the information stored in registers is commonly called an Arithmetic Logic Unit (ALU). The ALU receives the information from the registers and performs a given operation as specified by the control. A very simple ALU design is proposed to illustrate this principle. The control unit is made up of 4-1 multiplexer. The operation part consists of four kinds of operations listed as follows: and, or, addition and subtraction. The 'and' and 'or' operation are realized by using the basic logic gates. The addition and subtraction are realized using the ADDER user symbols as shown in Figure 1. A full adder could be defined as a combinational circuit that forms the arithmetic sum of three input bits [4]. A digital multiplexer made from MOS device

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selects one of the 4 operations results and directs it to a single output line. The full adder performs the computing function of the ALU. A full adder could be defined as a combinational circuit that forms the arithmetic sum of three key in or input bits. It consists of three inputs and two outputs as depicted in figure 5. Documenting the design of the ALU involves the designing of the Full Adder circuit. The Full Adder will have three inputs and two outputs. The three inputs consist of one bit for number A, one bit for number B, and a Carry-In. The outputs are the Sum and Carry-Out. The Sum is the totaling of A, B, and Cin. The Carry-Out will be used as the input into another ALU when we implement a multi-bit ALU using cascading. The ALU contains logical operators – AND, NOT, and PASS - as well as an Arithmetic operator - ADD. Make sure the carry out is active only during the ADD function. Control bits will specify which operation should be performed. Because this ALU will have four different operations, it is required to have two control bits to select which operation is to be performed [5]. Arithmetic functions for say resembling addition, subtraction, multiplication and division are some examples, which use adder as a main edifice or building block [6]. An arithmetic logic unit, or ALU (sometimes pronounced "Al Loo"), is a combinational network that implements a function of its inputs based on either logic or arithmetic functions. ALUs are at the heart of all computers as well as most digital hardware systems[7]. The arithmetic and logic unit (ALU) performs all arithmetic operations (addition, subtraction, multiplication, and division) and logic maneuvers. Logic operations test various conditions encountered during processing and allow for different measures to be taken based on the outcome. The data required to perform the arithmetic and logical functions are inputs from the designated CPU registers and operands. The ALU relies on fundamental items to perform its operations. An overall 1 bit ALU is depicted in Figure 5 which has 1 bit logical unit having AND and OR section figure 2, 1 bit adder section figure 3, and logic section of carry out bit figure 4. All these sections in combination decide which operation to be performed.

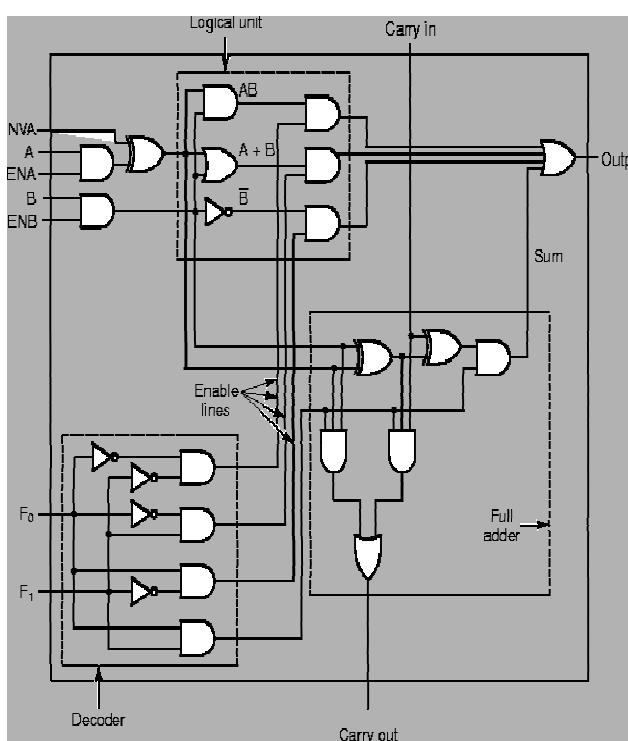


Figure 1: 1 bit ALU

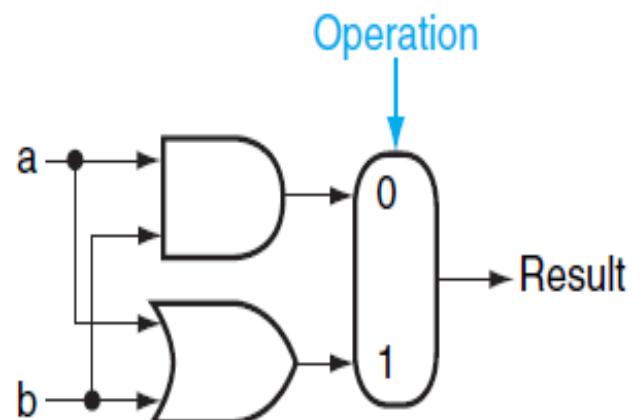


Figure 2: 1 bit logical unit for AND and OR.

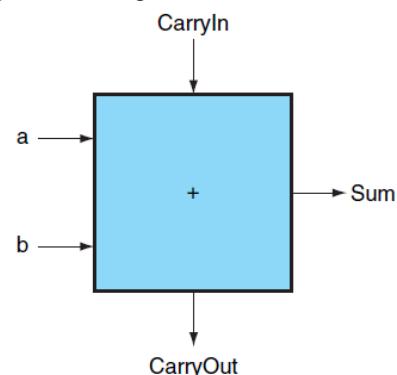


Figure 3: 1 bit adder

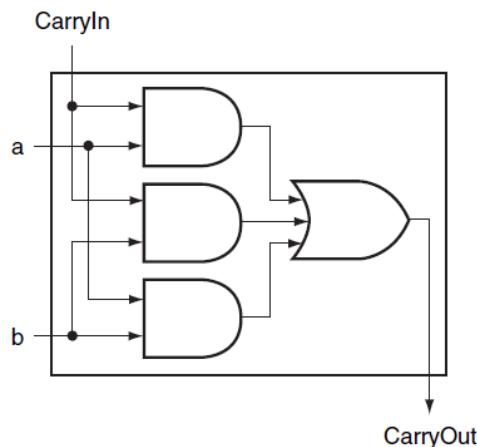


Figure 4: Logic of carry out bit.

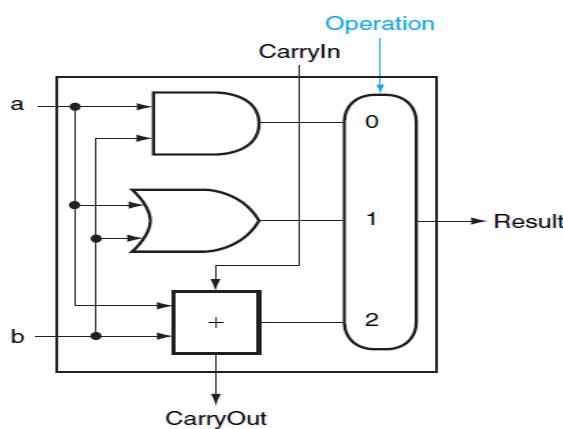


Figure 5: Overall 1 bit ALU

Table 1: ALU truth table

| ALU truth table |    | Select points | Result | Carry out      |
|-----------------|----|---------------|--------|----------------|
| F1              | F0 |               |        |                |
| 0               | 0  | Pass          | a      | 0              |
| 0               | 1  | Add           | a+b    | Carry from a+b |
| 1               | 0  | And           | a * b  | 0              |
| 1               | 1  | Not           | a'     | 0              |

Now drawing the Schematic diagram of 1 bit ALU using DSCH-3.5 EDA tool will result in the gate level implementation of the circuit as in Figure 6 and with simulation for some inputs on and off as in Figure 7. As in Figure 7 the red color shows that particular input has been pulled to logic '1'. Figure 8 and 9 will give the timing diagrams of the 1 bit ALU circuit with DSCH software showing the response of various inputs being on and off. The red light shows '1' and blue light shows '0'

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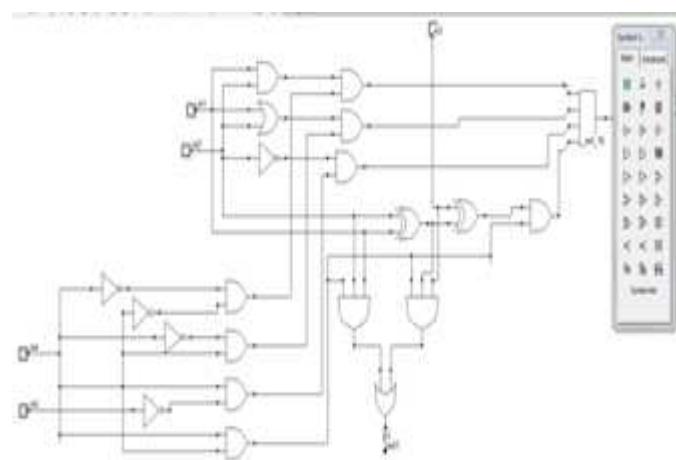


Figure 6: Schematic diagram of 1 bit ALU

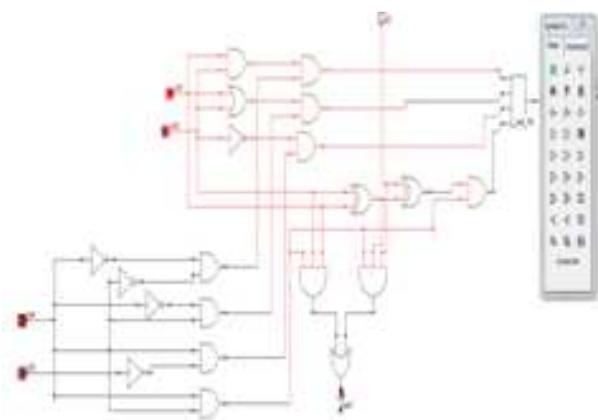


Figure 7: Schematic circuit with simulation.

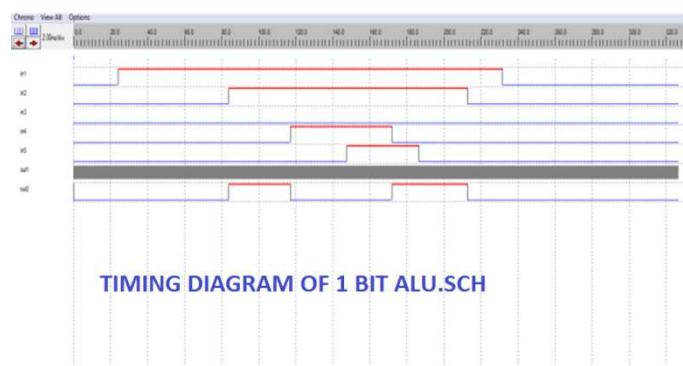


Figure 8: Timing diagram of 1 Bit ALU for Inputs and Outputs

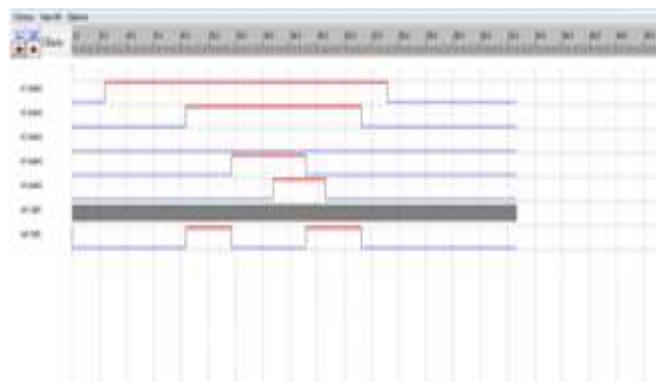


Figure 9 : Timing diagram from DSCH

Now we will compile this schematic diagram of 1 bit ALU in figure 3 using MICROWIND EDA tool to get the layout of the circuit along with the surface areas which is shown in Figure 10-15 with different channel length. Figure 16-18 will provide the analog simulation of the given layout which will give the power dissipation for the various channel lengths.

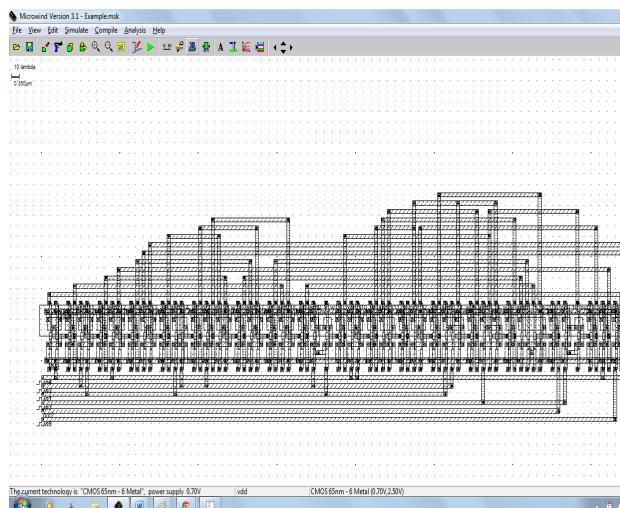


Figure 10: Layout of 1 bit ALU with 45 nm channel length

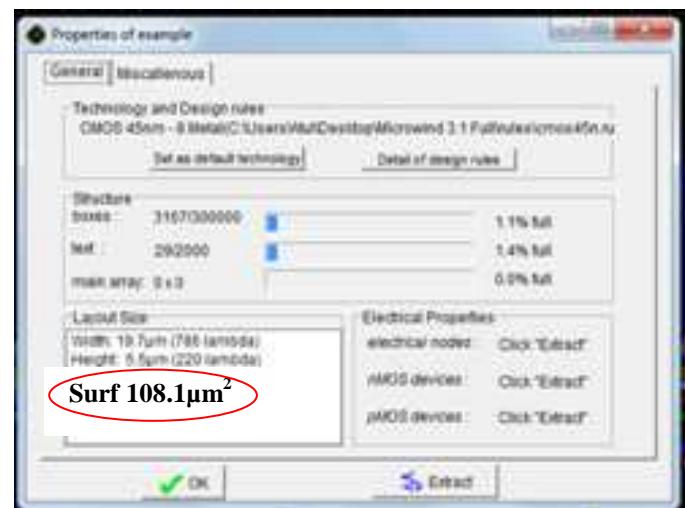


Figure 11: Surface Area of 45 nm channel length

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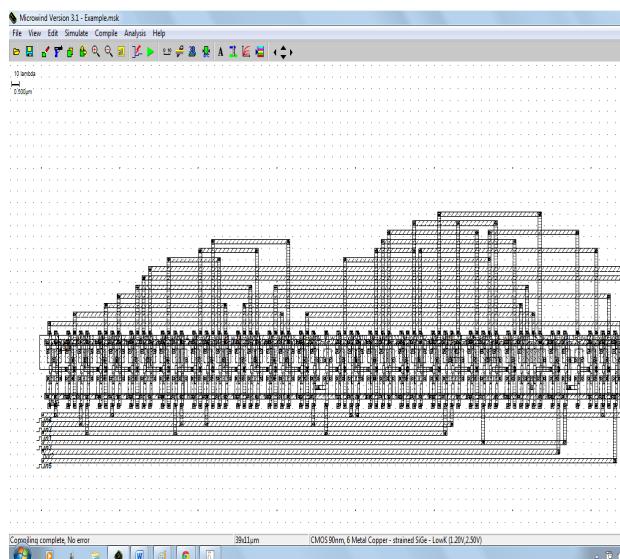


Figure 12: Layout of 1 bit ALU with 65 nm channel length

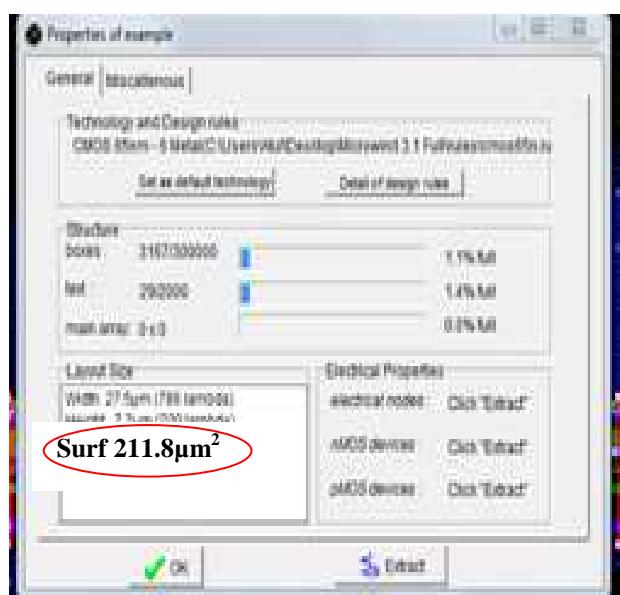


Figure 13: Surface Area of 65 nm channel length

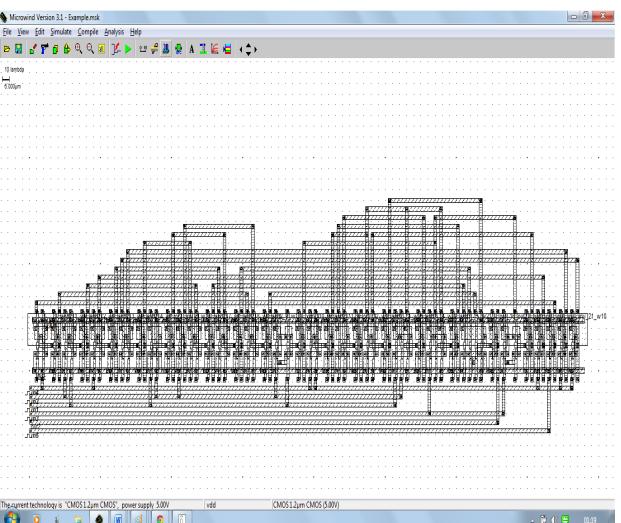


Figure 14: layout of 1 bit ALU with 90 nm channel length

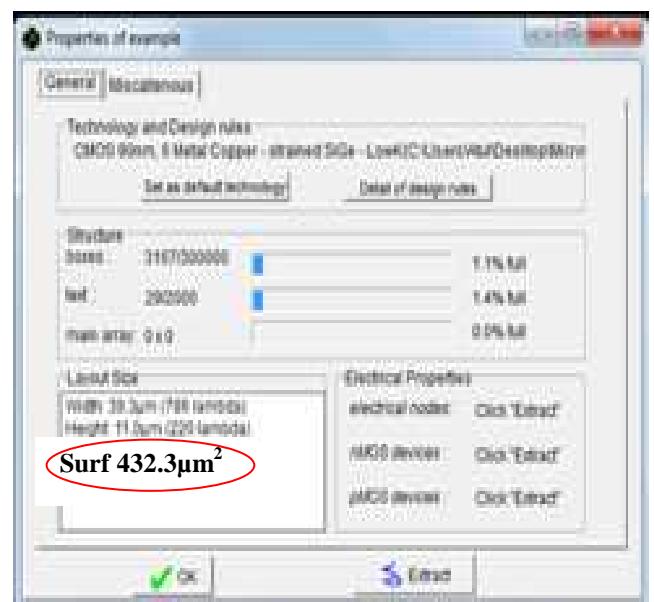


Figure 15: Surface Area of 90 nm channel length

### III. Device Models

SPICE provides a wide variety of MOS transistors models with various tradeoffs between complexity and accuracy. Level 1 and level 3 were historically important, but they are no longer adequate to accurately model very small modern transistors. BSIM model are accurate and are presently the most widely used. The SPICE level 1 is closely related to the Schokley model, enhanced with channel length modulation and the body effect [7]. The Berkeley Short-Channel IGFET Model (BSIM) is a very elaborate model that is widely used in circuit simulation. These use an enormous number of parameters to fit the behavior of modern transistors. BSIM4 model is widely used for gate leakage and other effects of very thin gates.

#### IV. Simulation Results

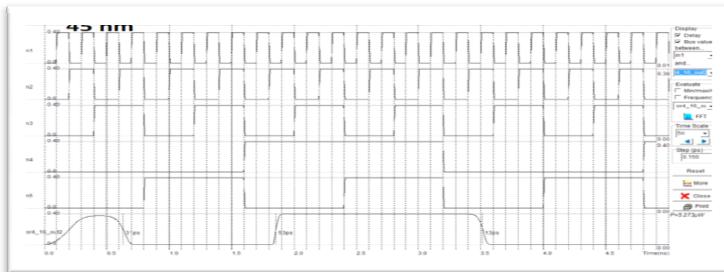


Figure 16: Analog Simulation of Power dissipation for 45nm

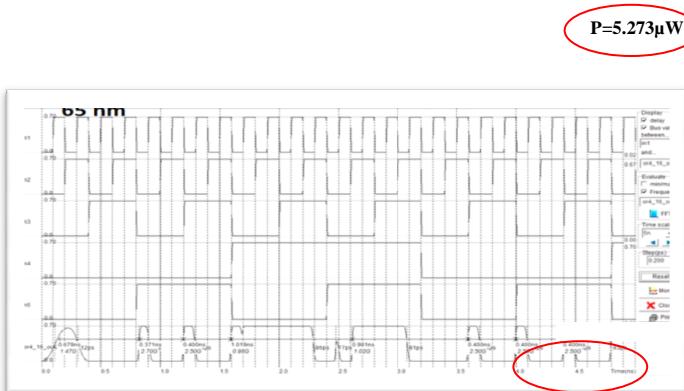


Figure 17: Analog Simulation of power dissipation for 65 nm

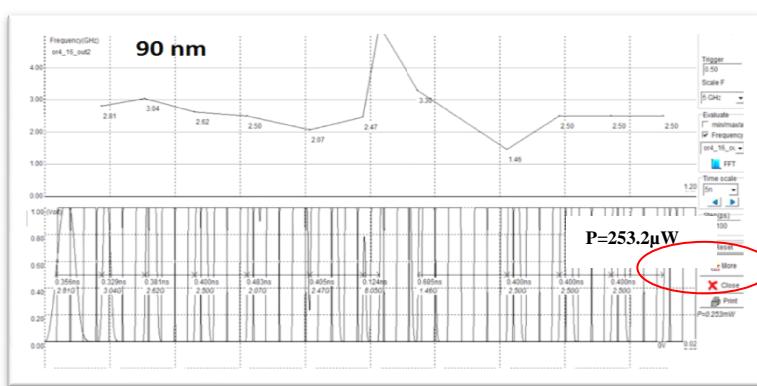


Figure 18: Analog Simulation of power dissipation for 90 nm

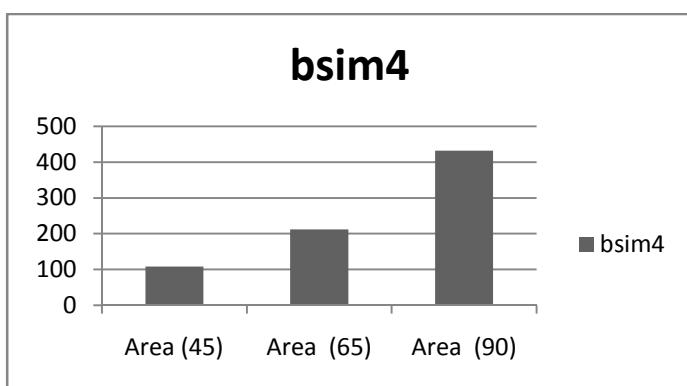
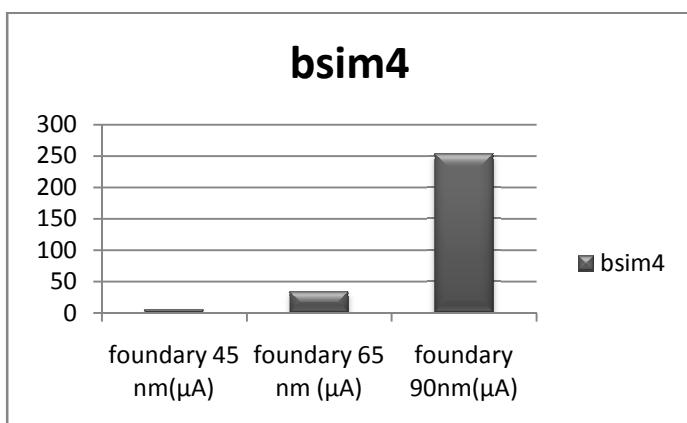
Table 2: Power dissipation of different channel lengths for BSIM4 model

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| foundaries | boundary<br>45<br>nm( $\mu$ W) | boundary<br>65 nm<br>( $\mu$ W) | boundary<br>90nm( $\mu$ W) |
|------------|--------------------------------|---------------------------------|----------------------------|
| bsim4      | 5.273                          | 33.885                          | 253.2                      |

Table 3 : Area of different boundaries for BSIM4 model

| Area  | Area<br>(45)             | Area<br>(65)             | Area<br>(90)             |
|-------|--------------------------|--------------------------|--------------------------|
| bsim4 | 108.1<br>$\mu\text{m}^2$ | 211.8<br>$\mu\text{m}^2$ | 432.3<br>$\mu\text{m}^2$ |



### V. Conclusions

As per the analysis the power consumption is minimum with the channel length of 45 nm for the BSIM4 model compared to that of BSIM4 model with channel length 90 nm. The  $I_{dd}$  average current is best for the BSIM4 model

with channel length as 90 nm. As the channel length decreases the average current decreases for all the device models. So there has to be a tradeoff between power dissipation and  $I_{dd}(\text{avg})$ .

## VI. Acknowledgement

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