

Lecture 8: SPICE Simulation

Outline

- ☐ Introduction to SPICE
- ☐ DC Analysis
- ☐ Transient Analysis
- ☐ Subcircuits
- ☐ Optimization
- ☐ Power Measurement
- ☐ Logical Effort Characterization

Introduction to SPICE

- ❑ **S**imulation **P**rogram with **I**ntegrated **C**ircuit **E**mphasis
 - Developed in 1970' s at Berkeley
 - Many commercial versions are available
 - HSPICE is a robust industry standard
 - Has many enhancements that we will use
- ❑ Written in FORTRAN for punch-card machines
 - Circuits elements are called *cards*
 - Complete description is called a SPICE *deck*

Writing Spice Decks

- ❑ Writing a SPICE deck is like writing a good program
 - Plan: sketch schematic on paper or in editor
 - Modify existing decks whenever possible
 - Code: strive for clarity
 - Start with name, email, date, purpose
 - Generously comment
 - Test:
 - Predict what results should be
 - Compare with actual
 - *Garbage In, Garbage Out!*

Example: RC Circuit

```
* rc.sp
* David_Harris@hmc.edu 2/2/03
* Find the response of RC circuit to rising input
```

```
*-----
* Parameters and models
*-----
```

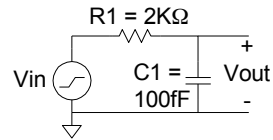
```
.option post
```

```
*-----
* Simulation netlist
*-----
```

```
Vin      in      gnd      pw1      0ps 0 100ps 0 150ps 1.0 1ns 1.0
R1        in      out      2k
C1        out      gnd     100f
```

```
*-----
* Stimulus
*-----
```

```
.tran 20ps 1ns
.plot v(in) v(out)
.end
```

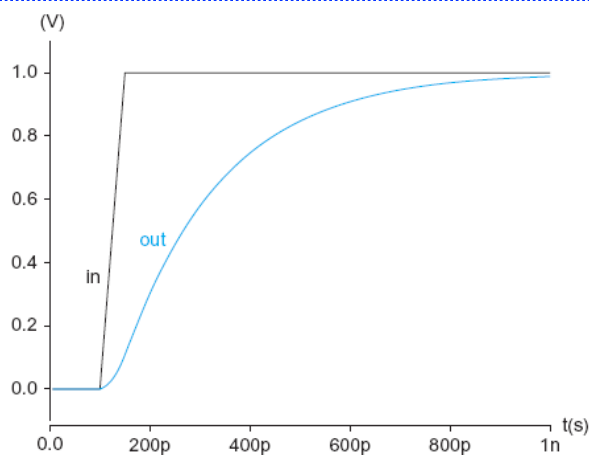


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Result (Graphical)



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Sources

☐ DC Source

vdd vdd gnd 2.5

☐ Piecewise Linear Source

vin in gnd pw1 0ps 0 100ps 0 150ps 1.0 1ns 1.0

☐ Pulsed Source

vck clk gnd PULSE 0 1.0 0ps 100ps 100ps 300ps 800ps

PULSE v1 v2 td tr tf pw per



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SPICE Elements

Letter	Element
R	Resistor
C	Capacitor
L	Inductor
K	Mutual Inductor
V	Independent voltage source
I	Independent current source
M	MOSFET
D	Diode
Q	Bipolar transistor
W	Lossy transmission line
X	Subcircuit
E	Voltage-controlled voltage source
G	Voltage-controlled current source
H	Current-controlled voltage source
F	Current-controlled current source

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Units

Letter	Unit	Magnitude
a	atto	10^{-18}
f	femto	10^{-15}
p	pico	10^{-12}
n	nano	10^{-9}
u	micro	10^{-6}
m	milli	10^{-3}
k	kilo	10^3
x	mega	10^6
g	giga	10^9

Ex: 100 femptofarad capacitor = 100fF, 100f, 100e-15

DC Analysis

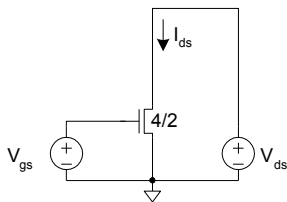
```

* mosiv.sp
*-----
* Parameters and models
*-----
.include '../models/ibm065/models.sp'
.temp 70
.option post

*-----
* Simulation netlist
*-----
*nmos
Vgs      g      gnd      0
Vds      d      gnd      0
M1       d      g      gnd      gnd      NMOS      W=100n  L=50n

*-----
* Stimulus
*-----
.dc Vds 0 1.0 0.05 SWEEP Vgs 0 1.0 0.2
.end

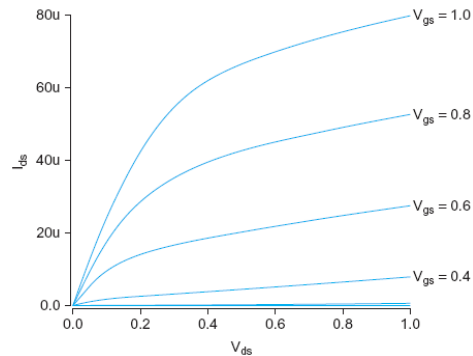
```



I-V Characteristics

□ nMOS I-V

- V_{gs} dependence
- Saturation



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MOSFET Elements

M element for MOSFET

Mname drain gate source body type

+ W=<width> L=<length>

+ AS=<area source> AD = <area drain>

+ PS=<perimeter source> PD=<perimeter drain>

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Transient Analysis

```

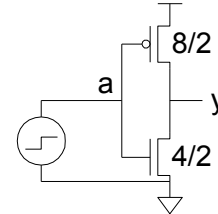
* inv.sp

* Parameters and models
*-----
.param SUPPLY=1.0
.option scale=25n
.include '../models/ibm065/models.sp'
.temp 70
.option post

* Simulation netlist
*-----
Vdd      vdd      gnd      'SUPPLY'
Vin      a        gnd      PULSE 0 'SUPPLY' 50ps 0ps 0ps 100ps 200ps
M1       y        a        gnd      gnd      NMOS    W=4    L=2
+ AS=20  PS=18  AD=20  PD=18
M2       y        a        vdd      vdd      PMOS    W=8    L=2
+ AS=40  PS=26  AD=40  PD=26

* Stimulus
*-----
.tran 0.1ps 80ps
.end

```



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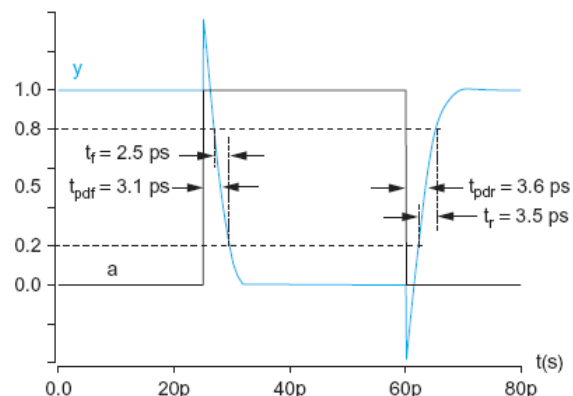
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Transient Results

□ Unloaded inverter

- Overshoot
- Very fast edges



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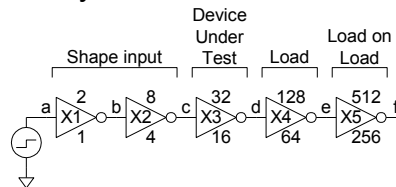
Subcircuits

❑ Declare common elements as subcircuits

```
.subckt inv a y N=4 P=8
M1 y a gnd gnd NMOS W='N' L=2
+ AS='N*5' PS='2*N+10' AD='N*5' PD='2*N+10'
M2 y a vdd vdd PMOS W='P' L=2
+ AS='P*5' PS='2*P+10' AD='P*5' PD='2*P+10'
.ends
```

❑ Ex: Fanout-of-4 Inverter Delay

- Reuse inv
- Shaping
- Loading



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F04 Inverter Delay

```
* fo4.sp
* Parameters and models
*-----
.param SUPPLY=1.0
.param H=4
.option scale=25n
.include '../models/ibm065/models.sp'
.temp 70
.option post

* Subcircuits
*-----
.global vdd gnd
.include '../lib/inv.sp'

* Simulation netlist
*-----
Vdd      vdd      gnd      'SUPPLY'
Vin       a       gnd      PULSE   0 'SUPPLY' 0ps 20ps 20ps 120ps 280ps
X1        a       b       inv      * shape input waveform
X2        b       c       inv      M='H' * reshape input waveform
```

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F04 Inverter Delay Cont.

```

X3      c      d      inv      M='H**2' * device under test
X4      d      e      inv      M='H**3' * load
x5      e      f      inv      M='H**4' * load on load

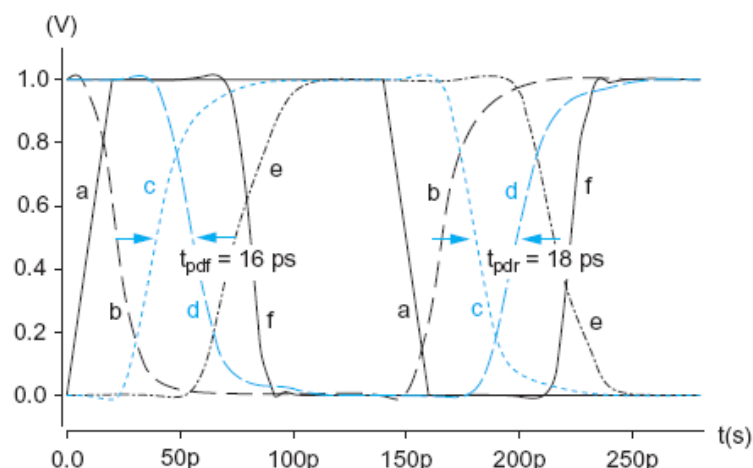
* Stimulus
*-----
.tran 0.1ps 280ps
.measure tpdr                                * rising prop delay
+   TRIG v(c)  VAL='SUPPLY/2' FALL=1
+   TARG v(d)  VAL='SUPPLY/2' RISE=1
.measure tpdf                                * falling prop delay
+   TRIG v(c)  VAL='SUPPLY/2' RISE=1
+   TARG v(d)  VAL='SUPPLY/2' FALL=1
.measure tpd param=(tpdr+tpdf)/2            * average prop delay
.measure trise                                * rise time
+   TRIG v(d)      VAL='0.2*SUPPLY' RISE=1
+   TARG v(d)      VAL='0.8*SUPPLY' RISE=1
.measure tfall                                * fall time
+   TRIG v(d)      VAL='0.8*SUPPLY' FALL=1
+   TARG v(d)      VAL='0.2*SUPPLY' FALL=1
.end
  
```

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F04 Results



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Optimization

- ❑ HSPICE can automatically adjust parameters
 - Seek value that optimizes some measurement
- ❑ Example: Best P/N ratio
 - We've assumed 2:1 gives equal rise/fall delays
 - But we see rise is actually slower than fall
 - What P/N ratio gives equal delays?
- ❑ Strategies
 - (1) run a bunch of sims with different P size
 - (2) let HSPICE optimizer do it for us

P/N Optimization

```
* fo4opt.sp
* Parameters and models
*-----
.param SUPPLY=1.0
.option scale=25n
.include '../models/ibm065/models.sp'
.temp 70
.option post

* Subcircuits
*-----
.global vdd gnd
.include '../lib/inv.sp'

* Simulation netlist
*-----
Vdd      vdd      gnd      'SUPPLY'
Vin       a        gnd      PULSE    0 'SUPPLY' 0ps 20ps 20ps 120ps 280ps
X1        a        b        inv        P='P1'      * shape input waveform
X2        b        c        inv        P='P1'      M=4      * reshape input
X3        c        d        inv        P='P1'      M=16     * device under test
```

P/N Optimization

```
X4      d      e      inv      P='P1'      M=64      * load
X5      e      f      inv      P='P1'      M=256      * load on load

* Optimization setup
*-----
.param P1=optrange(8,4,16)          * search from 4 to 16, guess 8
.model optmod opt itropt=30          * maximum of 30 iterations
.measure bestratio param='P1/4'      * compute best P/N ratio

* Stimulus
*-----
.tran 0.1ps 280ps SWEEP OPTIMIZE=optrange RESULTS=diff MODEL=optmod
.measure tpdr                      * rising propagation delay
+   TRIG v(c) VAL='SUPPLY/2' FALL=1
+   TARG v(d) VAL='SUPPLY/2' RISE=1
.measure tpdf                      * falling propagation delay
+   TRIG v(c) VAL='SUPPLY/2' RISE=1
+   TARG v(d) VAL='SUPPLY/2' FALL=1
.measure tpd param='(tpdr+tpdf)/2' goal=0 * average prop delay
.measure diff param='tpdr-tpdf' goal = 0 * diff between delays
.end
```

P/N Results

- ☐ P/N ratio for equal delay is 2.9:1
 - $t_{pd} = t_{pdr} = t_{pdf} = 17.9$ ps (slower than 2:1 ratio)
 - Big pMOS transistors waste power too
 - Seldom design for exactly equal delays

- ☐ What ratio gives lowest average delay?

```
.tran 1ps 1000ps SWEEP OPTIMIZE=optrange RESULTS=tpd MODEL=optmod
```

- P/N ratio of 1.8:1
- $t_{pdr} = 18.8$ ps, $t_{pdf} = 15.2$ ps, $t_{pd} = 17.0$ ps

- ☐ P/N ratios of 1.5:1 – 2.2:1 gives $t_{pd} < 17.2$ ps

Power Measurement

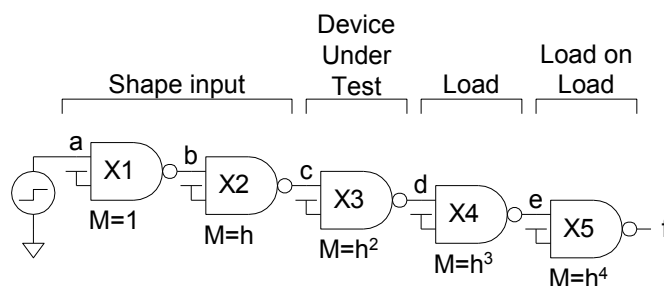
- ❑ HSPICE can measure power
 - Instantaneous $P(t)$
 - Or average P over some interval

```
.print P(vdd)
.measure pwr AVG P(vdd) FROM=0ns TO=10ns
```

- ❑ Power in single gate
 - Connect to separate V_{DD} supply
 - Be careful about input power

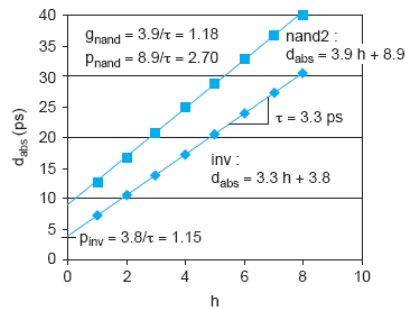
Logical Effort

- ❑ Logical effort can be measured from simulation
 - As with FO4 inverter, shape input, load output



Logical Effort Plots

- Plot t_{pd} vs. h
 - Normalize by τ
 - y-intercept is parasitic delay
 - Slope is logical effort
- Delay fits straight line very well in any process as long as input slope is consistent



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Logical Effort Data

- For NAND gates in IBM 65 nm process:

# of inputs	Input	Rising Logical Effort g_u	Falling Logical Effort g_d	Average Logical Effort g	Rising Parasitic Delay p_u	Falling Parasitic Delay p_d	Average Parasitic Delay p
2	A	1.40	1.12	1.26	2.46	2.48	2.47
	B	1.31	1.16	1.24	1.97	1.82	1.89
3	A	1.76	1.27	1.51	4.77	4.10	4.44
	B	1.73	1.32	1.52	3.93	3.60	3.77
	C	1.59	1.38	1.48	3.05	2.43	2.74
4	A	2.15	1.42	1.78	7.63	5.94	6.79
	B	2.09	1.48	1.78	6.67	5.37	6.02
	C	2.08	1.53	1.80	5.32	4.51	4.91
	D	1.90	1.59	1.75	4.04	2.93	3.49

- Notes:
 - Parasitic delay is greater for outer input
 - Average logical effort is better than estimated

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Comparison

Vendor		Orbit	HP	AMI	AMI	TSMC	TSMC	TSMC	IBM	IBM	IBM
Model		MOSIS	MOSIS	MOSIS	MOSIS	MOSIS	MOSIS	TSMC	IBM	IBM	IBM
Feature Size f	nm	2000	800	600	600	350	250	180	130	90	65
V_{DD}	V	5	5	5	3.3	3.3	2.5	1.8	1.2	1.0	1.0
FO4 Delay	ps	856	297	230	312	210	153	75.6	46.0	37.3	17.2
τ	ps	170	59	45	60	40	30	15	9.0	7.4	3.3
Logical Effort											
Inverter		1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
NAND2		1.13	1.07	1.05	1.08	1.12	1.12	1.14	1.16	1.20	1.26
NAND3		1.32	1.21	1.19	1.24	1.29	1.29	1.31	1.35	1.41	1.51
NAND4		1.53	1.37	1.36	1.42	1.47	1.47	1.50	1.55	1.62	1.78
NOR2		1.57	1.59	1.58	1.60	1.52	1.50	1.50	1.57	1.56	1.50
NOR3		2.16	2.23	2.23	2.30	2.07	2.02	2.00	2.12	2.08	1.96
NOR4		2.76	2.92	2.96	3.09	2.62	2.52	2.53	2.70	2.60	2.43
Parasitic Delay											
Inverter		1.08	1.05	1.18	1.25	1.33	1.18	1.03	1.16	1.07	1.20
NAND2		1.87	1.85	1.92	2.10	2.28	2.07	1.90	2.29	2.25	2.47
NAND3		3.34	3.30	3.40	3.79	4.15	3.65	3.51	4.14	4.10	4.44
NAND4		4.98	5.12	5.22	5.78	6.30	5.47	5.52	6.39	6.39	6.79
NOR2		2.86	2.91	3.29	3.56	3.52	2.95	2.85	3.35	3.01	3.29
NOR3		5.65	6.05	7.02	7.70	6.89	5.61	5.57	6.59	5.76	6.35
NOR4		9.11	10.3	12.4	13.9	11.0	8.76	8.95	10.54	9.11	10.16