DREXEL UNIVERSITY
Electrical and Computer Engineering
College of Engineering

Drexel University
Electrical and Computer Engineering Dept.
Electrical Engineering Laboratory IV, ECEL-304

TITLE: Step 3

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Objective

The objective of this lab was to test the limitation of the ADC0804 and DAC0808 by experimenting with the voltage and time resolutions. The analog voltage was fed into the ADC in CFR or continuous free running mode then reconstructed the analog voltage with the DAC along an 8 bit bus, as shown in figure 1. This experiment will be done at different frequencies to test the limits of the system.

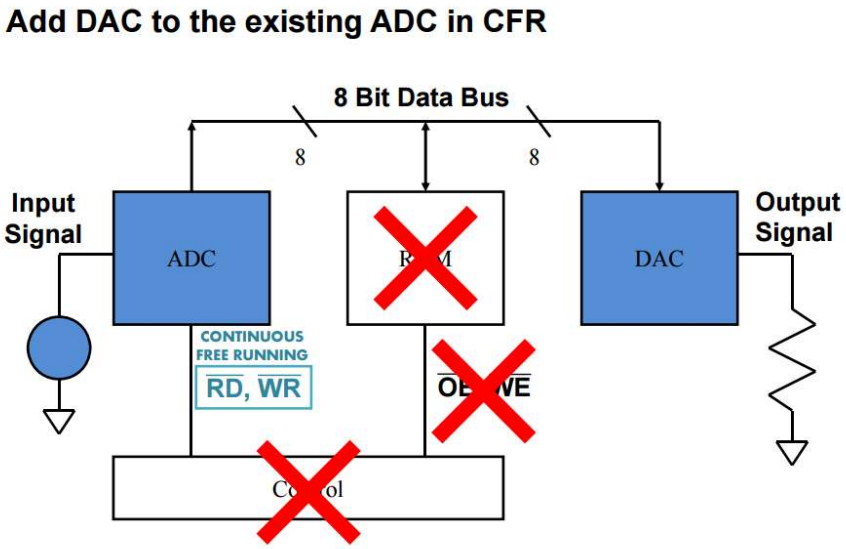

Figure 1: DAC and ADC system

Results

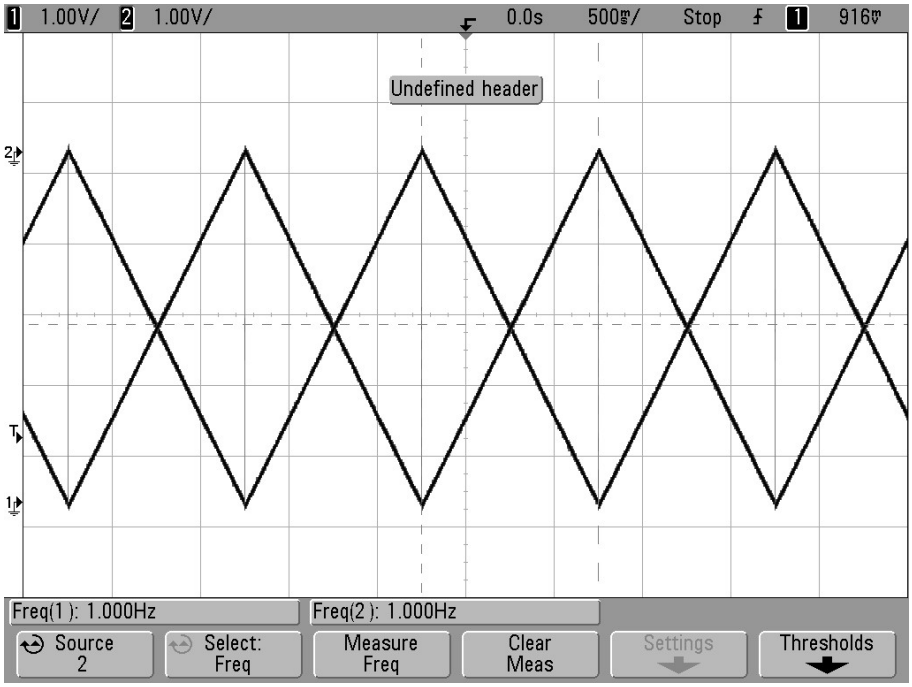

Figure 2: Input vs Output of DAC0808; 1 Hz Ramp input

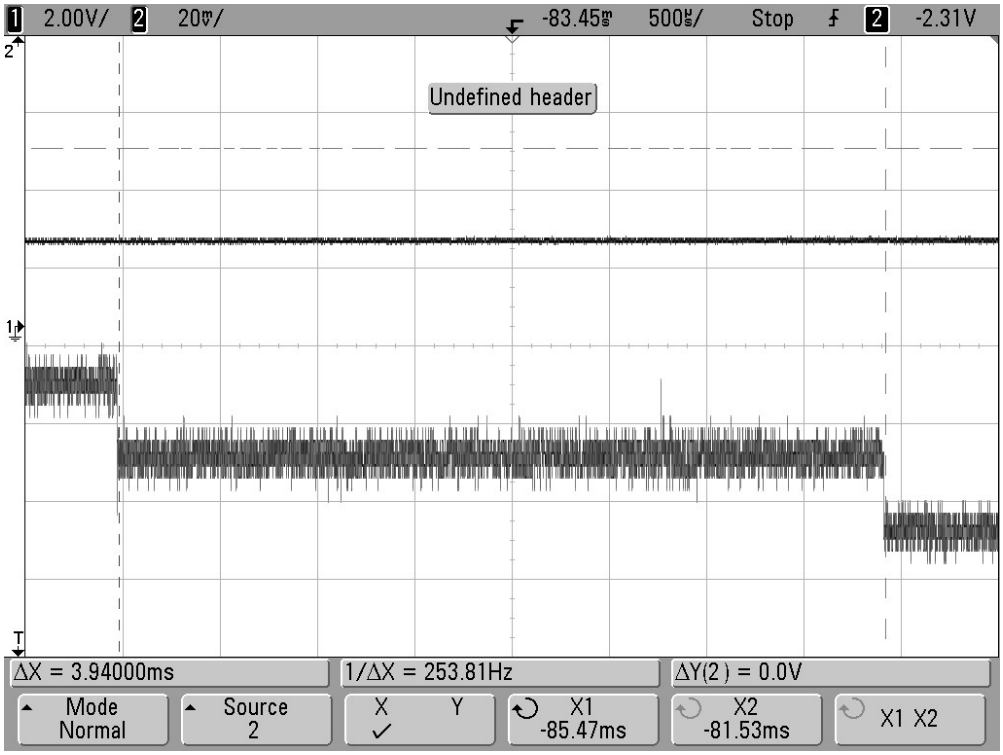

Figure 3: Time Step Measurement of output of DAC0808, 1 Hz Ramp input

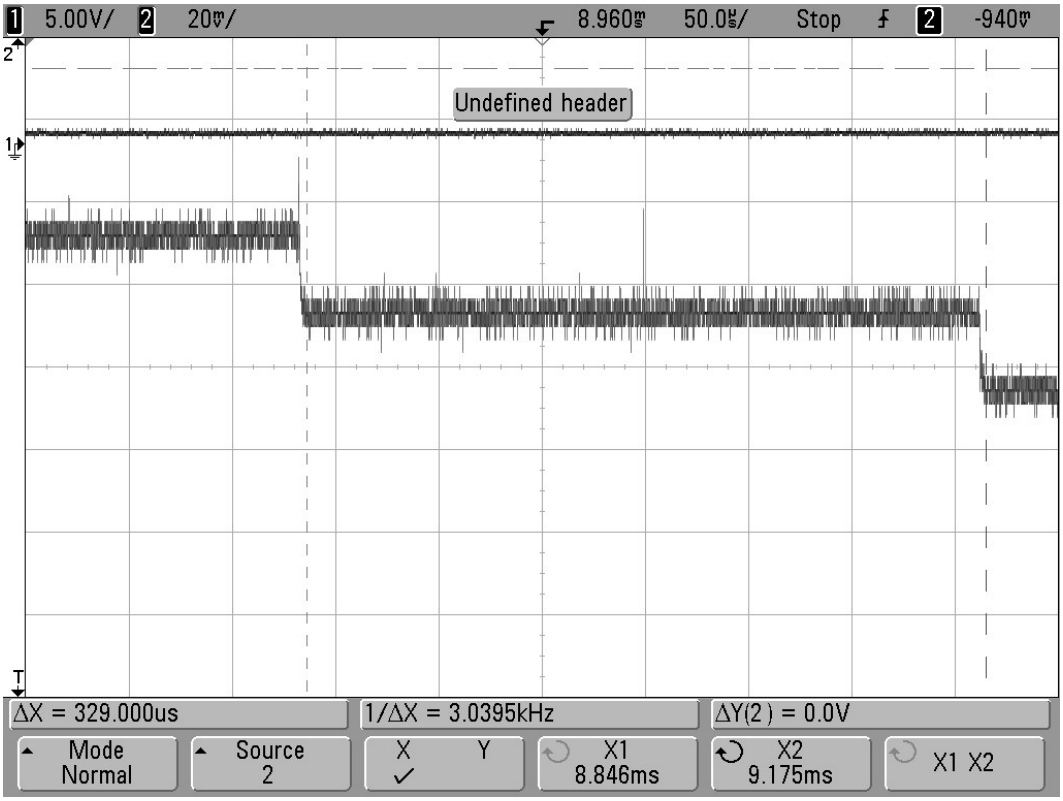

Figure 4: Time Step Measurement of output of DAC0808, 10Hz Ramp input

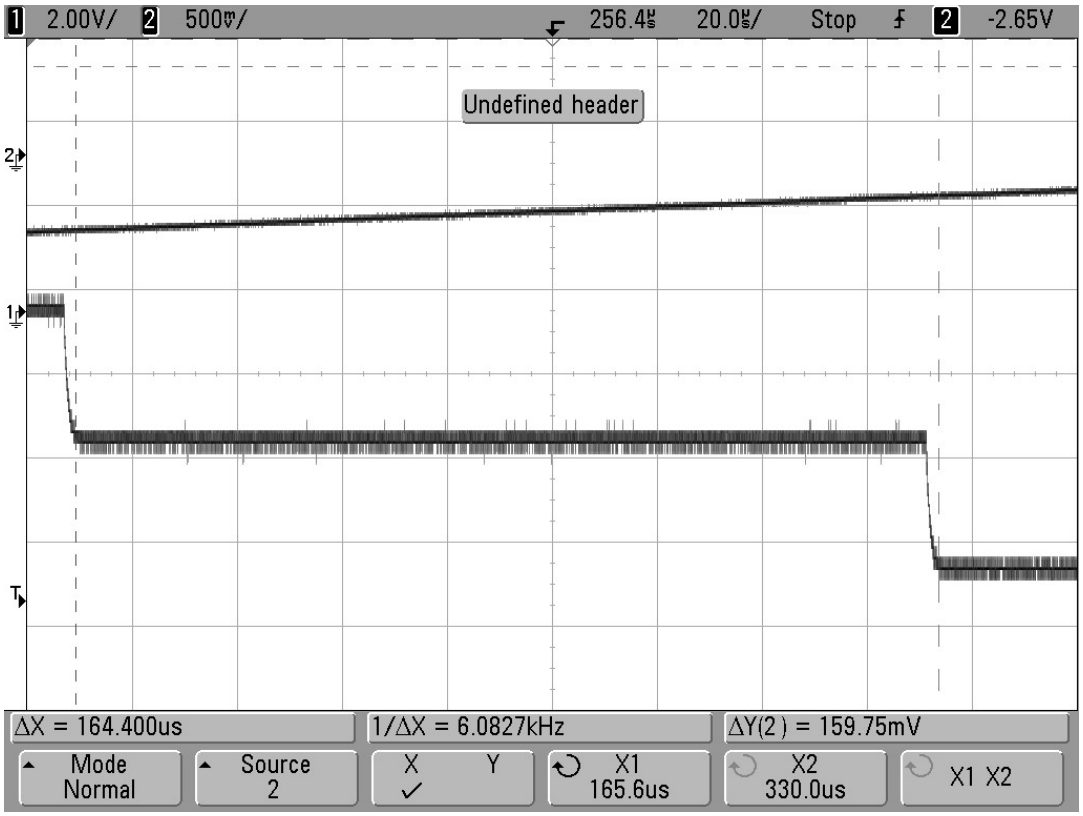

Figure 5: Time Step Measurement of output of DAC0808, 100 Hz Ramp input

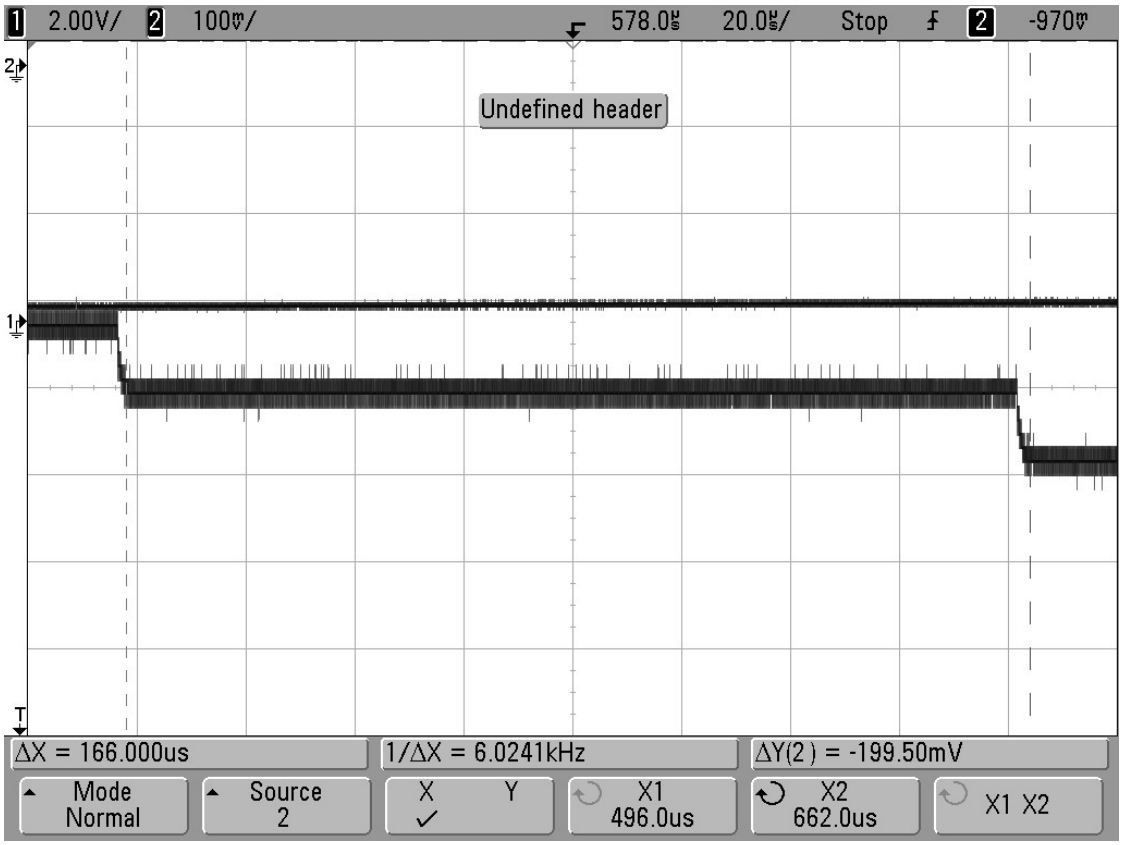

Figure 6: Time Step Measurement of output of DAC0808, 1k Hz Ramp input

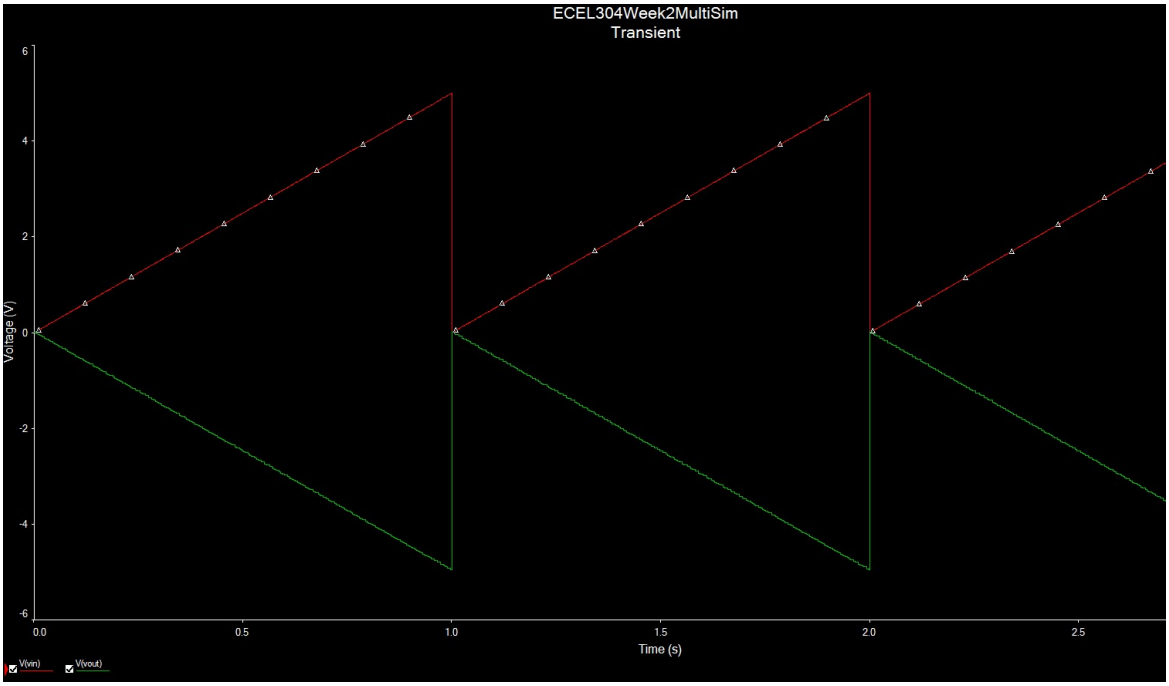

Figure 7: Input vs Output of Multisim Simulation, 1 Hz Ramp input

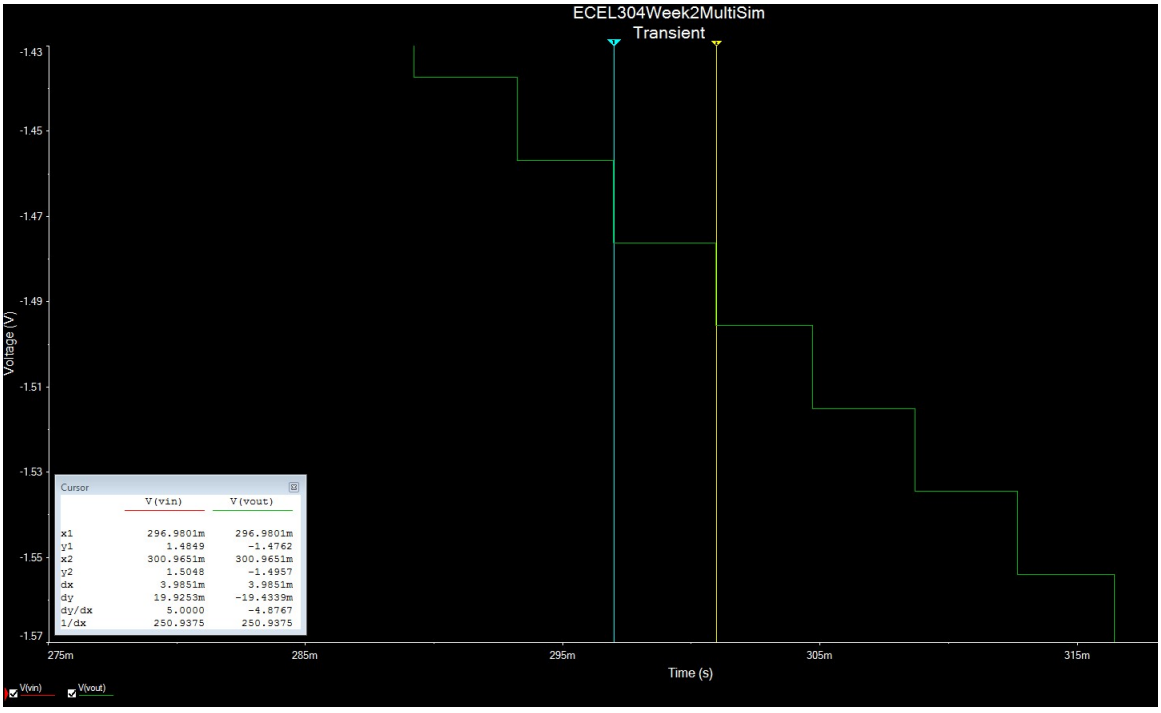

Figure 8: Time Step Measurement of Multisim Simulation, 1 Hz Ramp input

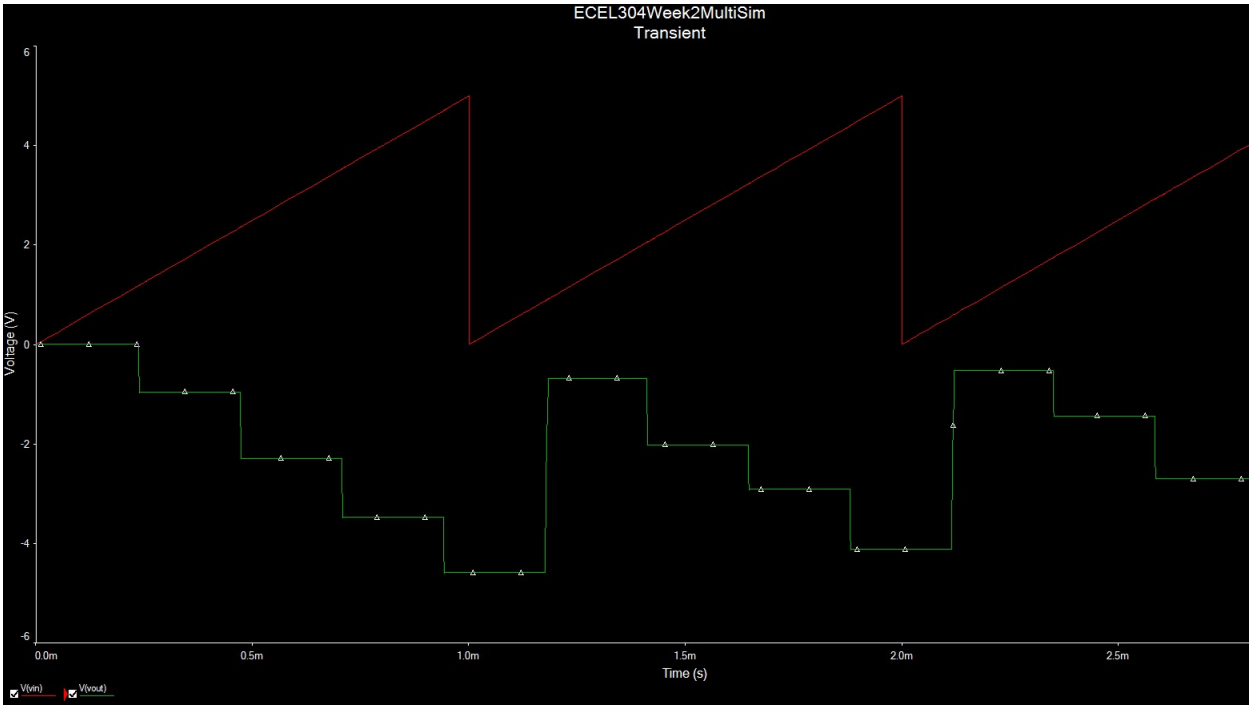

Figure 9: Input vs Output of Multisim Simulation, 1 kHz Ramp Input

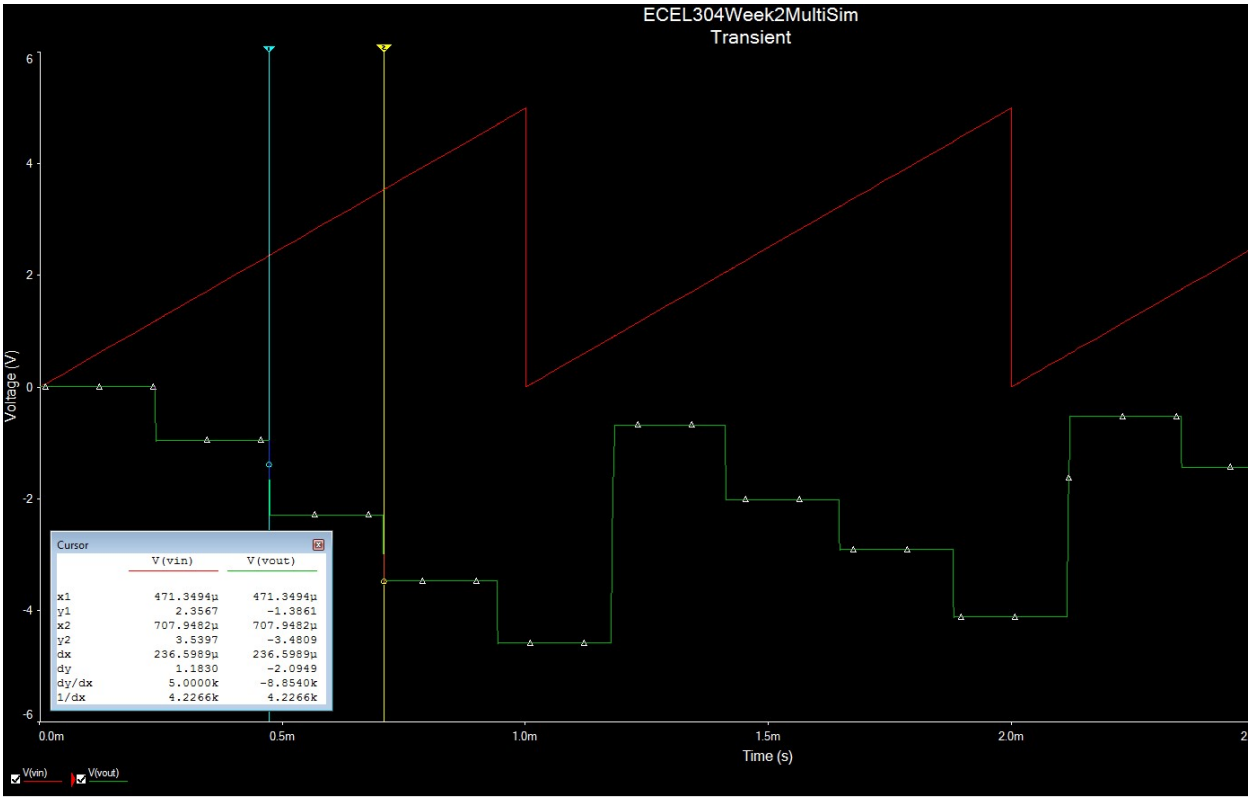

Figure 10: Time Step Measurement of Multisim Simulation, 1 kHz Ramp Input

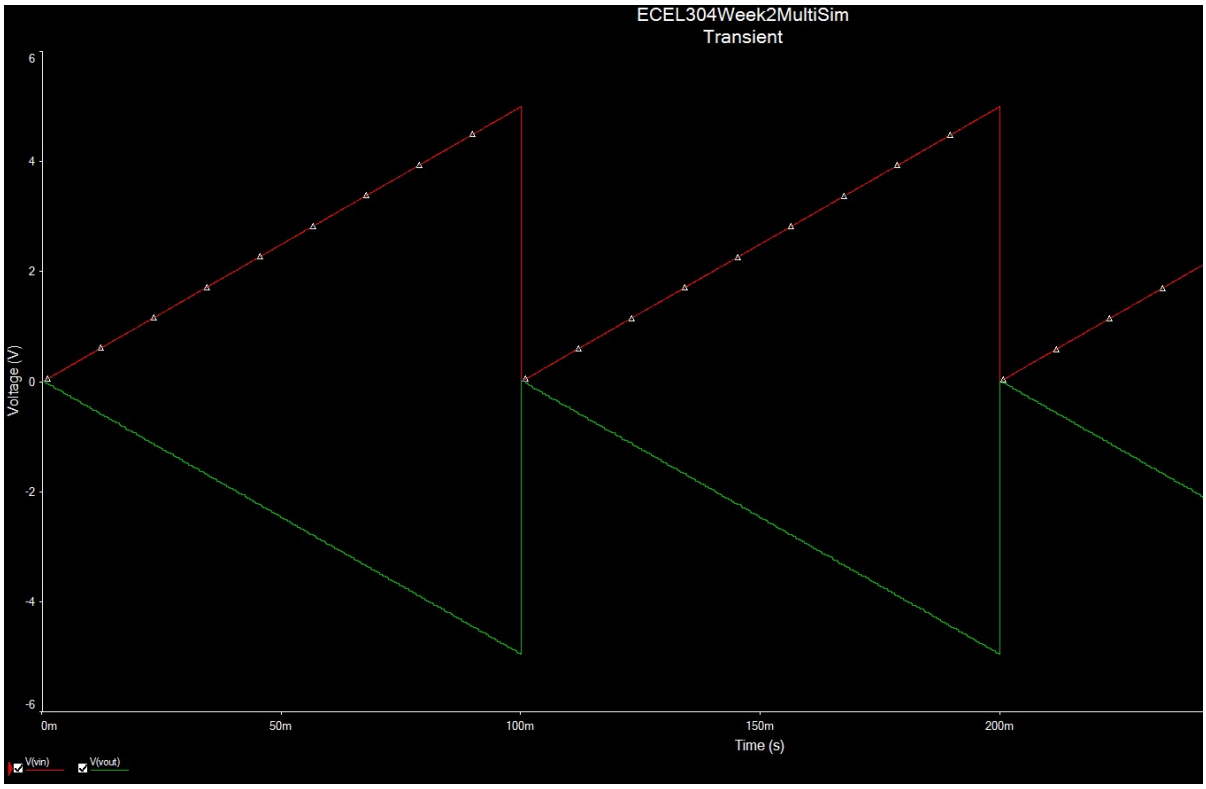

Figure 11: Input vs Output of Multisim Simulation, 10 Hz Ramp input

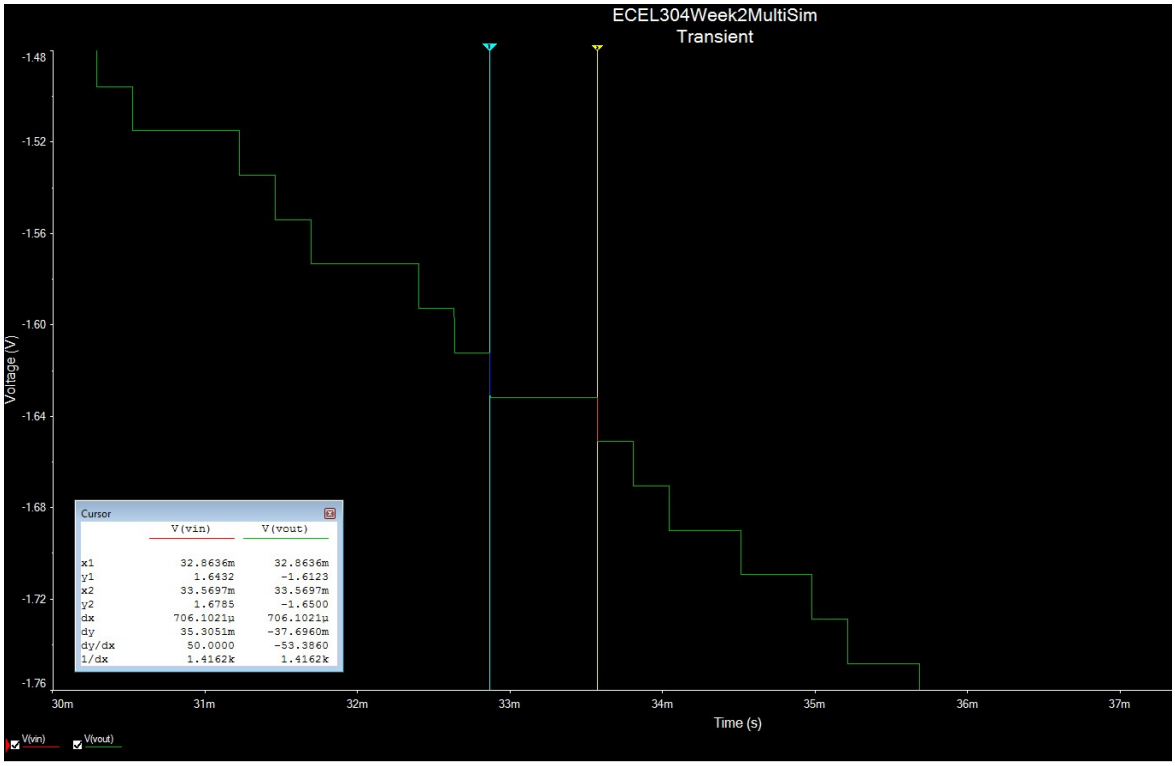

Figure 12: Time Step Measurement of Multisim Simulation, 10 Hz Ramp input

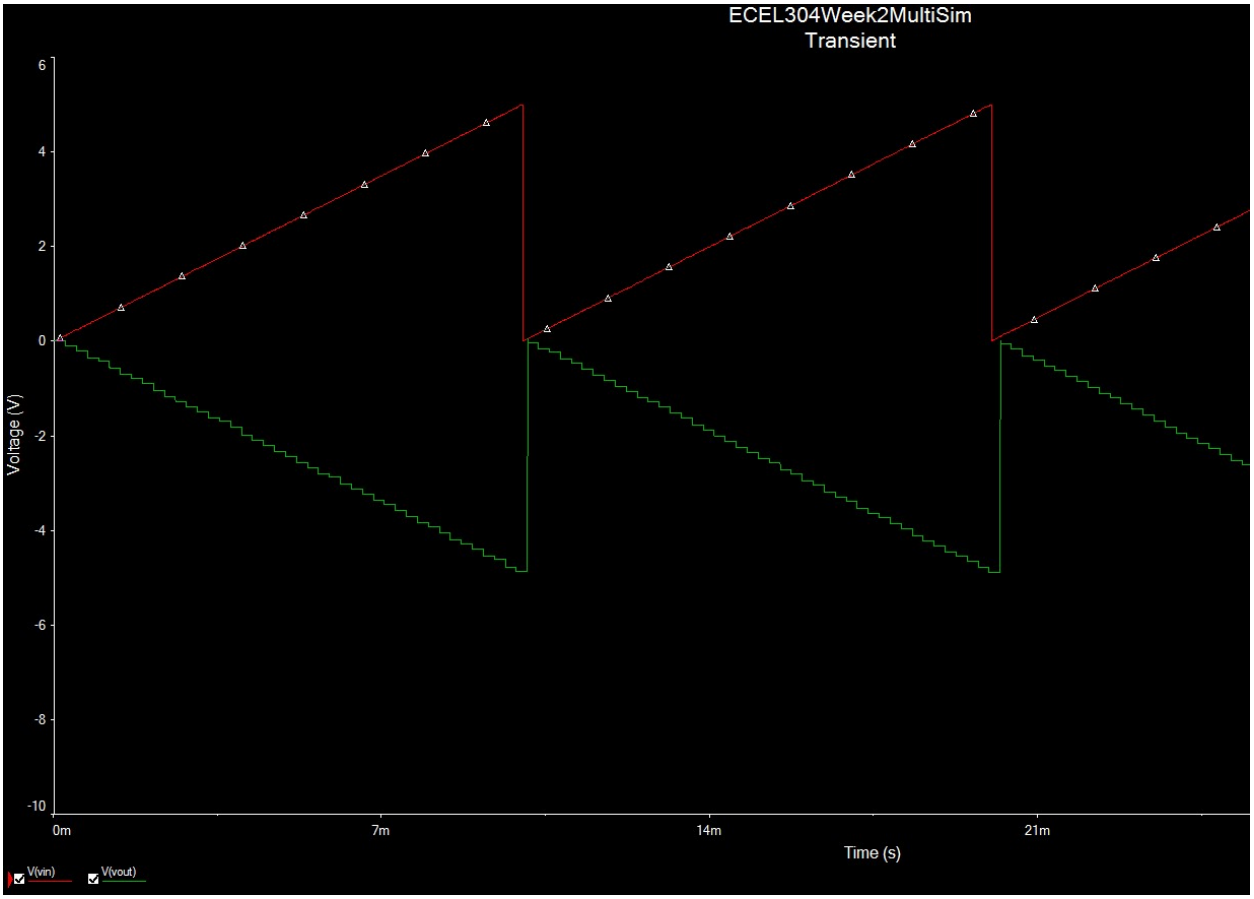

Figure 13: Input vs Output of Multisim Simulation, 100 Hz Ramp input

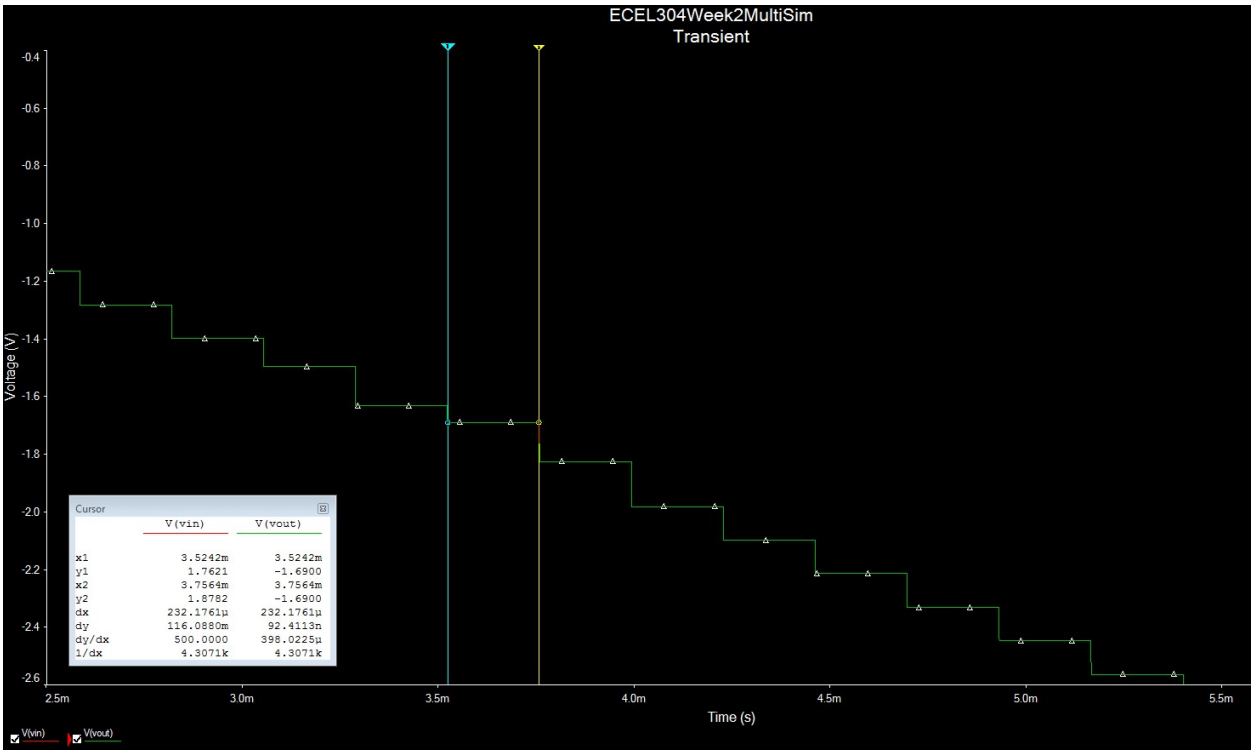

Figure 14: Time Step Measurement of Multisim Simulation, 100 Hz Ramp input

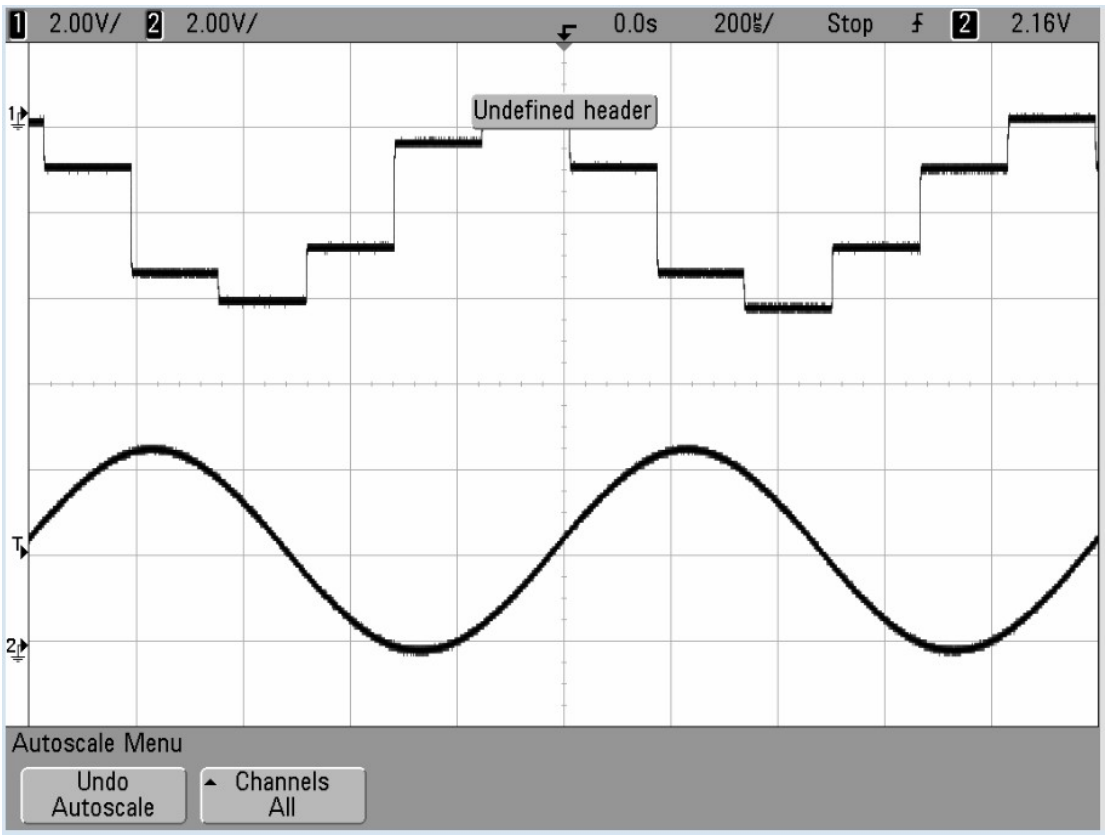

Figure 15: Output of DAC0808 aliasing, 1 kHz Sine Wave input

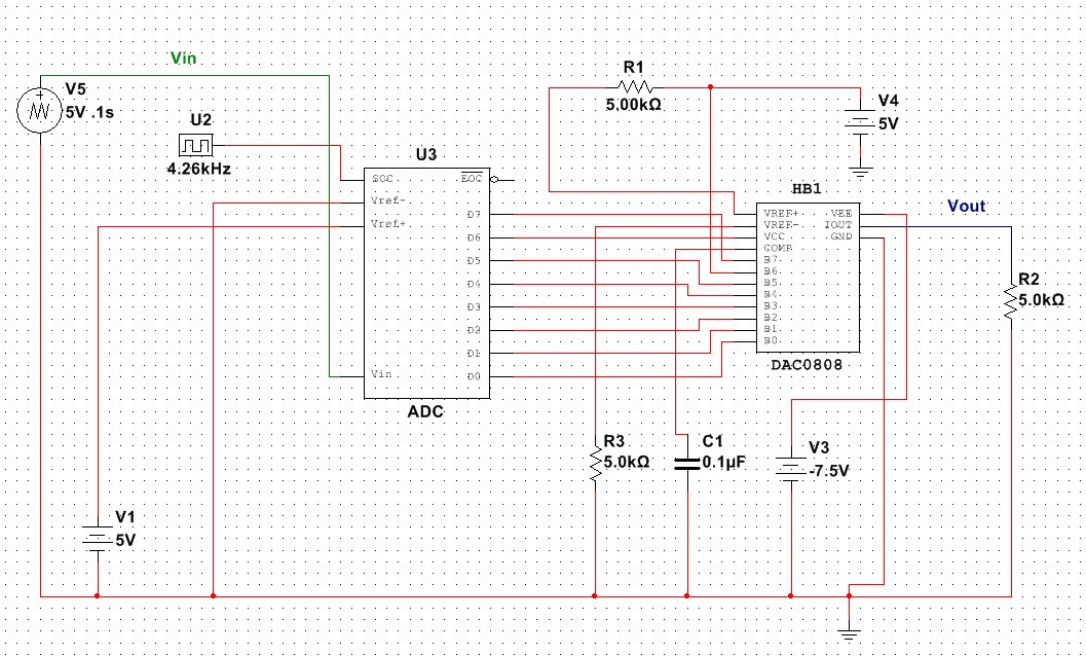

Figure 16: Schematic used for simulation in Multisim

Table 1: Comparing Simulation results with Actual Results

Input Freq (Hz)	Simulated Time Step (s)	Actual Time Step (s)	Time Step Percent Error (%)	Simulated Freq (Hz)	Actual Freq (Hz)	Freq Percent Error (%)
1	0.00398	0.00394	1.01%	250.9	253.81	1.16%
10	0.000706	0.000329	53.40%	1410	3003	112.98%
100	0.000232	0.000166	28.45%	4300	6002	39.58%
1000	0.000236	0.000164	30.51%	4220	6008	42.37%

$$\underline{Percent\ Errror = \frac{|Actual - Expected|}{Expected} * 100} \quad (1)$$

Explanation

The purpose of the lab was to tests the limits of the ADC and the DAC using several different methods, the results of the experiment are shown in figures 1 through figures 15. Table 1 also shows the simulation and hardware results side by side to compare them. As the Table shows there seems to be a correlation to the increase in frequency and the percentage error between both the experiments. This could have been from many factors; the first factor is the difference in the blocks used from the hardware to the simulation. In the simulation, there where generic ADCs, DACs, resistors, and capacitors used which could lead to the higher percentage errors. At 1hz the percentage errors where only at 1.01% and 1.16% respectively between time steps and frequency.

The DAC did a better job reproducing frequencies at the lower end, as you can see the times steps in the 1hz 10hz and 100hz, in figures 2 through 15. The signals are better quality of the reconstruction seems to very also as the frequency of the input signal increases. The resolution of a n-bit analog-to-digital Converter (ADC) is a function of how many parts the maximum signal can be divided into. The formula to calculate resolution is 2^n. For example, a 8 bit ADC has a resolution of 2^12 = 256. Therefore, our best resolution is 1 part out of 256.[1] An ADC takes an analog signal and turns it into a binary number. Thus, each binary number from the ADC represents a certain voltage level. Resolution is the smallest input voltage change a digitizer can capture. Resolution can be expressed in bits (LSB), in proportions, or in percent of full scale. Resolution limits the precision of a measurement. The higher the resolution (number of bits), the more precise the measurement. An 8-bit ADC divides the vertical range of the input amplifier into 256 discrete levels. With a vertical range of 10 V, the 8-bit ADC cannot ideally resolve voltage differences smaller than 39 mV. In comparison, a 14-bit ADC with 16,384 discrete levels can ideally resolve voltage differences as small as 610 µV. .[1]. In the system under test, this can be seen in the figures above how the bit resolution plays into the reconstruction of the signal and the step effect occurs.

There are some short comings to this design and any signal processing has there down sides. Here the resolution, device mechanics, and frequencies are play a role here. As in the voltage resolution the analyzing effect and so on, if the frequency increases to much the system cannot properly regenerate that signal. In all, the experiment was successful and the ADC and DAC were tested properly.

References

[1]N. Instruments, "Understanding resolution in high-speed Digitizers/Oscilloscopes," 2006. [Online]. Available: http://www.ni.com/white-paper/4806/en/. Accessed: Jan. 27, 2017.

[2]N. Instruments, "Aliasing and sampling at frequencies above the Nyquist frequency," 2006. [Online]. Available: http://www.ni.com/white-paper/3000/en/. Accessed: Jan. 27, 2017.