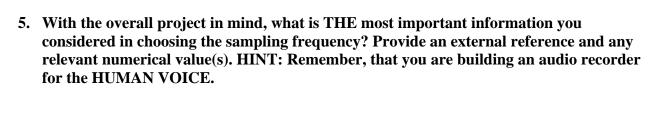
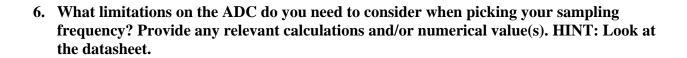
STEP 1: ADC Simulation and Testing Worksheet

ECEL 304: ECE Laboratory IV

Rev. 1

Se	ection:	Group No.:	Grade:/10
Na	ame(s):		
1.	Briefly explain why Mode).	$\overline{ ext{INTR}}$ and $\overline{ ext{WR}}$ is tied together in CF	TR (Continuous Free Running
2.	Why is \overline{RD} and \overline{CS} c	onnected to ground in CFR?	
3.	What purpose does	the button in CFR serve to do?	
4.		s being ACTIVE LOW mean? Why t numerical value(s). HINT: Look a heet.	





7. What did you choose as the sampling frequency? Why? What are the advantages and limitations of you picking this frequency? HINT: Consider Nyquist/Shannon's Theorem when picking your sampling frequency.

8. Show/explain all the work you did in order to calculate the timing resistor and capacitor. Be sure to explain how you determined the CCPS (Clock Cycles Per Sample) used in your calculation.

9. What factors determine the voltage resolution on an ADC? Can those factors be changed on a given ADC to improve the resolution? If not, why?

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10. Compare your calculated/desired sampling and clock frequency with your measured ones. Is the discrepancy significant and what would cause it?

11. Briefly explain why/how the ramp produces a "counting" effect on the digital outputs/LEDs.