AN OPTIMUM VLSI DESIGN OF A 16-BIT ALU

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***Abstract* -- The key parameters for the performance measure of any VLSI design are logic delay, power consumption and chip area. This paper describes the VLSI design of a 16 Bit ALU and design is optimized in terms of Speed, Power Consumption and Chip Area. Different logic families are used in the design for various logic modules. The choice of logic families for each module is determined by considering speed and power consumption as the important parameters offered by each logic family. The adder circuit being the most important module used by the arithmetic operations of an ALU, detailed analysis of the variety of adder circuit configurations are carried out and the best suited configuration for the ALU design i.e. Carry Skip Adder configuration is used to design the optimum ALU. Finally a 16 bit Arithmetic Logic unit is designed using mixed logic families such as CMOS for basic logic functions, pseudo-NMOS for AND logic and Pass Transistor logic for multiplexers, in order to optimize the overall performance of the design. Schematic editor DSCH is used to validate the design at gate level implementation and IC Layout editor Microwind is used to implement the chip level design.**

Keywords- Adders, ALU, VLSI design

I. INTRODUCTION

Arithmetic Logic Unit is the main module of the Central Processing unit which performs arithmetic operations like addition, subtraction multiplication and division, of binary numbers and logical operations such as INVERT, AND, OR, XOR and other Boolean functions. Binary Adder circuit is one of the basic units in an ALU used to perform the arithmetic operations. There are different configurations of binary adder circuits based on methods of carry propagation. Key constraints that adder circuits faces are chip area, speed and the power consumption.

The conventional adder circuits are ripple carry adder implemented using cascaded full adders. Each full adder add three single bits giving one bit sum and a carry bit as outputs. The conventional Ripple Carry Adder (RCA) introduces delay in the propagation of carry bit from LSB to MSB as the no. of bits in the input increases. To improve the speed of the addition, other 'fast adders' have been developed which computes carry bit separately to complete the addition operation faster. Some of the faster adder configuration include Carry Look-ahead Adder (CLA), Carry Skip Adder and Carry Select Adder[5]. In this paper, delay caused due to carry propagation in longer word adder circuit is analysed at transistor level with the help of routing delays resulted from software simulation. The optimum adder circuit is then used to design the 16 bit ALU for optimum performance. Various logic families are compared against their performance to be used for implementing different functions of the ALU. Finally an optimum 16 bit ALU to perform 16 different operations is designed and validated using schematic editor DSCH and layout editor Microwind.

II. BINARY ADDER CIRCUITS

A Ripple Carry Adder consists of full adders in cascade to form 'n' bit adder units as shown in figure 1 below.

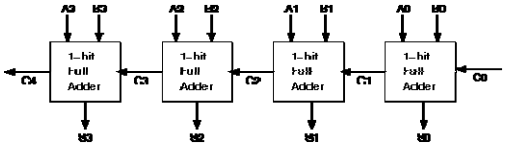

Fig.1. Four bit binary Ripple Carry Adder

Carry Look-ahead Adder on the other hand compute the carry bit C_{i+1} for next higher significant pair of input bits from the carry propagate ($P_i = A_i \oplus B_i$) and carry generate ($G_i=A_i.B_i$) using the input bits A_i and B_i. This Carry bit produced by the CLA generator as shown in figure 2 allows Sum bit to be computed to each bit pair simultaneously at the cost of an extra level of hardware. The advantage of this circuit is the speed of the adder circuit is independent of the number of bits in the word to be added unlike in RCA.

However the CLA circuit is more complex than a ripple carry adder as the carry of each stage has to be derived individually from the input data bits. The level of complexity increases as the number of bits in the input data increase.

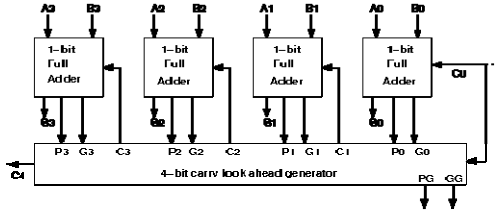

Fig.2. Four bit Carry Look Ahead Adder

Another fast configuration of the adder circuit is *Carry Skip Adder*. The skip sub-module passes the carry-in when the ANDed result of propagate values P_i of each bit is not binary one. If the value is a binary one, the carry is taken through the ripple path. This configuration can make it appear as if the carry-in skips the full adder units [1].

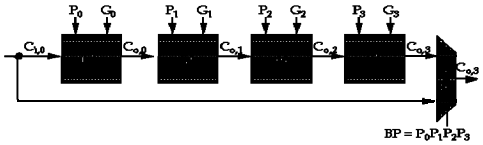

Fig.3. Four bit Carry Skip Adder circuit

A carry-skip adder reduces the carry-propagation time by skipping over groups of consecutive adder stages. The carry-skip adder is usually comparable in speed to the carry look-ahead technique, and it requires less chip area and consumes less power

The underlying strategy of the *Carry Select Adder* is similar to the conditional-sum adder. Each group generates two sets of sum bits and an outgoing carry. One set assumes that the incoming carry into the group is 0, the other assumes that it is 1. When the incoming carry into the group is assigned, its final value is selected out of the two sets. In this configuration, the sizes of the k^{th} group is chosen so as to equalize the delay of the ripple-carry within the group and the delay of the carry-select chain from group 1 to group k.

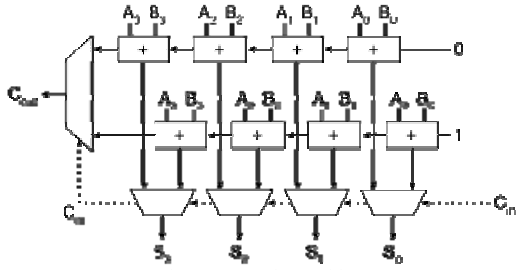

Fig.3. Four bit Carry Select Adder

Carry Save Adders can be used to reduce the gate delay when it is desired to add more than two numbers together. The straightforward way of adding together m numbers (all n bits wide) is to add the first two, then add that sum to the next, and so on. This requires a total of m − 1 additions, for a total gate delay of O(m log n) (assuming carry look ahead adders). Using carry save addition, the delay can be reduced further. The idea is to take 3 numbers that we want to add together, x + y + z, and convert it into 2 numbers c + s such that x + y + z = c + s, and do this in O(1) time. In carry save addition, we refrain from directly passing on the carry information until the very last step. Since the performance evaluation is done based on the operations on two data, this configuration is not considered.

Among all other configurations, the ripple carry adder gives best result in terms of chip area; it requires the least area to be fabricated. The circuit complexity is less in this design, but the carry of such a configuration has the most delay compared to all other adder configurations.

III. TRANSISTOR LOGIC FAMILIES

During 80's NMOS logic was more widely used as CMOS technology was under development. CMOS having NMOS and PMOS Transistors are used in majority of ICs for their inherent advantages such as high noise margin, low power consumption and less sensitivity to variations in device parameters. CMOS circuits have an NMOS pull-down and a resistor or a PMOS in the pull-up path. When pull-down is OFF the output is pulled high and when ON it opposes the static resistive load. The load is kept weak so that the output stays within threshold levels giving good binary ones and zeros. Even with large noise, CMOS IC gives stable output but with more gate delays. Hence its required to have other circuit families which can give better performance compared to conventional CMOS logic families for specific applications.

Ratioed circuits operate well for some applications based on the W/L Ratios of the transistors. There are constraints on the ratio between the pull-down network and the load. If the load is stronger, the output has less delay but the noise margin is also reduced and more static power is consumed. An improvement over a resistive load is using a single PMOS that is kept ON throughout with the gate grounded. The widths of the PMOS are taken to be a quarter of the effective width of NMOS network that is pulled-down network. This improves the noise margin and reduce the propagation delay.

Pass transistor configurations are preferred for data transfer switching circuits. Inputs are given to the Drain or Source terminal of the MOS transistor in Pass transistor mode of operation. Switches are built using either NMOS or PMOS or a parallel combination of both.

The parallel combination of NMOS and PMOS is a transmission gate. Transmission gate configuration have better speed and power performance over CMOS.

Full adders can be efficiently constructed using pass transistors which gives stable output. However, since a single transistor is used in pass transistor configuration, the issue of threshold drop creeps in. Additional circuitry are required to pull-up the output to perfect 'one'. In Transmission gates this issue is resolved with the use of parallel transistors. The PMOS would pass a good logic '1' and NMOS a good zero.[2]

The analysis of CMOS logic family are widely supported by CAD tools and have large number of standard cell libraries[4]. A schematic editor – **DSCH** by **Microwind** is used to validate the circuit architecture and analyse the behaviour for different process technologies. DSCH facilitates the simulation for each process technology with its corresponding rule files. The critical path i.e. path with the largest delay in the circuit can be determined and the power consumption can be calculated for each layout.

IV. THE ALU DESIGN

The design of a 16 bit ALU considered here is assumed to perform eight functions that include two basic arithmetic operations such as Addition, Subtraction and six logic operations such as NOR, NAND, OR, AND, XOR, and Invert. Different transistor logics are employed for different functions based on the advantages offered by each logic families. The criteria for selecting different logic families for optimum performance of the ALU are discussed below.

The very important part of the ALU which determine the overall performance of the design is the full adder for the arithmetic operations. The basic logic circuit of the full adder is the EX-OR logic gate. The subtraction operation can be performed as addition of negative numbers. The negative number can be derived using inverters the output of which is one's compliment and input carry to the LSB is made logic one to obtain the two's compliment of the subtrahend. An efficient method using multiplexer is employed for the ALU design which uses less power as well as delay. Multiplexers are also tested for good zeros and ones at the output.

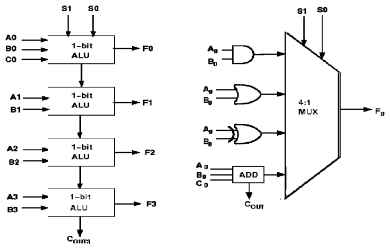

Fig.5. A Four bit ALU using single bit ALU

The block diagram of a four bit ALU derived using four single bit ALUs performing four functions is shown in figure 5. Each module of the 16 bit ALU is designed individually to give the optimum overall performance i.e. to minimise overall delay and power consumption.

The basic logic operations are implemented using the conventional CMOS logic gates. The 8 to 1 Multiplexer to select one among 8 arithmetic and logic operations is implemented using NMOS logic. It gives the advantage of reduced area. As the multiplexer is always operational, reduced delay and power consumption is preferred over other parameters.

On analysing the various adder circuit configuration, its found that the carry skip adder gives better result than other configurations in terms of propagation delay and power dissipation. The results are tabulated in the following section.

In Carry Skip Adder using RCA, the propagate value of each bit is AND-ed and fed into a 2:1 multiplexer to select appropriate output carry bit. The 2:1 multiplexer chooses carry bit from ripple carry if the AND result is one or chooses input carry in all other cases. This carry skip implementation is helpful in majority of the cases, as it avoids the ripple carry path.

A detailed analysis on carry skip adder and CLA, it is found that Carry Skip Adder topology is favourable over Carry Look-Ahead adder for power and area. As the number of bit increases, complexity of the carry look-ahead adder increases thus increasing the area and power consumption.

The AND operation in the Carry Skip Adder is performed using 16 input pseudo- NMOS AND gate. This logic family is used here considering the fact that the propagate is always fed into AND gate, and the operation is continuous. The power consumption in this logic family is slightly higher since the PMOS is always grounded resulting in static power consumption, whereas the delay and area is less. The output Carry from the carry skip adder is fed to a 2:1 multiplexer implemented using transmission gates.

Transmission gate multiplexer has the advantage of less delay and a good zero and one output compared to that of CMOS logic. The reason for choosing transmission gate based multiplexer in this section of the circuit is to have a stable output with the required output capacitance.

V. DESIGN VERIFICATION

Individual arithmetic circuits such as Adder, Subtractor, and logic functions such as AND and OR are independently verified at transistor and gate level simulation.

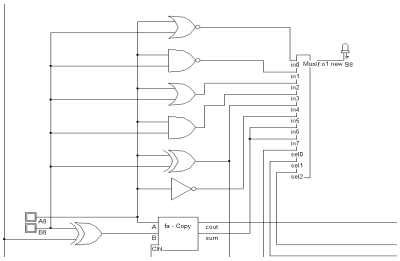

Fig 6: Schematic diagram of a Single bit module of the ALU

Each of the modules are then integrated to form a single bit ALU initially. The single bit ALU circuit is simulated to determine its propagation delay and power consumption. The single bit Arithmetic logic units are appended to obtain a 4 bit Arithmetic logic unit and further extended to 16 bit ALU.

Microwind and DSCH Software from Microwind Inc. is used for the design and simulation of the circuits at IC layout level upto 45nm process technology.

Microwind IC Layout editor integrates the front-end and back-end chip design into an integrated flow, accelerating the design cycle with reduced design complexities. It tightly integrates mixed-signal implementation with digital implementation, circuit simulation, transistor-level extraction and verification. Performance parameters like area, power dissipation and propagation delay can be analysed conveniently using this software. The Verilog file of the validated circuit schematic in DSCH is extracted and complied in Microwind to obtain the IC layout using specific process technologies.[7]

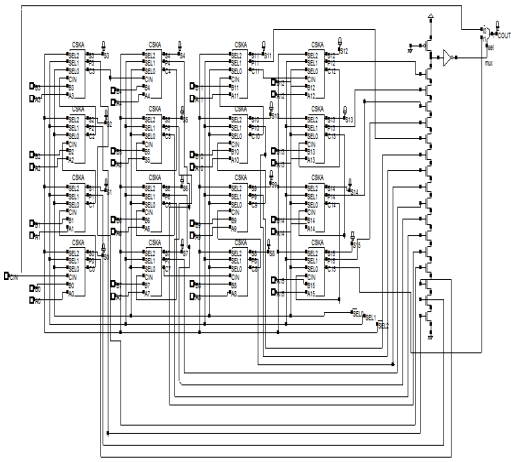

Fig 7: Schematic diagram of Carry Skip Adder based 16 Bit ALU

VI. SIMULATION RESULTS

The parasitic capacitance, inductance, resistances and crosstalk between adjacent paths have been considered while carrying out simulations, by varying the W/L of the PMOS and NMOS transistors for design optimization. The design is simulated using an 8pF capacitive load.

The power and delay report from the simulations are recorded and analysed. An optimum 16 bit ALU IC layout is developed and its architecture is verified using the schematic editor DSCH in different CMOS process technologies. The IC chip level simulation is carried out using Microwind.

As carrier density in PMOS is less compared to NMOS, the width of the PMOS transistors are chosen higher than NMOS so that the rising and falling time is balanced.

The PMOS and NMOS W/L chosen are:

PMOS: W= 0.525; L= 0.070

NMOS: W= 0.140; L= 0.070

The simulation results of 4 different adder circuits using various configurations are tabulated as shown in Table1. From the table of results, its inferred that Carry Skip Adder would be optimum among all other configurations.

Table 1 : Comparison of 4 Bit adder configurations

ADDER CONFIGURATION	Delay	Power Consumption
RIPPLE CARRY ADDER	1.550ns	0.763 mW
CARRY LOOKAHEAD ADDER	1.490ns	1.500 mW
CARRY SKIP ADDER	1.550ns	0.890 mW
CARRY SELECT ADDER	1.640 ns	1.764 mW

Simulation results of 16 bit ALU using Carry Skip Adder is tabulated below. The result below shows the critical path delay and the Power-Delay product of the 16- bit ALU using mixed logic proposed in this paper gives improved performance compared to conventional CMOS logic.

	CMOS Logic	Mixed Logic
Critical Delay	2.840 ns	2.750 ns
Power Consumption	2.775mW	2.810mW
Power-Delay Product	7.881	7.7275

VII. CONCLUSION

A 16-bit arithmetic logic unit with 8 functions is designed and the design is validated using the schematic editor DSCH. The physical layout for the circuit is simulated using a software tool by Microwind, France.

The 16-bit ALU design uses 4 bit carry skip adder modules as it gives the least power dissipation and comparable critical path delay for carry to be propagated compared to other 4 bit adder topologies considered.

Different logic families are preferred for each module so as to optimise the overall performance of the 16 bit ALU. The 16 bit ALU has been designed using a carry skip adder and optimized using mixed logic families in the design.

In this paper, VLSI design of an optimum 16- bit ALU design is presented which utilises the advantages of three different logic families such as CMOS, Pseudo-NMOS and Pass Transistors.

The Full Adder used in the ALU is designed using multiplexer based logic with 12 transistors[3]. The design is optimized for an output load capacitance of 8pF. The Power-Delay product for the proposed design is 1.9477% lower than the CMOS design of the same ALU.

The implementation of the different logic families in the same circuit has helped in optimizing the overall circuit performance in terms of delay and power consumption

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