DREXEL UNIVERSITY
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TITLE: Part 4

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SECTION: 62

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Objective

The objective of this lab is to design and implement a state machine driven by an RC debounce circuit and test the propagation delays of various gates. This state machine will allow the audio recorder to be placed into two states a recording state and playback. The RC values will be used to filter out any noise of the debouncing of the button which then will be fed into the flip-flop. The design will be tested in both simulation and hardware.

Results

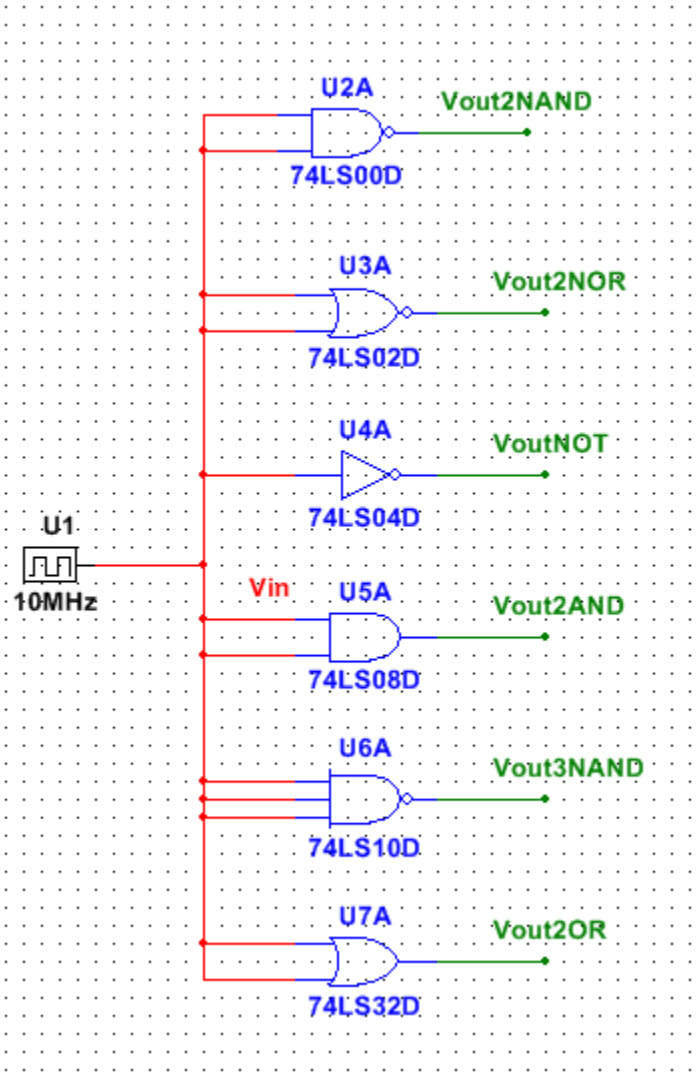

Figure 1: Multisim Schematic used to test propagation delay of different gates

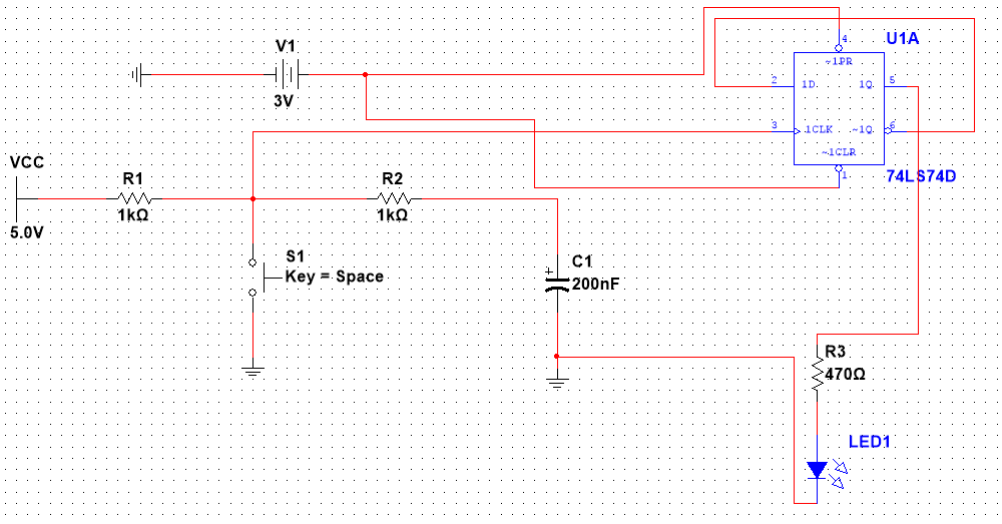

Figure 2: Multisim Schematic for State Machine using D FlipFlop

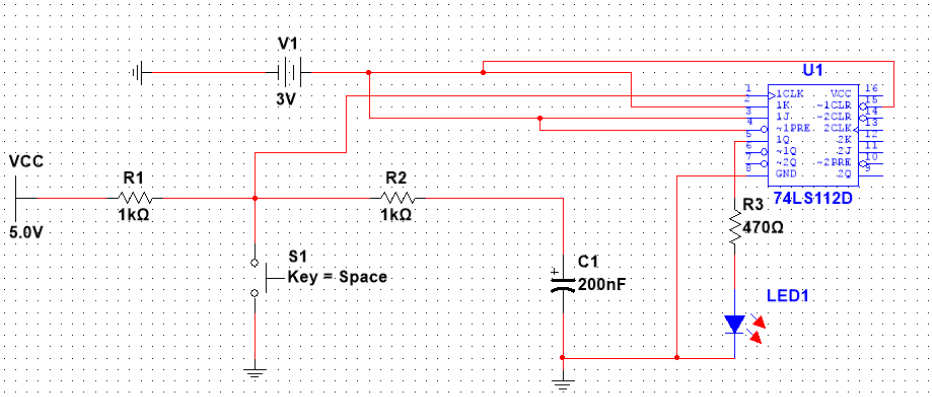

Figure 3: Multisim Schematic for State Machine using JK FlipFlop

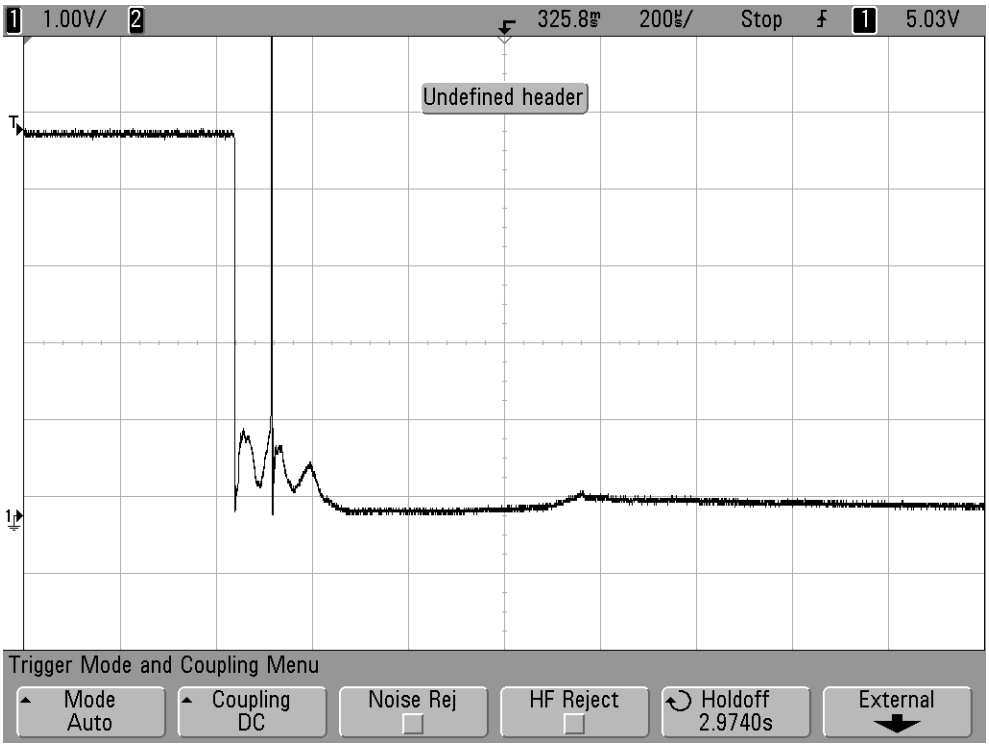

Figure 4: Output after SPDT button is debounced

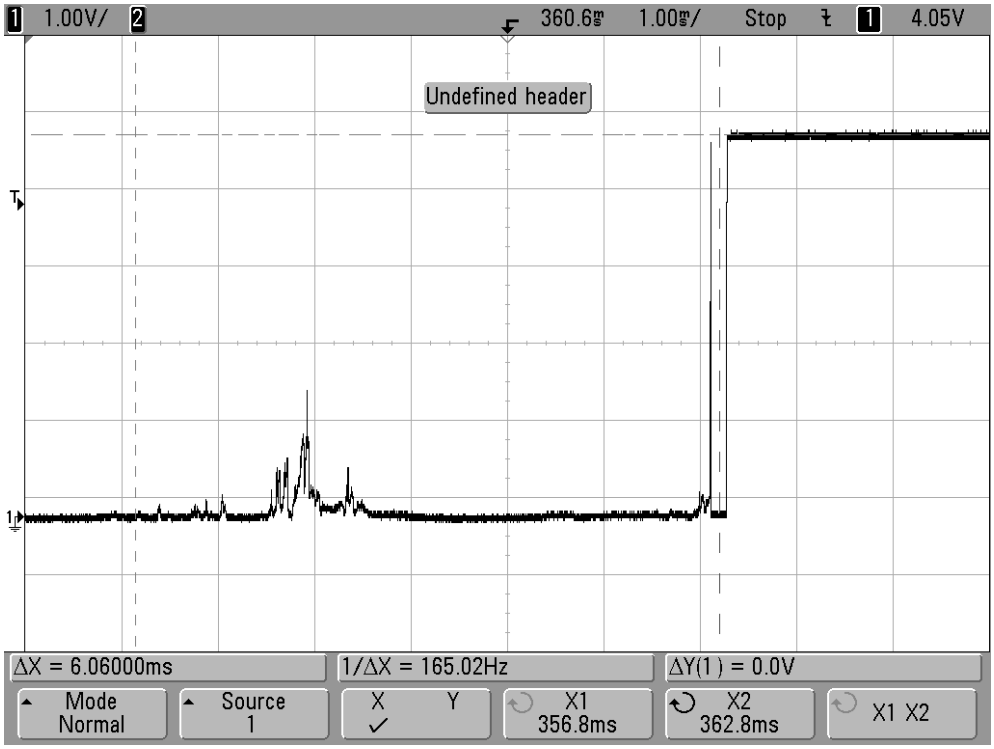

Figure 5: Output after SPDT button is debounced with 20 pF capacitor

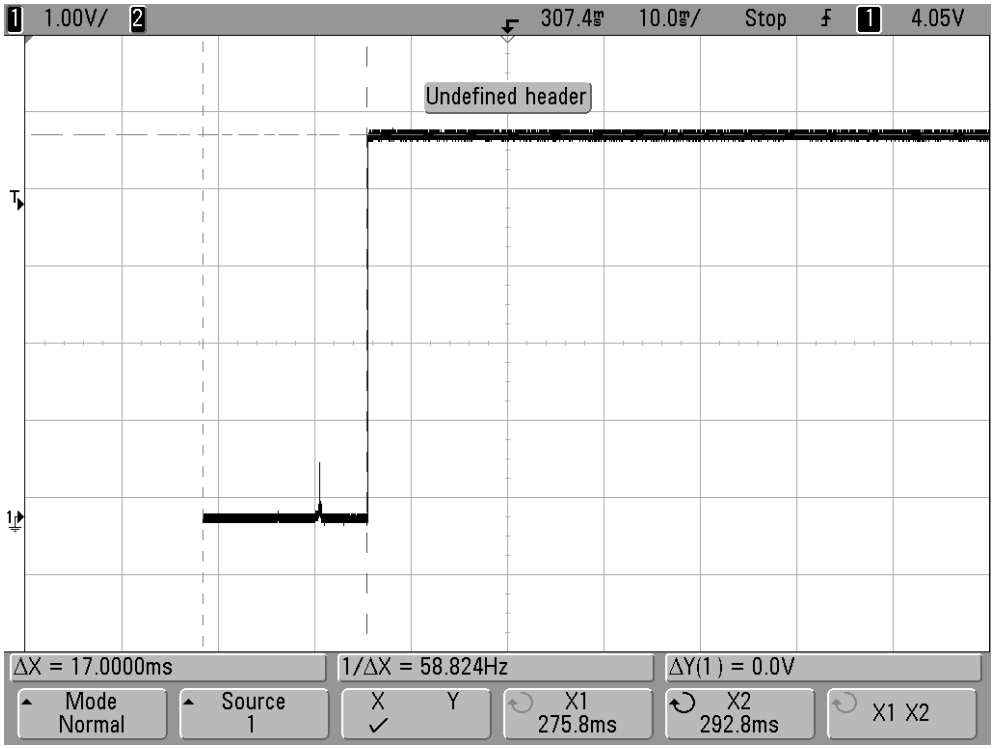

Figure 6: Output after SPDT button is debounced with capacitor

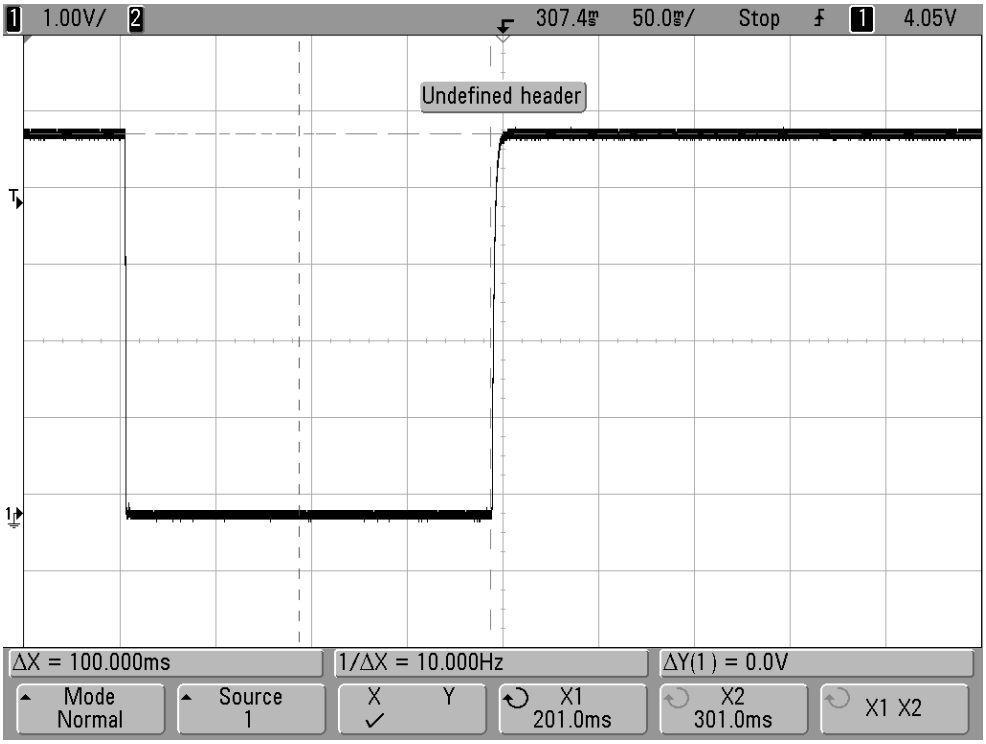

Figure 7: Output after SPDT button is debounced with capacitor

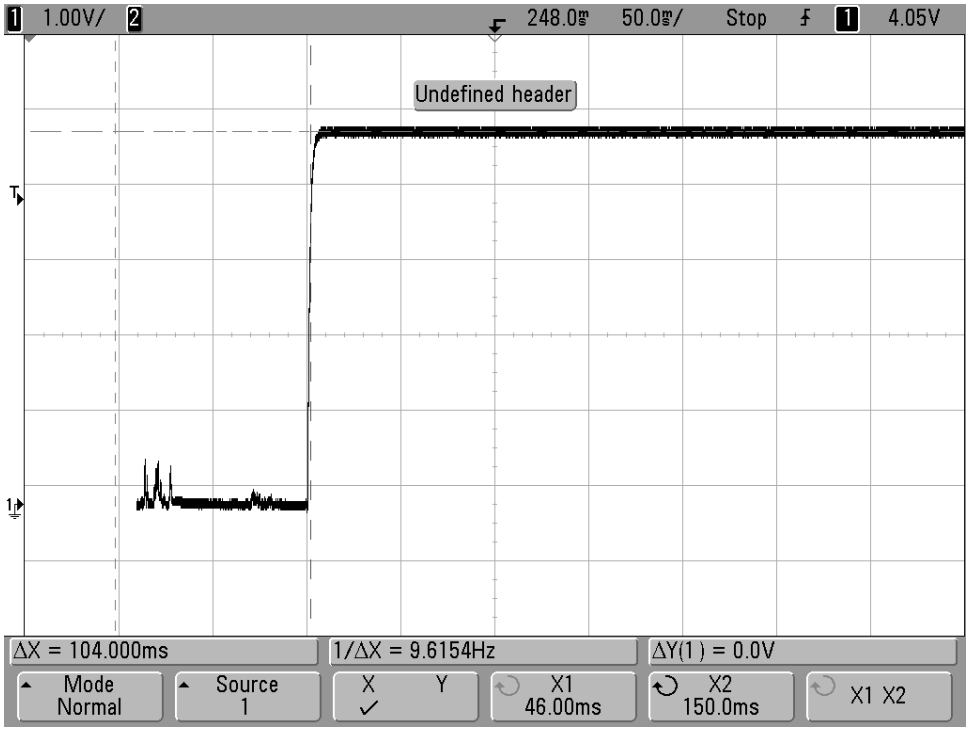

Figure 8: Output after SPDT button is debounced with capacitor

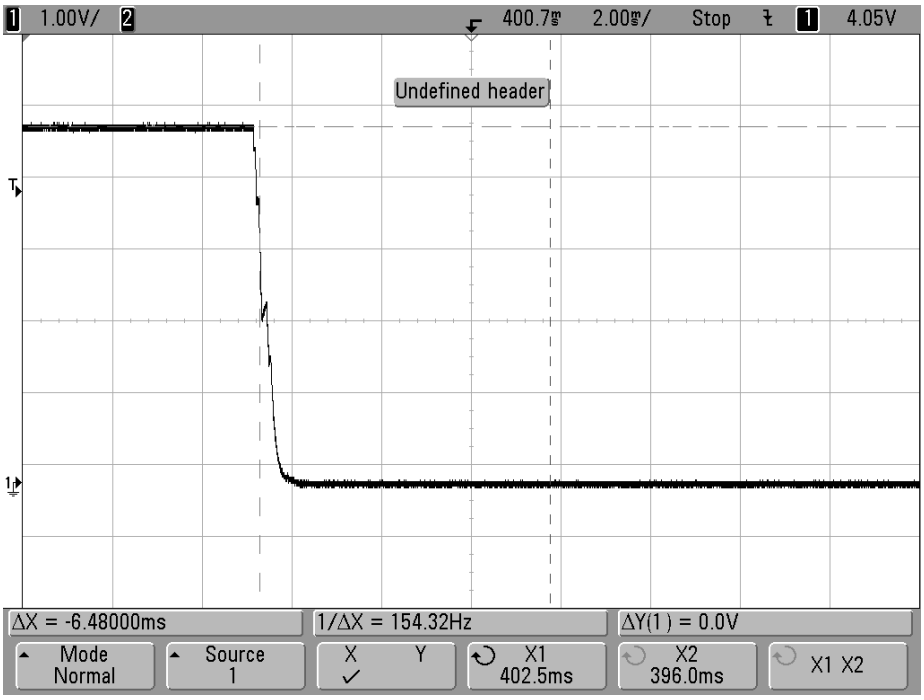

Figure 9: Output after SPDT button is Debounced with capacitor

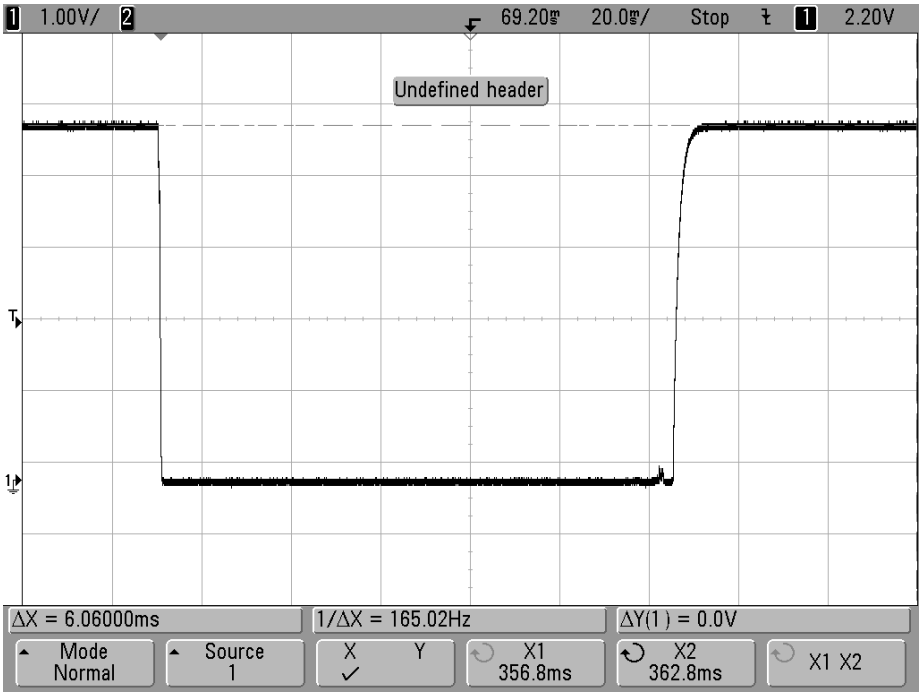

Figure 10: Output after SPDT button is Debounced with capacitor

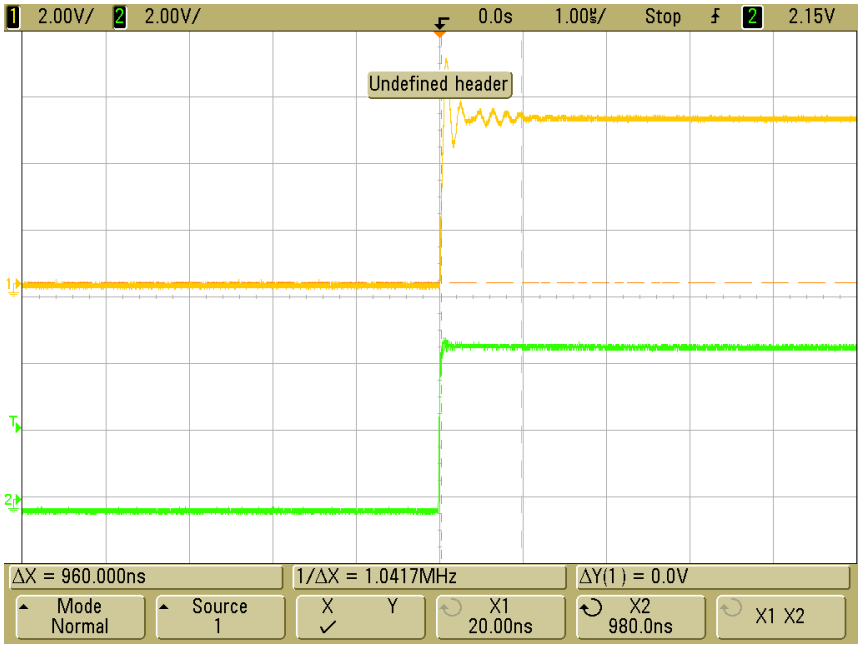

Figure 51: Propagation Delay of And Gate 74LS08

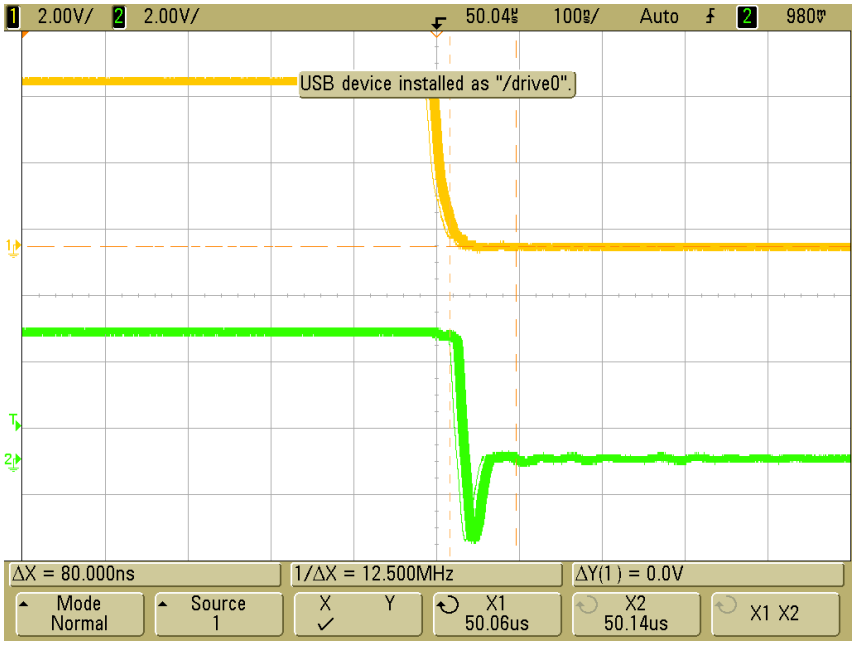

Figure 62: Propagation Delay of And Gate 74LS08

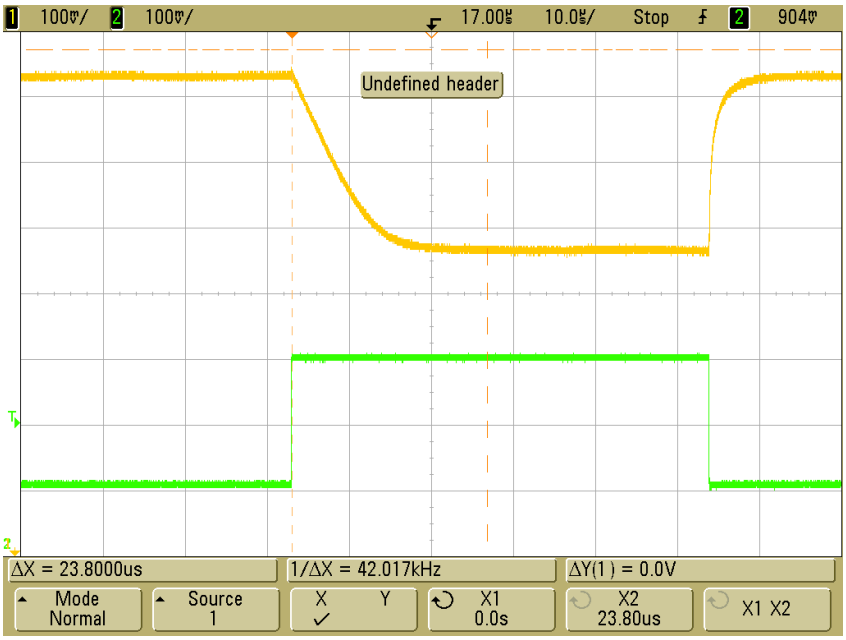

Figure 13: Propagation Delay of Nand Gate 74LS00

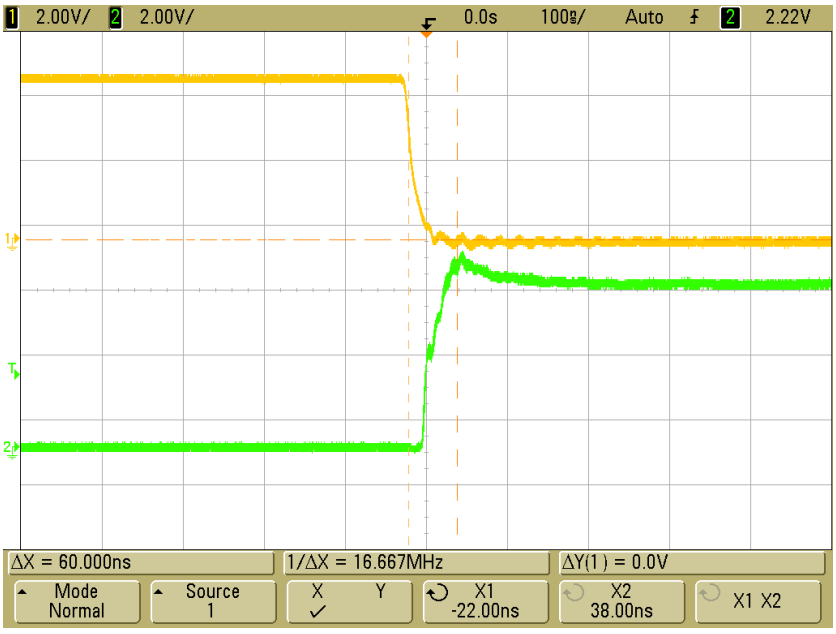

Figure14: Propagation Delay of Nand Gate 74LS00

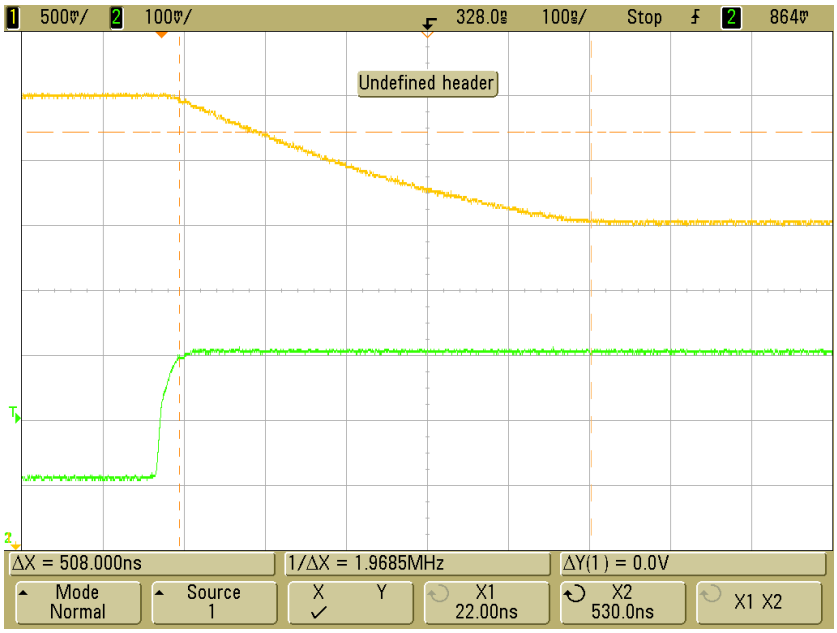

Figure15: Propagation Delay of Not Gate 74LS04

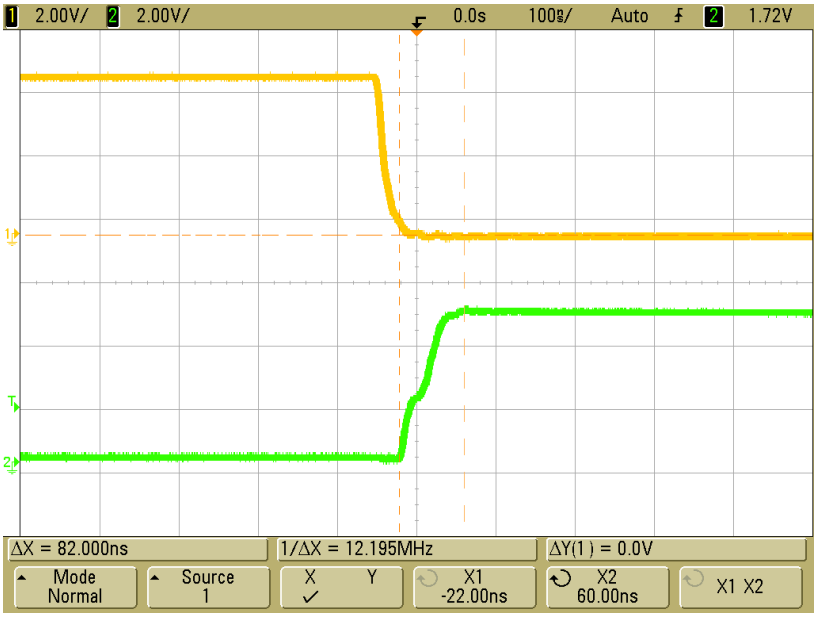

Figure16: Propagation Delay of Not Gate 74LS04

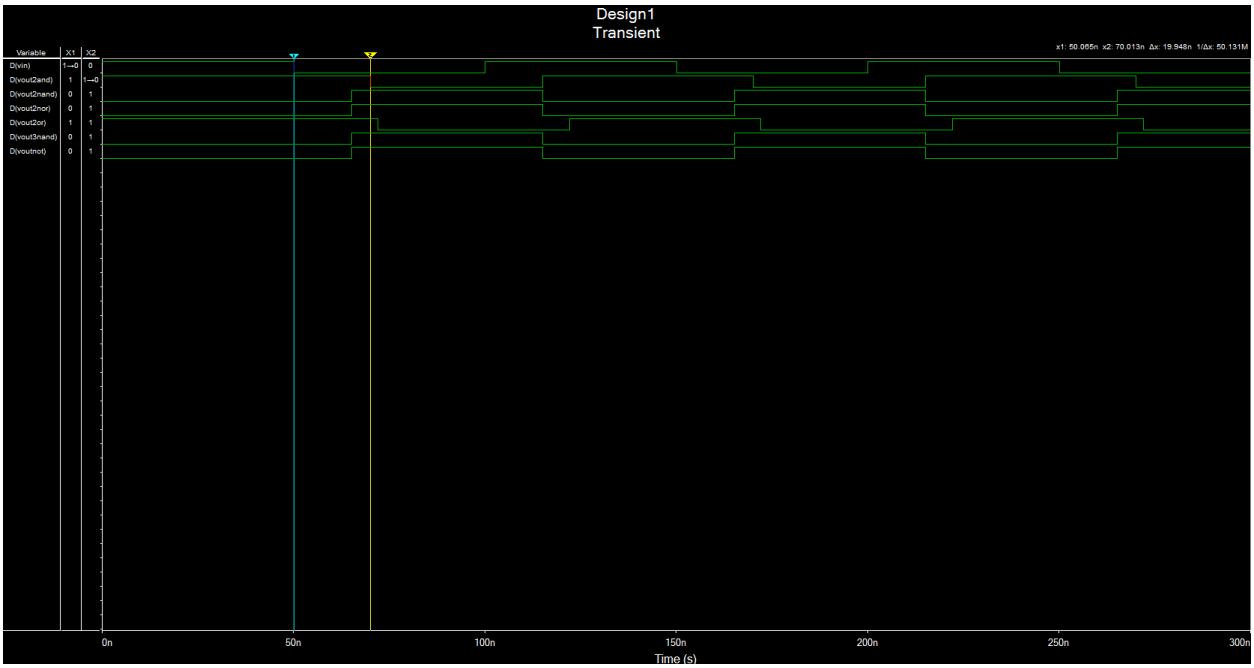

Figure 77:Propagation Delay High to Low And Gate in Multisim, 19.948 ns

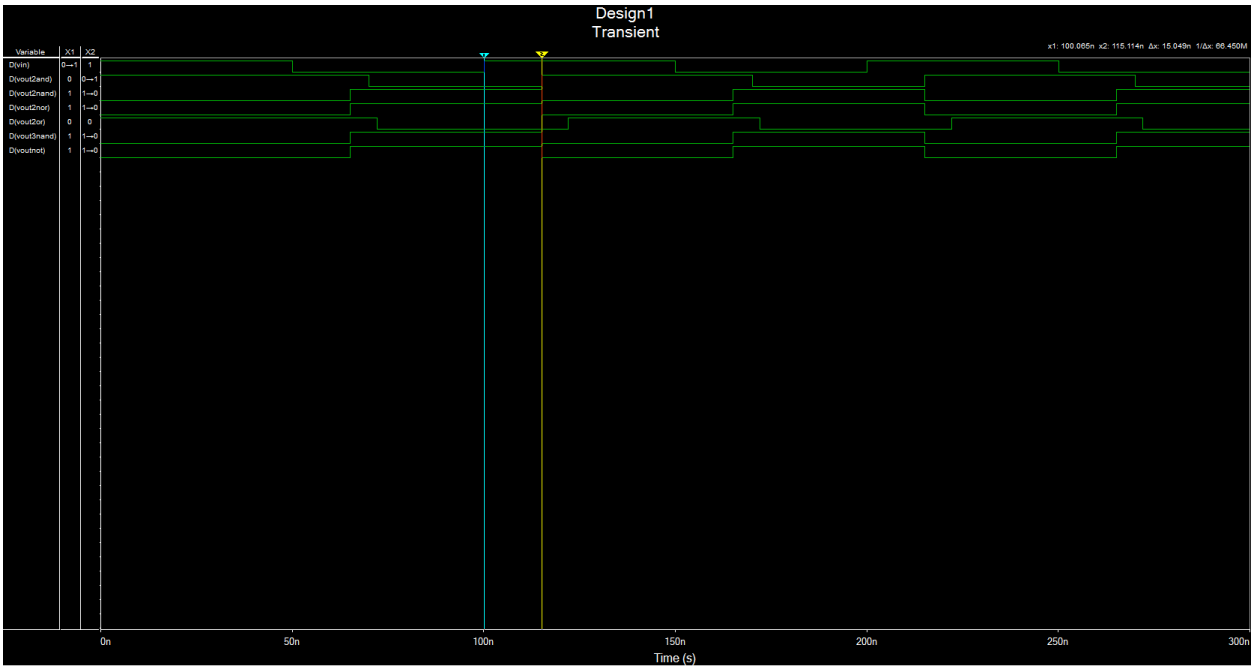

Figure 88: Propagation delay High to Low Nand, Nor, 3 input Nand, Not Gate in Multisim, 15.049 ns

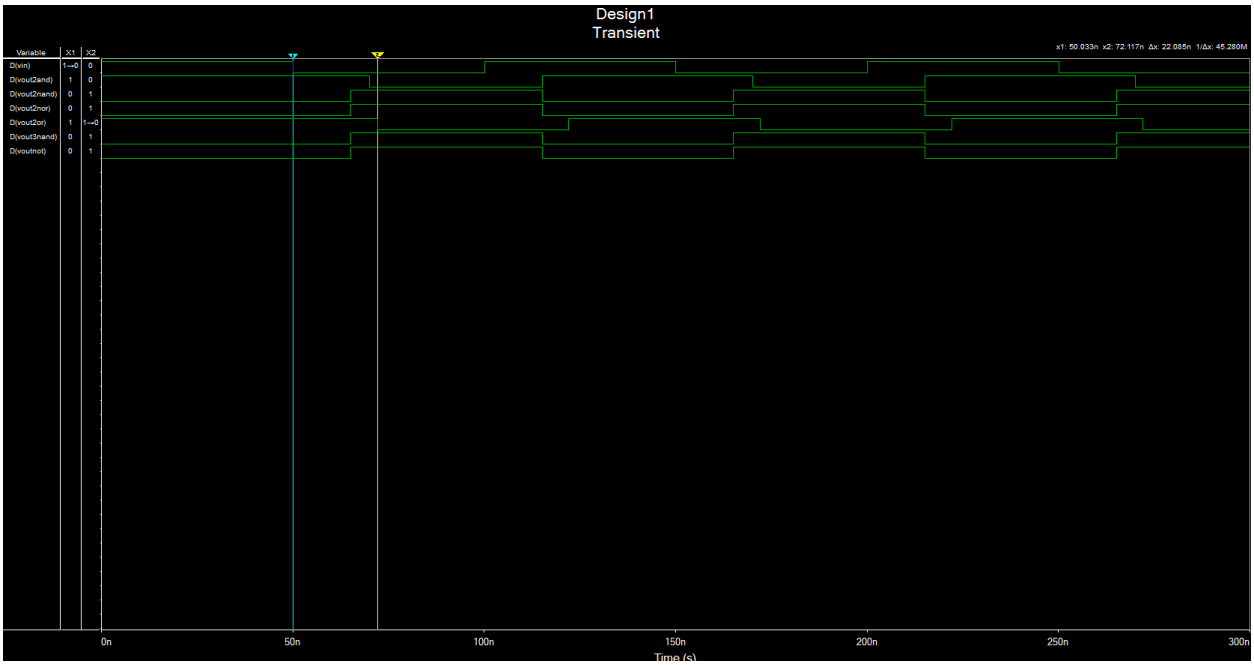

Figure19: Propagation delay High to Low Or Gate, 22.085 ns

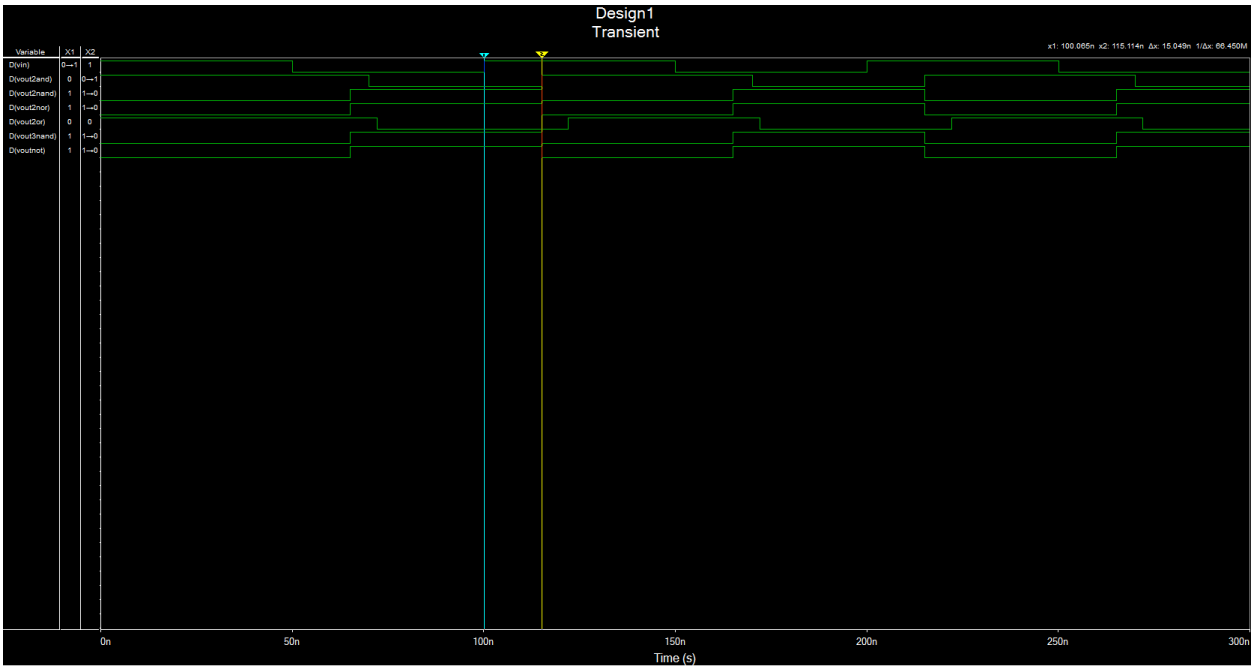

Figure 20: Propagation delay Low to High and Gate, 15.049 ns

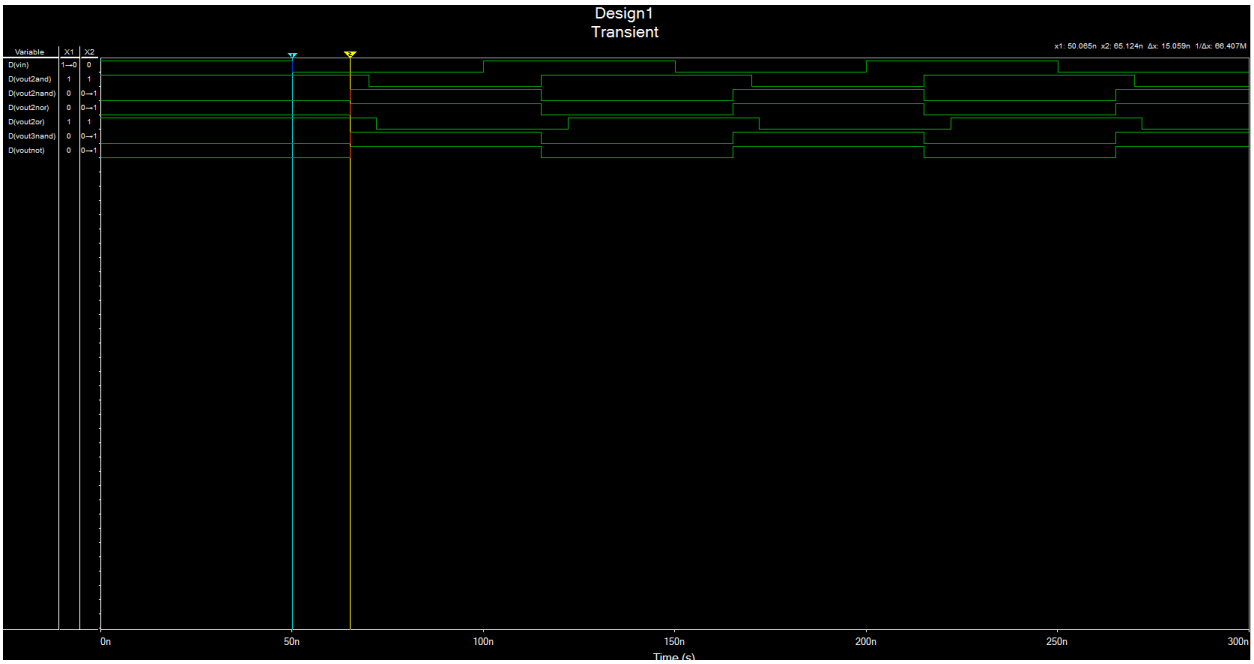

Figure 91: Propagation delay Low to High nand, Nor, 3 input nand , Not Gate 15.059 ns

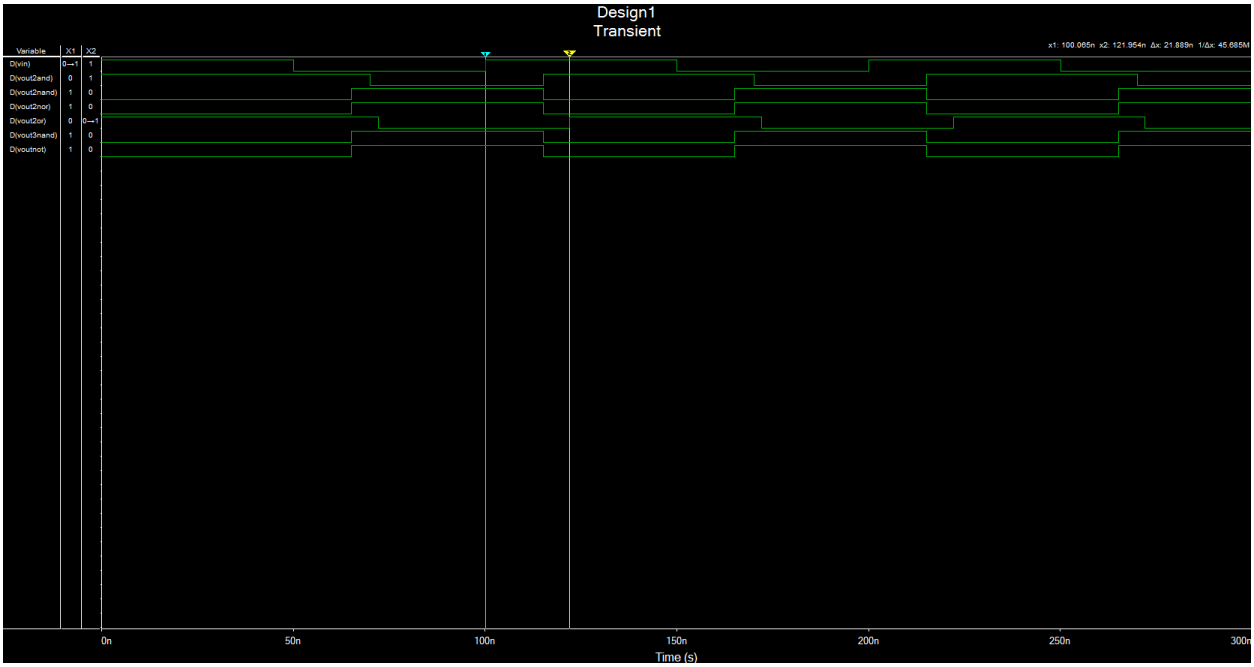

Figure22: Propagation delay Low to High Or Gate, 21.889 ns

$$Percent\ Error = \frac{|Theoretical - Actual|}{Theoretical} * 100 \quad (1)$$

$$T = C(R1 + R2) \quad (2)$$

Table 1: Comparison of Propagation Delay Theoretical, Simulation, and Hardware

Boolean Gates	Theoretical Propagation Delay (ns)	Simulation Propagation Delay (ns)	Hardware Propagation Delay (ns)	Percent Error Theory vs Simulation	Percent Error Theory vs Hardware
And T_{PLH}	8	15.049	960	88.11%	11900.00%
And T_{PHL}	10	19.948	80	99.48%	700.00%
2 input Nand T_{PLH}	9	15.059	60	67.32%	566.67%
2 input Nand T_{PHL}	10	15.049	23.8	50.49%	138.00%
Not T_{PLH}	9	21.825	82	142.50%	811.11%
Not T_{PHL}	10	14.977	508	49.77%	4980.00%
Nor T_{PLH}	10	15.059	N/A	50.59%	N/A
Nor T_{PHL}	10	15.049	N/A	50.49%	N/A
3 input Nand T_{PLH}	9	15.089	N/A	67.66%	N/A
3 input Nand T_{PHL}	10	15.049	N/A	50.49%	N/A
Or T_{PLH}	14	21.889	N/A	56.35%	N/A
Or T_{PHL}	14	22.085	N/A	57.75%	N/A

Explanation

The essential problem with switches is that they are mechanical and often cheaply made, which causes the denounce effect or noise which triggers multiple false positives. The first step of the lab was to use the single pull double throw switch or and SPDT switch. This switch was used to take an observation of the contact debounce and the time at which it is accruing. The time at which the debounce was accruing was used to design an RC filter to filter the noise. Figure 3 shows the results of the button pressed before the filter was applied. The results show that the bouncing is happening around 1.00ms which is the time constant used in order to calculate the RC values for the circuit. Equation 2 was used to calculate the capacitance and resistance used in order to filter out the noise.

Using this time constant drawn from the debouncing without the RC circuit, and RC circuit was designed. Figures 5 through 10 show the results of the RC values being added to the system where the deboucing of the circuit was being filtered. The best RC value were found based on the how well the signal of being filtered from a low to a high state. Figure 9 shows the final RC circuit chosen. For the first calculation R1 was given as 5.476 KΩ and R2 was .462 KΩ . Using these resistor values 20pf was chosen. Due to the issues with the values chosen here the RC values were as 10 KΩ R1 R2 as 10 KΩ and a C value of 1nf.

The button was next used to drive the state machine, and a flip flop was used for logic implementation. The first design that was implemented was in the simulation, Figure 3 shows the circuit diagram of the JK Flip Flop design. To verify logic switching the LED was used, when on the system would be in one state and off the system would be in the next. The JK flip flop will toggle when both J and K or set to high. When the clock or in this case the button, press is asserted the J and K values get asserted only on an edge. The next step was to implement this in hardware due to set backs and malfunction of the J k flip flop design. The Hardware was implemented using the D flip flop the circuit can be seen in Figure 2, The D flip flop does not toggle, when the clock is asserted on the rising edge and the D input is high the out or Q becomes high.

The last step in the lap was to test the propagation delay of certain gates and comparing the values to simulation and experimental results. The propagation delay or gate delay is the time taken for the output to change after input is changed, which will be needed when implementing these gates in our circuit design. Figure 1 shows the circuit diagram of these gates using a 10Mhz clock input. Figures 17 through 22 show the results of the propagation delay in Multisim. Due to the lack of time, only three of the gates were implemented and tested in hardware shown in figures 11 through 16. The gates that were implemented in hardware was the 2 input and gate, the 2 input nand gate, and the inverter.

The results from all three measurements can be seen in Table 1. The error in the results seems high, the worse error was at 11,900% error. This higher percentage error could be due to

many experimental factors. First the simulation and the gates very in the fact that the gates are do not take in to consideration the real-life tolerance from chip to chip. Also, another factor that might have led to this very higher percentage error was the noise on the signal, as seen in Figures 11 through 16 there is a lot of noise on the output signal. Another possibility is human error in measuring the correct delay value.

In all, the lab was a success the goal of the lab was to build a state machine to drive the system and measure the propagation delays of gates. This goal was reached building a properly working state machine and propagation measurements were taken. Although some of the measurements had a higher percentage error then anticipated the overall lab was a success.

Appendix

Appendix 1: State Machine Schematic using D Flip Flop