ECEL 304
LECTURE 1

This course offers laboratory experience, using both modeling software and digital and analog hardware relevant to both electrical and computer engineers.

Personnel

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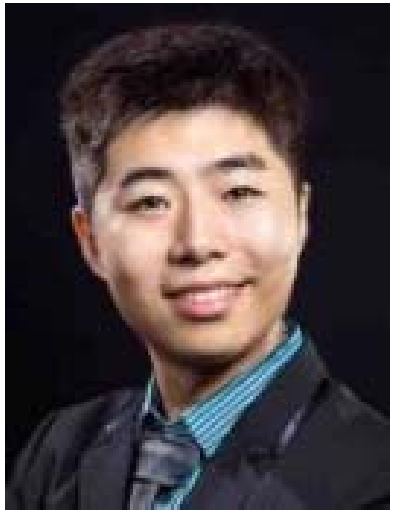

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BY APPOINTMENT ONLY

Course Description

- **Build an audio recorder**
  - **10 week design project (entire term)**
  - **Record from mic, playback through speaker**
  - **ADC, DAC and RAM**
  - **Counters, Timers, Gates, Flip-flops, etc.**
- **Practical experience with circuit building and design**
  - **Design aspect will be stressed**
- **Circuit simulations done in Multisim**
  - **Very Similar to OrCAD Cadence**

Course Operation

- 1 Hour Lecture in Nesbitt 111
  - Lecture will be recorded and posted within a day
  - No electronic devices (phones, laptops, etc.)
- 2 Hour Lab in Bossone 205
  - No open toed-shoes
  - Come to lab prepared
- Primarily rely on BBLearn
  - Currently in progress of getting it up…
  - All communication/announcements
  - Lab report submissions
  - Grade distribution
  - Lecture videos
  - Make sure you enable email notifications

Expectations

- Attendance is mandatory!
  - Work in groups of 2 (same group entire term)
  - Equal work between all group members
- At LEAST 4-6 Hours of work outside of lab
- Assignments turned in on time
  - Late policy explained later
- Academic honesty
  - See Drexel's policy on this: http://www.drexel.edu/provost/policies/academic_dishonesty.asp
  - WILL FOLLOW VERY STRICTLY

Grading

Attendance	**5%**
Quizzes	**20%**
Worksheets	**20%**
Reports	**20%**
Initial Project Checkoff	**15%**
Final Project Checkoff	**20%**
Extra Credit #1	**5%**
Extra Credit #2	**5%**

Attendance

- Attendance is MANDATORY
  - For both Lecture AND Lab
- Lecture Attendance (5%)
  - Use Dragoncard to sign-in
  - Your responsibility to make sure you sign in
- Lab Attendance
  - Determined by worksheet checkoff
  - Report will NOT be accepted if absent

Quizzes (20%)

- Each quiz is 10 Points and 10 Minutes Long
- Will be given at the very beginning of lab
- NO make-up quizzes will be given
  - Unless you have a doctor's note, funeral, etc.
  - Do NOT miss a lab
  - Do NOT show up late to lab
- Will cover material from previous weeks
  - Pay attention during lecture AND lab
- Format will vary
  - Multiple Choice, Short Answer, True/False, etc.
- Announced ahead of time
  - During lecture and/or through BBLearn

Worksheet (20%)

- Each worth 10 Points
- Group assignment (1 worksheet/group)
  - Cannot work outside of your group
  - Same grade for all individuals in the group
- To be checked off by the end of lab
  - Will NOT be accepted after lab is over
  - Will be at the complete discretion of your TA
  - Your responsibility to get it checked off
- Keep worksheet after it is checked off
  - Use as reference to write your lab report
  - Do NOT just copy & paste from your worksheet
  - Do NOT submit your worksheet with your report

Proj. Checkoff (35%)

- **Initial Project Checkoff (15%)**
  - Ensure you are on track and nearly complete
  - Successfully recording from Function Generator
  - Successfully playing back on Oscilloscope
- **Final Project Checkoff (20%)**
  - Fully completed AND functional audio recorder
  - Successfully recording from microphone
  - Successfully playing back on speaker
- **Rubric used for each project checkoff**
  - Will be based on your projects design, quality and performance

Extra Credit (10%)

- Extra Credit #1 (5%)
  - Implement additional functionality to recording/playback that wasn't covered
  - Including but not limited to: advanced filtering, bass boost, automatic gain control, etc.
- Extra Credit #2 (5%)
  - Use microcontroller to replace external circuitry
  - Control logic, amplifier, maybe even RAM?
- Partial credit given
  - Depends on complexity and completeness
- May do either one, both or neither
- More details to follow…

Reports (20%)

- 100 Points
- Individually written reports
  - See "Academic Honesty Policy" in syllabus
- Due Friday by 11:59 PM (BEFORE MIDNIGHT)
  - Friday of the next calendar week the lab was performed
  - Submit via BBLearn (Do NOT email it)
  - 3% penalty per day late
  - Not accepted after 4 weeks

Report Format

- Cover Page (5%)
  - Use the one provided on BBLearn!
- Objective (10%)
  - State what you're trying to accomplish/purpose
  - Very concise summary of what you did
  - DO NOT paraphrase the lab procedure
  - Some background info (provide reference if required, cite properly)
  - 1 - 2 paragraphs long

Report Format

- **Results (35%)**
  - **Tables**
    - **Manual voltage sweep, resistor tolerances, etc.**
  - **Graphs (Any and all collected)**
    - **Multisim output, oscilloscope screen capture, etc.**
  - **Equations**
  - **Correctly labeled**
  - **Elaborate where appropriate**

Report Format

- **Explanation (50%)**
  - **1 – 2 pages long**
  - **Discusses and explains your results (reference your graphs, tables and equations)**
  - **Compare theoretical, simulated and experimental**
  - **Answer any/all questions in lab procedure**
  - **Discussion of errors AND sources of error**
  - **Example:**
    - **"We calculated the theoretical voltage to be 3.53 V (Equation 2) but the experimental design yielded 3.49 V (Table 6), an error of 1.13% (Table 7). This is attributable to the tolerance of the resistor (Table 5) being..."**
  - **Make a conclusion, did you achieve your objective?**

Report Format

- References
  - Optional, but you MUST provide this if you used an outside source
  - MUST use IEEE format
- Appendix
  - Also optional
  - Include only if you have data that isn't required but feel should be included
  - Calculations, figures, tables, etc..

Report Structure

- **FOLLOW GIVEN FORMAT!!!**
- **General guidelines apply**
  - **Page numbering, labeling equations, figures and tables appropriately (IEEE formatting)**
  - **Points WILL be taken off for incorrect spelling/grammar/formatting**
- **Use worksheet as a guide to help you**
  - **Do NOT copy and paste from worksheet**
- **See "Lab Report Structure Guide"**

Report Recap

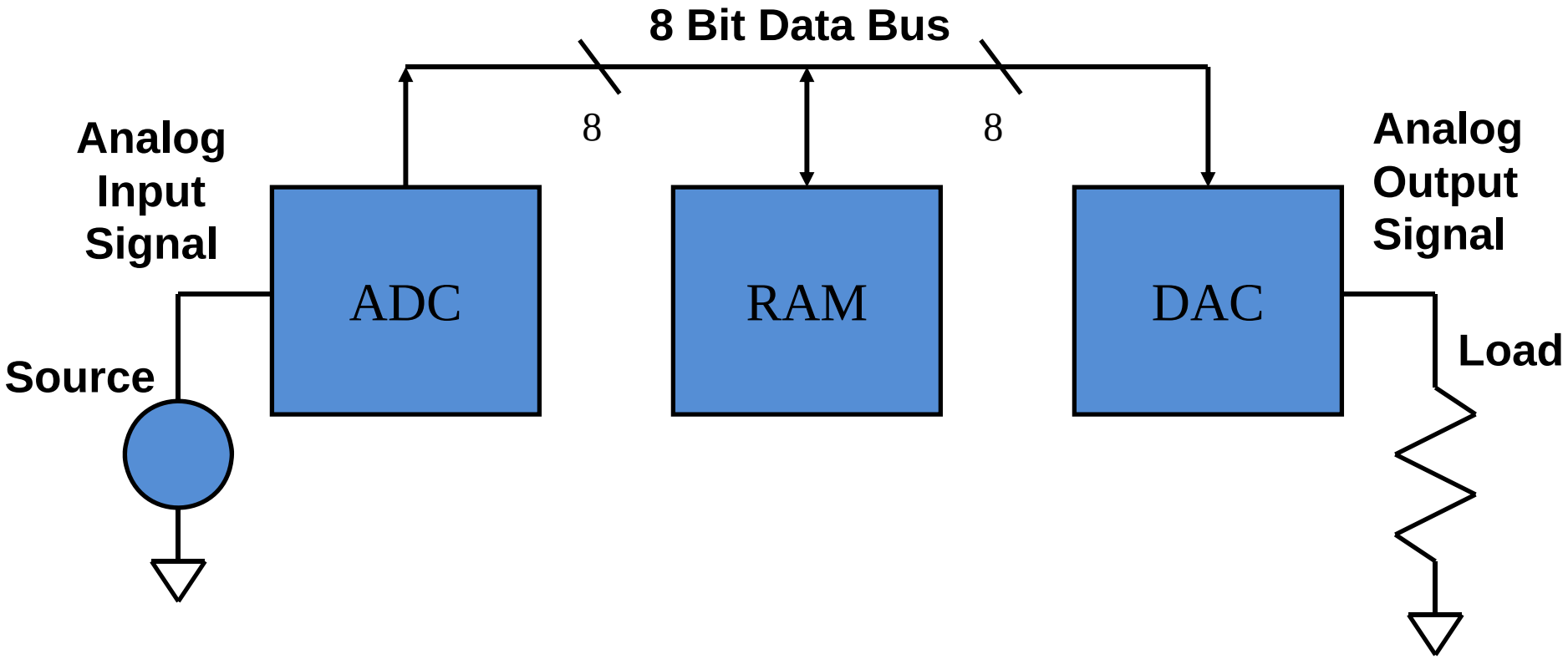
- Cover Page (5%)
- Objective (10%)
- Results (35%)
- Explanation (50%)
- References (Optional)
- Appendix (Optional)

Worth 20% of your final grade

Questions?

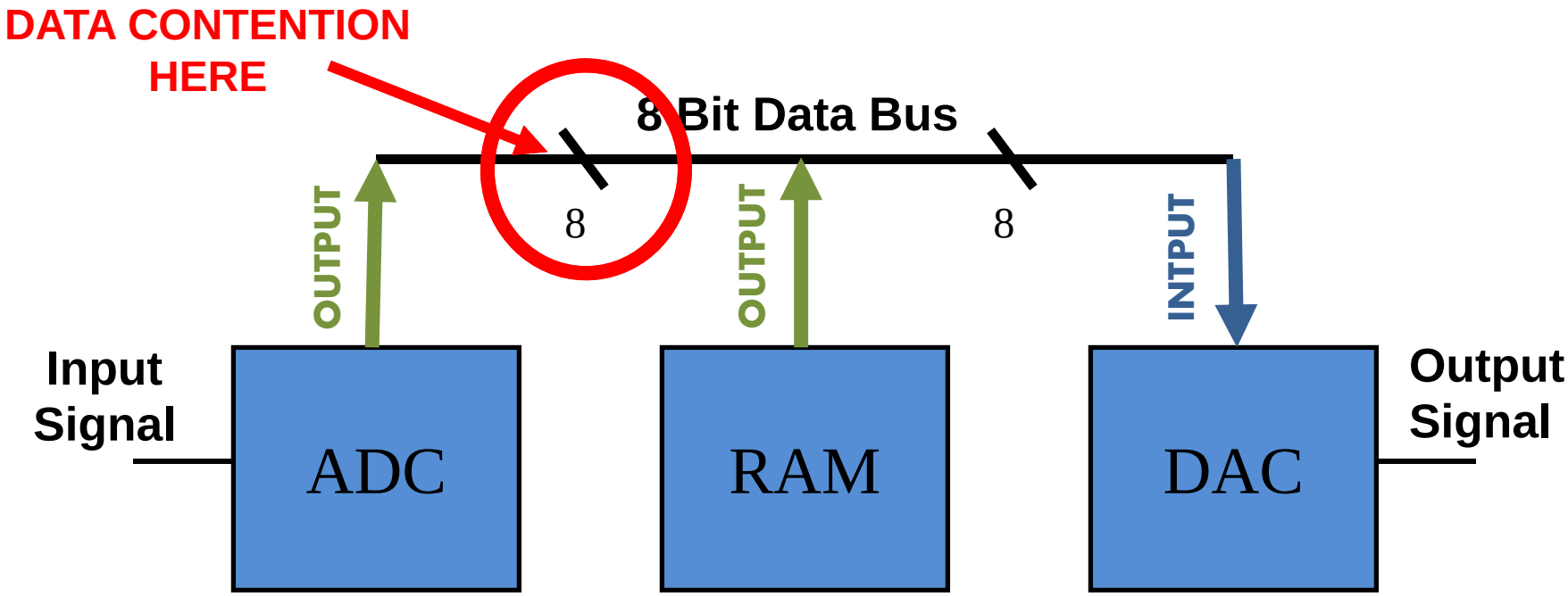
Project Overview

Eventually try to achieve this:



- **ANALOG INPUT goes into ADC, converts to DIGITAL**
- **DIGITAL goes into DAC converts back to ANALOG**
- **DIGITAL goes/comes out of the RAM**

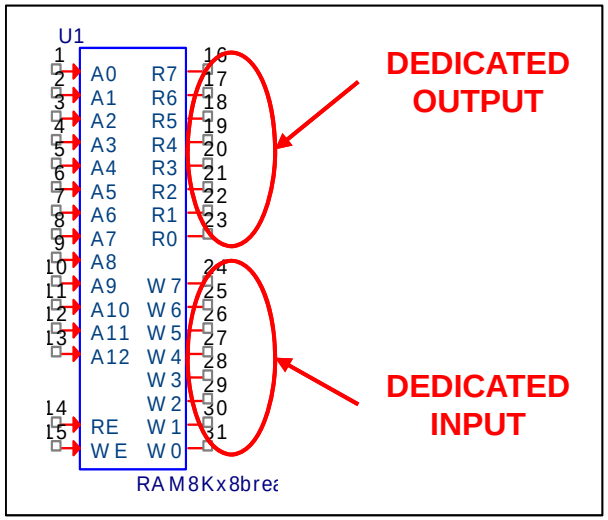
Data/Bus Contention

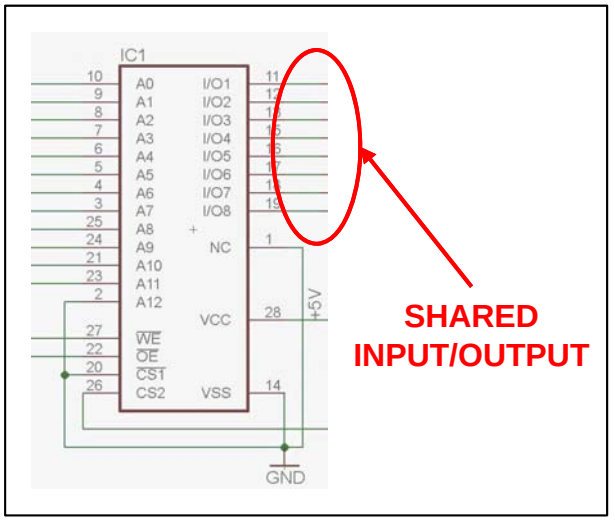


- **Two simultaneous outputs**
  - **Outputs "fight" to assert value on line**
  - **Leads to ambiguous or unknown data**
  - **Could damage hardware**
  - **AVOID AT ALL COSTS!!!**

Data/Bus Contention

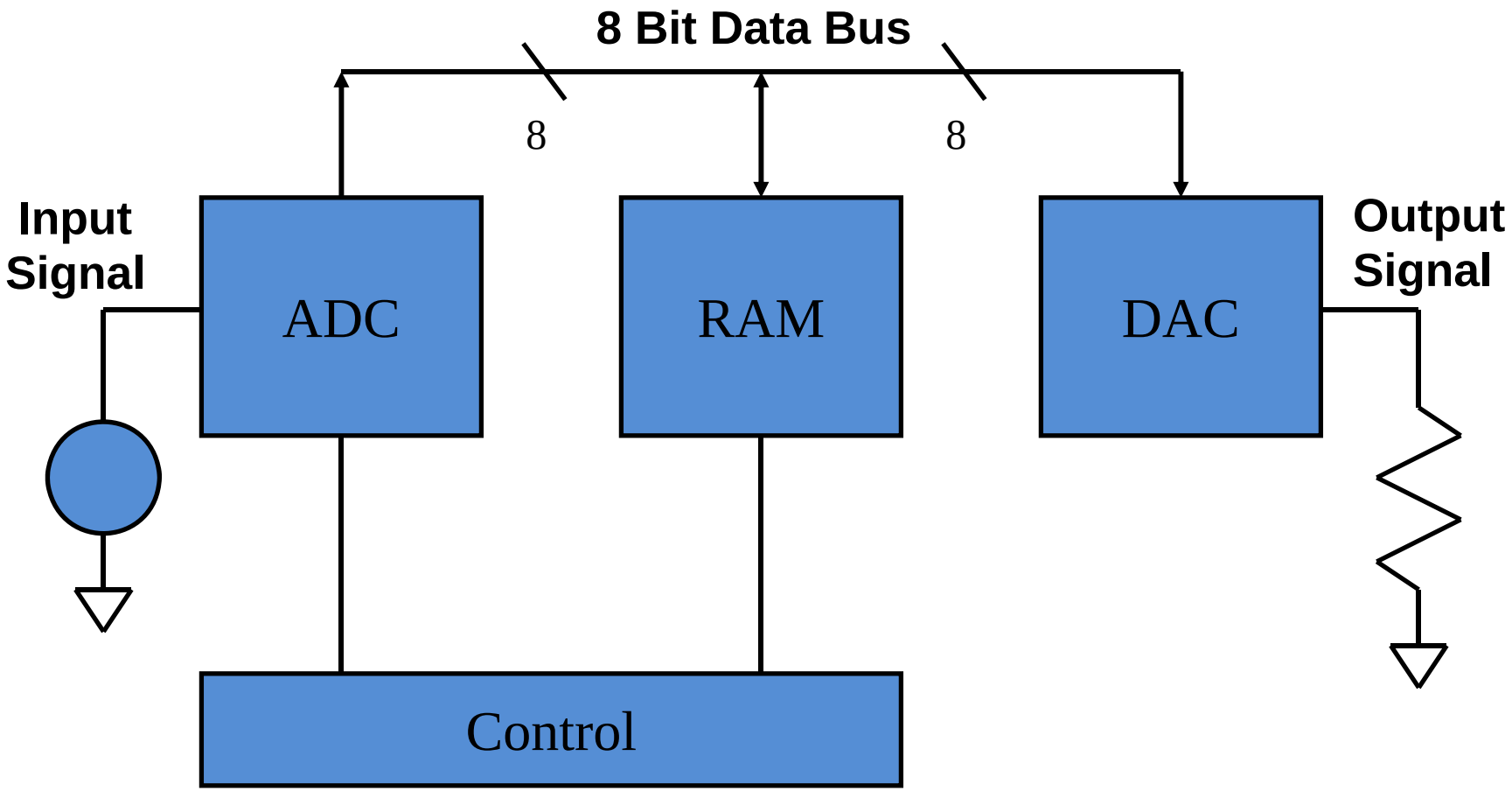
- Problem arises because of the RAM
- Most RAMS use the same lines for INPUTS AND OUTPUTS
  - MUST switch between READ or WRITE
  - Can either READ or WRITE to RAM at a time
  - CANNOT do BOTH simultaneously



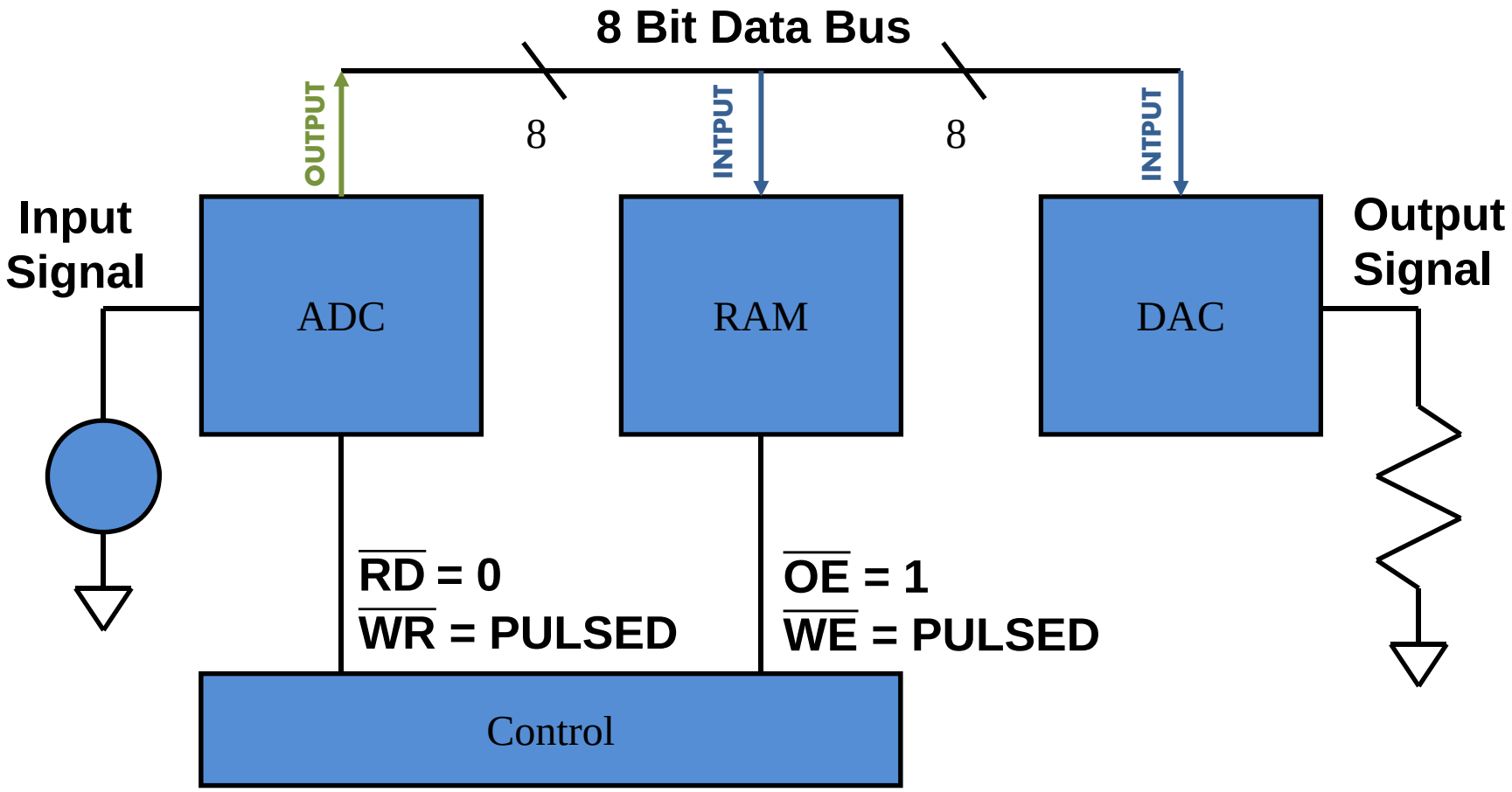


Contention Solution

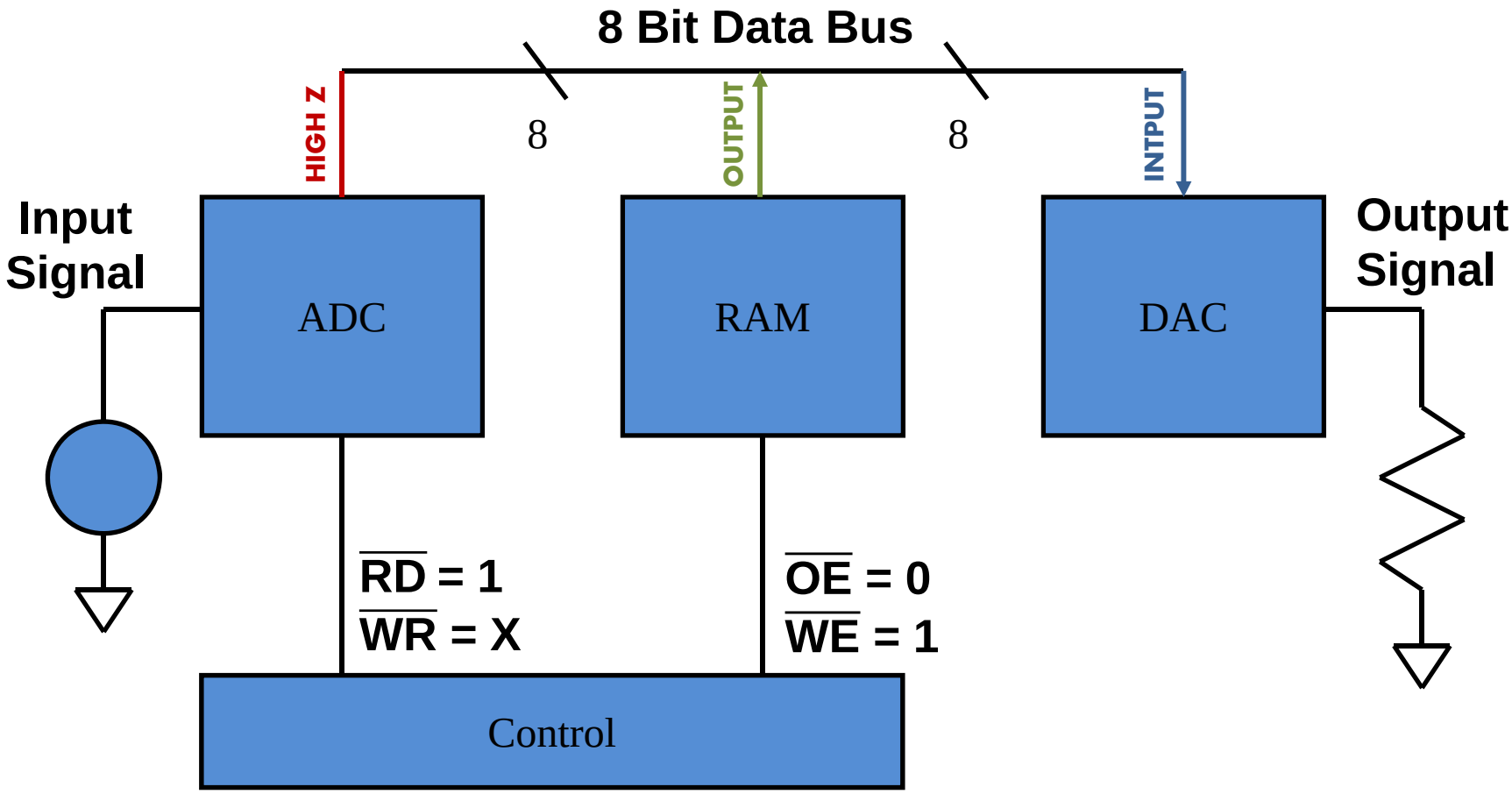
- **Add Control Circuitry to the system**
- **ADC MUST have control pins**



Recording Phase



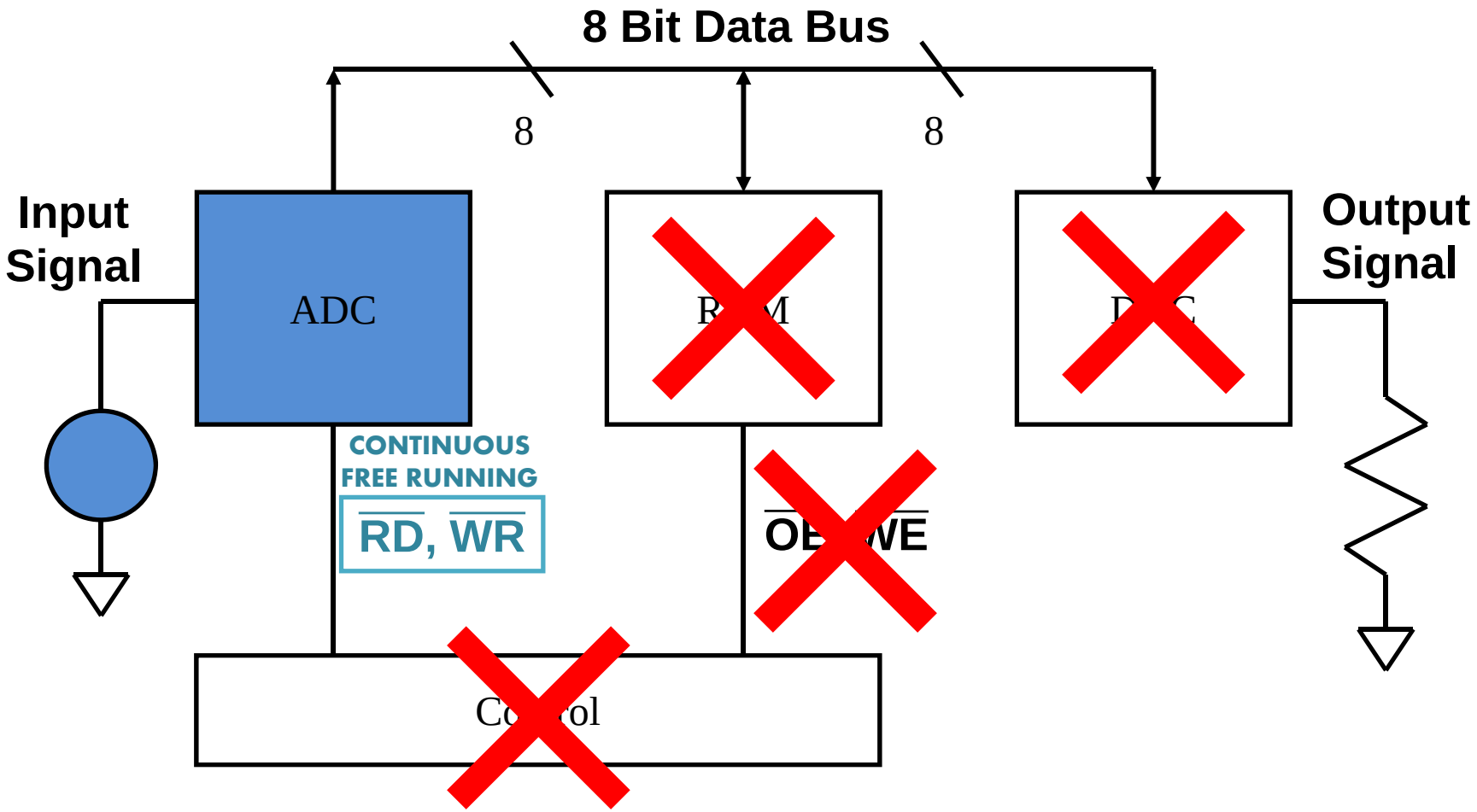
Playback Phase



NOTE: ADC is put into HIGH Z state, ADC output is disabled

Lab Overview

For this week, we'll do the following:



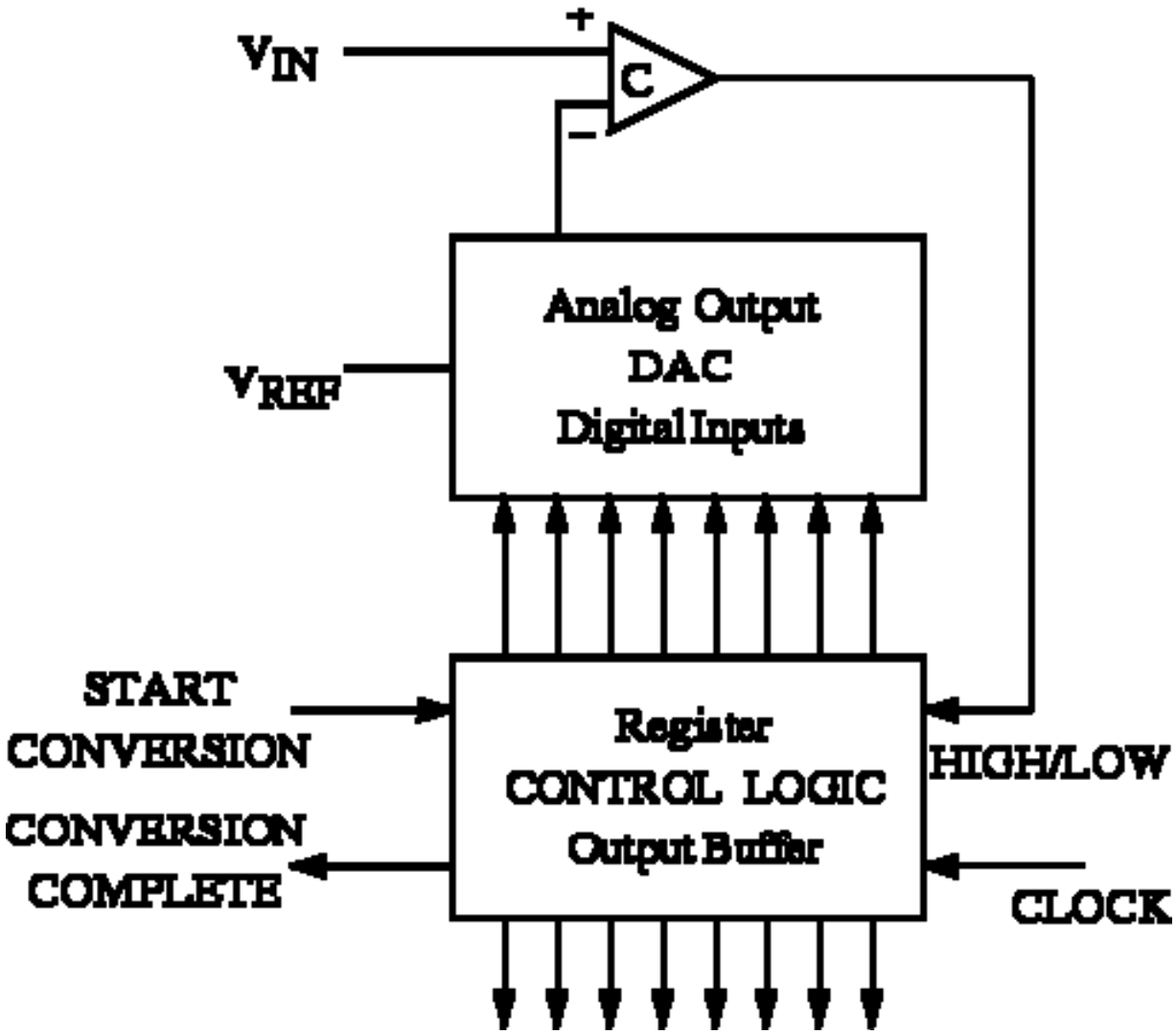
ADC Reintroduced

- ADC (Analog to Digital Converter)
  - Should be familiar from ECEL 303
  - Converts a given voltage input into digital bits
    - Number of digital bits or outputs vary depending on the ADC
- Will be using the ADC 0804
  - 8 bit output
  - Capable of self-clocking
  - Can disable output (Put in High Impedance)
- Will test on ECEL 304 Board this week

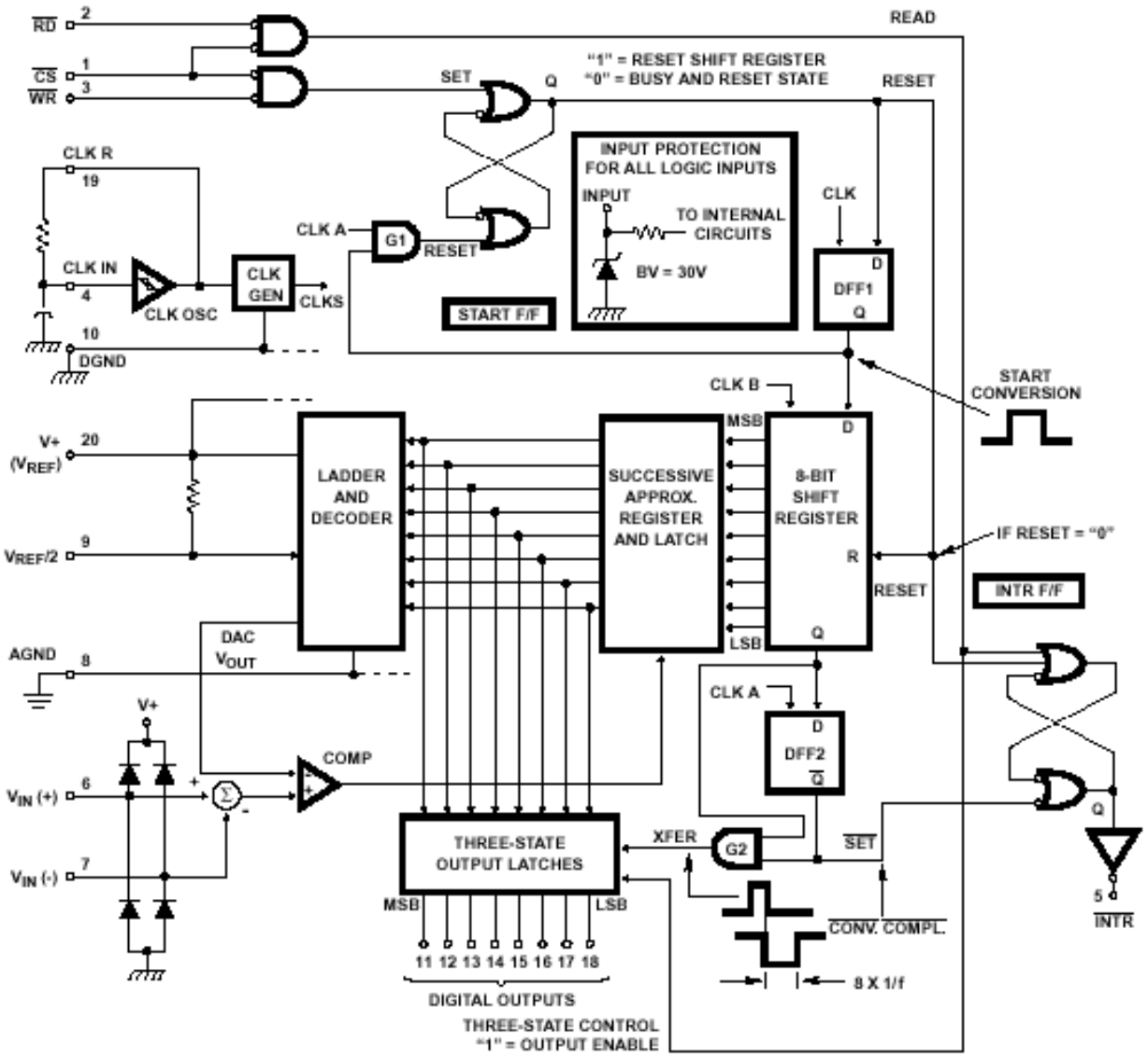
Suc. Approx. ADC

- **Successive Approximation ADC**
  - **This design requires only a single comparator and will be only as good as the DAC used in the circuit.**
  - **The analog output of a high-speed DAC is compared against the analog input signal.**
  - **The digital result of the comparison is used to control the contents of a digital buffer that both drives the DAC and provides the digital output word.**

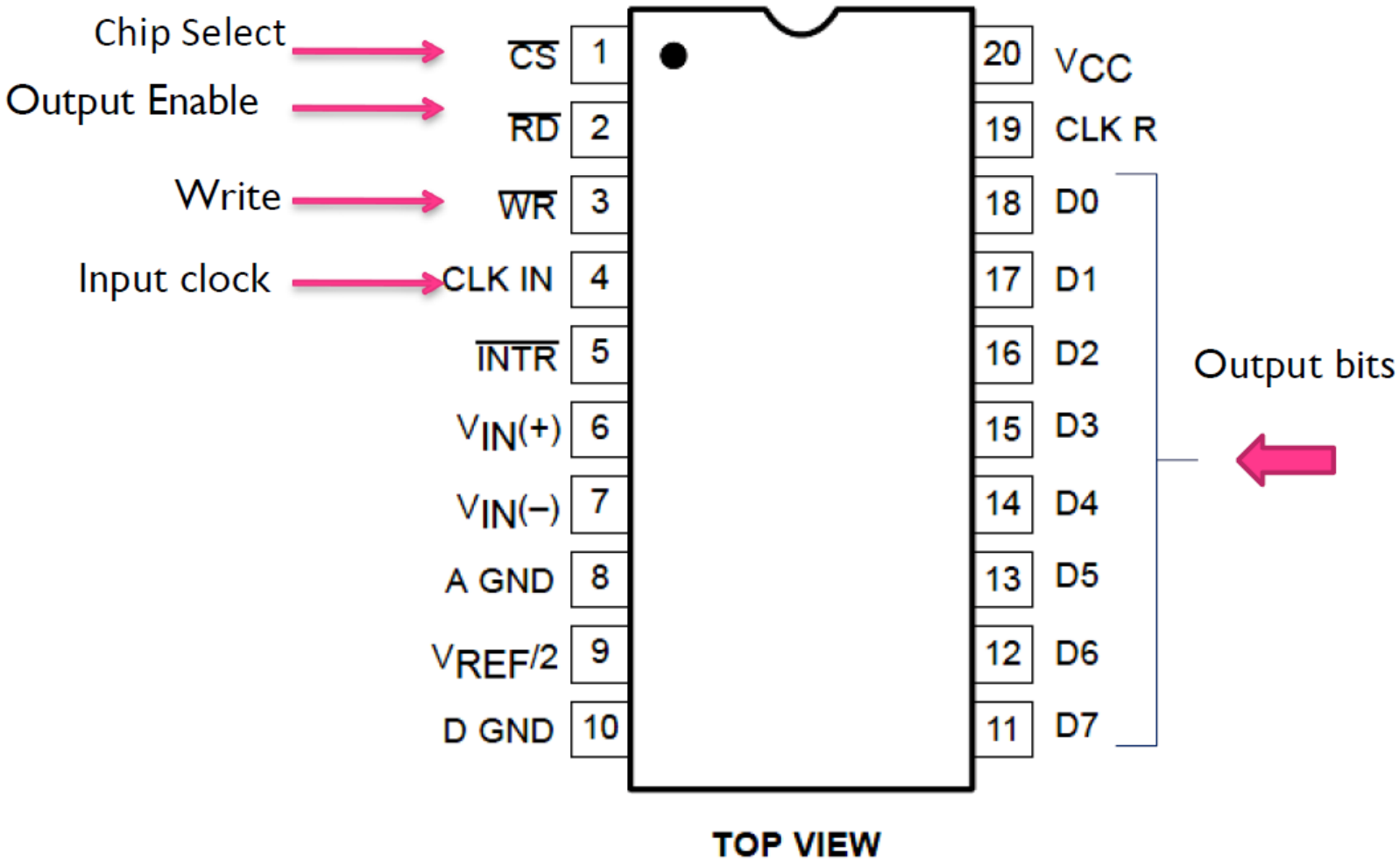
Suc. Approx. ADC



Inside the ADC 0804



ADC 0804 Schematic



ADC Operation

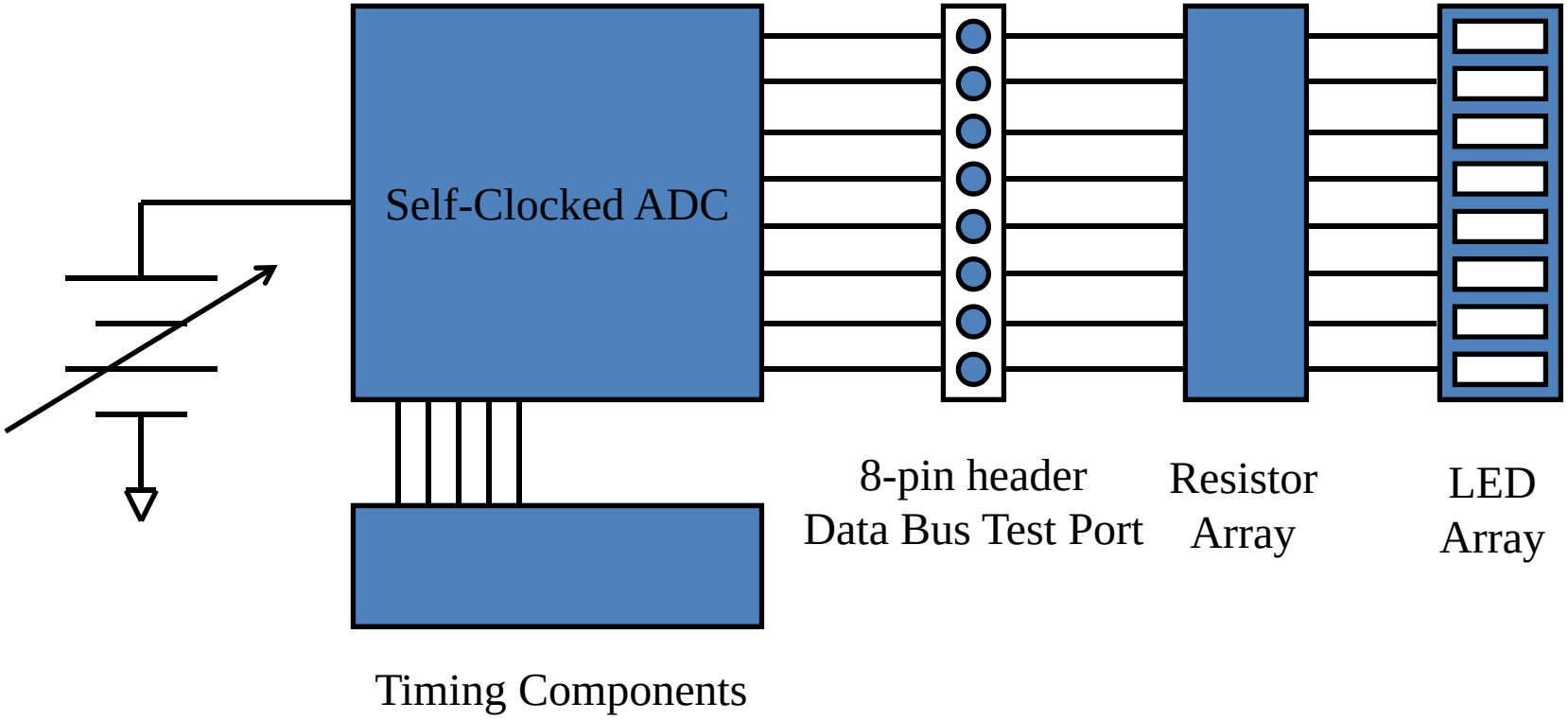


Figure 17/18, ADC0804 data sheet

Self Clocked Mode

- All synchronous digital IC requires a clock signal
  - Allows control over different components used in circuit
  - Keeps components running at same speed or synchronized
  - Components normally operate on either rising or falling edge of clock signal
- ADC 0804 has an internal clock generator
  - Does not need external clock
  - Set by a single timing resistor and capacitor

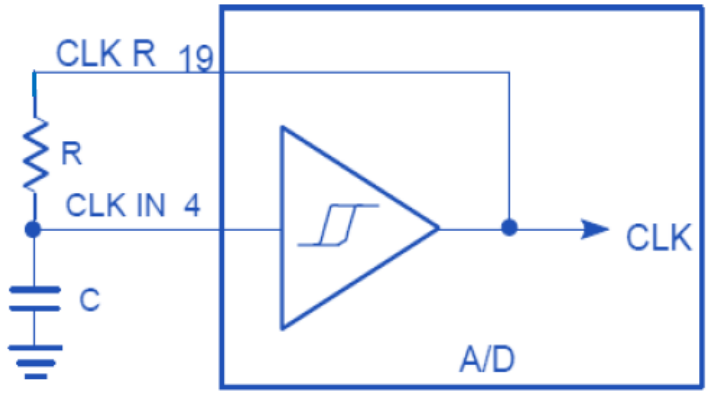
Clock Modes

External Clocking

- An external clock is applied to the clock input of the convertor, pin 4

Internal or self clocking comparator with hysteresis

- Pin 19 is connected to pin 4, the input clock signal
- Clock frequency can be controlled by R and C

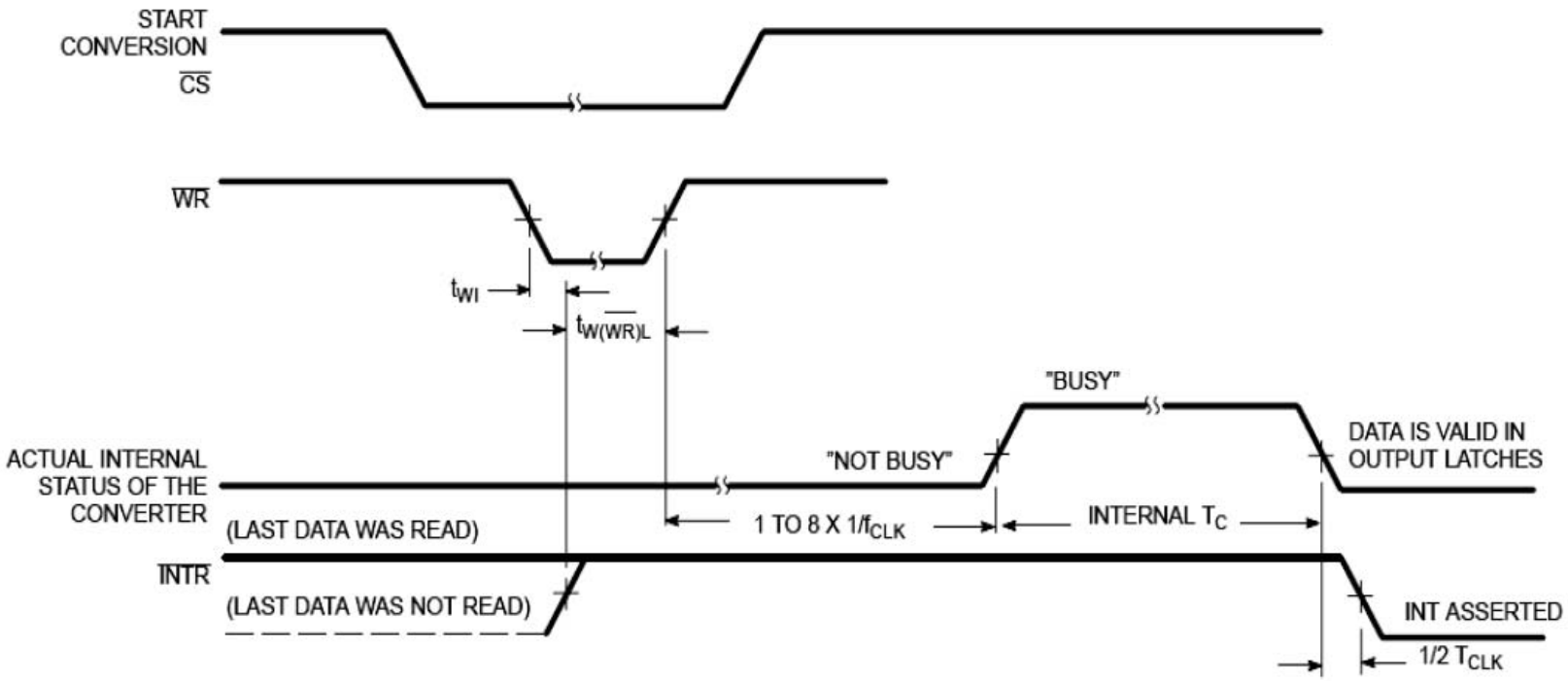


$$f = \frac{1}{1.1RC}$$

ADC 0804 Signals

- **Remember, signals with a bar on top are ACTIVE LOW**
  - **Normally High or 1**
- **Signals (BLUE – OUTPUT, GREEN - INPUT):**
  - $\overline{\text{WR}}$ - **Rising edge of signal starts sampling**
  - $\overline{\text{RD}}$ - **Enables/disables the output**
  - $\overline{\text{INTR}}$ - **Pulses low when done sampling**
  - $\overline{\text{CS}}$ - **Chip select, always goes to ground**
  - GND - **Ground**
  - VCC - **Power, usually +5 V**

Timing Diagram



T_c is 64 clock cycles, total ADC conversion time is about 73 clock cycles

Cont. Free Running

- **ADC will be operated in Continuous Free-Running Mode**
  - **Continuous - Immediately starts sampling again after last sample is determined**
  - **Free-Running - No external circuitry required to make it operate**
  - **In other words, in this mode, the ADC continuously samples the input without any external trigger**

Free Running Mode

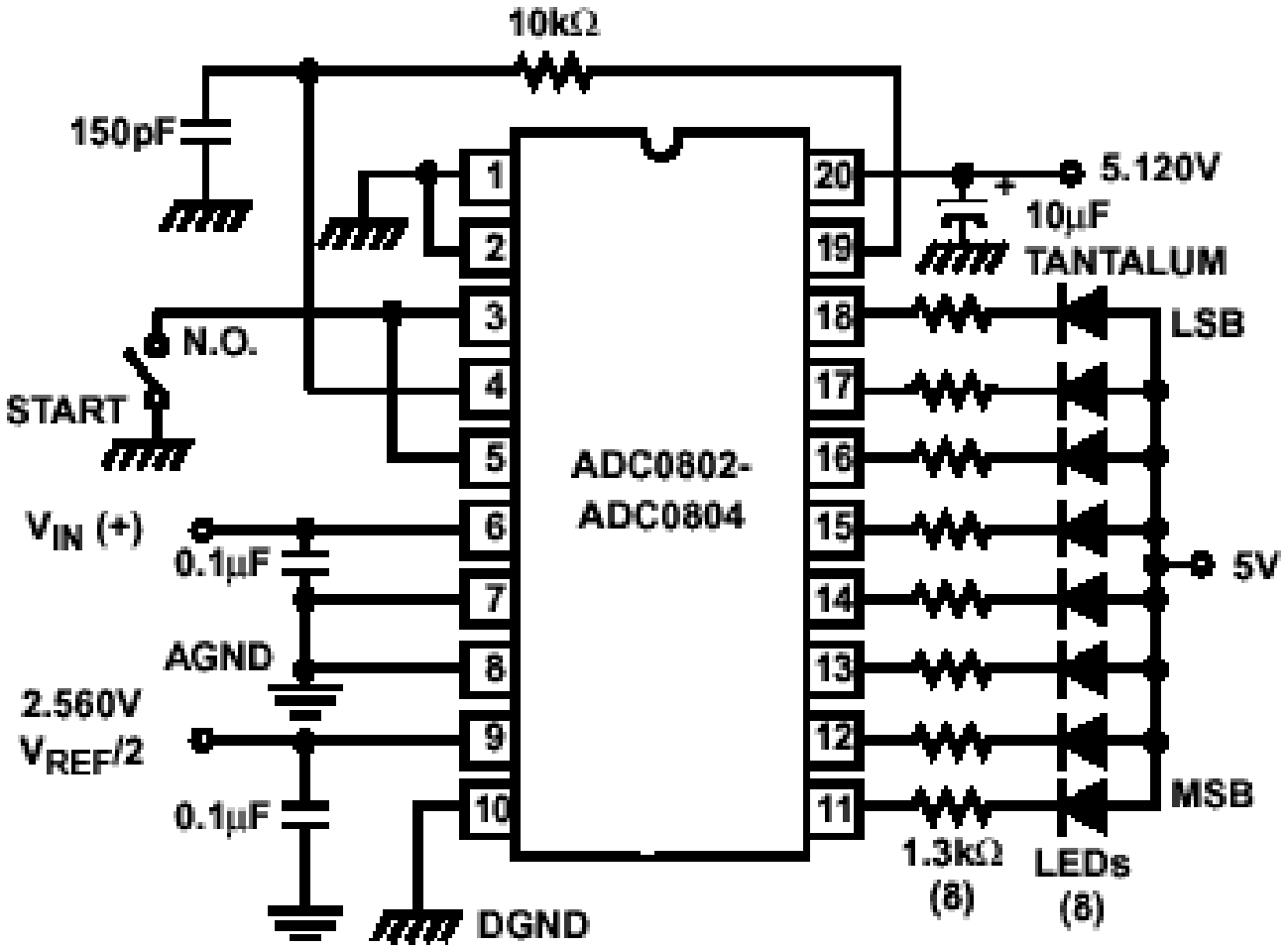


FIGURE 18. BASIC TESTER FOR THE A/D

Calculating Freq

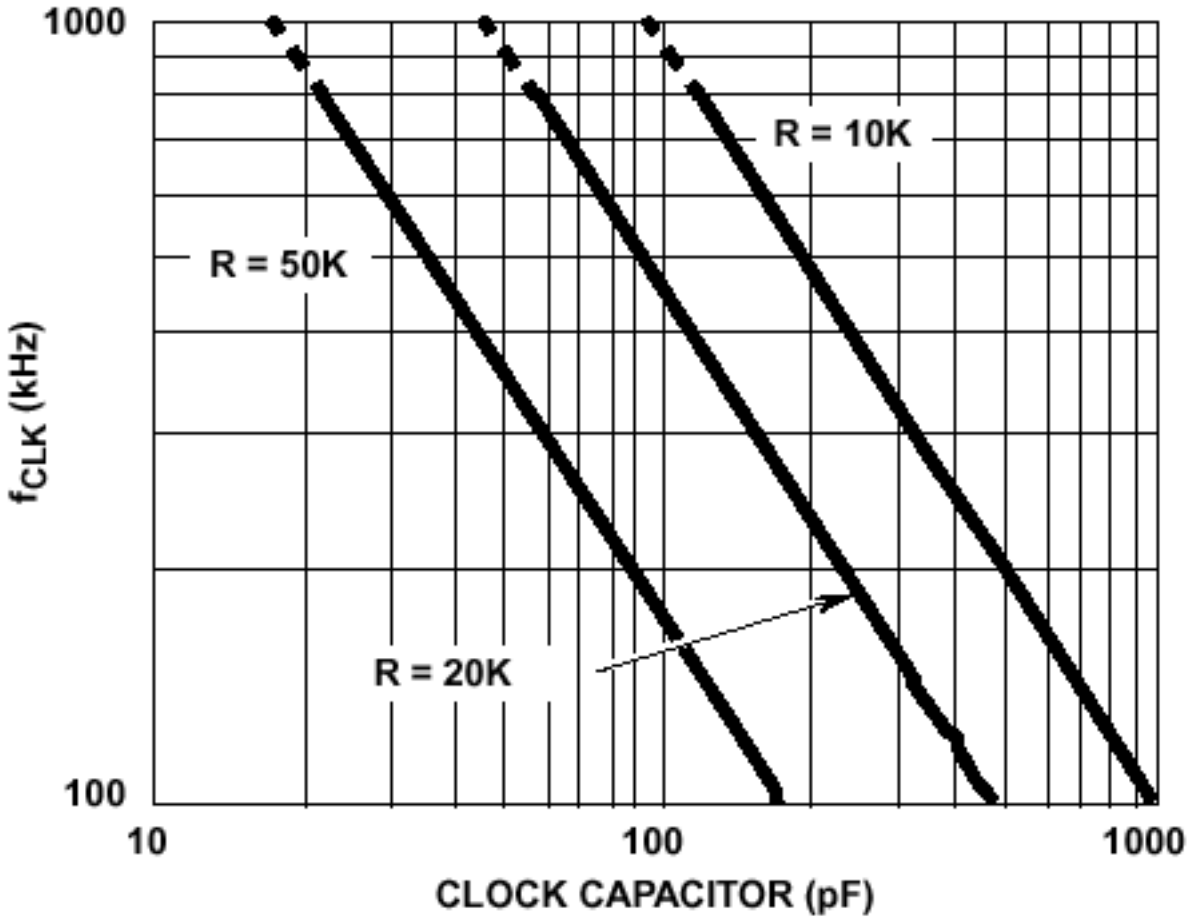


FIGURE 5. f_{CLK} vs CLOCK CAPACITOR

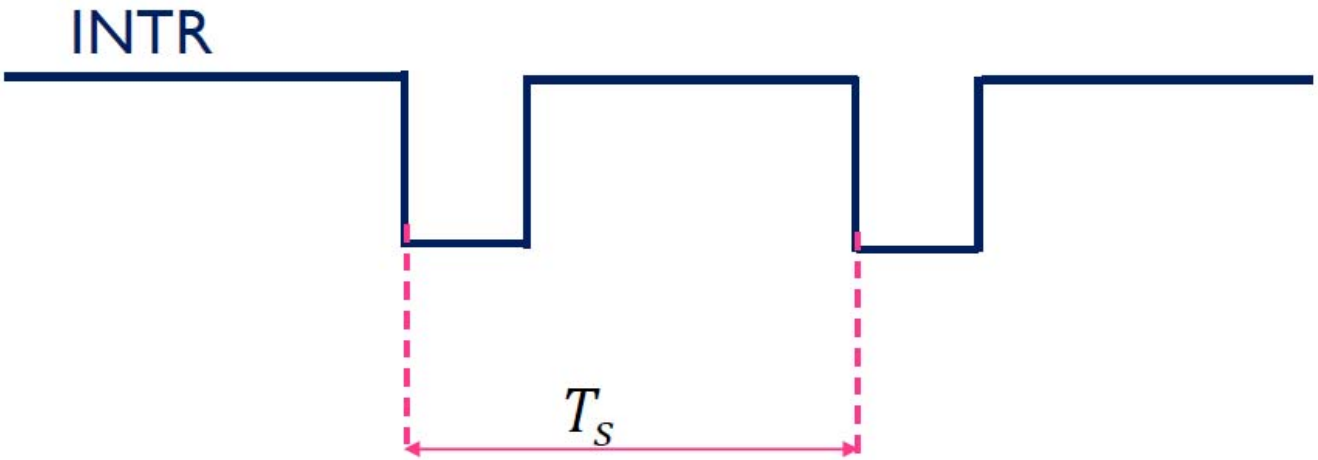
$$f_{CLK} = \frac{1}{1.1RC}$$

$$f_S = \frac{f_{CLK}}{CCPS}$$

$CCPS$:
Clock Cycles
Per Sample

INTR in CFR Mode

T_c= clock cycle or period
f_c = clock frequency



Sampling Frequency $f_s = \frac{1}{T_s}$

$$\frac{f_c}{f_s} = \frac{T_s}{T_c} = \#\ of\ clock\ cycles\ required\ for\ one\ conversion$$

Binary to Decimal

- **Use Base-2 Radix Formula:**

$$N = 2^n B_n + 2^{n-1} B_{n-1} + .. + 2^1 B_1 + 2^0 B_0$$

- **Example: Convert 1001 into decimal**

$$N = 2^3(1) + 2^2(0) + 2^1(0) + 2^0(1) =$$
$$2^3 + 2^0 = 8 + 1 = 9$$

- **BE CAREFUL WHEN CALCULATING FOR ADC!!!**
  - **LEDs are active LOW!!!**
  - **MUST invert (flip) bits first**

Voltage Calculation

- **Your ADC will output 8 bits, which can be grouped as 4 high (MS – Most Significant) and 4 low (LS – Least Significant) bits**
- **The voltage represented by the digital output is given by:**

$$V_{out} = \left(\frac{MS}{16} + \frac{LS}{256}\right) V_{ref}$$

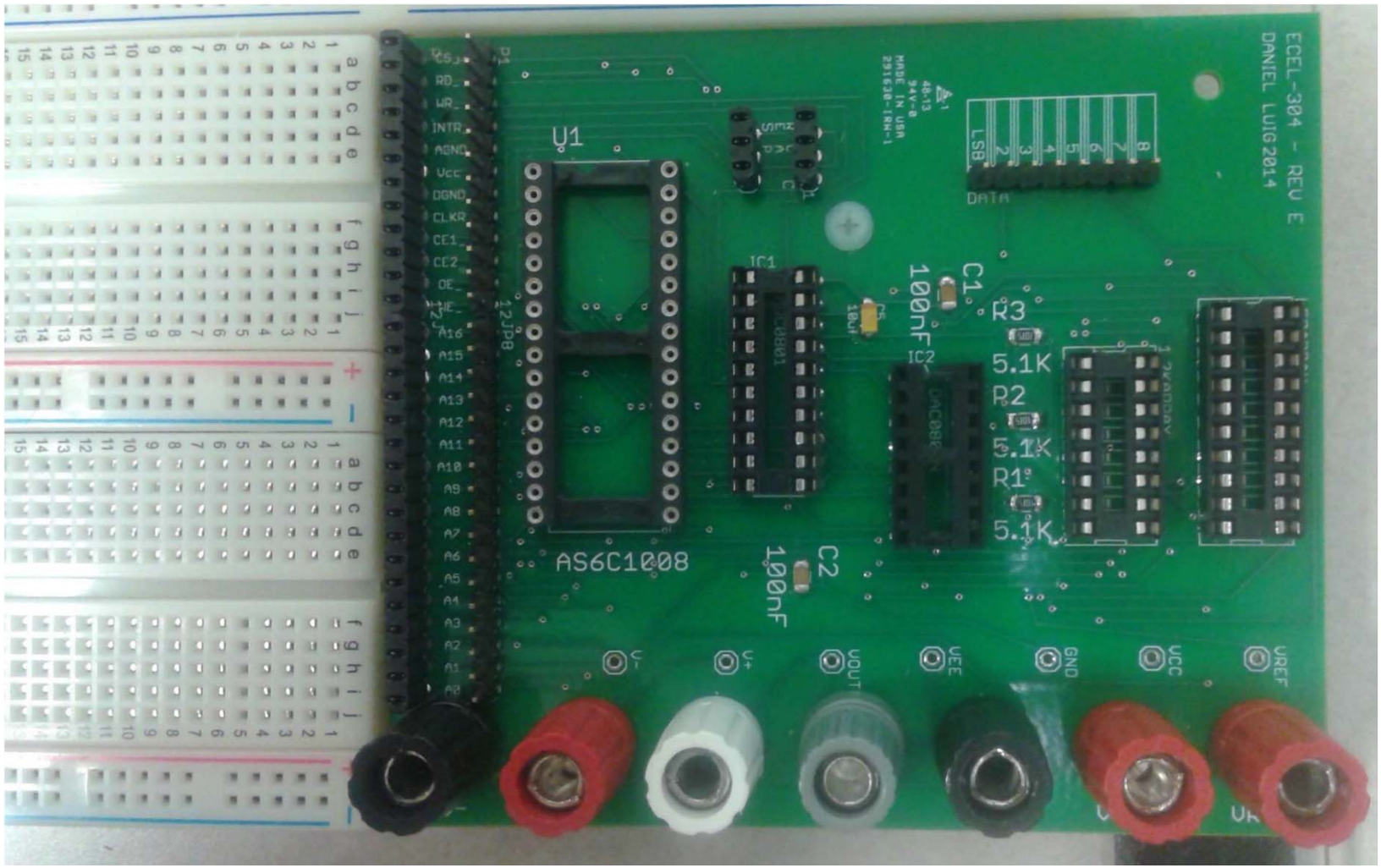
Lab Overview

- Design and build ADC circuit
  - Pick timing resistor and capacitor
  - Some additional wiring
- Change DC input voltage and record output
  - Verify accuracy
  - Determine ADC voltage resolution
- Apply analog voltage
  - Measure output using logic analyzer
  - Using a ramp input, observe binary count
  - Observe operation of ADC internal clock
- Simulate the all hardware steps in Multisim

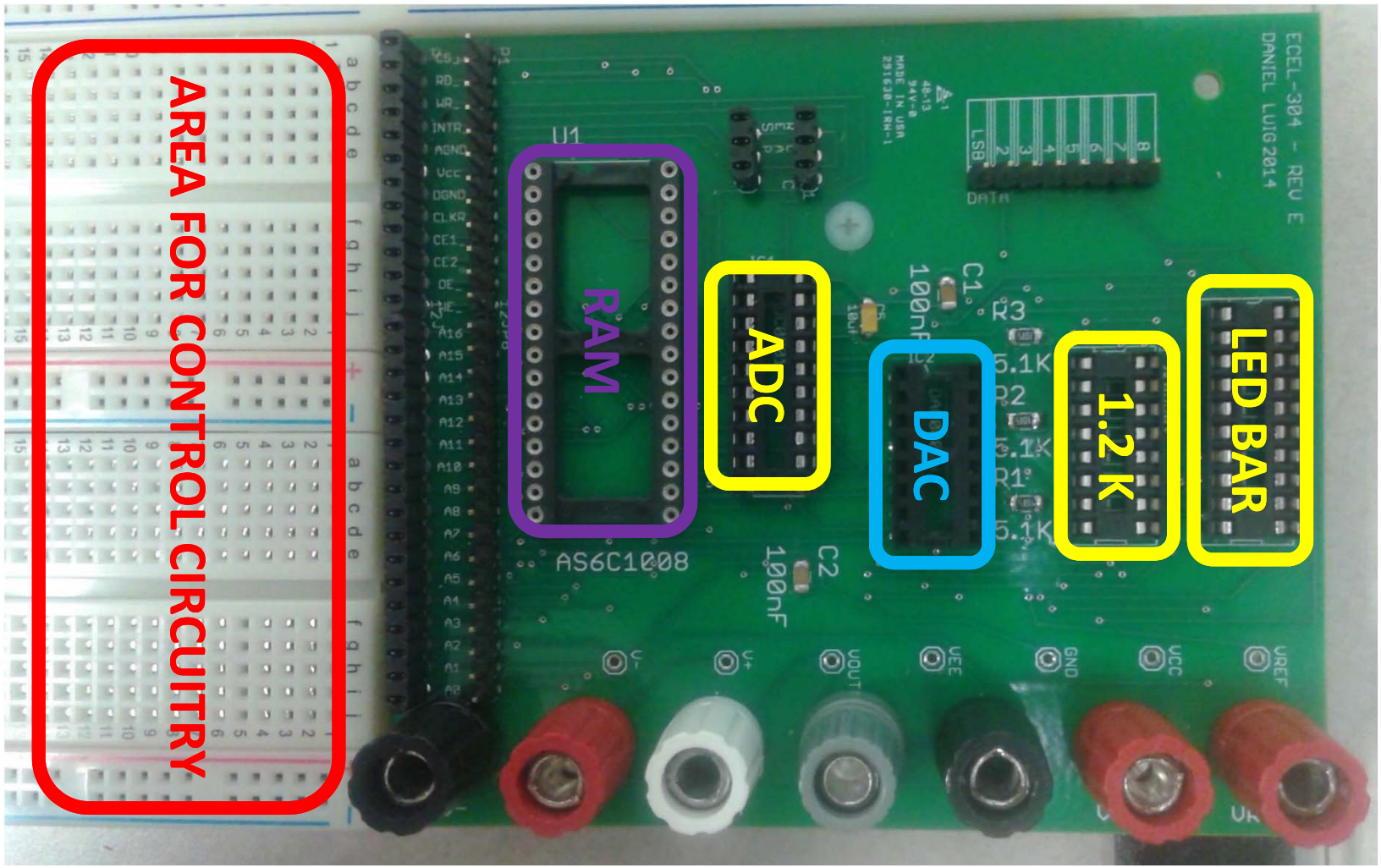
Design Consideration

- What is the bandwidth of human speech?
  - Provide a reference in your report
- At what frequency should I sample?
  - Higher frequency
    - Higher quality
    - Short recording/playback time
  - Lower frequency
    - Lower quality
    - Longer recording/playback time
- Provide clear justification for your choice
- Performance limitations of this ADC chip?
  - READ THE DATASHEET!!!

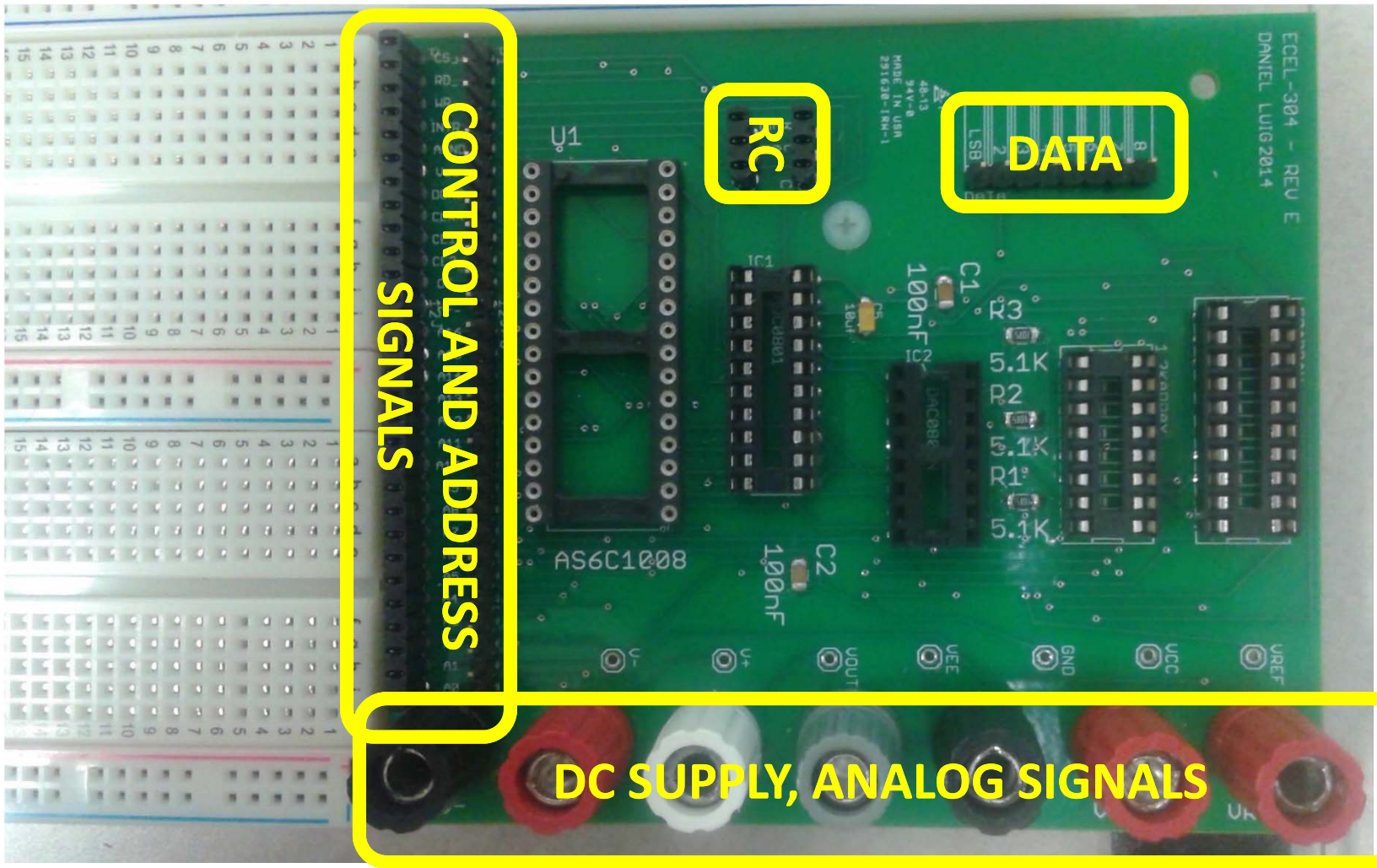
Data Acq. Board



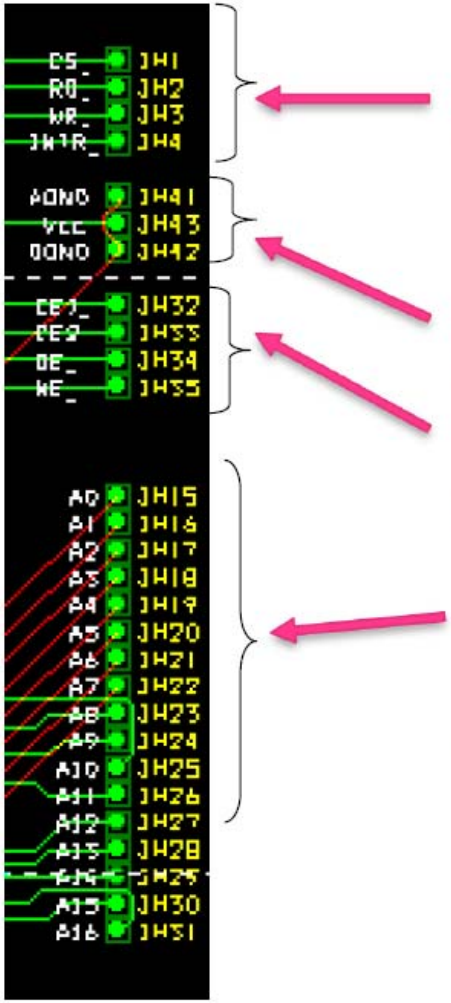
Sockets


AREA FOR CONTROL CIRCUITRY
RAM
ADC
DAC
1.2 K
LED BAR
U1
AS6C1008
C1
100nF
C2
100nF
R3
5.1K
R2
5.1K
R1
5.1K
DATA
LSB
ECEL-304 - REV E
DANIEL LUIG 2014

Headers/Terminals



Control Signals



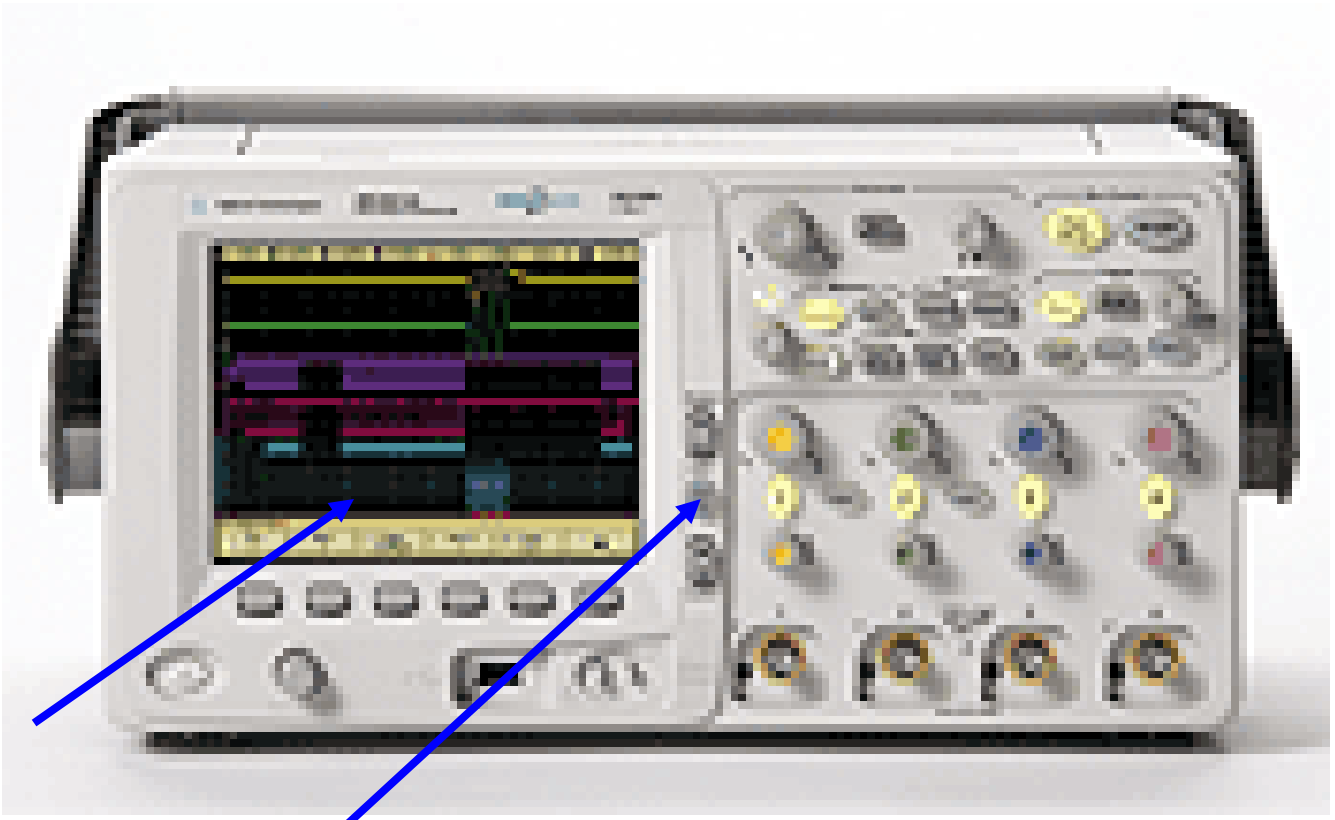
- ADC Control
  - CS_, RD_, WR_, INTR_
- Power, GND
- RAM Control
  - CE1_, CE2, OE_, WE_
- RAM Addresses
  - A16 - A0

Layout Concerns

- Place chips that interact with each other nearby
  - Less delay
- Wire Length makes a difference
  - Shorter Wires – Less Resistance/Capacitance
  - Longer Wires – More Resistance/Capacitance
- Keep Analog Circuitry away from Digital Circuitry
  - Potential problems with “crosstalk” – wireless interference between close signals

Logic Analyzer

Use *Intuilink* to capture data



Analog and digital displays

Digital Menu Access Button

Digital Menu Access Button

Logic Analyzer

- There is an HP mixed-signal scope in each rack in Bossone 205
- The digital portion of the scope (logic analyzer) serves the same purpose as the LEDs, but it can do it at a higher speed
- To capture data, you need to capture screenshots from the Intuilink software on the lab computer
- Be sure to capture and save all data/screens

Preparing For Lab

- Make sure to read over the instructions before the lab
  - Will make some changes to it (clear up some instructions)
- Familiarize yourself with Multisim
  - Watch videos posted on BBLearn
- Go over ADC 0804 Lab from ECEL 303
  - Also posted on BBLearn
- Watch video on using the Logic Analyzer
  - To be posted later today…

Next Week

- No in-class lecture next week
  - MLK day, University Holiday
- Lecture video will be posted on BBLearn
  - Expect it posted by Monday evening
  - Must watch before MIDNIGHT, Tuesday, Jan. 17
  - Will count towards lecture attendance
- Quiz next week during Lab
  - On the lecture/lab content from this week
  - Message will be sent out outlining content

Questions?