# ALU Design Problems Research with VLSI CAD “Kovcheg 2.2”

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***Abstract* – In paper possibility of ALU's realization on MPGA 5503 XM2 developed on microprocessor MOS Technology 6502 (USA) first demonstrated. Design cycle of ALU has been done, including modeling of truth table and topology formation. Shown, that 5503 library is functionally complete and support effective design of all components of 6502 microprocessor's ALU.**

***Index terms* – ALU, microprocessor, modeling, topology, logic elements library.**

## I. Introdution

MICROPROCESSOR (MP) IS CORE CHIP practically of any digital system and defines it's features and characteristics. Obviously, that having studied characteristics of MP, performance about capabilities and characteristics of digital circuit, created on this MP, could be obtained. Arithmetic-logic unit (ALU) is the central part of MP. Thus, the development of methods and techniques for design and analysis of the ALU for MP is an actual task of science and technology of digital devices. Moreover, effective solutions to the ALU and MP can be found and verified on MPGA with a larger cycle time, because their efficiency is generally proportional to save for subsequent increases in the clock frequency required for real industrial realization.

In this paper ALU MP MOS Technology 6502 was chosen for design and analysis. Domestic VLSI CAD “Kovcheg 2.2” [1] used for ALU design, which allows full development cycle specialized LSI on MPGA series 5503 [2] basis.

6502 is an 8 bit MP developed by MOS technology in 1975 [3] – [5]. When it appeared, it was cheaper than similar products of competitors companies (Motorola and Intel. Despite this, as well as a lower clock frequency, on average, it showed a similar performance by deliberate ways of addressing memory, short-cycle execution of commands and some piping. The appearance of such processors as 6502 and Zilog Z80, ultimately determined the appearance of home computers in the late 1970s. One of the known applications of 6502 there was a computer "Apple I", submitted in 1976. It was also used later in the line of Apple II and Commodore PET. 6502 later used in the family home computers Atari, BBC Micro, game console Nintendo Entertainment System, as well as in other applications [6]. Further development of 6502 was an 8 bit 65S02 with a number of small improvements implemented technology-based CMOS.

Western Design Center continues to manufacture and licensing MP 65C02, which is actively used in cars, pacemakers and defibrillators, as well as in embedded systems [7].

## II. Problem Definition

Mask programmable gate arrays (MPGA) are universal crystal blanks arranged on semiconductor wafer [8]. Such crystals are called base, since all the photomasks except switching layers for fabrication are constant and do not depend on the implemented circuit. The simplest elements are arranged in the nodes of a rectangular crystal lattice, therefore, it is called the matrix. LSI fabrication on MPGA is controlled by switching elements using a single-layer or multilayer wiring.

MP 6502 was designed for n-MOS technology, so after processing circuit for CMOS technology to design an ALU can apply MPGA 5503 XM2. MPGA 5503 XM2 contains 1296 logic gates of transistors 4, which is sufficient to accommodate the circuit ALU MP 6502.

## III. Conversion ALU's Electric Circuit In Logical

For ALU MP 6502 design was taken circuit developed by Rockwell Automation. It shows on Fig. 1. Circuit is consist of n-MOS transistors with induced channel (see Fig. 2a) and n-MOS transistors with integrated channel (see Fig. 2b). The latter are used in circuit as load.

Circuit is mainly consist of logical elements (LE), shown in Table I.

To enter the circuit in VLSI CAD “Kovcheg 2.2” is used circuit editor OrCAD [10]. In editor OrCAD circuits described by functional-logical level, so it is necessary to convert electrical circuit to the logical. Making the substitution elements in accordance with the Table I, logic circuit ALU obtained (see Fig. 3). Further, this ALU scheme was introduced in VLSI CAD "Kovcheg 2.2" with the circuit editor OrCAD.

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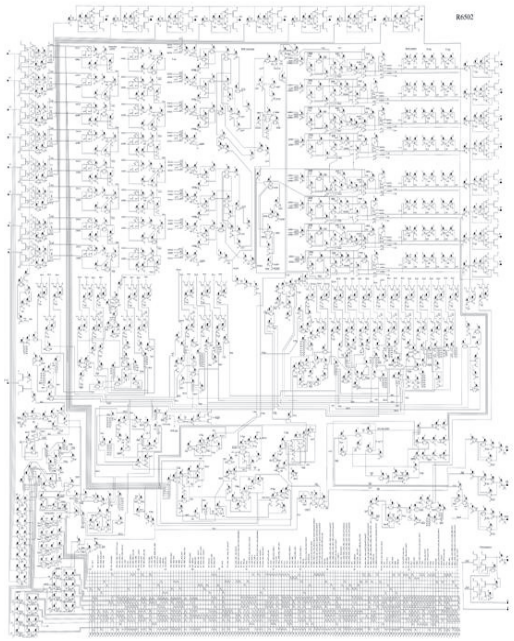


Fig. 1. Electrical circuit of 6502 [9].

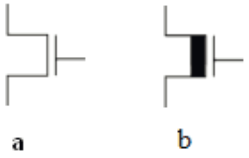
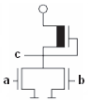
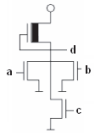
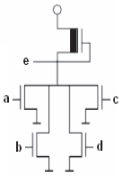
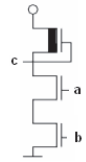
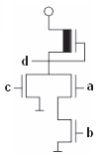
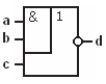
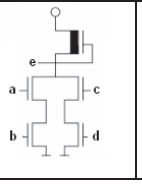
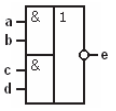
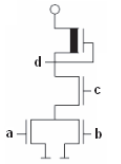
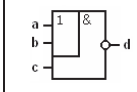
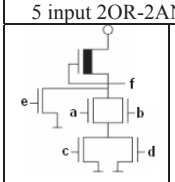
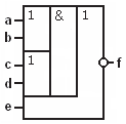
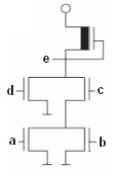
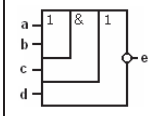



Fig. 2. Symbols n-MOS transistors in the circuit diagram.

TABLE I
SATISFACTION OF ELEMENT SYMBOLS OF ELECTRICAL AND LOGICAL CIRCUITS [12] – [16]

| Electrical circuit LE | Symbol LE | Electrical circuit LE | Symbol LE |
|---|---|---|---|
| Invertor | | 2 input NOR | |
|  |  |  |  |
| 3 input NOR | | 4 input NOR | |
|  |  |  |  |
| 2 input NAND | | 3 input NAND | |
|  |  |  |  |

| 4input 2AND-2OR-NOT | | 3 input 2OR-AND-NOT | |
|---|---|---|---|
|  |  |  |  |
| 5 input 2OR-2AND-OR-NOT | | 4 input 2OR-AND-OR-NOT | |
|  |  |  |  |

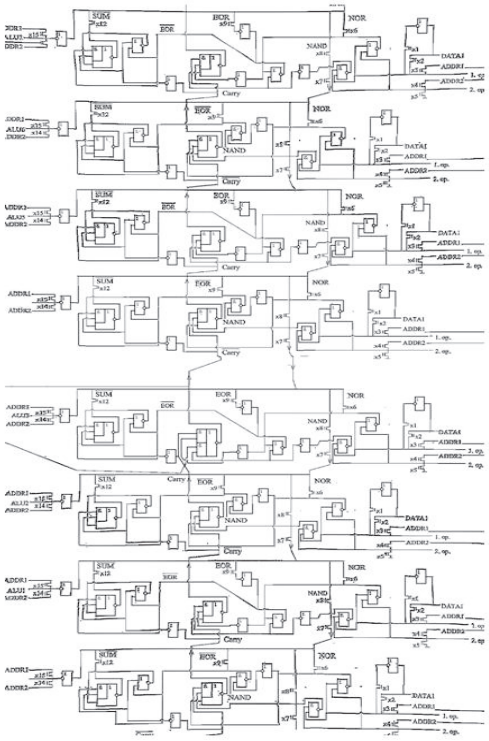


Fig. 3. ALU logical circuit [11].

ALU circuit separated from MP 6502 circuit. ALU MP 6502 is an 8 bit. This compact combination circuit, which is located in a block of registers and uses the same internal buses that registers. ALU is consist of eight cells. Each cell has two input operands, carry input of the less significant bit, right shift input, carry and right shift outputs. ALU performs the following operations: sum, shift to the right, AND, OR, XOR. What will be the output, defined by keys.

## IV. ALU MODELING

Simulation is carried out using the subsystem of functional logic modeling (FLM) of VLSI CAD "Kovcheg 2.2". Input information of FLM presented by:

- structural description of the VLSI project;

- test inputs description;
- description of array of control points.

Truth table used for ALU's modeling shown in Fig. 4. For each operation on ALU's inputs (buses ADDR1, ADDR2) given two eight bit operands. For sum operation additionally given inverse input CARRY1, SR2 – output shift, CARRY2 – output carry.

| Busses | $\overline{CARRY2}$ | Sum | | | | | | | | $\overline{CARRY1}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| ADDR1 | | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | |
| ADDR2 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| ALU | | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | |
| ADDR1 | | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | |
| ADDR2 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| ALU | | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | |
| | | AND | | | | | | | | |
| ADDR1 | | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | |
| ADDR2 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| ALU | | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | |
| | | OR | | | | | | | | |
| ADDR1 | | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | |
| ADDR2 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| ALU | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | |
| | | XOR | | | | | | | | |
| ADDR1 | | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | |
| ADDR2 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| ALU | | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | |
| | | Right Shift | | | | | | | | |
| ADDR1 | | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | |
| ADDR2 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| ALU | | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | |

Рис. 4. ALU's truth table [11].

In VLSI CAD "Kovcheg 2.2" simulation results present as timing diagrams (Fig. 5). Arithmetic operations modeled: addition $01110100_2$ and $00100011_2$ with input carry, addition $01110111_2$ and $10010011_2$ without input carry and right shift operation. Logical bit-by-bit operations: AND between operands $10101100_2$ and $01011010_2$, OR between operands $01011010_2$ and $10101100_2$, XOR between operands $10101100_2$ and $01011010_2$.

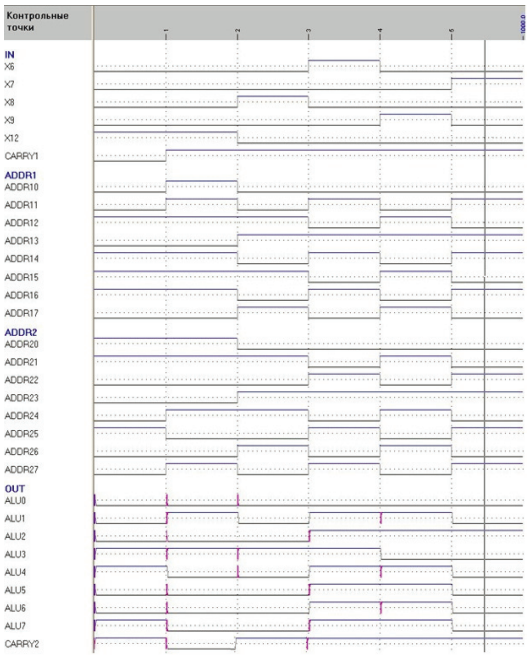



Fig. 5. Timing diagrams of ALU.

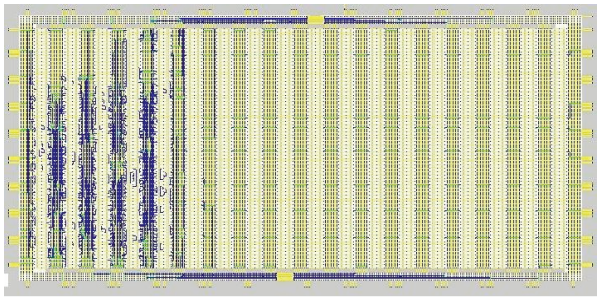


Fig. 6. Topology of ALU [17].

## V. Discussion Of Results

Comparison of timing diagrams and truth table (Fig. 4) present their full coincidence. Minor risks have not led to disruption of the ALU in the above examples (see Fig. 5). Result formation of topology of VLSI CAD tools "Kovcheg 2.2" presented in Fig. 6 shows the functional completeness of library 5503 and its sufficiency for the design of the ALU MP 6502, because the topology of all its elements built.

## VI. Conclusion

The paper shows the possibility of designing the ALU of MP 6502 at MPGA 5503 XM2 by domestic VLSI CAD "Kovcheg 2.2". Timing diagrams of the ALU and its topology were obtained.

Thus, the results obtained allow us to go simply by the computer simulation to study the effectiveness of such architectural decisions as conveying the execution of the operations, the prediction (trace) of further progress in the program, the parallel execution of instructions and multithreading on a new version of VLSI CAD "Kovcheg 3.01."

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The link to the biographic data provided in the network encyclopedia "Scientists of Russia": http://www.famous-scientists.ru/5866

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