# ECEC–471\571 Introduction to VLSI Design

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## Drexel University
## Electrical and Computer Engineering

## Lab Assignment #2, CMOS Inverter

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# 1 Objective

The primary objective of this laboratory assignment is to learn how to design a CMOS inverter. First, a minimum sized CMOS inverter is designed. Next, the CMOS inverter is sized to obtain a symmetric inverter which has the rise time ($t_r$) equal to the fall time ($t_f$). Transient and DC simulations are performed to achieve symmetric rise/fall times. The assignment concludes by constructing the layout of the symmetric inverter. All the tasks are performed using Cadence Virtuoso suite. The task list is itemized below:

- Build an *Inverter* using transistors in the *Schematic View* of *Virtuoso*
- Simulate the schematic inverters using *Virtuoso*
- Size the inverter such that the switching threshold is half of *Vdd*
- Complete transient simulation on the schematic to verify the symmetric behavior
- Complete DC simulation on the schematic to verify the switching threshold
- Build the *Symmetric Inverter* in *Layout View* of *Virtuoso* without any DRC (Design Rule Check) errors
- Match the *Schematic View* with the *Layout View* of the *Symmetric Inverter* using LVS (Layout Versus Schematic)

# 2 Prepare your PC for Cadence Virtuoso

Follow the guidelines in Lab Assignment #1(b) to configure your PC for using Virtuoso.

# 3 Design Requirements

Different technology libraries contain different feature sizes and design rules. The **CMOS7RF** (0.18 $\mu m$) technology library will be used throughout this quarter unless noted otherwise. **All standard cells designed in this class should have the same height of** 7.2 $\mu$**m.**

# 4 Procedure

Please follow the detailed tutorials provided on BBLearn to construct the schematic and layout of the CMOS Symmetric Inverter. In there any questions about the tutorials, please ask.

# 5 Lab report

Please upload your lab report in pdf format. Late submissions will be penalized as per the guidelines provided in the syllabus. The reports are due before the next lab class. A sample lab report is uploaded in the bblearn for the reference.

The lab report should include the following:

1. A screen shot of the *Schematic view* of the Symmetric Inverter
2. The screen shot of the *Layout view* of the Symmetric Inverter
3. The layout DRC and LVS verification results
4. The DC sweep simulation plot which is used to choose the pmos channel width
5. The pmos channel widths of the transistors you have chosen
6. The DC simulation results for the Schematic
7. The transient simulation result for the Symmetric Inverter. Mark the timing information on the plot including the rise time $t_r$, fall time $t_f$ and propagation delay $t_{prop}$
8. The functionality of the **Schematic-based** simulations:
   (a) Mark the timing information on the plot including the rise time $t_r$, fall time $t_f$ and propagation delay $t_{prop}$
   (b) Report all the measurement results in a **table**, such as:

| Sim type | $t_r$ | $t_f$ | $t_{prop}$ |
|---|---|---|---|
| Front end sim | | | |