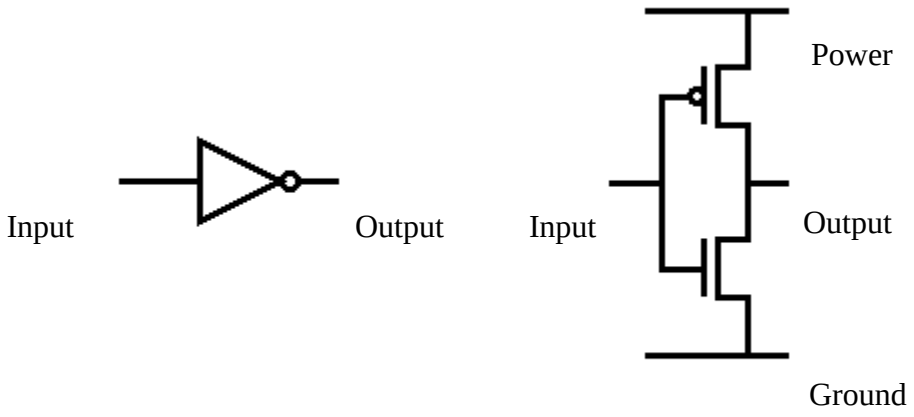
Introduction to VLSI Design –Laboratory
ECEC 571

CMOS Inverter

Objective: Design of schematic and layout of a CMOS inverter using Cadence Virtuoso. Starting with designing an arbitrary sized inverter schematic, the ultimate goal is to obtain a symmetric inverter by adjusting the switching threshold to VDD/2 through DC simulation and parametric analysis. Finally, design of the inverter layout and with physical verification (DRC and LVS).

Introduction: CMOS inverter is a basic building block of analog and digital ICs. An inverter can be designed by one *pmos* and one *nmos* transistor where the pmos section is called pull-up network and nmos part is called pull-down network. The basic function of the inverter is to invert the input signal but it can also be used as a buffer by cascading two inverters or interchanging pmos and nmos. Pull-up network pulls the output potential form low to high. However, pull-down network drops the output from high to low potential. The term complementary refers to the fact that pull-up and pull-down network complements each other.

The gate level and transistor level representation of an inverter can be given as the following figures:



Gate Level Representation Transistor Level Representation

Inverter Sizing

The size of pmos and nmos of an inverter has great significance in terms of proper performance and operation. Careful consideration on relative sizing of nmos and pmos must be taken into account to make sure the symmetric (i.e. equal rise time and fall time) behavior.

Rise time and fall time:

Rise time can be defined as the time required for the output signal to reach 90% (high) from 10% (low) of output signal/voltage.

Fall time can be defined as the time required for the output signal move to 10% (low) from 90% (high) of output signal/voltage.

Propagation delay:

Propagation delay is the measure of time it takes to get the output after applying input. Theoretically, it is the time difference from 50% of input rise transition to 50% of output rise transition.

Symmetric Inverter:

An inverter is said to be a symmetric inverter only if it has same rise and fall time. With same rise and fall time both low-high and high-low transitions will coincide in a potential that is half of VDD. In order to obtain symmetric behavior the physical size of transistor width can be adjusted. The norm is to keep the transistor length constant throughout a particular design process since changing transistor length leads to changing the channel (gate) length.

Simulation process and results:

Schematic design: The following (Fig - 1) schematic of inverter has been designed using Cadence Virtuoso Schematic Editor. Initially the length and width of the transistors has been selected as:

PMOS: Width – 500nm Length – 180nm

NMOS: Width - 600nm Length – 180nm

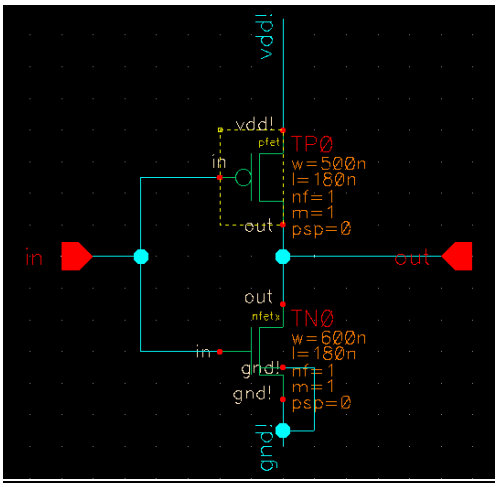


Figure 1: Transistor-level schematic of non-symmetric CMOS inverter

In order to simulate the transient and DC behavior of this inverter a 500fF capacitive load and voltage source (Amplitude – 1.8V, rise time – 1ps, fall time – 1ps, and pulse width – 500ns) has been connected with this inverter. The resultant top level inverter schematic is given in the following Figure 2.

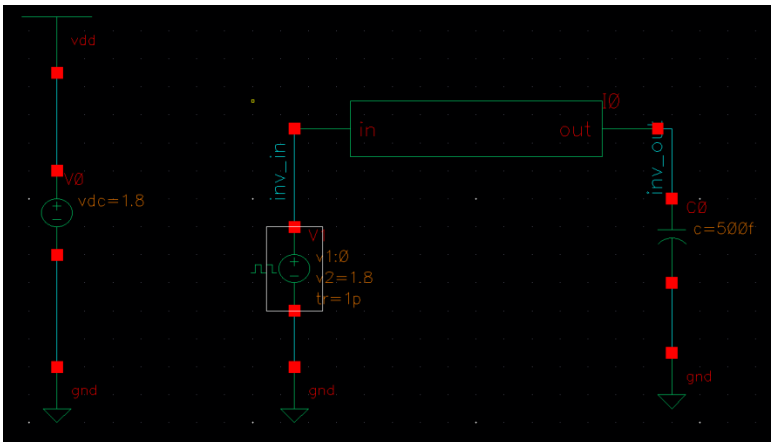


Figure 2: CMOS inverter with source and load

Rise time, fall time, and propagation delay have been observed through transient analysis and symmetric behavior of the inverter has been observed through DC analysis. The results of transient and DC simulation are given in Figure 3 and 4 respectively.

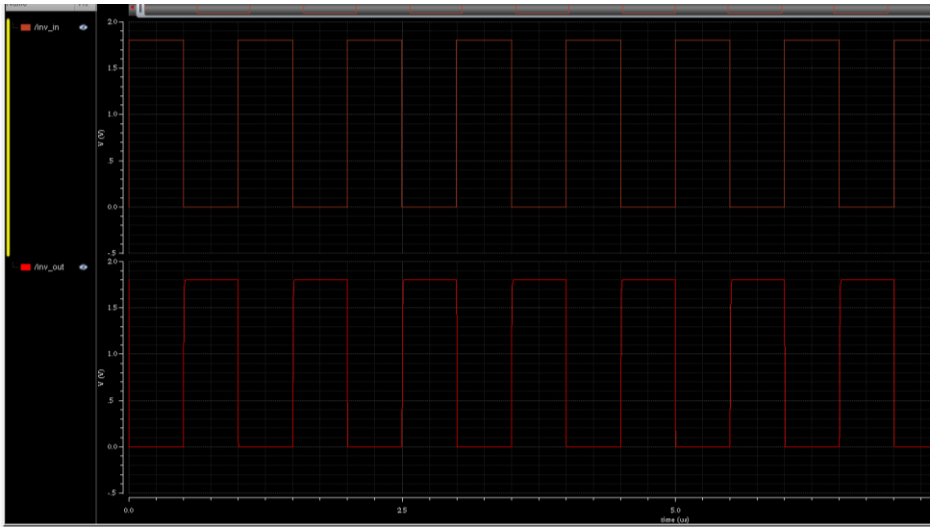


Figure 3: Transient simulation

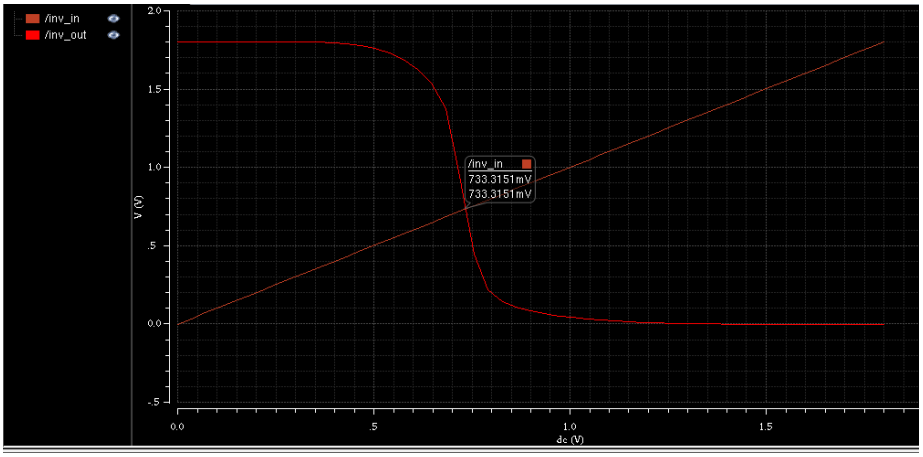


Figure 4: DC simulation showing non-symmetric behavior

The switching threshold has been found to be approximately 0.7V (Figure 4) which is not the desired switching voltage (0.9V) since the value of applied supply voltage is 1.8V. That means at this point the inverter is not symmetric.

In order to obtain the symmetric behavior parametric analysis has been done using Virtuoso Analog Design Environment to find appropriate transistor size (width). In this case the

parametric analysis has been done on PMOS since the target is to adjust the width of PMOS. The required width of PMOS for symmetric behavior has been found as 1.8um as shown in the following Figure 5.

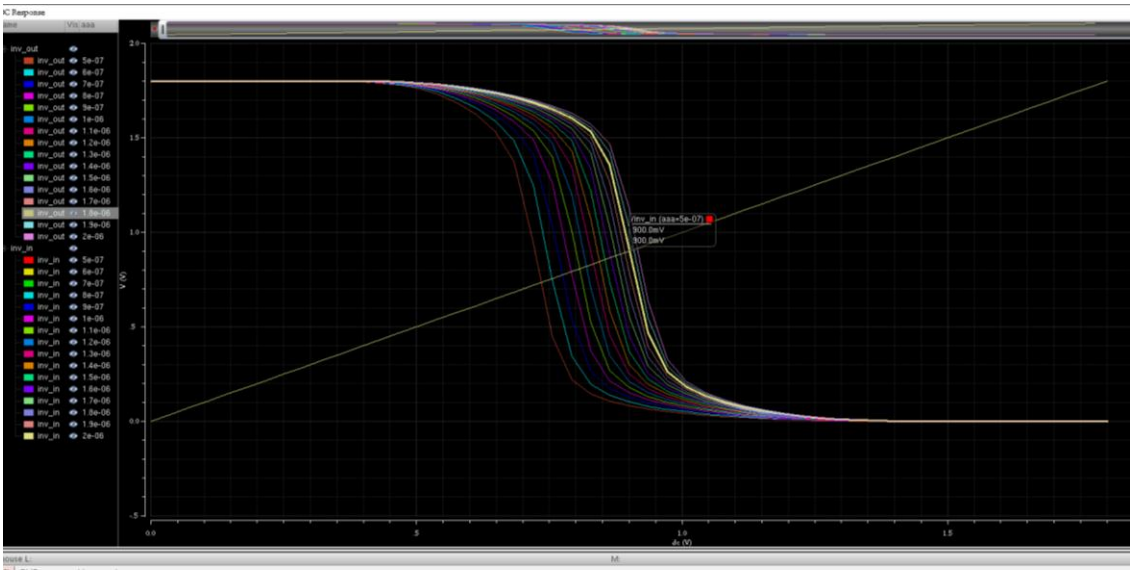


Figure 5: Parametric analysis to find PMOS width

Now, the PMOS transistor has been updated with new width (1.8um) and DC simulation has been performed again to make sure that the inverter is symmetric. The updated schematic and DC simulation results are given in the following Figure 6 and 7 respectively.

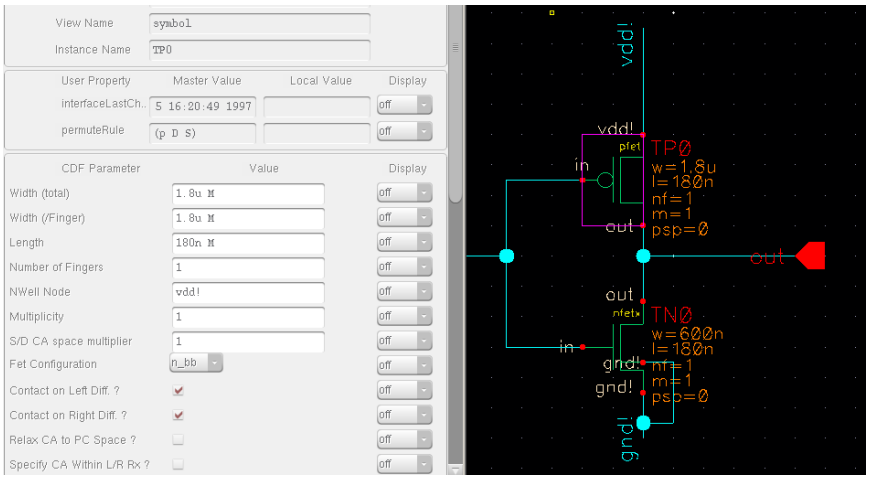


Figure 6: Updated PMOS transistor having width of 1.8um

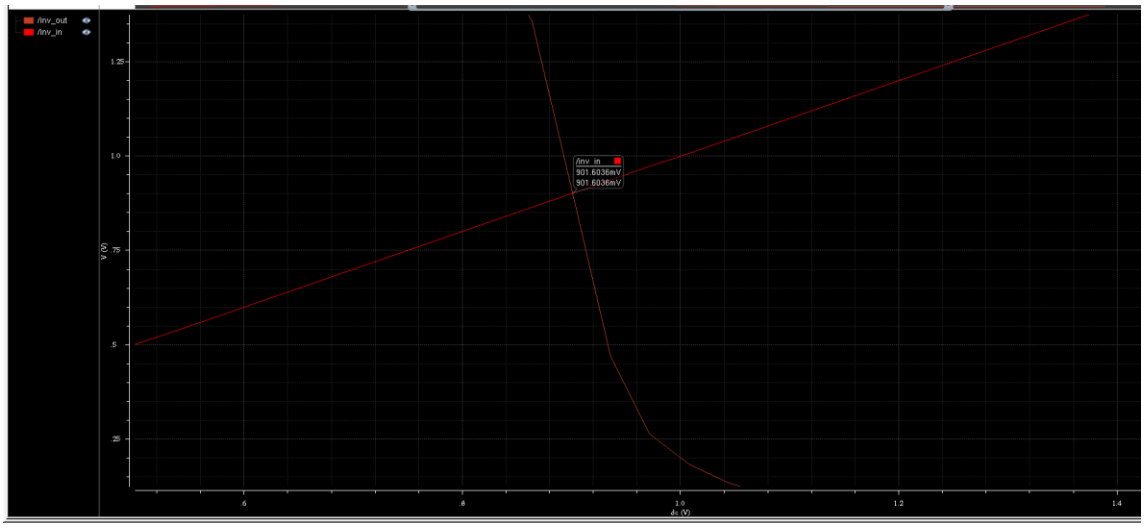


Figure 7: DC simulation showing the symmetric behavior of inverter

From the above DC simulation it can be easily observed that now the switching threshold is 0.9V which is the desired value for symmetric behavior of inverter. So, at this point the inverter is a symmetric inverter with equal rise and fall time and updated transistor sizes can be tabulated as the following:

PMOS: Width – 1.8um Length – 180nm

NMOS: Width - 600nm Length – 180nm

In the later sections creation of physical layout of this symmetric inverter has been demonstrated.

Layout design of symmetric inverter:

The schematic of symmetric inverter has been designed in the previous section where the appropriate transistor sizing has been performed in order to achieve symmetric behavior. The physical layout of this inverter has been designed using Virtuoso Layout Suite L. At first the PMOS and NMOS transistor have been created with the following dimension.

PMOS: Width – 1.8um Length – 180nm

NMOS: Width - 600nm Length – 180nm

The layout view of PMOS and NMOS transistor is given in Figure 8 and 9 with the indication of transistor length and width.

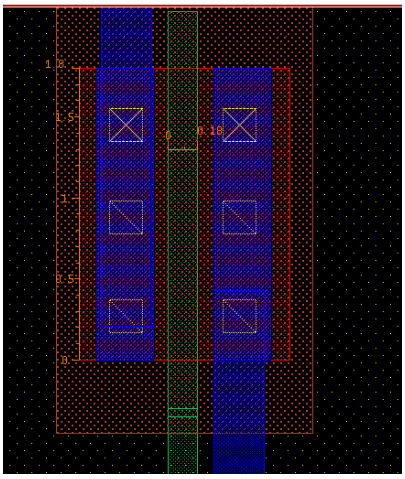


Figure 8: Layout view of PMOS transistor (W – 1.8um and L – 180nm)

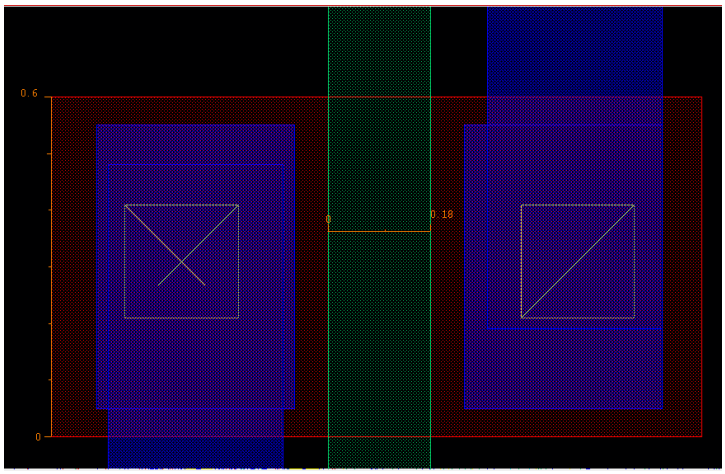


Figure 9: Layout view of NMOS transistor (W – 600nm and L – 180nm)

In addition to PMOS and NMOS transistors, power and ground rails has also been placed. After that two transistors have been connected with each other and with power/ground rails by metal routing and contact vias. The resultant inverter layout is given in the following Figure 10.

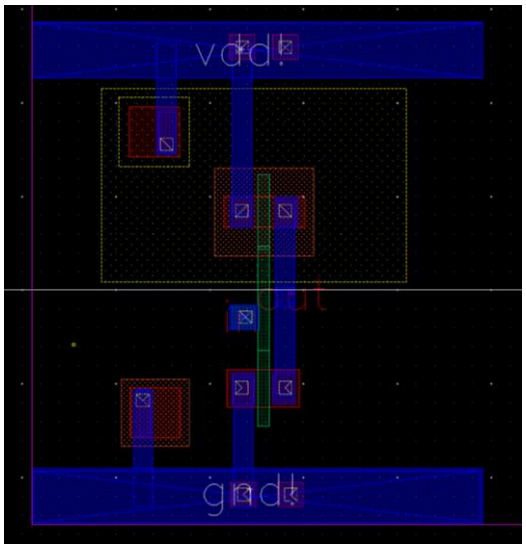


Figure 9: Layout view symmetric CMOS inverter

At this point both schematic and layout have been designed for a symmetric inverter. In the next section the physical verification steps has been demonstrated.

Physical Verification:

After the completion of schematic and layout design physical verification has been performed for the inverter. Two types of verification have been performed in this laboratory – 1. Design Rule Checking and 2. Layout versus Schematic Checking.

Design Rule Checking (DRC): Once the layout is completed, it is required to check the layout for possible design rule violations through Design Rule Checking (DRC). The DRC has been performed through Assura and no violations found in layout design. The DRC result is given in Figure 10.

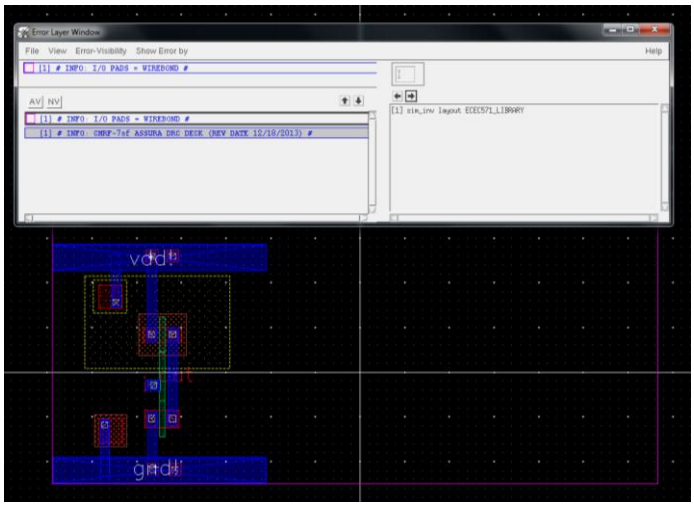


Figure 10: DRC result showing no design rule violation

Layout versus Schematic Checking (LVS): Once the layout has passed DRC checking, the LVS checking has been performed to make sure that the physical layout exactly mimics the schematic in terms of connectivity. LVS checking has been successfully performed using Assura and the result (Figure 11) shows that the schematic and layout matches.

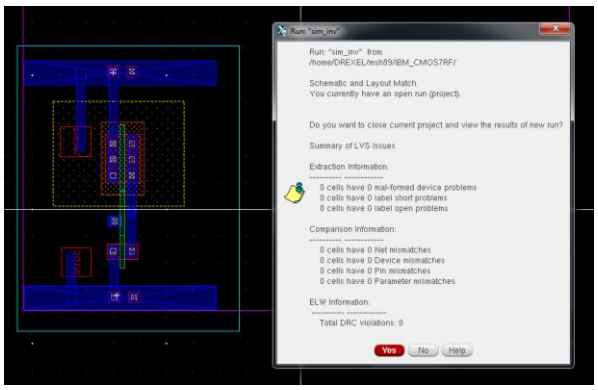


Figure 11: LVS result showing schematic and layout are matched

Analysis of simulation results:

Transistor sizing and symmetric behavior:

Propagation delay: During schematic design and simulation, propagation delay has been chosen as 0ns. But from the transient simulation propagation delay found as 1.0248ns (Figure 12)

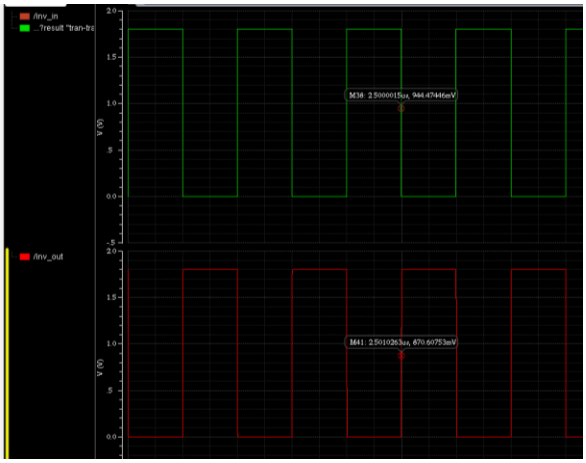


Figure 12: Propagation delay calculation from transient simulation

Here, a small amount of delay (1.0248ns) has been observed although delay has been chosen 0ns. It means it takes 1.0248ns to get the output response with respect to the input. In the physical layout a slightly more delay can be found since RC parameters from the interconnect will also be counted in the layout view and in the actual circuit even more delay can be found depending on the accuracy of simulation and design process.

Rise time and fall time: During schematic design and simulation, rise time and fall time have been defined as 1ps. In order to find the rise and fall time from the transient simulation, markers have been placed on the waveform as the following.

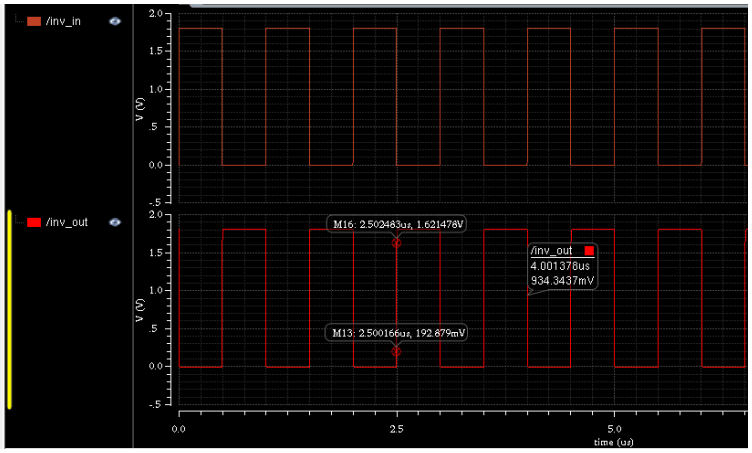


Figure 12: Rise time calculation from transient simulation

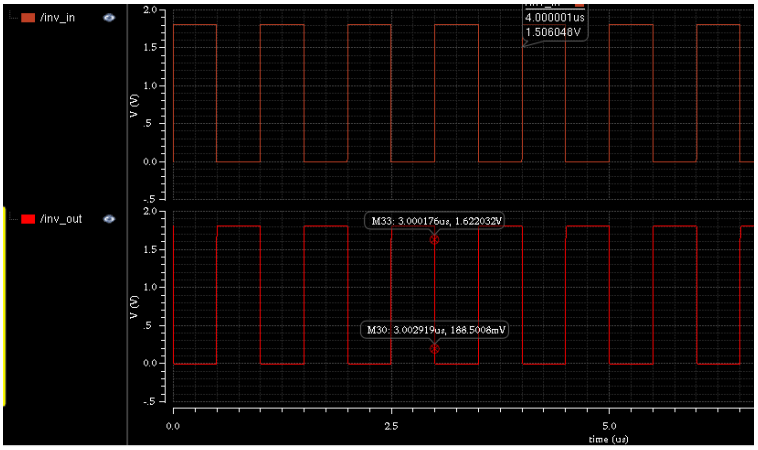


Figure 13: Fall time calculation from transient simulation

The calculated rise and fall time from the transient simulation can be given as the following:

Table 1: Rise and fall time analysis

	Time (ps)	**Voltage levels (10% to 90% or 90% to 10%)**	
Rise time	2.32	0.192879V	1.621478V
Fall time	2.74	1.922032V	0.188501V

Although it has been demonstrated that this is a symmetric inverter through the result of DC simulation but a slightly different rise time and fall time has been observed from the transient

simulation. Some minor errors have also observed in the simulation. Although rise time and fall time are meant to be calculated from 10% to 90% and 90% to 10% of voltage respectively, the markers have not been placed exactly at (0.18V) 10% or 90% (1.62V) of the input voltage. Actual positions of markers have been shown in Table 1. This minor error in marker placement could be responsible for this minor deviation in rise and fall time.

Conclusion:

The CMOS inverter circuit and layout are designed in this laboratory. The symmetric behavior is obtained through parametric and DC analysis. The physical verification (DRC and LVS) process ensures the correctness of the layout. The expected inverter behavior is observed from the transient simulation. In addition to that, rise time, fall time, and propagation delay are measured from the transient analysis, which characterizes the symmetric behavior and performance of the inverter.