INVERTER LAYOUT TUTORIAL

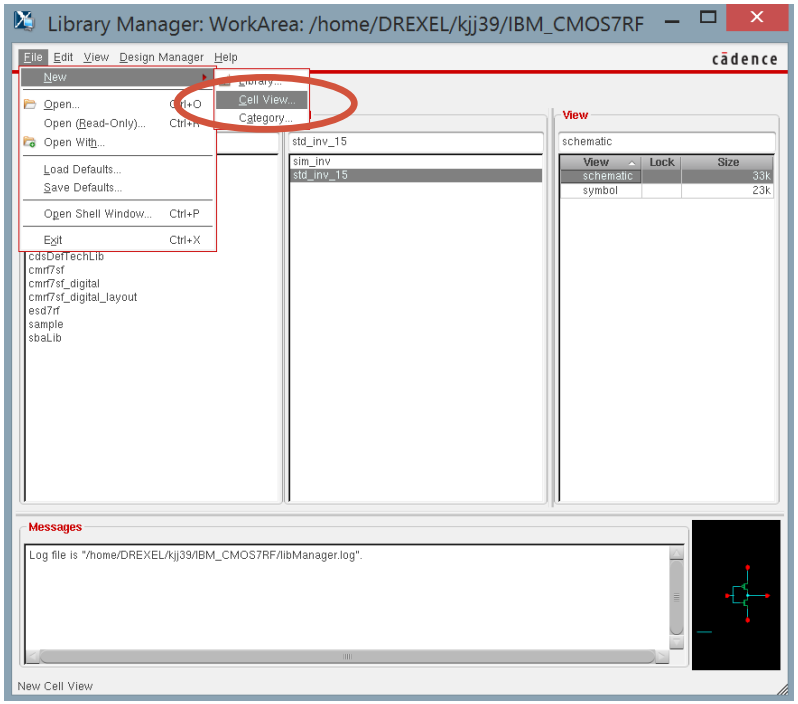
3 Build your layout

- Part 3 demonstrates:
  - The physical design (layout)
  - Design rule check (DRC)
  - Layout vs. schematic (LVS)

  using the design rules for the IBM CMOS7RF 180nm
- It is important that you always have a verified functional schematic before beginning layout. If the schematic is not correct, the layout will also be incorrect. The layout should contain:
  - The same pin names and same connections.
  - Same transistors in same size as those in the schematic.

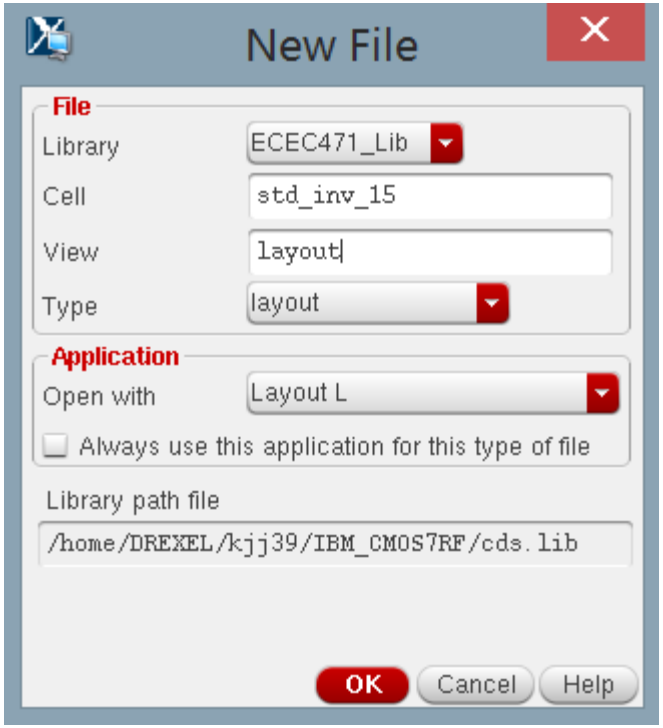
3.1 Create a new layout view

- In the Library Manager window
- Select your library in the left column and select the cell view of your inverter (Ex. std_inv_15)
- Select File->New->Cellview



3.1 Create a new layout view

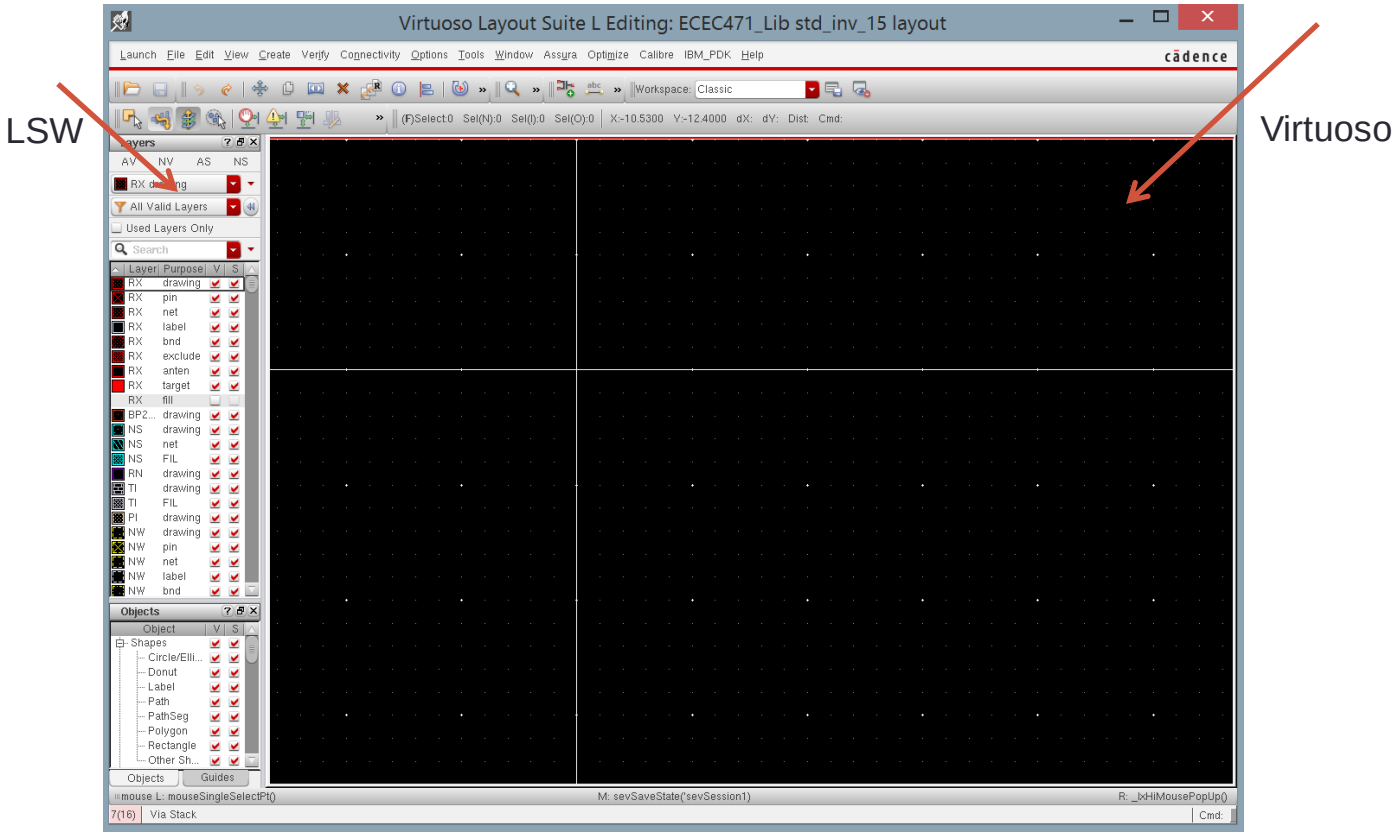
- A dialog box Create New File will pop up.
- Library name: your design library
- Cell Name: Same as the one you already have schematic and symbol
  e.g. std_inv_15
- View name: layout



3.1 Create a new layout view

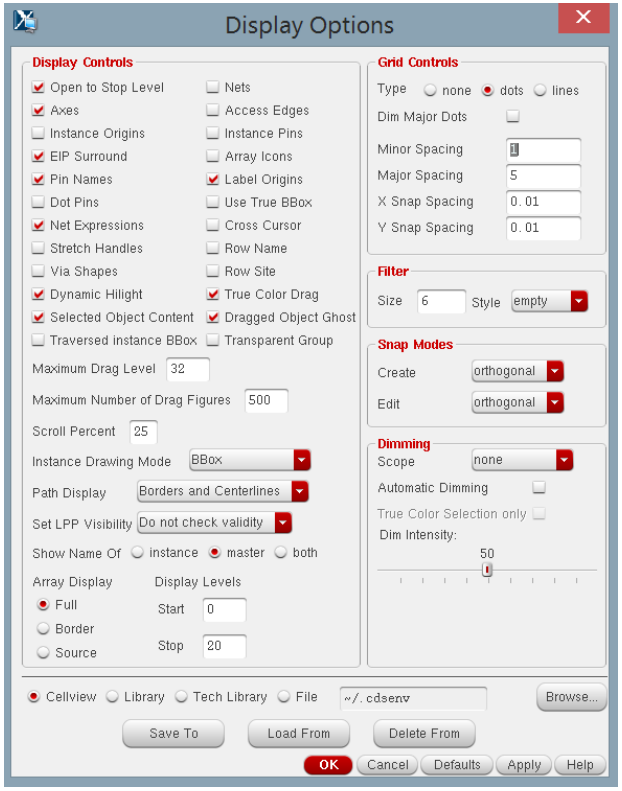
- Two design windows (Virtuoso and LSW) will pop-up.
- The Layer Selection window (LSW) lets the user select different layers of the mask layout. Virtuoso will always use the layer selected in the LSW for editing. The LSW can also be used to determine which layers will be visible and which layers will be selectable. To select a layer, simply click on the desired layer within the LSW.
- Virtuoso is the main layout editor of Cadence design tools. Commonly used functions can be accessed by pressing the buttons/icons of the toolbar on the left side of this window. There is an information line at the top of the window which shows (from left to right) the X and Y coordinates of the cursor, number of selected objects, the distance traveled in the X and Y directions, the total distance, and the command currently in use. This information can be very handy while editing. At the bottom of the window, another line shows the function of each mouse button. Note that the mouse button functions will change according to the command you are currently executing. The default mouse mode is selection, and as long as you do not choose a new mode you will remain in that mode. To quit from any mode or command and return to the default selection mode, the ‘ESC’ key can be used.

3.1 Create a new layout view



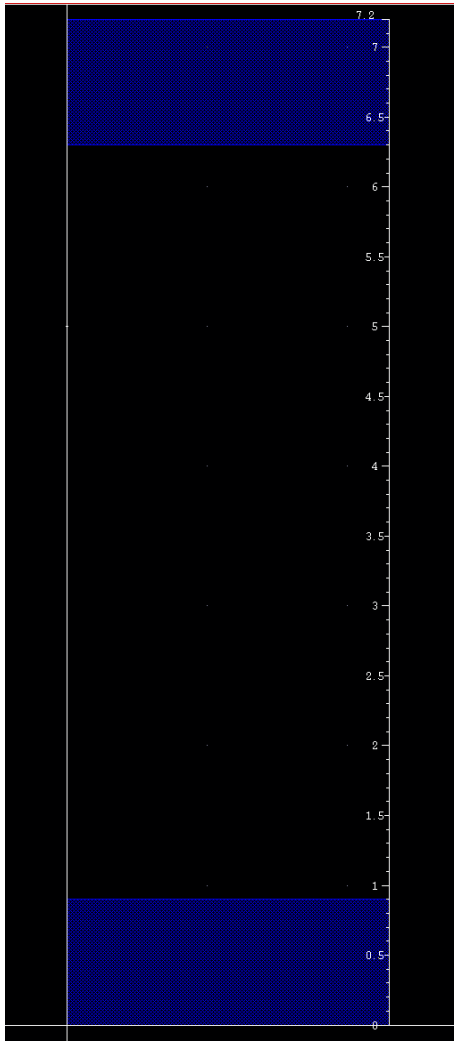
3.2 Build the layout of inverter std cell

- Display setup
- In the Virtuoso Layout Editing window,
- select Options->Display (or type e). The Display Options window will pop up.
- Type in the following settings:
  - Minor Spacing 0.3
  - Major Spacing 1.5
  - X Snap Spacing 0.01
  - Y Snap Spacing 0.01
- Then click OK.



3.2 Build the layout of inverter std cell

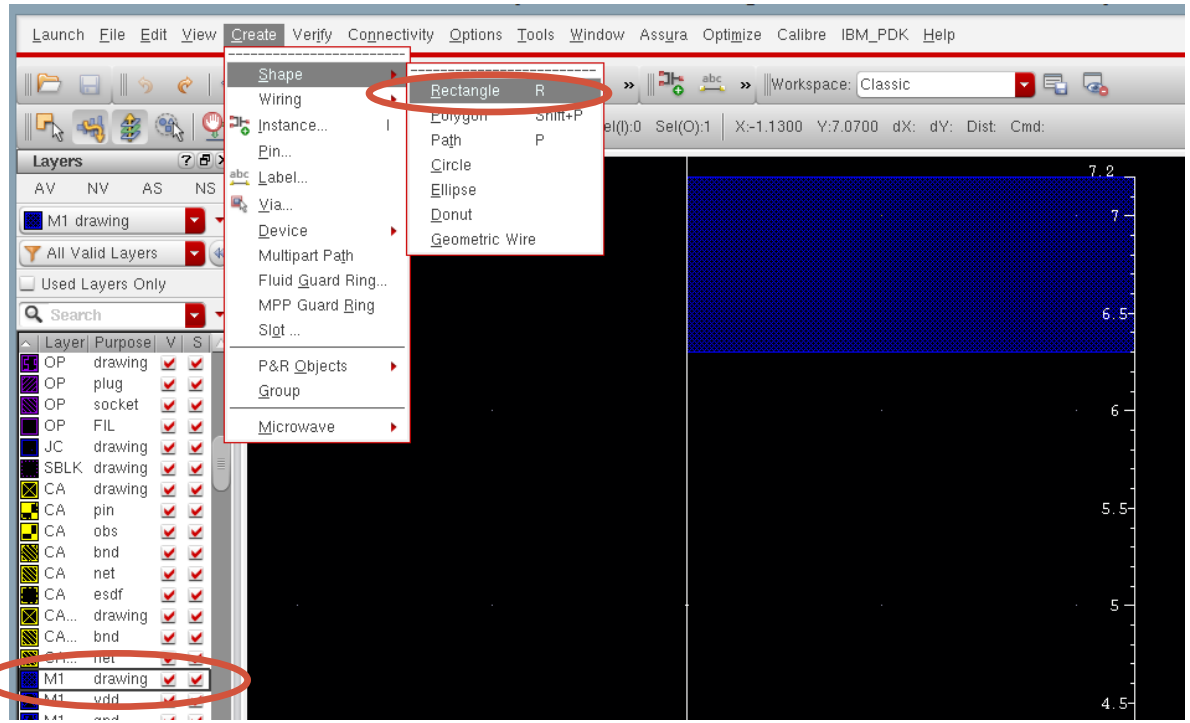
- Create VDD and GND rails.
- Metal1(drw) is used to create VDD and GND rails
- The standard cell pitch (height from bottom of the GND rail to top of the VDD rail) is 7.2um.
- The thickness of the rails shown is 0.9um.



3.2 Build the layout of inverter std cell

- Create rectangle
  - In the Layout selection window select the M1 drawing layer
  - In the Virtuoso Layout Editing window,

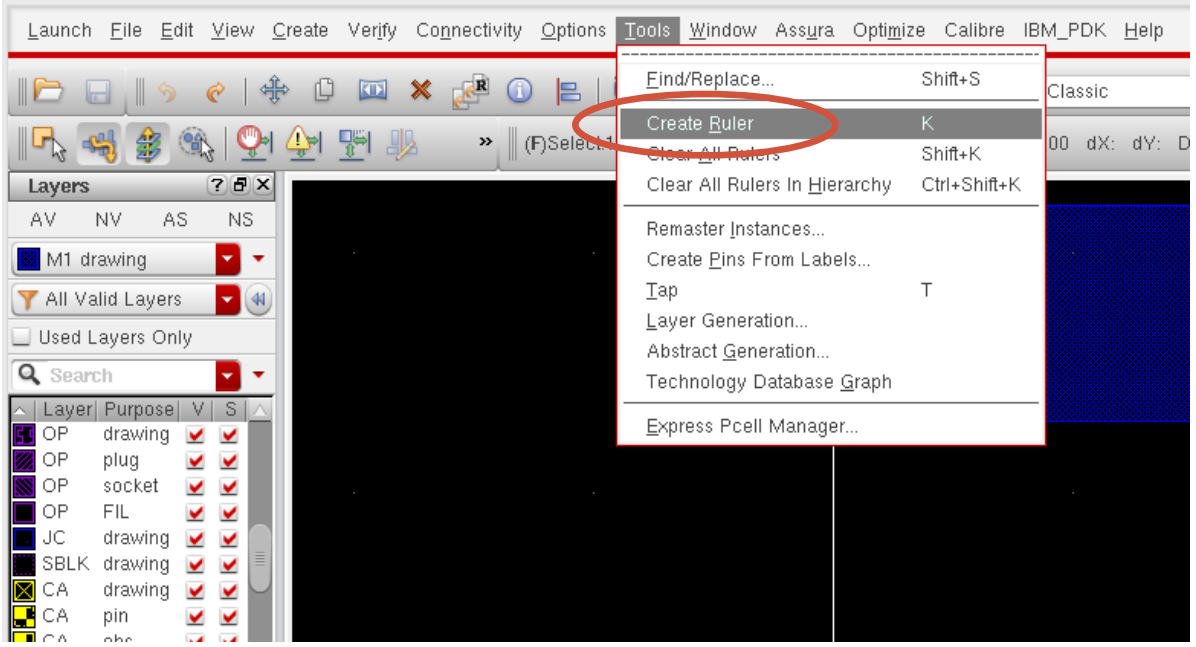
    select Create->Shape->Rectangle (or type r).
  - Go back to the Virtuoso Layout Editing window, click once left mouse, release the mouse, the shape of the rectangle changes along with you mouse.
  - Then click left mouse once again to finish build the rectangle.



3.2 Build the layout of inverter std cell

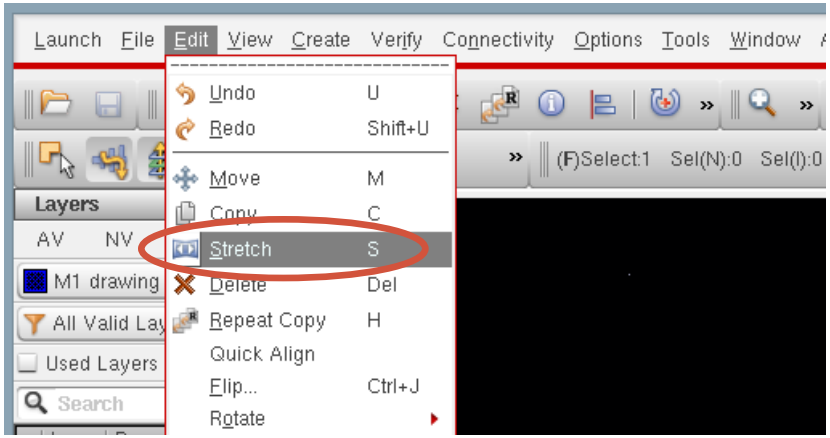
- Useful editing tools
- Ruler: You can find ruler from
  - Tools->Create Ruler (or press k)
- Move, copy, delete,… are

the same as in schematic.



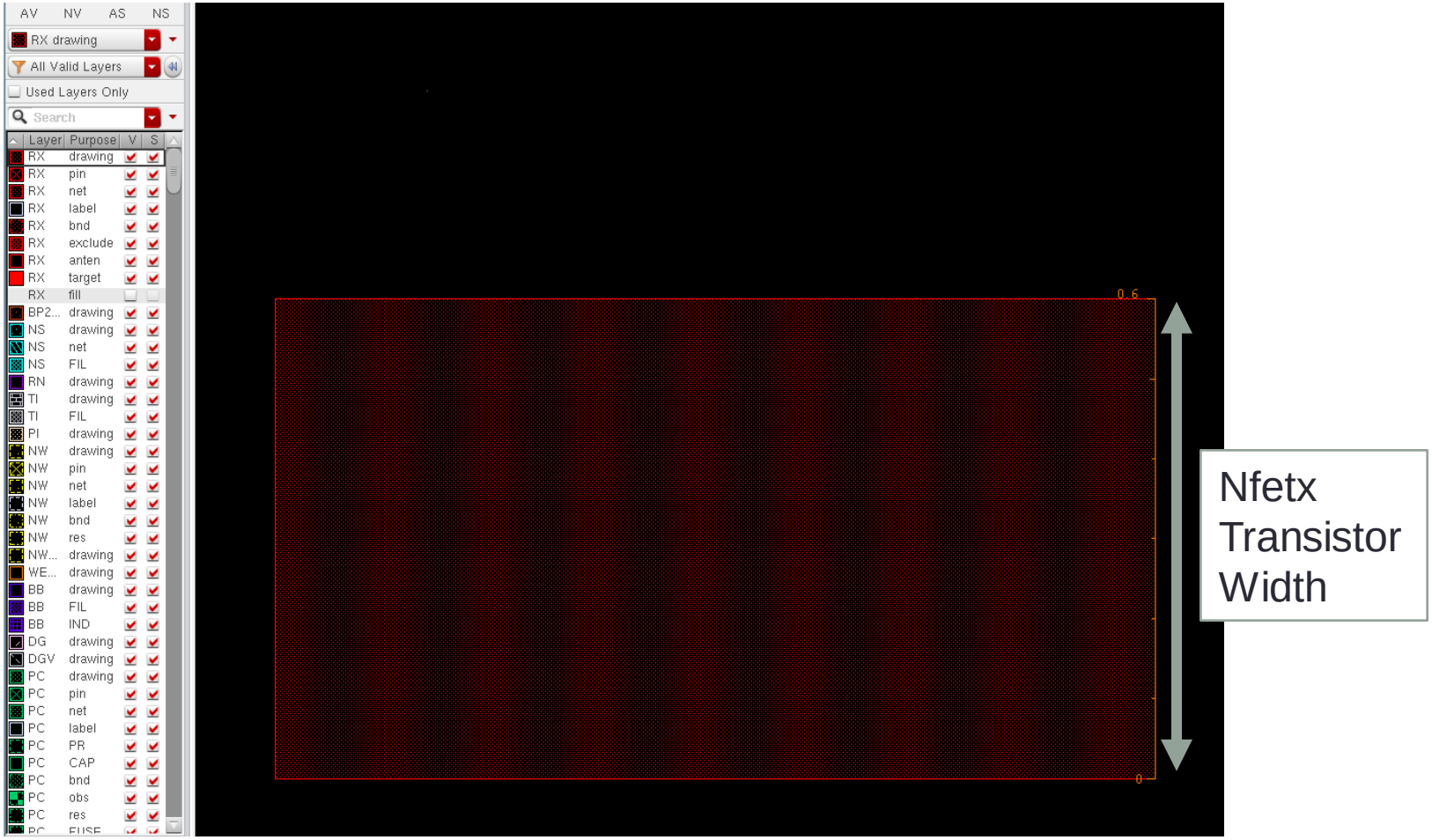
3.2 Build the layout of inverter std cell

- Useful editing tools
- Stretch:
  - Edit->Stretch (or hit s)
- How to use stretch?
  - Hit s
  - On the dialog box Stretch, hit hide.
  - Go back to the Virtuoso Layout Editing window, click on one edge of a rectangular with left mouse, release the mouse, the edge moves around with your mouse. Then click again to finish stretch.



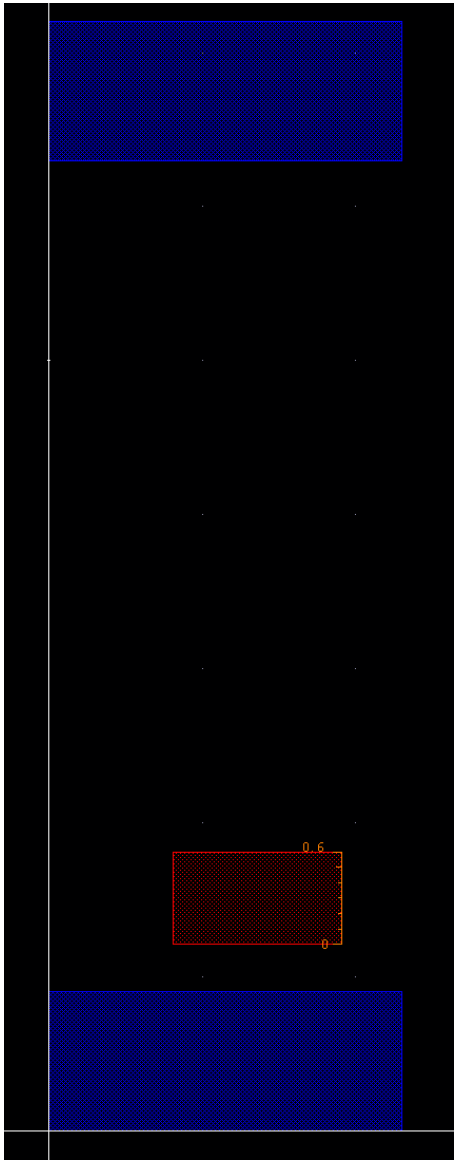
3.2 Build the layout of inverter std cell

- Draw a rectangle on the RX drawing layer
- The width of the rectangle corresponds to the width of your nfetx in the schematic view (Ex. The tutorial showed an neftx width of 0.6um)



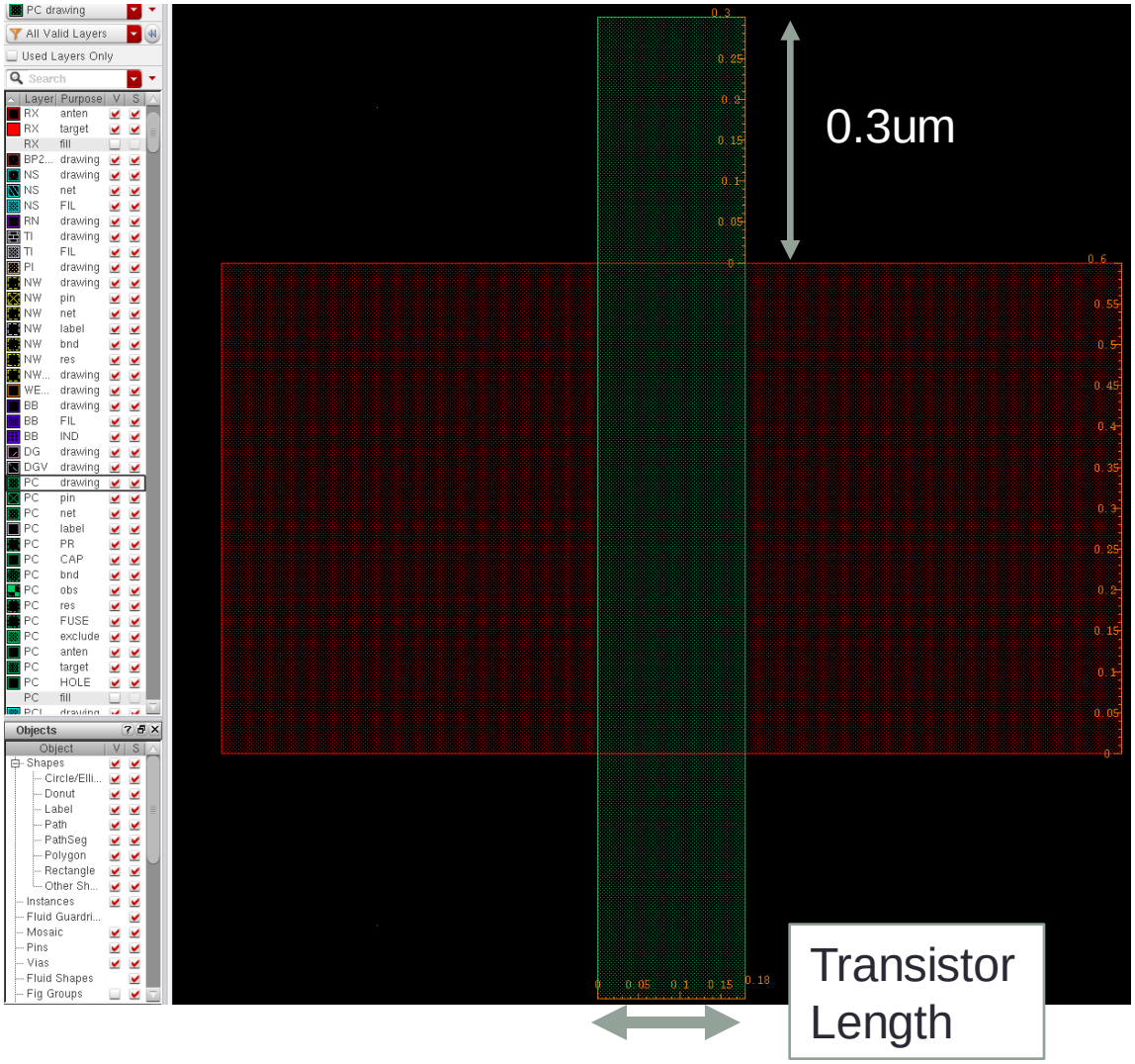
3.2 Build the layout of inverter std cell

- Place the RX rectangle just created near the GND rail
- To the right is a diagram for size and scale



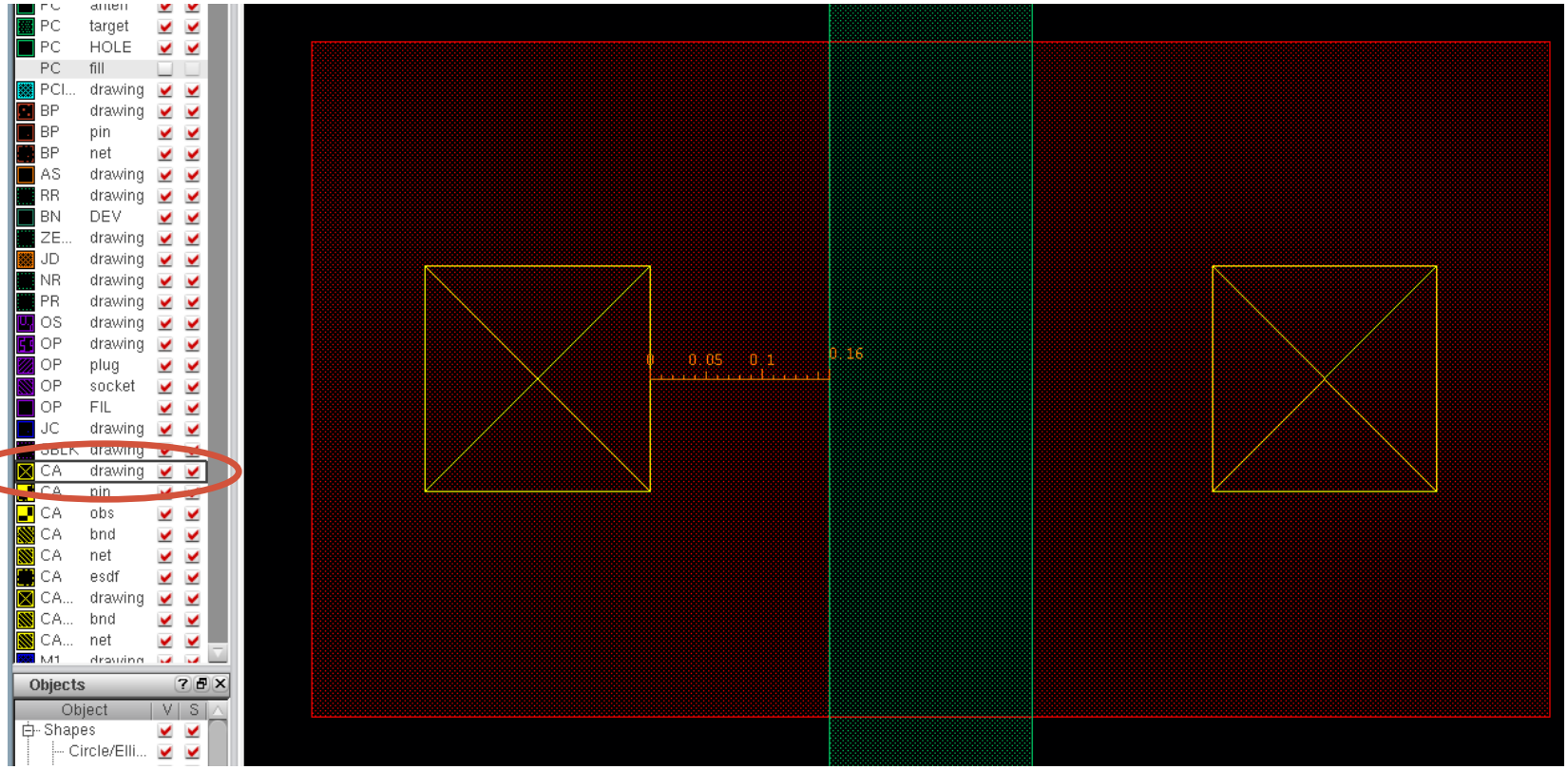
3.2 Build the layout of inverter std cell

- Draw the gate on the PC drawing layer
- The length of the gate is determined by the technology being used. Since 180nm technology is being used the length of the gate should be 0.18um
- Ensure that the poly sticks past the RX layer by 0.3um on each side or a DRC error will result



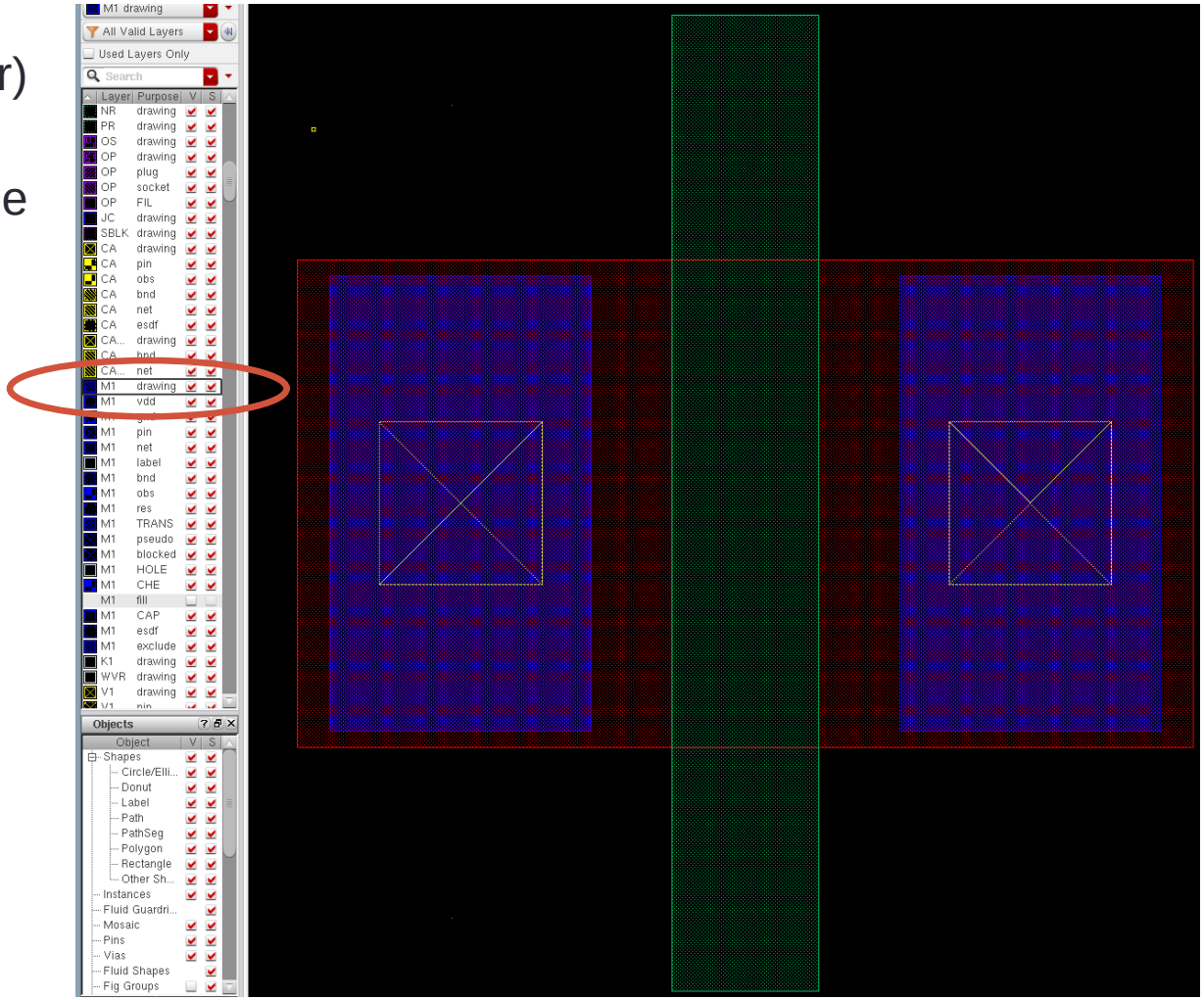
3.2 Build the layout of inverter std cell

- Create 2 contacts on the CA drawing layer
- The size of the contacts should be 0.2um x 0.2um
- The contacts should also be 0.16um away from the poly (PC drawing layer)



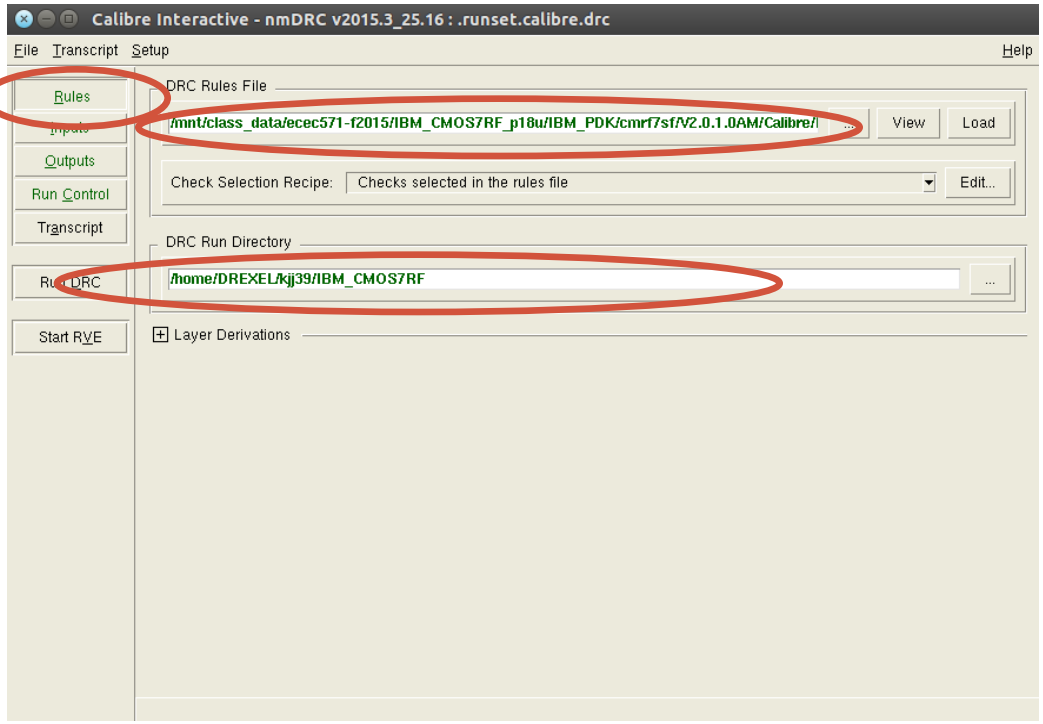
3.2 Build the layout of inverter std cell

- Cover the contacts with metal1 (M1 drawing layer)
- Note: The area of the metal 1 rectangle must be 0.172 sq. um or larger



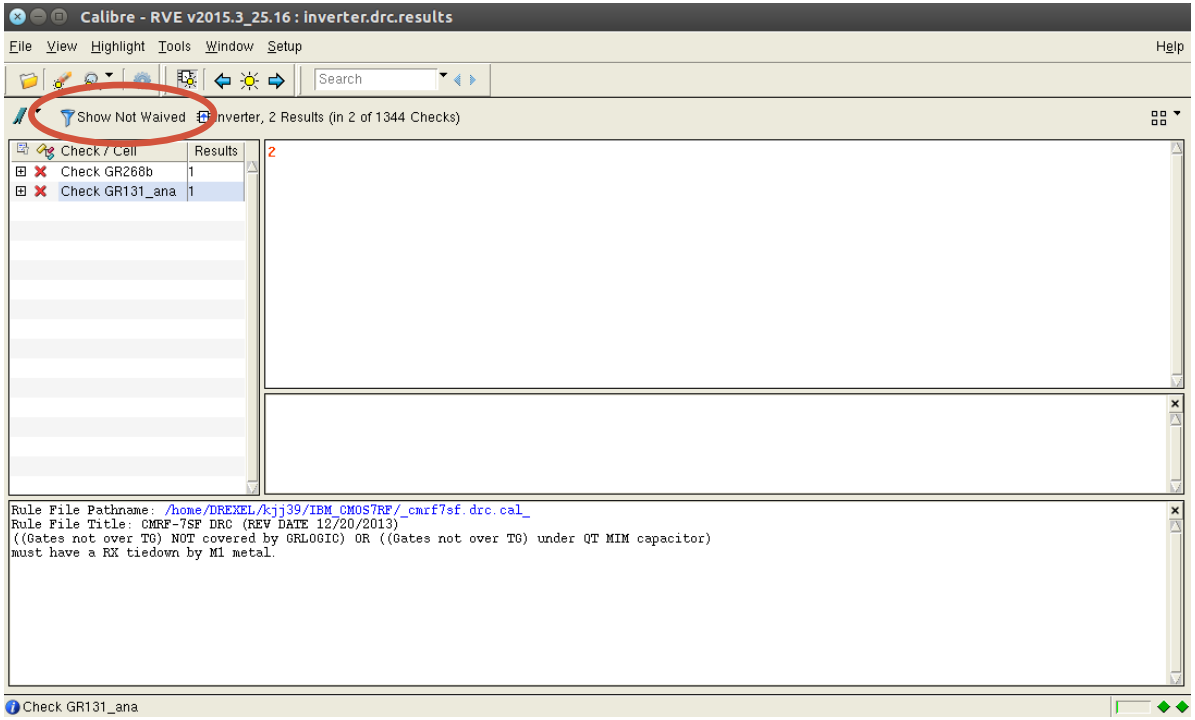
3.2 Build the layout of inverter std cell

- Now that the nfetx has been created in layout a DRC check will be run to verify the layout done so far
- Open Calibre -> Run nmDRC
- Click on the Rules tab on the left hand side
- Ensure the DRC Rules file has the following path /mnt/class_data/ecec571-f2015/IBM_CMOS7RF_p18u/IBM_PDK/cmrf7sf/V2.0.1.0AM/Calibre/DRC/cmrf7sf.drc.cal
- DRC Run directory can be set to your working directory.
- Click Run DRC



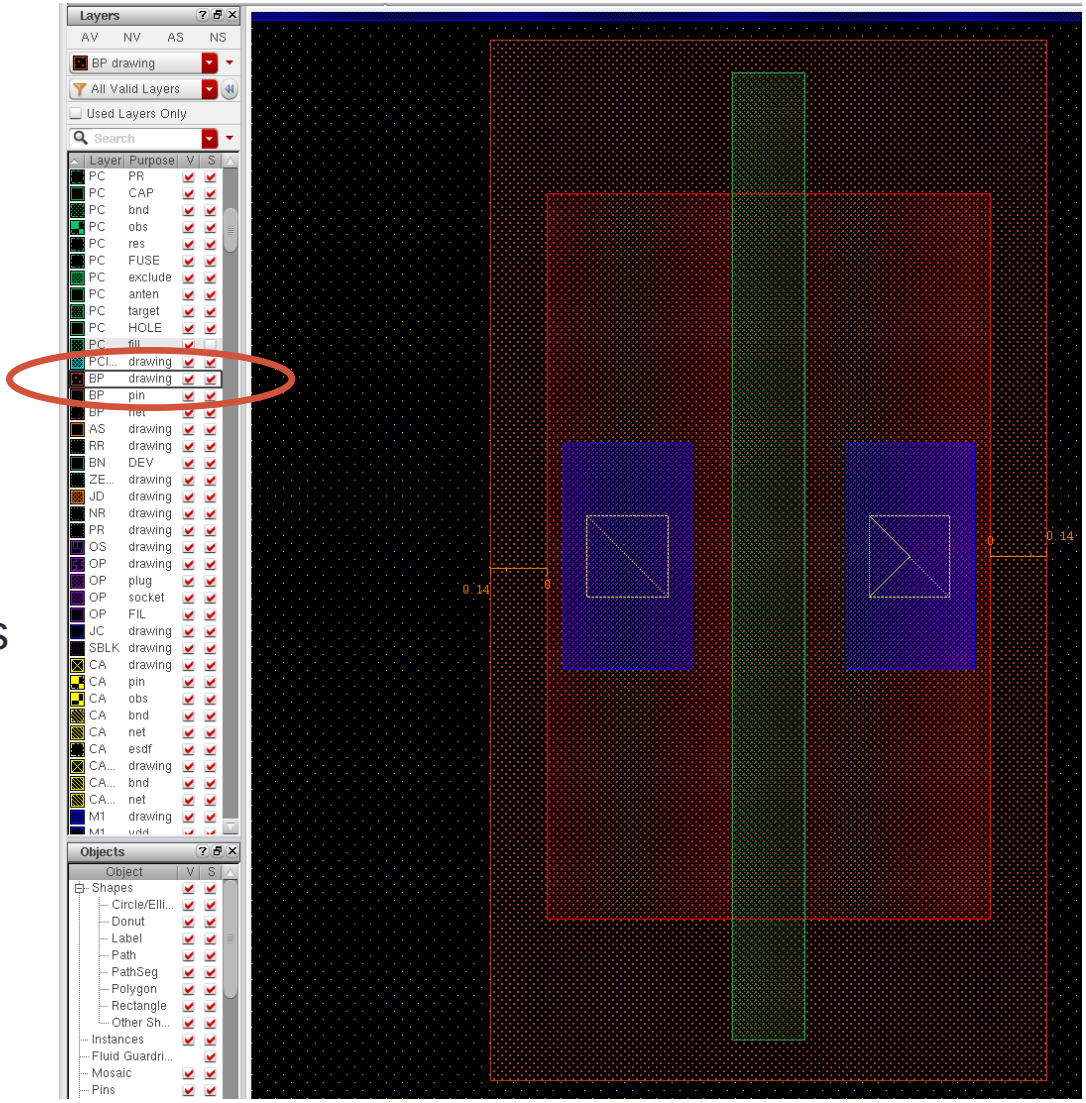
3.2 Build the layout of inverter std cell

- If the DRC run was successful you should see the following screen
- Clicking the Show All button and clicking Show Not Waived will show any errors
- The errors GR268b and GR131_ana should be showing
  - GR268b – (RX N+ Junction to RX Psub Contact) outside of NW for no latchup <= 53.0um
  - GR131_ana – ((Gates not over TG) NOT covered by GRLOGIC) OR ((Gates not over TG) under QT MIM capacitor)
- If you have any other errors try to fix them and re-run DRC



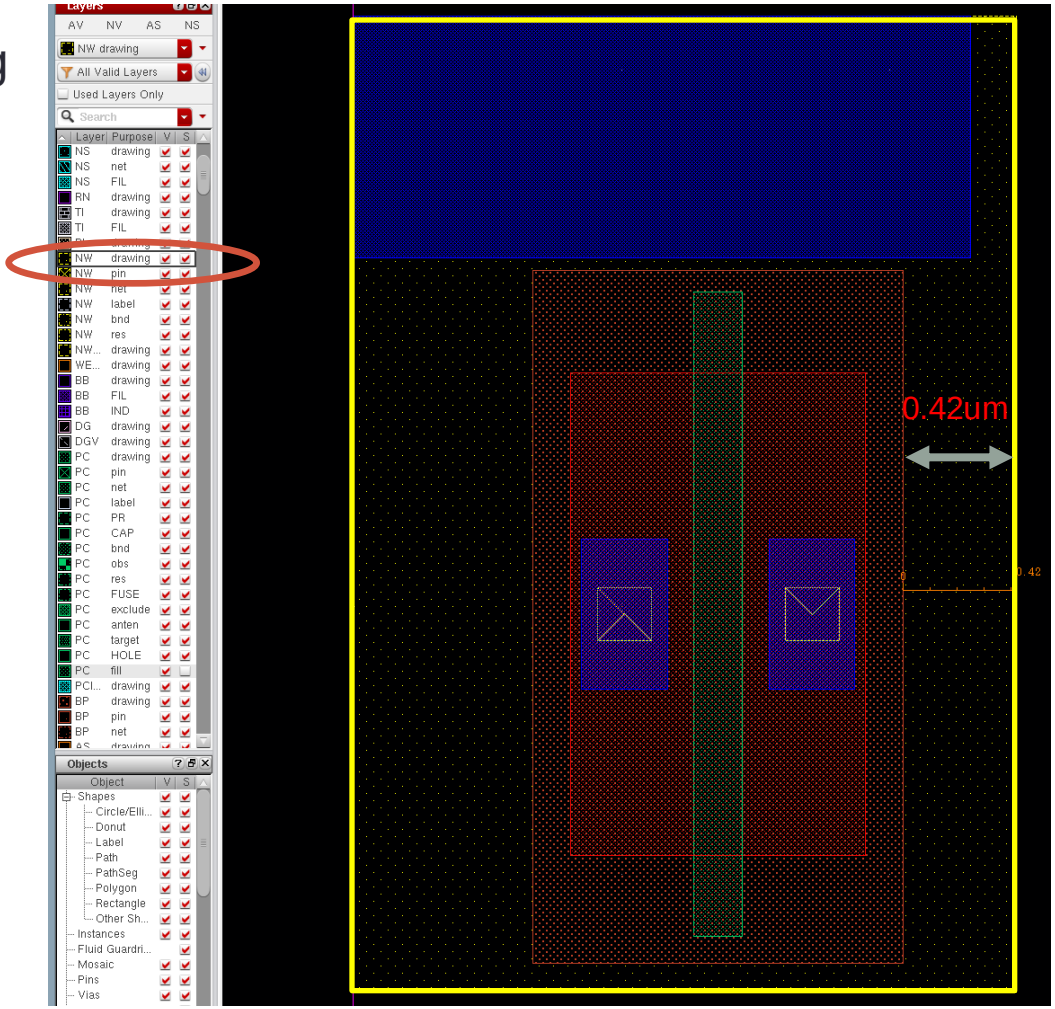
3.2 Build the layout of inverter std cell

- Now we are going to create the pfet
- It is ok to copy the nfetx and change the width to match the width in the schematic
- Once the width has been changed add a rectangle of BP drawing layer around the RX of the pfet
- Make sure the BP layer extends past the RX layer by 0.14um



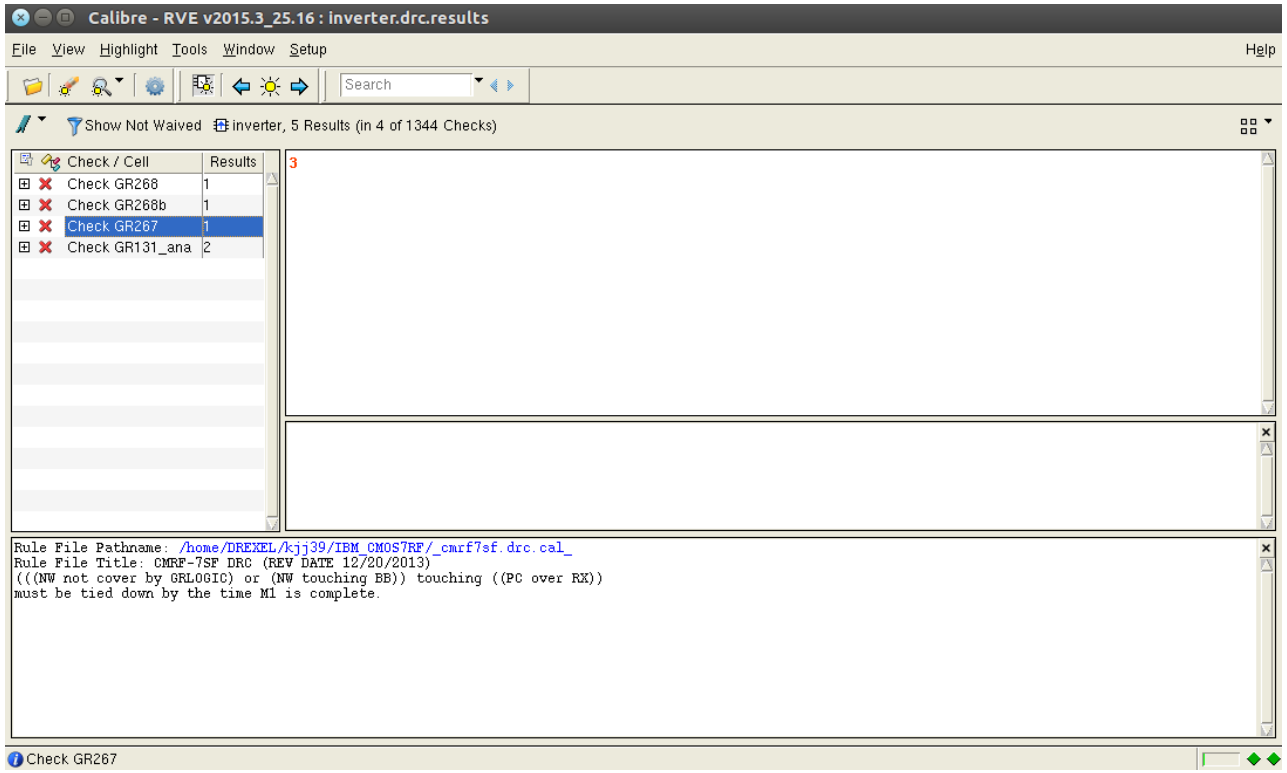
3.2 Build the layout of inverter std cell

- Add a rectangle of NW drawing layer around the BP of the pfet
- Make sure the NW layer extends past the BP layer by 0.42um
- Note: The NW layer is highlighted in the picture to the right with a yellow box, which will not be shown in the actual layout



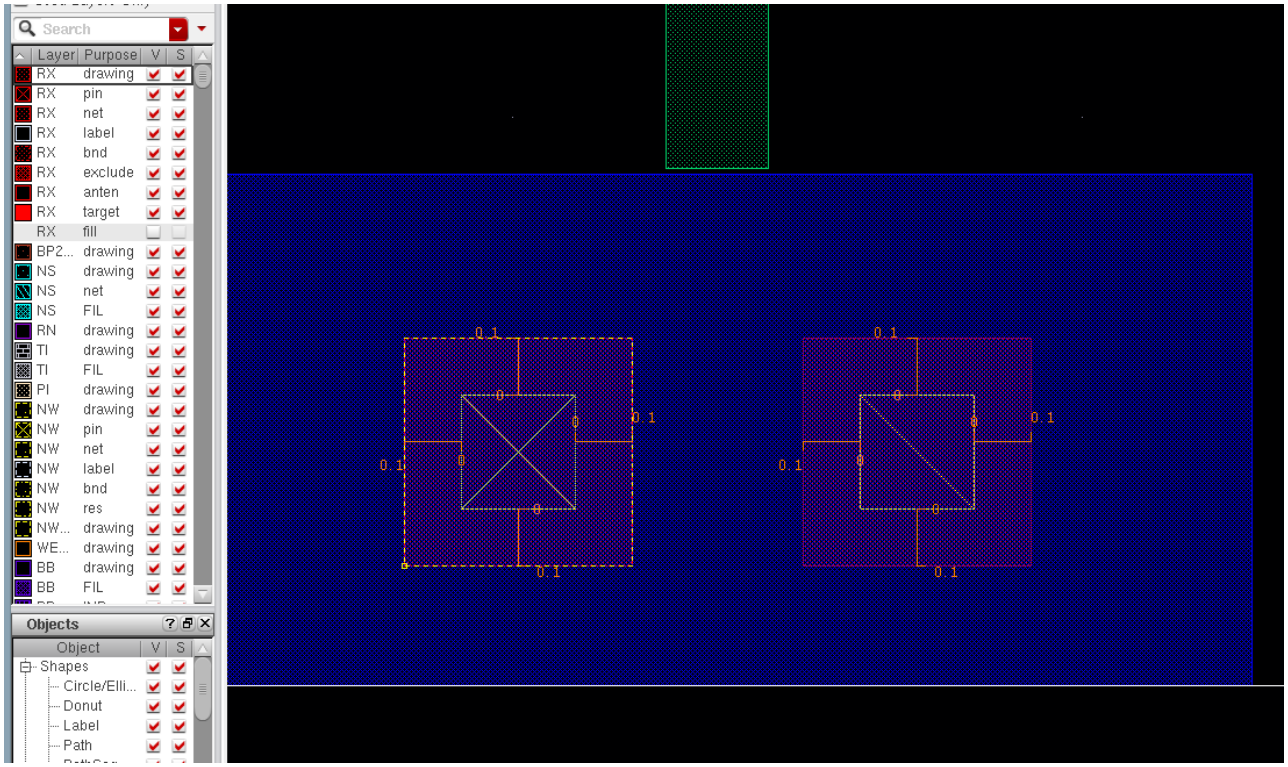
3.2 Build the layout of inverter std cell

- Run DRC again with the pfet now inserted
- There will be two additional expected errors
  - GR268 – (RX P+ Junction to RX NW Contact) outside of NW for no latchup <= 53.0um
  - GR267 - ((NW not cover by GRLOGIC) OR (NW touching BB)) touching ((PC over RX)) must be tied down by the time M1 is complete
- If you have any other errors try to fix them and re-run DRC



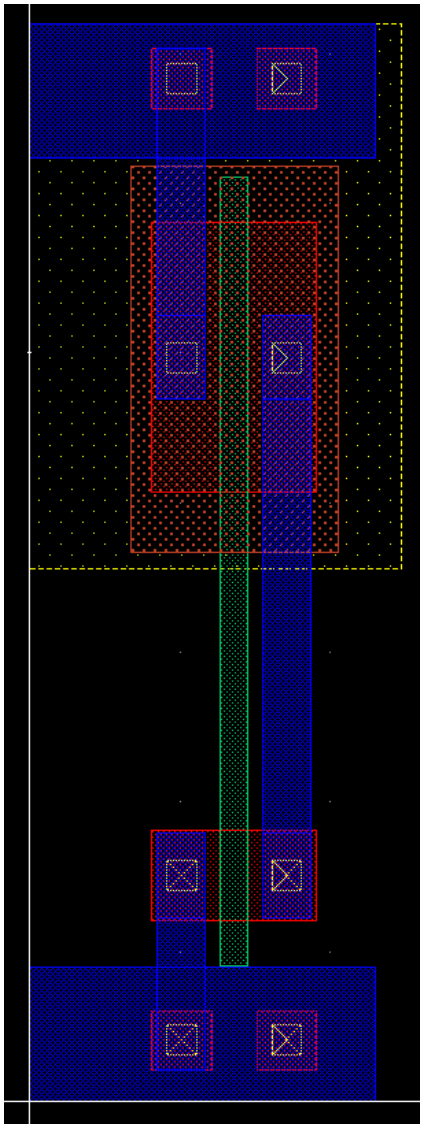
3.2 Build the layout of inverter std cell

- Create CA drawing layer contacts and surround them with RX drawing layer
- The CA contacts should be 0.2 x 0.2 um and the RX should extend the CA by 0.1um
- Create two of these contacts on both the GND and VDD rails



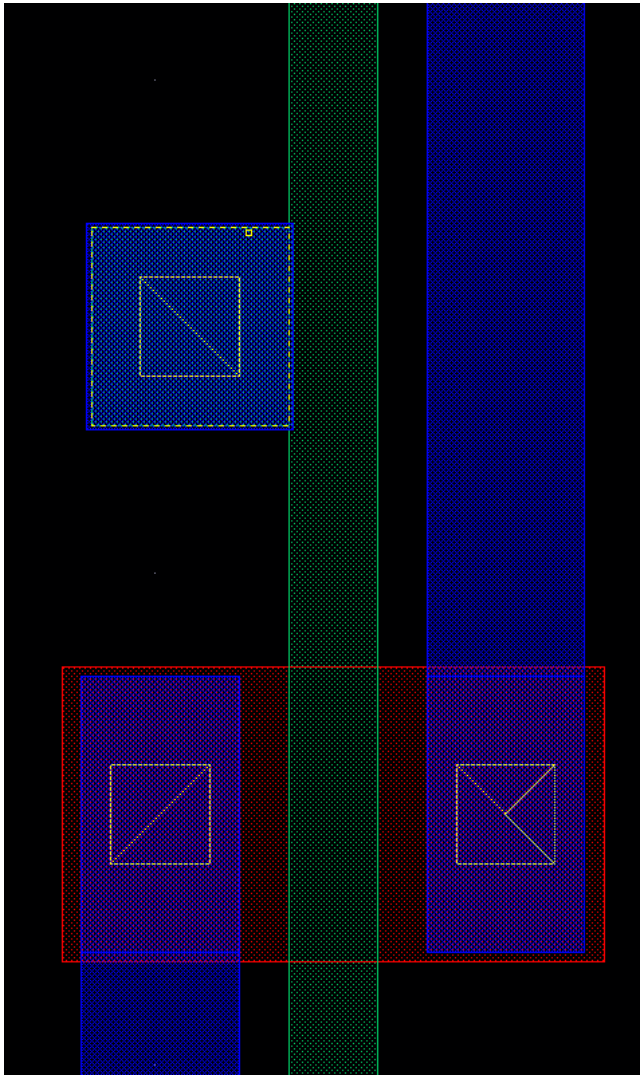
3.2 Build the layout of inverter std cell

- Make the connections
  - Connect gate of nfetx and pfet
  - Connect Source of PMOS to VDD
  - Connect Source of NMOS to GND
  - Tie two Drains together
- The connections should be identical with the schematic



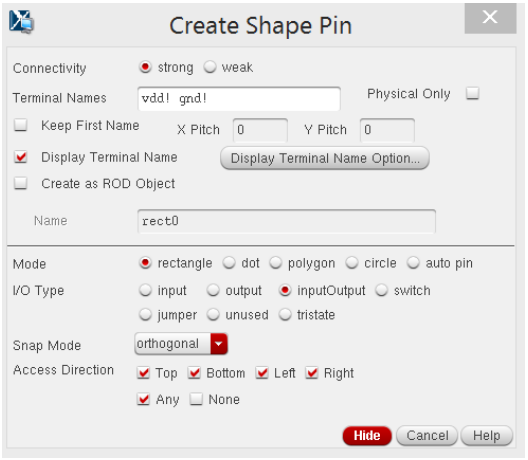
3.2 Build the layout of inverter std cell

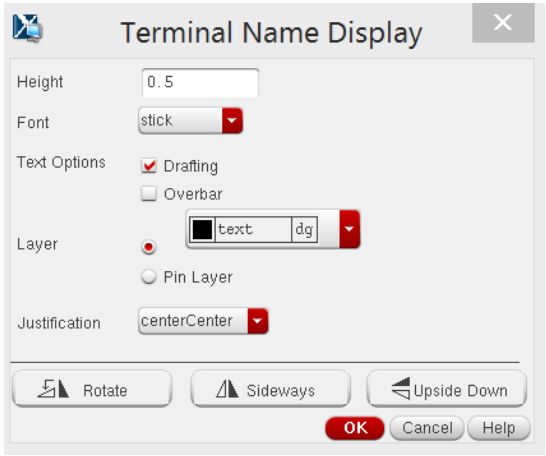
- Make I/O nodes available in Metal1
  - As a standard practice that will help when connecting multiple cells (logic gates), we need to ensure that all of our input and output nodes have a connection in Metal1.
  - The inverter design only has its input that is not connected to Metal1 at this stage
  - Create a contact on CA similar to the previous steps, and create M1 drawing and PC drawing surrounding the contact similar to the diagram to the right



3.2 Build the layout of inverter std cell

- Add Pins to I/O nodes
- In the Virtuoso Layout Editing window select
- Create -> Pin to open the Create Symbolic Pin window.
  - Set the **global power pins**.
    - Click on M1 pin in the LSW
    - In the Terminal Names field, enter vdd! gnd! which are the names of the two global power pins. Put both names in this field, separate by a space.
    - Select Display Terminal Name. In I/O Type select inputoutput.
    - Click on Display Terminal Name Option… And change the Height to 0.5 for the size of the text.
    - **The pin labels must be on the metal label layer (For Metal 1: M1 – Label) for LVS to work!**
    - **Since the M1-Label layer isn't available when placing the pin, click on the pin label after creation and press q to edit the text layer of the label**



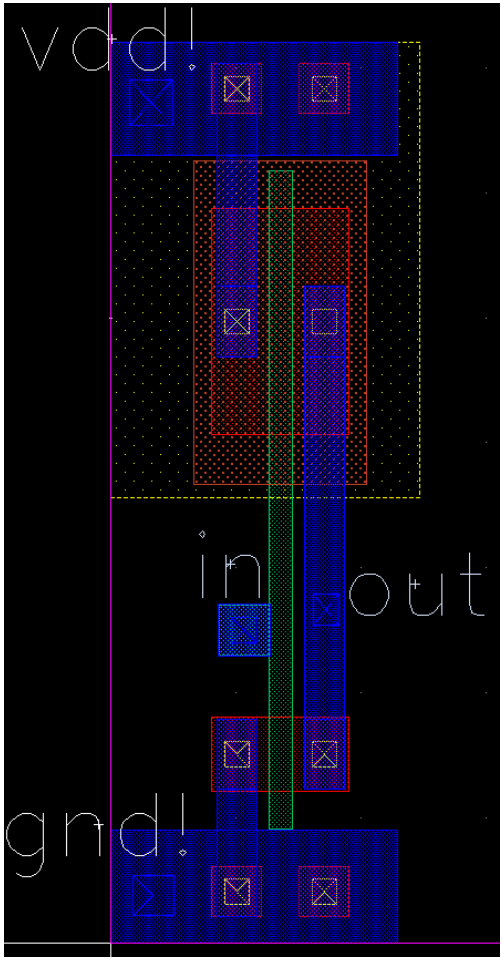


3.2 Build the layout of inverter std cell

- Add Pins to I/O nodes
- In the Virtuoso Layout Editing window select
- Create -> Pin to open the Create Symbolic Pin window.
  - Click on M1 pin in the LSW
  - In the Terminal Names field, enter in from the input name of the inverter
  - Select Display Terminal Name. In I/O Type select input.
  - Click on Display Terminal Name Option... And change the Height to 0.5 for the size of the text.
  - Place the pin
  - Change label layer to M1-Label
- Create -> Pin to open the Create Symbolic Pin window.
  - Click on M1 pin in the LSW
  - In the Terminal Names field, enter out from the output name of the inverter
  - Select Display Terminal Name. In I/O Type select output.
  - Click on Display Terminal Name Option... And change the Height to 0.5 for the size of the text.
  - Place the pin
  - Change label layer to M1-Label

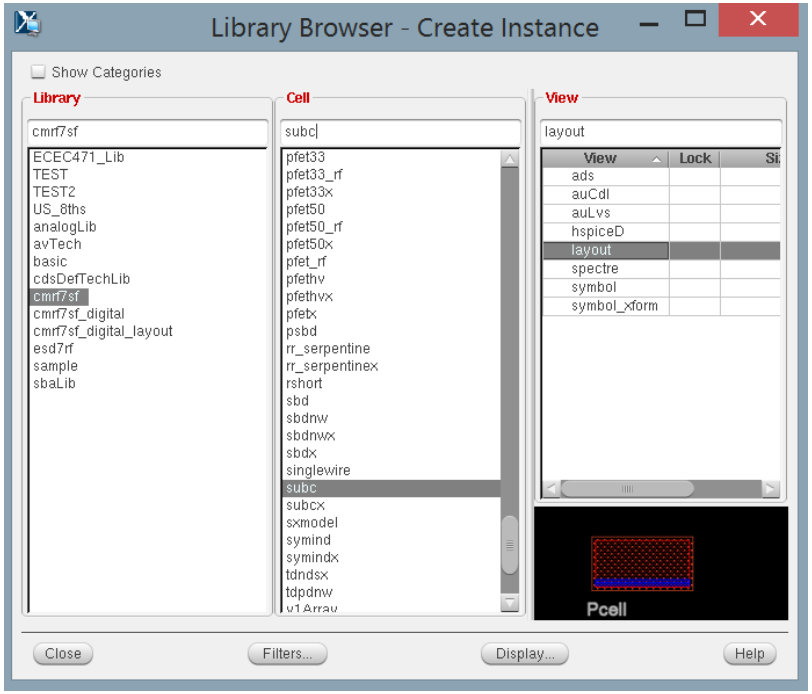
3.2 Build the layout of inverter std cell

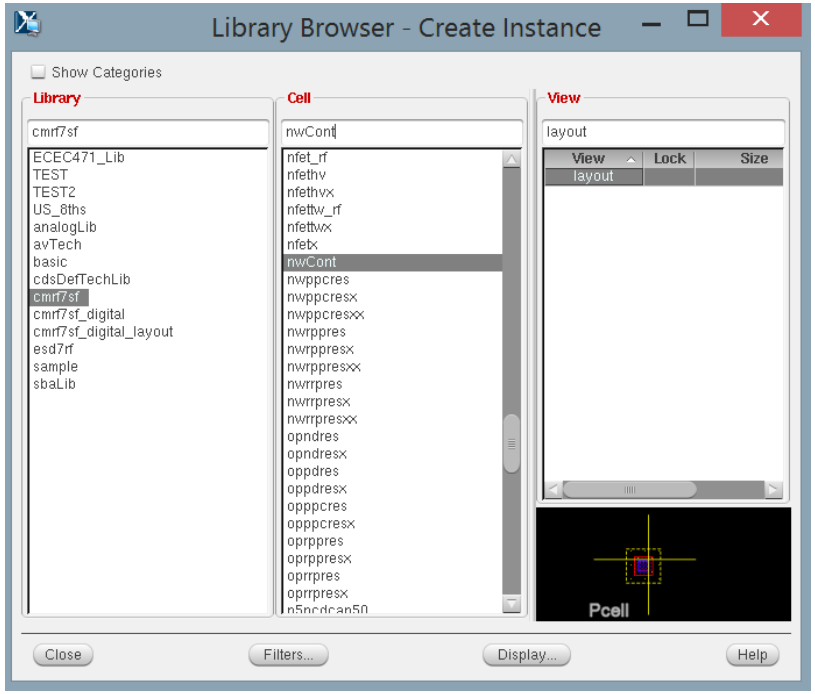
- After the pins are placed the layout should now look similar to the following



3.2 Build the layout of inverter std cell

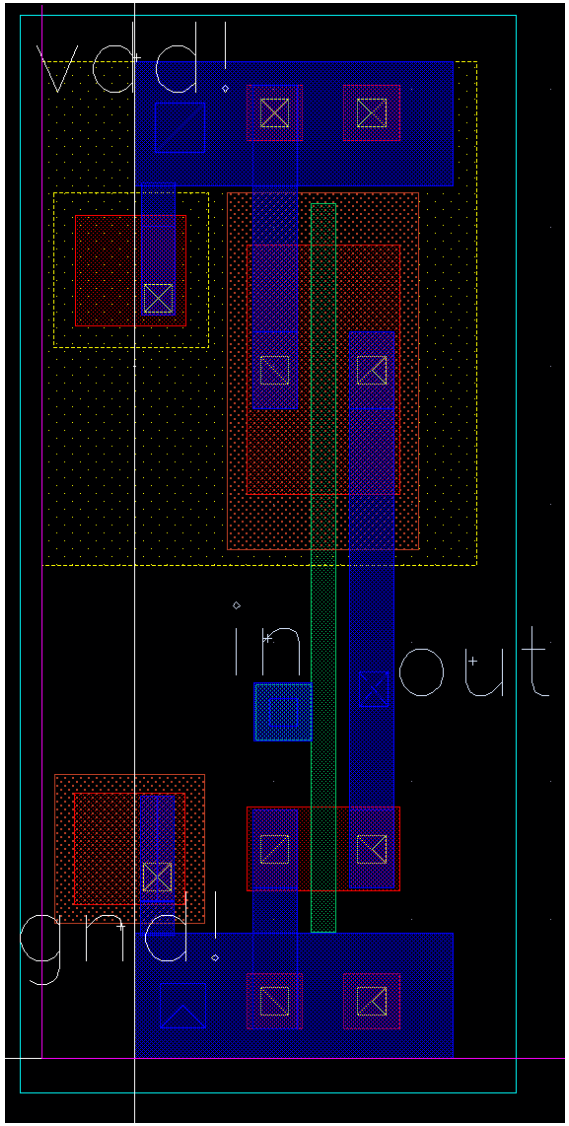
- Add nwcont and subc instances to design
- Connect the nwcont to the vdd! rail
- Connect the subc to the gnd! rail





3.2 Build the layout of inverter std cell

- Ensure the nwcont is connected to the nw drawing layer already in the design
- Add a GR logic rectangle around the entire inverter
- The layout should look similar to the follows



3.2 Build the layout of inverter std cell

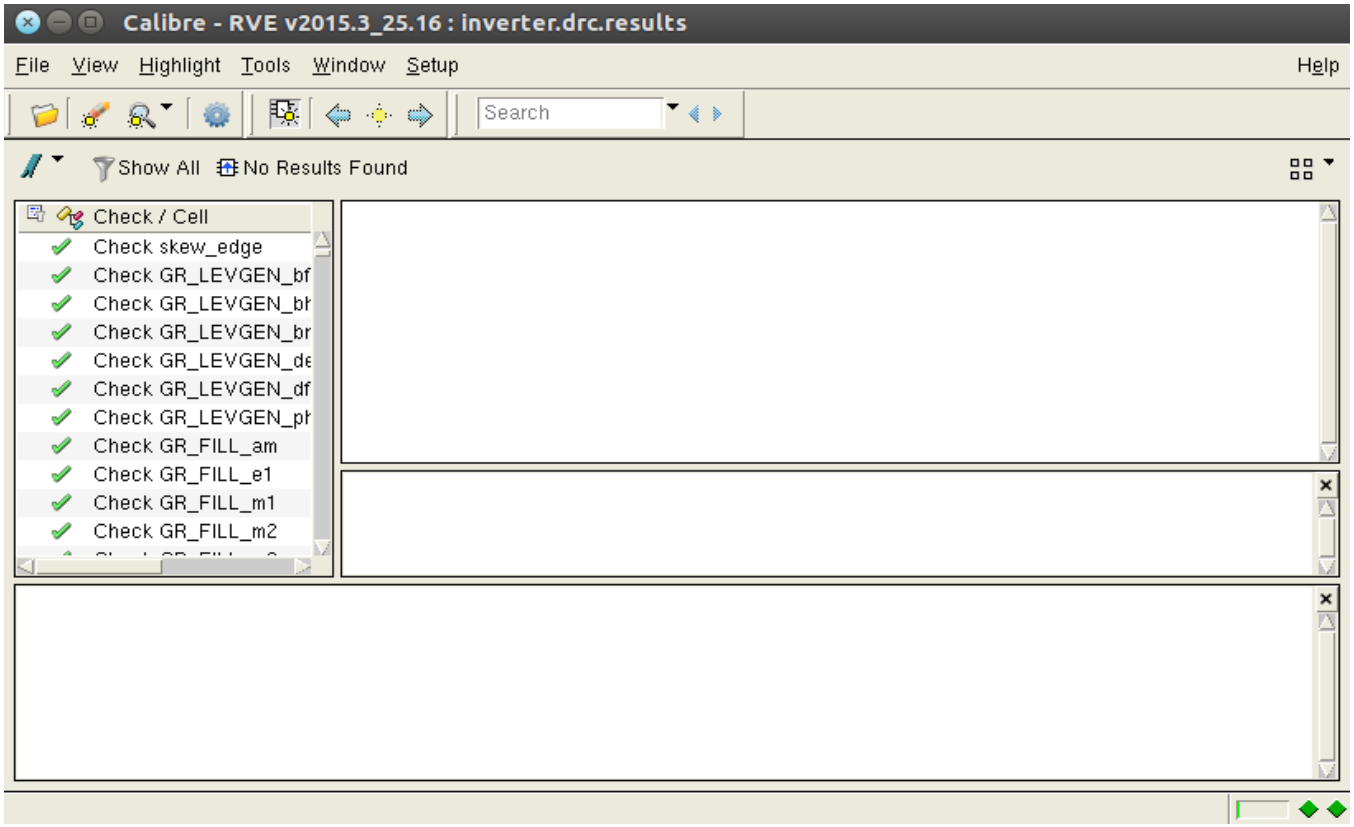
- Minimize the width of the layout
  - There is no strict guidelines for minimize the width.
  - Rules of thumb:
    - Let the VDD and GND rails extend beyond the boundary of p-select/n-select, active region, poly for easy connection (when you connects multiple standard cells in one row.)
    - PMOS in one row can share a N-WELL but not the active region or p-select.
    - NMOS in one row cannot share the n-select.

3.3 Design Rule Check (DRC)

- Layout must be drawn according to strict design rules. An automatic program checks every polygon in your design against these design rules and report violations.
- This process is Design Rule Checking (DRC) and MUST be done for every layout to ensure it will function properly when fabricated.
- Do DRC frequently along with you adding layers into your layout.

3.3 Design Rule Check (DRC)

- Run DRC on your final layout and make sure the output is as shown
- If you have any additional errors fix them now
- No Errors should be remaining



3.4 Layout vs. Schematic (LVS)

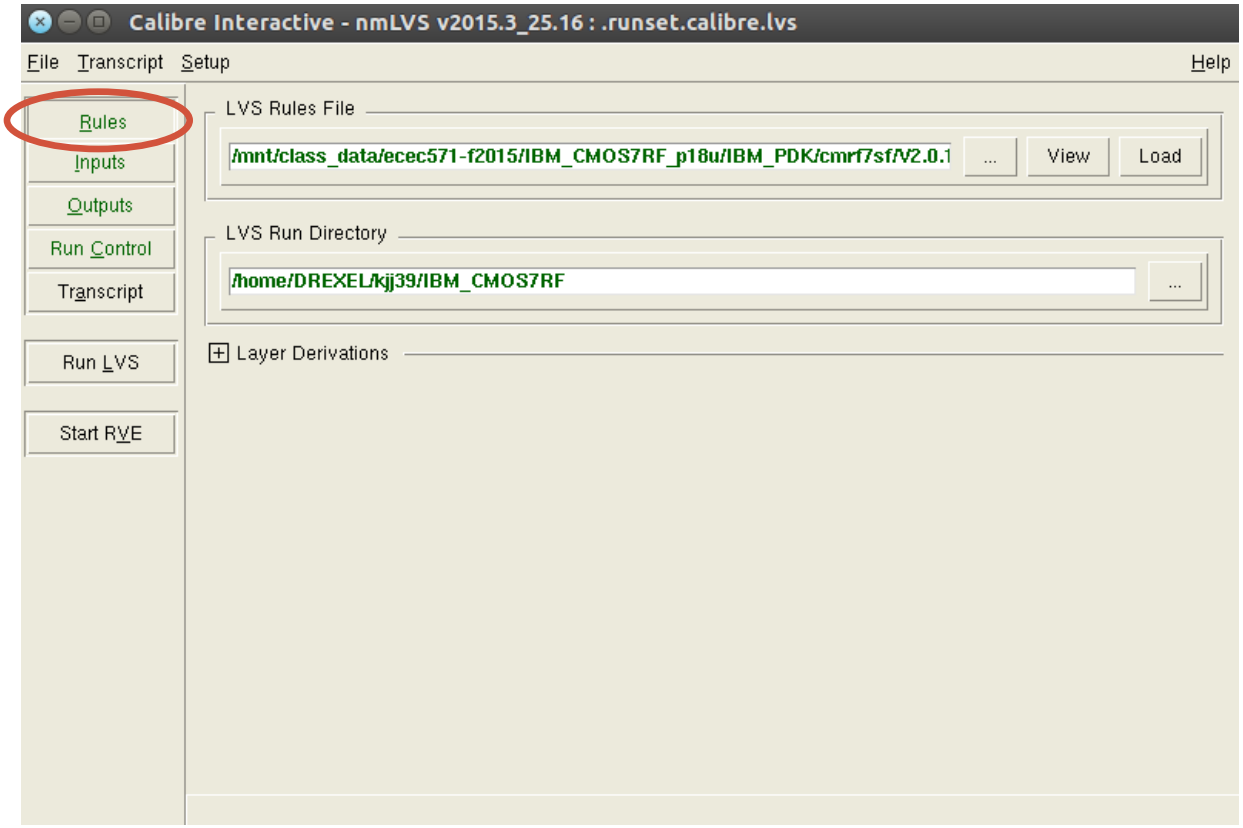
- The Layout vs. Schematic (LVS) process will ensure that the components in the schematic match the layout.
- Do LVS after the layout is complete and DRC is clean.

3.4 Layout vs. Schematic (LVS)

- Open Calibre->Run nmLVS…
- Make sure the LVS Rules Rile is as follows

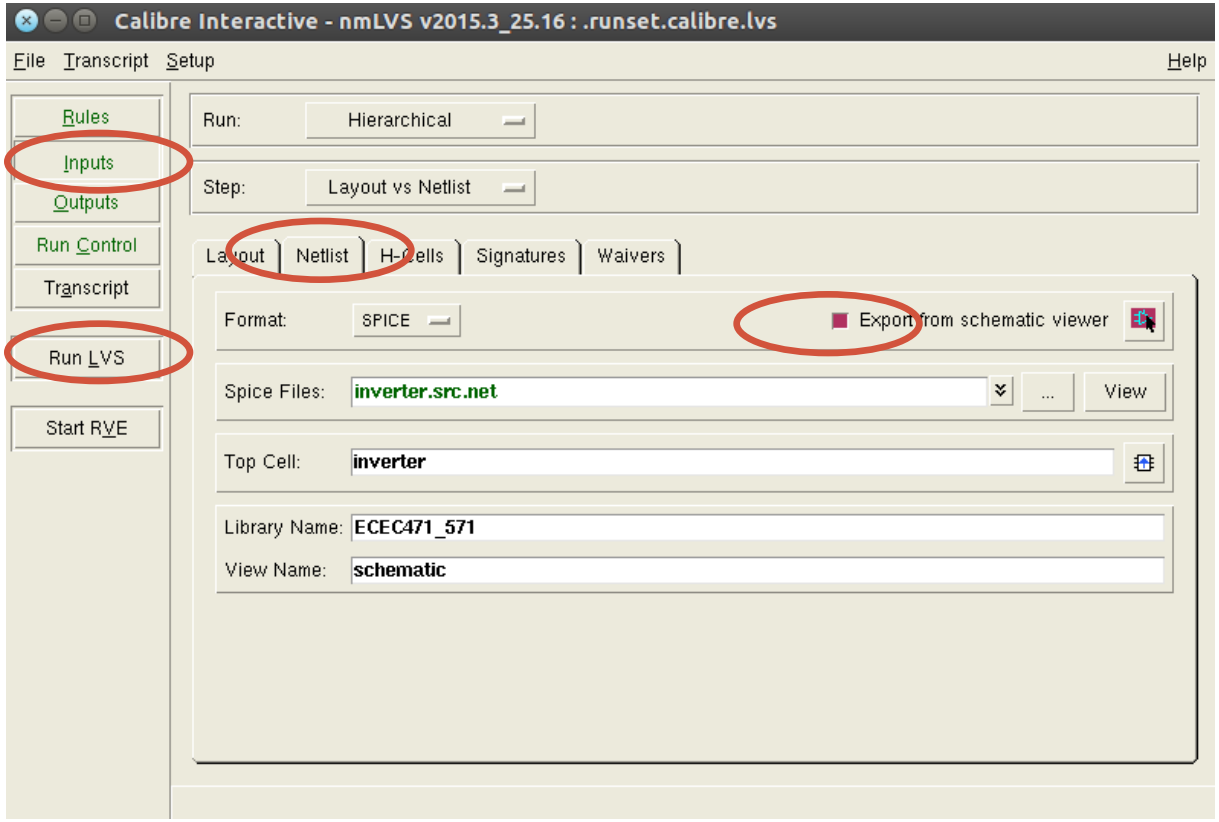
/mnt/class_data/ecec571-f2015/IBM_CMOS7RF_p18u/IBM_PDK/cmrf7sf/V2.0.1.0AM/Calibre/LVS/cmrf7sf.lvs.cal

- Ensure the LVS Run Directory is set to where you want to run LVS



3.4 Layout vs. Schematic (LVS)

- Click the Inputs tab
- Select the Netlist tab within and select Export from schematic viewer
- Then select Run LVS



3.4 Layout vs. Schematic (LVS)

- If the LVS run is successful the following will pop-up
- If the run is not successful use the LVS Debug environment that pops up to examine the issues in the design
- Note: if LVS fails completely check the CIW for information