**Introduction to VLSI Design –Laboratory**

**ECEC 471**

**CMOS Inverter**

**Objective:**

The object of this lab is to design a schematic and layout of a CMOS inverter using Cadence Virtuoso. Starting with designing a non-symmetric inverter schematic, the ultimate goal is to obtain a symmetric inverter by adjusting the switching threshold to VDD/2 through DC simulation and parametric analysis. Then at the end verifications of both schematic and layout will be done.

**Introduction:**

CMOS or Complementary metal-oxide-semiconductor inverter is a base of any circuit design. Which can be designed by one *pmos* and one *nmos* transistor where the pmos is the pull-up network and nmos is the pull-down network. The function of this inverter is take a high signal and output a low, and a low signal and output a high.

**Inverter Characteristics**

Inverter Sizing

In order to produce a symmetric inverter, the sizing of the transistors needs to be taken account for. Since the pmos works with holes to conduct and nmos works with charge carries the pmos needs to be proportionally larger than the nmos to create a symmetric inverter.

Rise time and fall time:

Rise time can be defined as the time required for the output signal to reach 90% (high) from 10% (low) of output signal/voltage.

Fall time can be defined as the time required for the output signal move to 10% (low) from 90% (high) of output signal/voltage.

Propagation delay:

Propagation delay is the measure of time it takes to get the output after applying input. Theoretically, it is the time difference from 50% of input rise transition to 50% of output rise transition.

Symmetric Inverter:

An inverter is said to be a symmetric inverter only if it has same rise and fall time. With same rise and fall time both low-high and high-low transitions will coincide in a potential that is half of VDD. In order to obtain symmetric behavior, the physical size of transistor width can be adjusted. The norm is to keep the transistor length constant throughout a particular design process since changing transistor length leads to changing the channel (gate) length.

**Simulation process and results:**

Schematic design:

The Schematic Design was implemented using Cadence Virtuoso Schematic Editor. The Initial length and width of both PMOS and PMOS was 600nm X 180nm. As shown below in Fig 1.

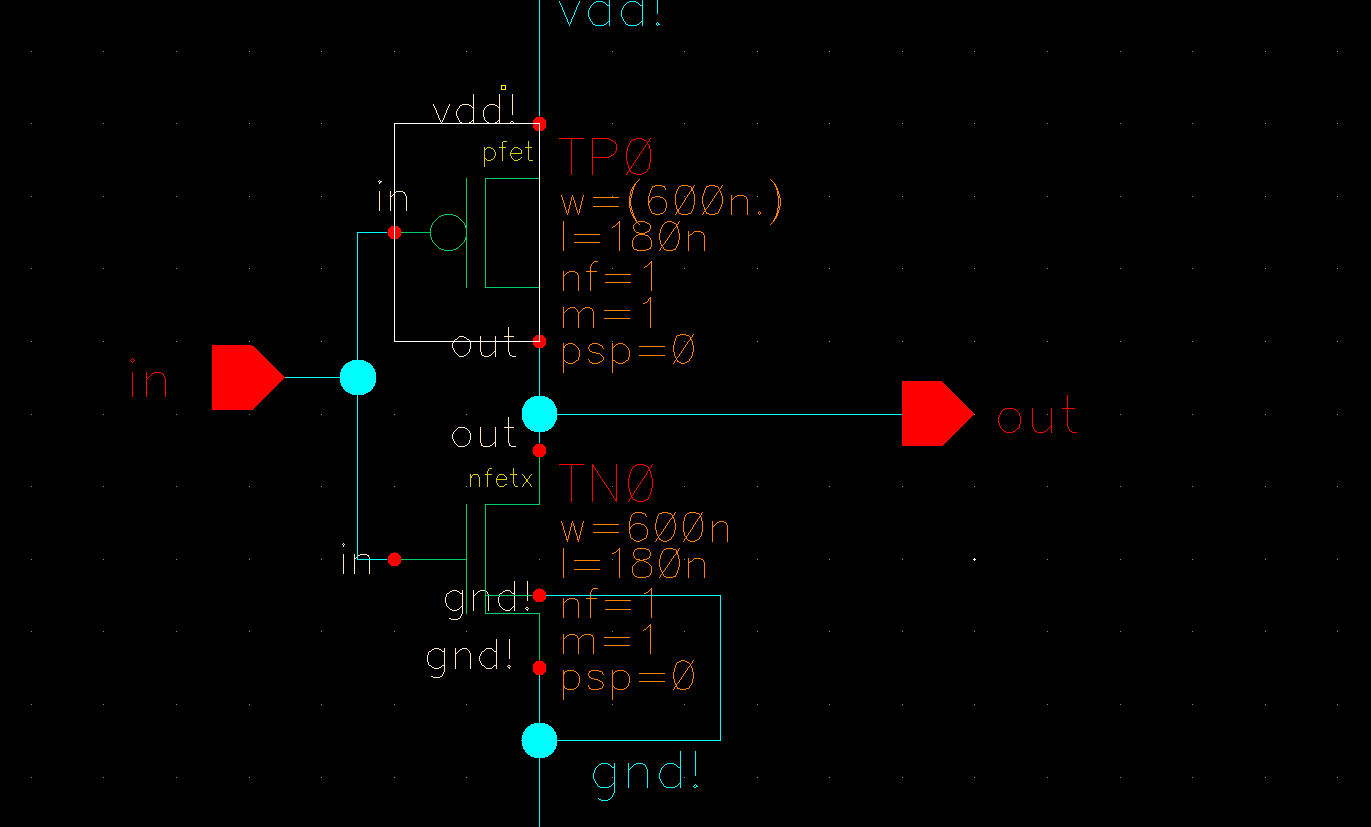


Figure 1: unsymmetrical inverter schematic

In order to simulate the transient and DC behavior of this inverter a 500fF capacitive load and voltage source (Amplitude – 1.8V, rise time – 1ps, fall time – 1ps, and pulse width – 500ns) has been connected with this inverter. The resultant top level inverter schematic is given in the following Figure 2.

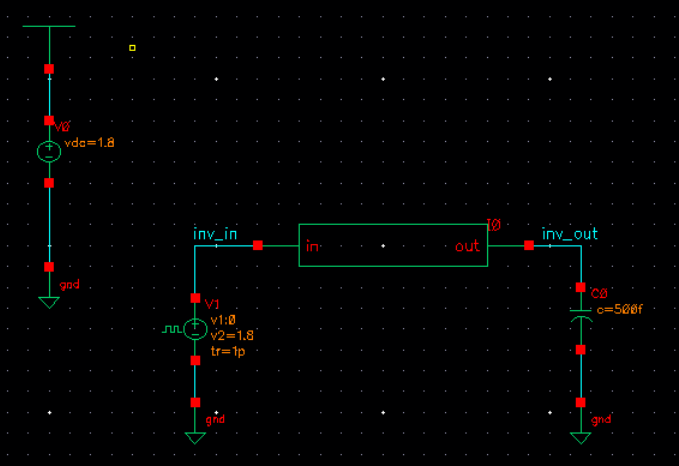


Figure 2: CMOS inverter with source and load

Through transient analysis Rise time, fall time, and propagation delay have been observed, also a DC simulation was done to create a symmetric inverter. The results of transient and DC simulation are given in Figure 3 and 4 respectively.

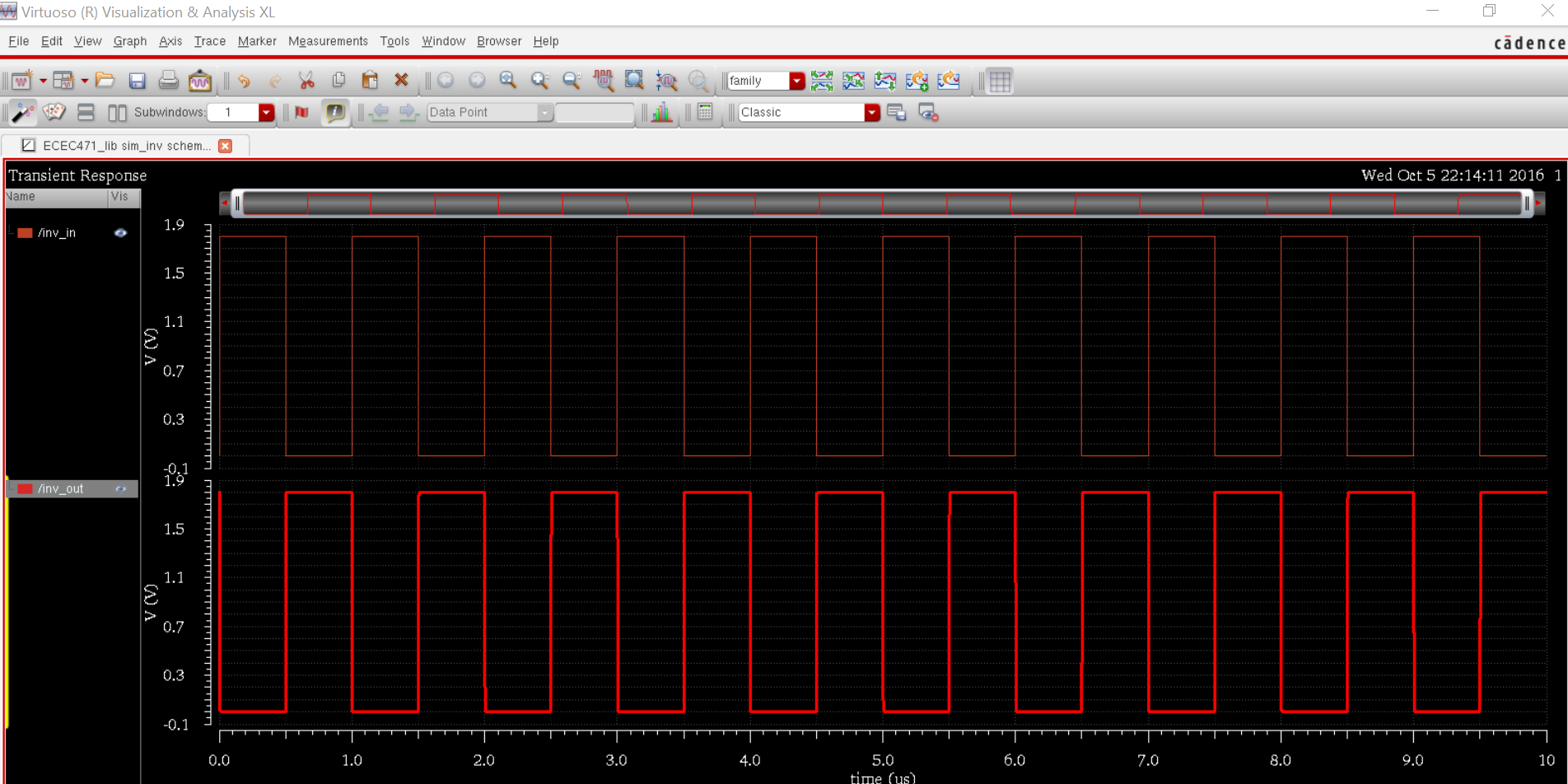


Figure 3: Transient simulation

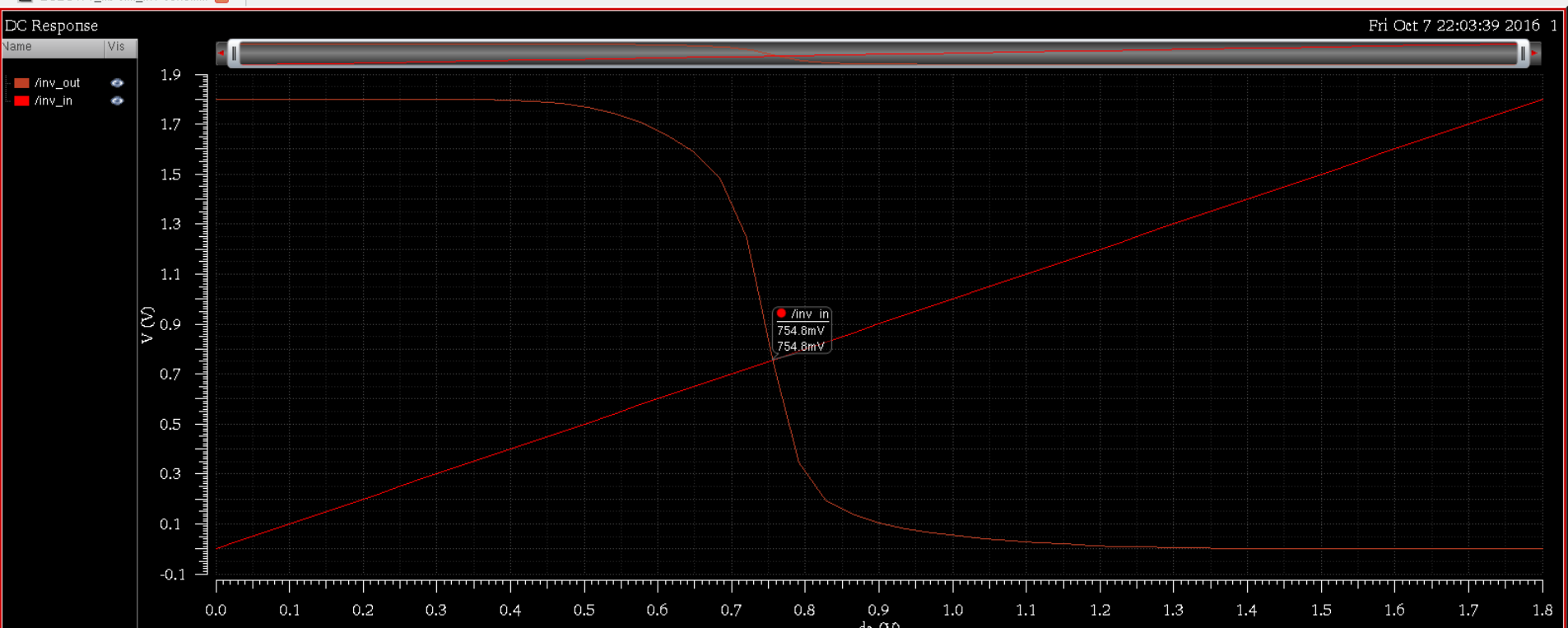


Figure 4: DC simulation showing non-symmetric behavior

The switching threshold has been found to be approximately 0.7V (Figure 4) which is not the desired switching voltage (0.9V) since the value of applied supply voltage is 1.8V. That means at this point the inverter is not symmetric.

In order to obtain the symmetric behavior parametric analysis has been done using Virtuoso Analog Design Environment to find appropriate transistor size (width). In this case the

parametric analysis has been done on PMOS since the target is to adjust the width of PMOS. The required width of PMOS for symmetric behavior has been found as 1.8um as shown in the following Figure 5.

Now, the PMOS transistor has been updated with new width (1.8um) and DC simulation has been performed again to make sure that the inverter is symmetric. The updated schematic and DC simulation results are given in the following Figure 6 and 7 respectively.

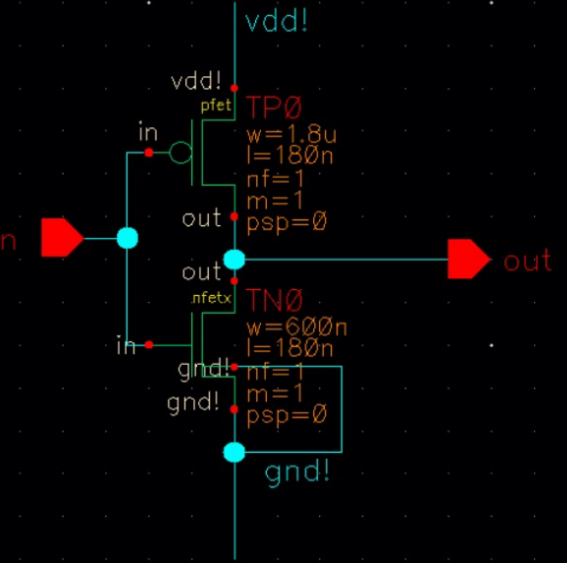


Figure 6: Updated PMOS transistor of width 1.8um



Figure 7: DC sweep of widths for PMOS to achieve 0.9V

**Layout design of symmetric inverter:**

The schematic of symmetric inverter has been designed in the previous section where the appropriate transistor sizing has been performed in order to achieve symmetric behavior. The physical layout of this inverter has been designed using Virtuoso Layout. The layout view of PMOS and NMOS transistor is given in Figure 8 with the indication of transistor length and width.

PMOS: Width – 1.8um Length – 180nm

NMOS: Width - 600nm Length – 180nm

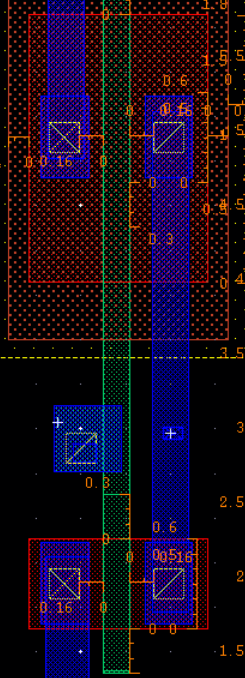


Figure 8: Layout view of PMOS/NMOS transistors (W – 1.8um and L – 180nm,

(W – 600nm and L – 180nm)

In addition to PMOS and NMOS transistors, power and ground rails has also been placed. After that two transistors have been connected with each other and with power/ground rails by metal routing and contact vias. The resultant inverter layout is given in the following Figure 10.

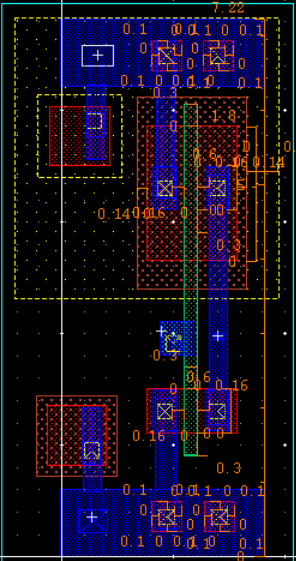


Figure 9: Layout view symmetric CMOS inverter

**Physical Verification:**

After the completion of schematic and layout design physical verification has been performed for the inverter. Two types of verification have been performed in this laboratory – 1. Design Rule Checking and 2. Layout versus Schematic Checking.

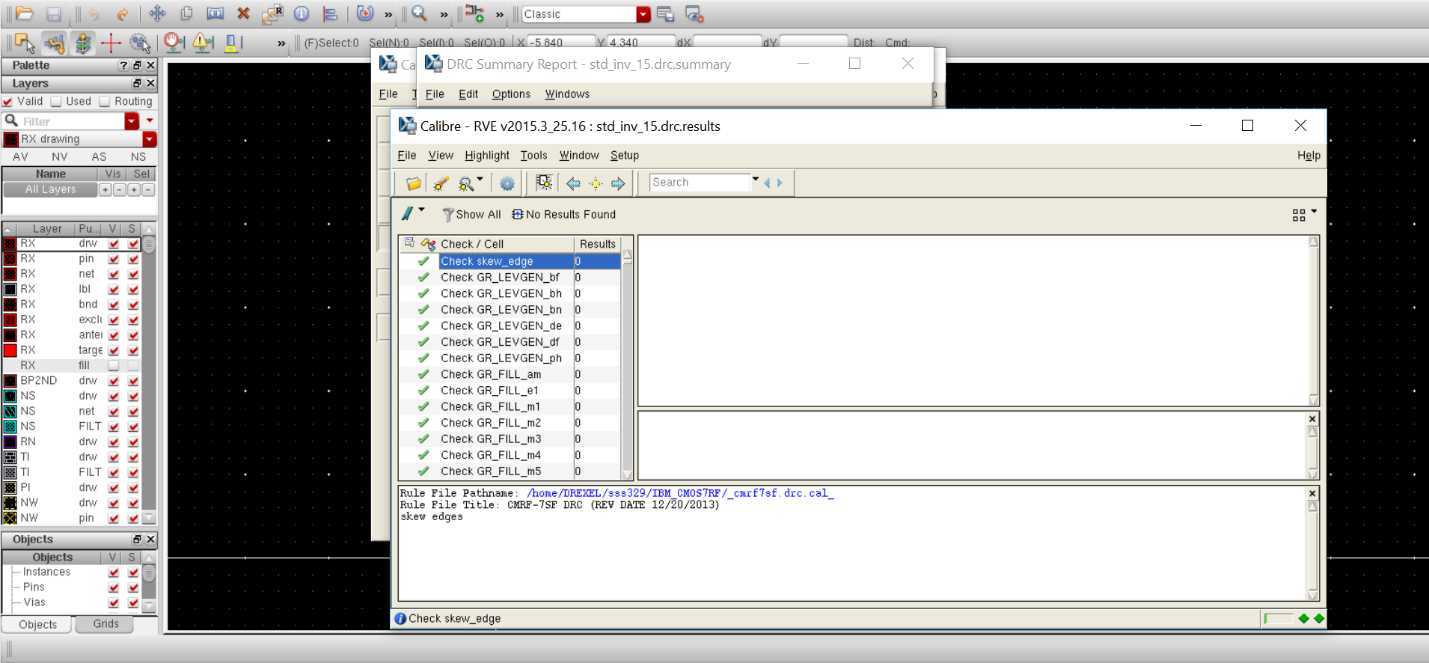
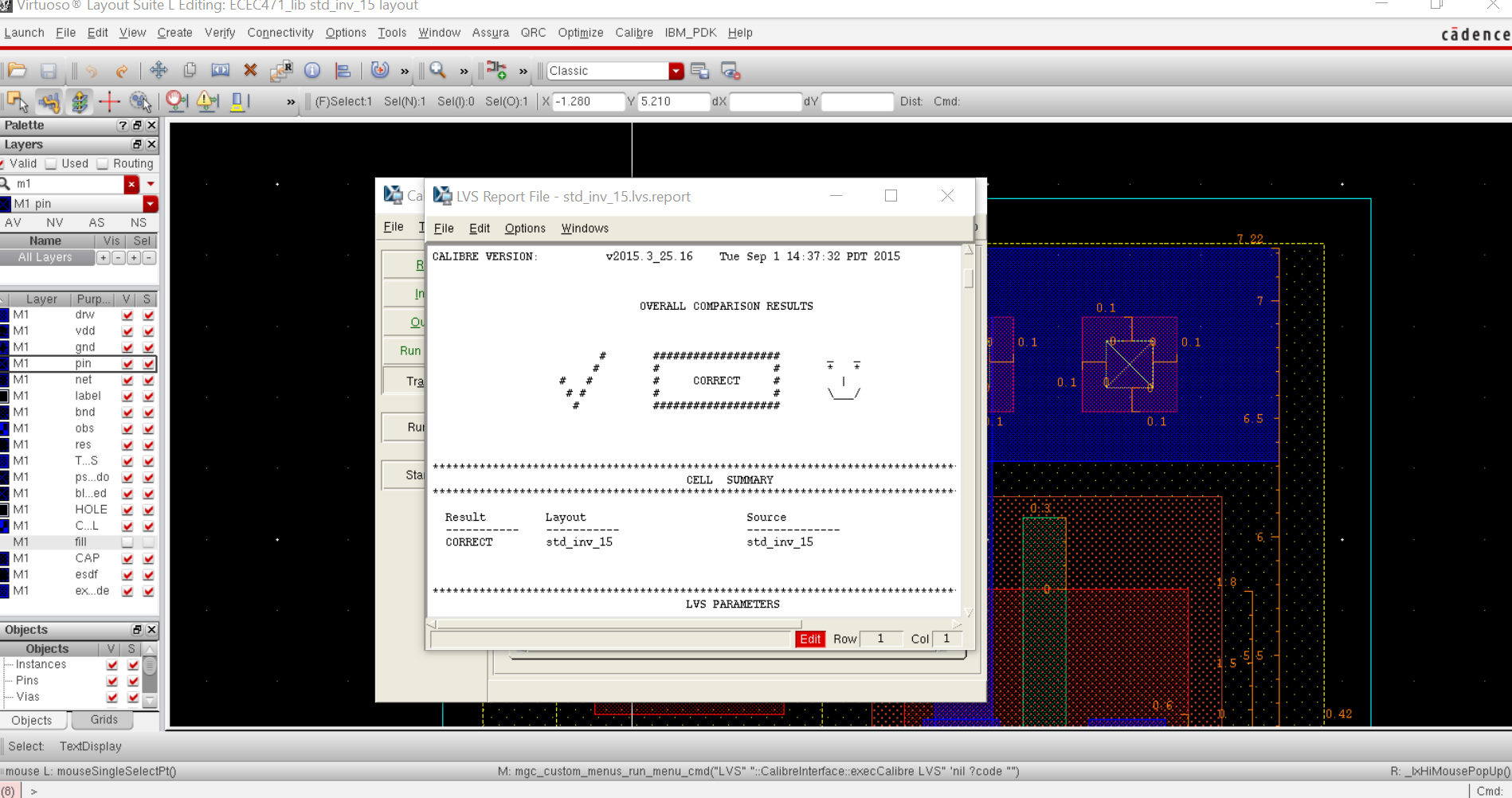
Design Rule Checking (DRC): Once the layout is completed, it is required to check the layout for possible design rule violations through Design Rule Checking (DRC). The DRC has been performed through Assura and no violations found in layout design. The DRC result is given in Figure 10.

Figure 10: DRC result showing no design rule violation

Layout versus Schematic Checking (LVS): Once the layout has passed DRC checking, the LVS checking has been performed to make sure that the physical layout exactly mimics the schematic in terms of connectivity. LVS checking has been successfully performed using Assura and the result (Figure 11) shows that the schematic and layout matches.

Figure 11: LVS result showing schematic and layout are matched



**Analysis of simulation results:**

Transistor sizing and symmetric behavior:

Propagation delay: During schematic design and simulation, propagation delay has been chosen as 0ns. But from the transient simulation propagation delay found as 1.199ns shown in Figure 12.

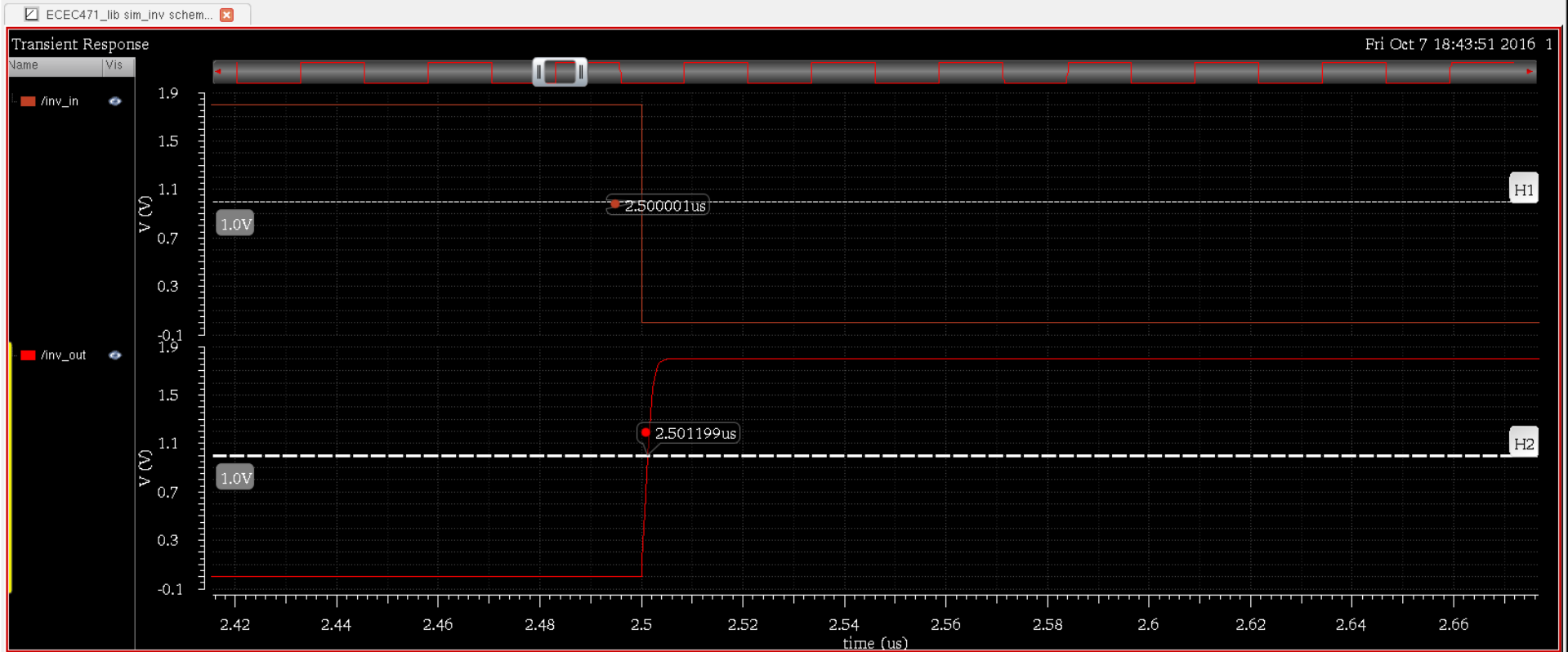


Figure 12: Propagation delay calculation from transient simulation

Here, a small amount of delay of 1.199ns has been observed although delay has been chosen 0ns. Meaning it takes 1.199ns to get the output out from the inverter after a given input has been applied. Even future in accuracy will depend on how well the simulations are running and how good the fabrication process will be.

Rise time and fall time: During schematic design and simulation, rise time and fall time have been defined as 1ps. In order to find the rise and fall time from the transient simulation, markers have been placed on the waveform as the following and recorded in the table below in Table 1.

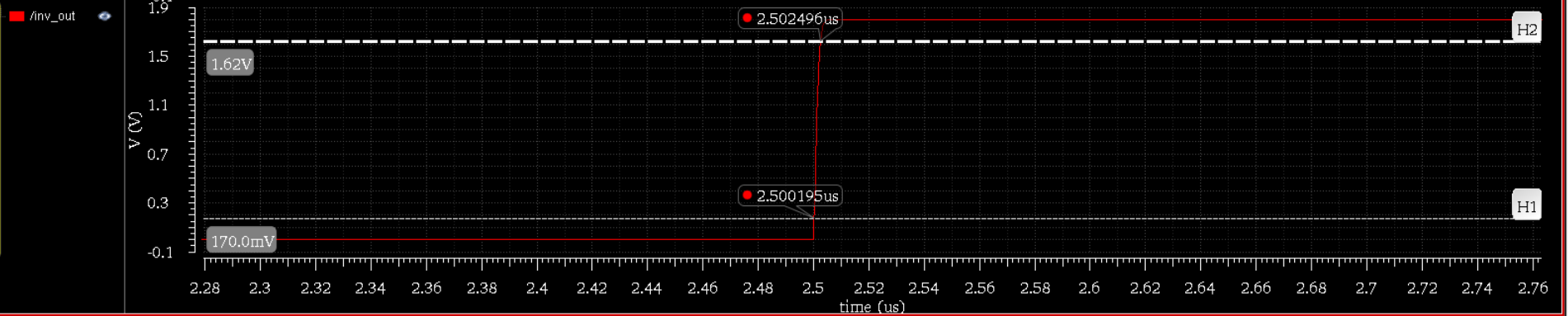


Figure 12: Rise time calculation from transient simulation

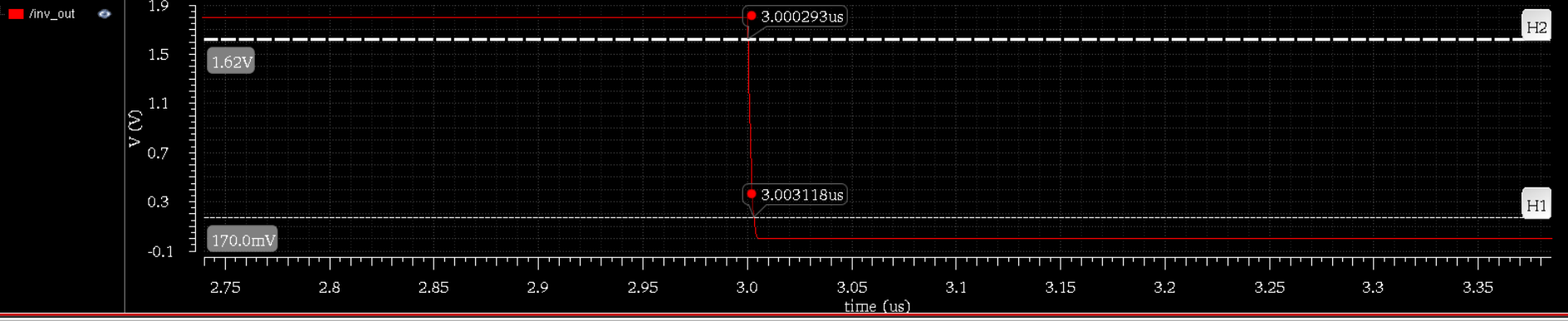


Figure 13: Fall time calculation from transient simulation

Table 1. output characteristics

|  |  |  |  |
| --- | --- | --- | --- |
| **Sim Type** | **tr** | **tf** | **tprop** |
| **Front End Sim** | 2.2995ns | 2.825ns | 1.199ns |

Some error will still persist due to error in marker placement and simulation or layout design.

**Conclusion:**

The CMOS inverter circuit and layout are designed in this laboratory. The symmetric behavior is obtained through parametric and DC analysis. The physical verification (DRC and LVS) process verifies the correctness of the layout vs. the schematic and rules given. The expected inverter behavior is observed from the transient simulation. In addition to that, rise time, fall time, and propagation delay are measured from the transient analysis, which characterizes the symmetric behavior and performance of the inverter.