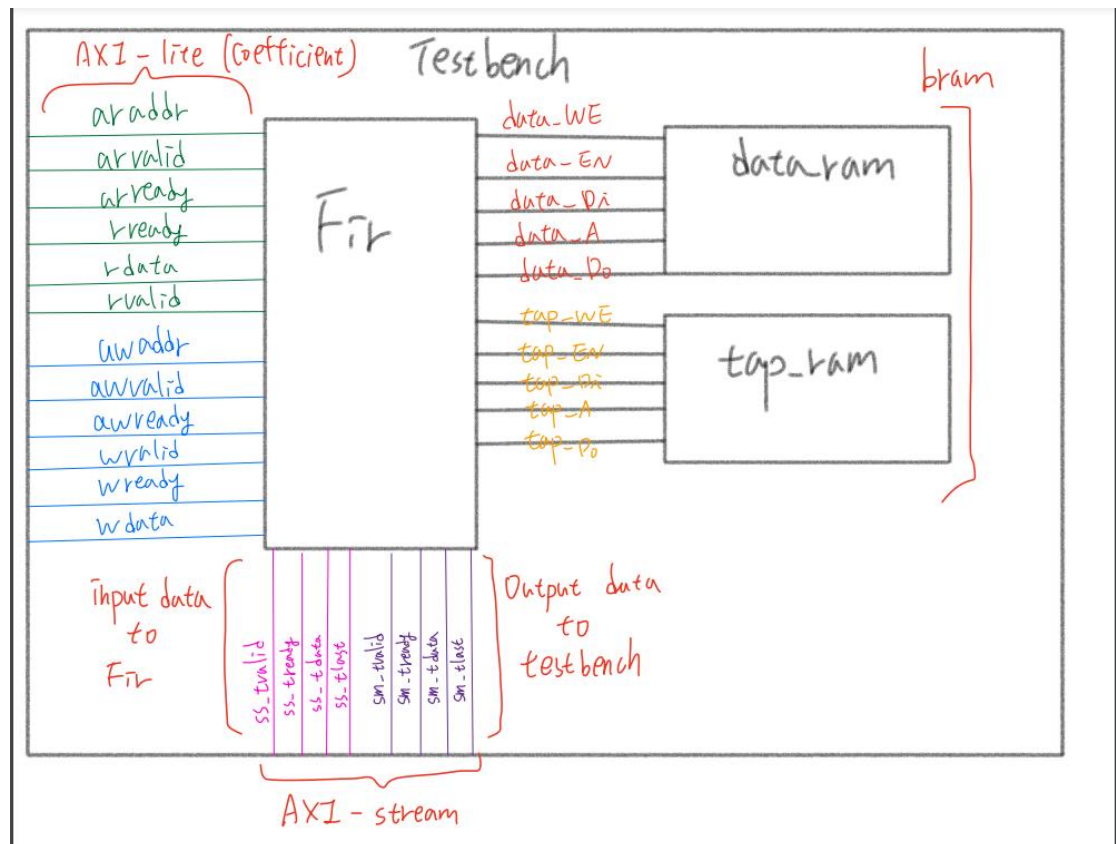- Block Diagram

- Describe operation

一開始先把 coefficient 透過 axi-lite 傳到 fir 再傳到 sram 存取，

axi-lite 的 protocol 主要有 5 個 channel，分別是 AW、AR、W、R

和 B，主要是用前面 4 個 channel，每個 channel 都有 valid ready

來做 handshake，再透過 SRAM 的 EN 和 WE 搭配上 tvalid 和

tready 去控制讀寫。Xn 的部分是透過 axi-stream 傳送 input data

送進 fir 運作，在 testbench 是由 task ss 來負責傳輸 input。在 fir

裡面用 fsm 控制整個系統的運作。最後計算出來的結果再透過

axi-stream 送到 testbench 由 task sm 來做驗證。

- Resource usage: including FF, LUT, BRAM

```
+-----------------------+------+-------+------------+-----------+-------+
|       Site Type       | Used | Fixed | Prohibited | Available | Util% |
+-----------------------+------+-------+------------+-----------+-------+
| Slice LUTs*           |   77 |     0 |          0 |     53200 |  0.14 |
|   LUT as Logic        |   77 |     0 |          0 |     53200 |  0.14 |
|   LUT as Memory       |    0 |     0 |          0 |     17400 |  0.00 |
| Slice Registers       |  247 |     0 |          0 |    106400 |  0.23 |
|   Register as Flip Flop |  247 |     0 |          0 |    106400 |  0.23 |
|   Register as Latch   |    0 |     0 |          0 |    106400 |  0.00 |
| F7 Muxes              |    0 |     0 |          0 |     26600 |  0.00 |
| F8 Muxes              |    0 |     0 |          0 |     13300 |  0.00 |
+-----------------------+------+-------+------------+-----------+-------+
```

```
2. Memory
---------

+----------------+------+-------+------------+-----------+-------+
|   Site Type    | Used | Fixed | Prohibited | Available | Util% |
+----------------+------+-------+------------+-----------+-------+
| Block RAM Tile |    0 |     0 |          0 |       140 |  0.00 |
|   RAMB36/FIFO* |    0 |     0 |          0 |       140 |  0.00 |
|   RAMB18       |    0 |     0 |          0 |       280 |  0.00 |
+----------------+------+-------+------------+-----------+-------+
```

- Timing Report

  - Slack

  - Timing Summary

  - Max delay path

- Simulation Waveform, show
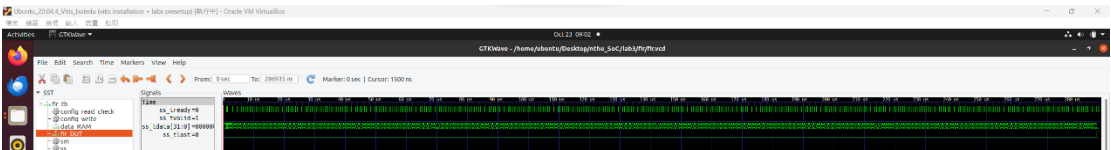 - Coefficient program

  - Coefficient read back
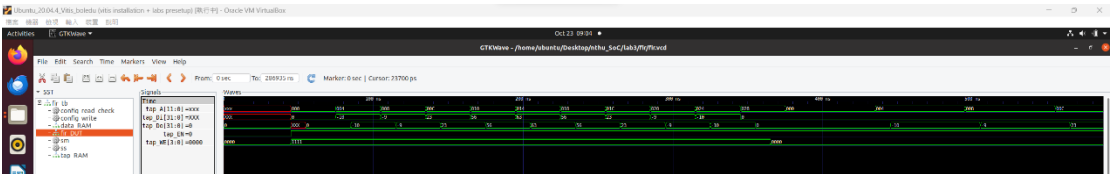

  - Data-in stream-in
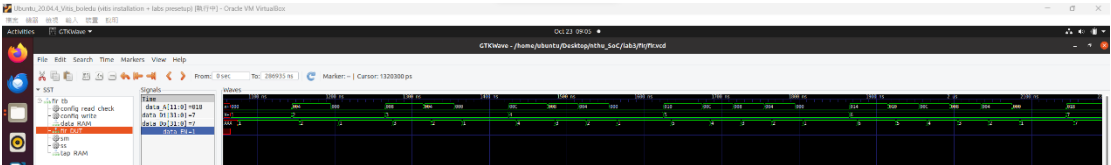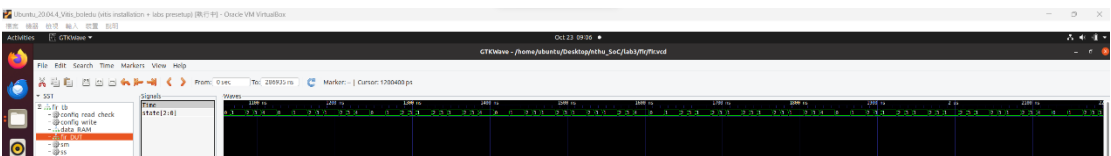

  - Data-out stream-out

  - Tap RAM access control

  - Data RAM access control

  - FSM

遲交原因：原本以為 10/25 以前繳交即可，所以沒有馬上寫

report 和整理檔案。