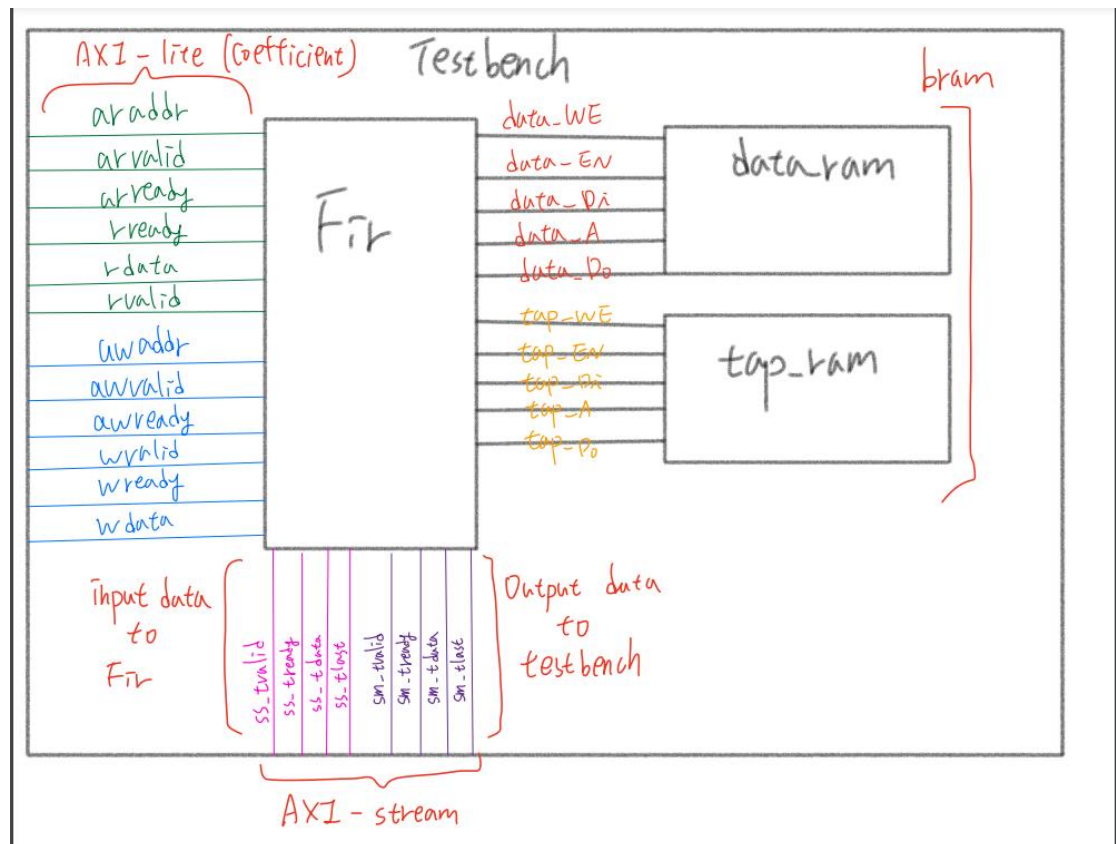


- Block Diagram



- Describe operation

一開始先把 coefficient 透過 axi-lite 傳到 fir 再傳到 sram 存取，

axi-lite 的 protocol 主要有 5 個 channel，分別是 AW、AR、W、R 和 B，主要是用前面 4 個 channel，每個 channel 都有 valid ready 來做 handshake，再透過 SRAM 的 EN 和 WE 搭配上 tvalid 和 tready 去控制讀寫。Xn 的部分是透過 axi-stream 傳送 input data 送進 fir 運作，在 testbench 是由 task ss 來負責傳輸 input。在 fir 裡面用 fsm 控制整個系統的運作。最後計算出來的結果再透過 axi-stream 送到 testbench 由 task sm 來做驗證。

- Resource usage: including FF, LUT, BRAM

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	77	0	0	53200	0.14
LUT as Logic	77	0	0	53200	0.14
LUT as Memory	0	0	0	17400	0.00
Slice Registers	247	0	0	106400	0.23
Register as Flip Flop	247	0	0	106400	0.23
Register as Latch	0	0	0	106400	0.00
F7 Muxes	0	0	0	26600	0.00
F8 Muxes	0	0	0	13300	0.00

## 2. Memory

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	140	0.00
RAMB36/FIFO*	0	0	0	140	0.00
RAMB18	0	0	0	280	0.00

- Timing Report

- Slack

Timing			
Design Timing Summary			
Setup		Hold	Pulse Width
Worst Negative Slack (WNS): 6.101 ns		Worst Hold Slack (WHS): 0.137 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns		Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0		Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 402		Total Number of Endpoints: 402	Total Number of Endpoints: 248
All user specified timing constraints are met.			

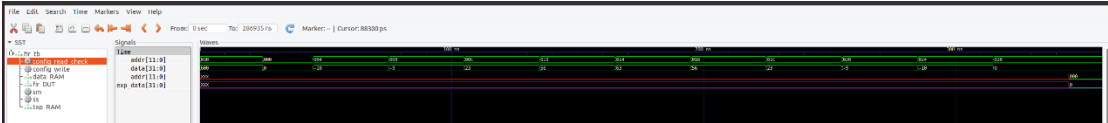
- Timing Summary

Design Timing Summary											
WNS(ns)	TNS(ns)	TNS Failing Endpoints	TNS Total Endpoints	WHS(ns)	THS(ns)	THS Failing Endpoints	THS Total Endpoints	WPWS(ns)	TPWS(ns)	TPWS Failing Endpoints	TPWS Total Endpoints
6.101	0.000	0	402	0.137	0.000	0	402	4.500	0.000	0	248
All user specified timing constraints are met.											
Clock Summary											
Clock	Waveform(ns)	Period(ns)	Frequency(MHz)								
axis_clk	(0.000 5.000)	10.000	100.000								

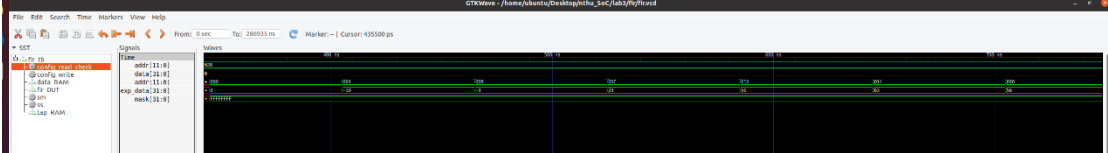
- Max delay path

Max Delay Paths	
Slack (MET) : 6.101ns (required time - arrival time)	
Source:	awready_reg/C
Destination:	tap_A_reg[0]_1/R
Path Group:	axis_clk
Path Type:	Setup (Max at Slow Process Corner)
Requirement:	10.000ns (axis_clk rise@10.000ns - axis_clk rise@0.000ns)
Data Path Delay:	3.162ns (logic 0.897ns (28.368%) route 2.265ns (71.632%))
Logic Levels:	2 (LUT5=1 LUT6=1)
Clock Path Skew:	-0.145ns (DCD - SCD + CPR)
Destination Clock Delay (DCD):	2.128ns = ( 12.128 - 10.000 )
Source Clock Delay (SCD):	2.456ns
Clock Pessimism Removal (CPR):	0.184ns
Clock Uncertainty:	0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
Total System Jitter (TSJ):	0.071ns
Total Input Jitter (TIJ):	0.000ns
Discrete Jitter (DJ):	0.000ns
Phase Error (PE):	0.000ns

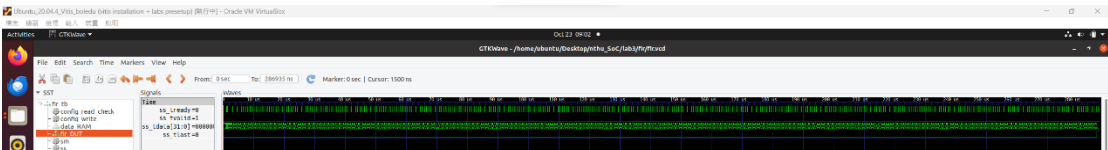
- Coefficient program



- Coefficient read back



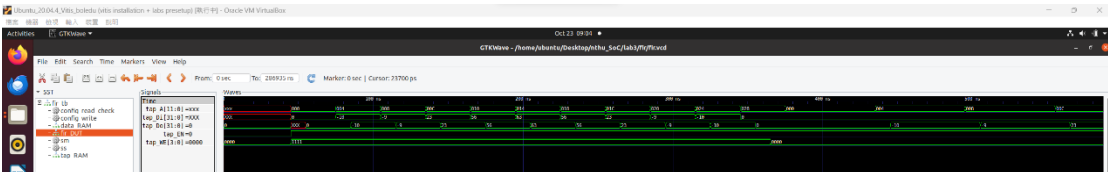
- Data-in stream-in



- Data-out stream-out



- Tap RAM access control



- Data RAM access control



■ FSM

