- Brief introduction about the overall system

  這個 lab 主要是介紹 interface 的部分，透過 GUI 設定 interface 或是用 directive 設定這兩種方法，interface 的部分有 MAXI 和 Stream，而 design 是實作 FIRN11 filter。

- What is observed & learned

  透過這個 lab 我學到關於 interface 設定的相關操作，跟前一個 lab 比，還多了一塊 FPGA 板可以使用，kv260 的 processor 需要做一些設定，還有在 stream interface 的時候有使用到 DMA 的 ip。

- Screen dump - MAXI

  - Performance

```
+ Performance & Resource Estimates:

    PS: '+' for module; 'o' for loop; '*' for dataflow
    +-----------------------------------+-----+-----+--------+--------+---------+--------+-----+----------+-----+---------+-----------+-----------+-----+
    |              Modules              | Issue|      | Latency | Latency| Iteration|        | Trip |          |     |         |           |           |     |
    |              & Loops              | Type | Slack| (cycles)|  (ns)  |  Latency | Interval| Count| Pipelined| BRAM |   DSP   |     FF    |    LUT    | URAM|
    +-----------------------------------+-----+-----+--------+--------+---------+--------+-----+----------+-----+---------+-----------+-----------+-----+
    |+ fir_n11_maxi                     |     -|  0.00|       -|       -|        -|       -|     -|        no|     -|  33 (2%)|  2117 (~0%)|  2681 (2%)|    -|
    | + fir_n11_maxi_Pipeline_XFER_LOOP |     -|  0.00|       -|       -|        -|       -|     -|        no|     -|  33 (2%)|   463 (~0%)|  756 (~0%)|    -|
    |  o XFER_LOOP                      |     -|  7.30|       -|       -|        4|       1|     -|       yes|     -|        -|           -|          -|    -|
    +-----------------------------------+-----+-----+--------+--------+---------+--------+-----+----------+-----+---------+-----------+-----------+-----+
```

  - Utilization

```
================================================================
== Utilization Estimates
================================================================
* Summary:
+-----------------+---------+------+--------+--------+-----+
|       Name      | BRAM_18K|  DSP |    FF  |   LUT  | URAM|
+-----------------+---------+------+--------+--------+-----+
|DSP              |        -|     -|       -|       -|    -|
|Expression       |        -|     -|       0|      40|    -|
|FIFO             |        -|     -|       -|       -|    -|
|Instance         |        0|    33|    1467|    2466|    0|
|Memory           |        -|     -|       -|       -|    -|
|Multiplexer      |        -|     -|       -|     175|    -|
|Register         |        -|     -|     650|       -|    -|
+-----------------+---------+------+--------+--------+-----+
|Total            |        0|    33|    2117|    2681|    0|
+-----------------+---------+------+--------+--------+-----+
|Available        |      288|  1248|  234240|  117120|   64|
+-----------------+---------+------+--------+--------+-----+
|Utilization (%)  |        0|     2|      ~0|       2|    0|
+-----------------+---------+------+--------+--------+-----+
```

· Detail:
  * Instance:

Instance	Module	BRAM_18K	DSP	FF	LUT	URAM
control_s_axi_U	control_s_axi	0	0	294	436	0
grp_fir_n11_maxi_Pipeline_XFER_LOOP_fu_242	fir_n11_maxi_Pipeline_XFER_LOOP	0	33	463	756	0
gmem_m_axi_U	gmem_m_axi	0	0	710	1274	0
Total		0	33	1467	2466	0

  * Expression:

Variable Name	Operation	DSP	FF	LUT	Bitwidth P0	Bitwidth P1
add_ln16_fu_289_p2	+	0	0	40	33	2
Total		0	0	40	33	2

  * Multiplexer:

Name	LUT	Input Size	Bits	Total Bits
an32Coef_address0	65	12	4	48
ap_NS_fsm	65	15	1	15
gmem_ARVALID	9	2	1	2
gmem_AWVALID	9	2	1	2
gmem_BREADY	9	2	1	2
gmem_RREADY	9	2	1	2
gmem_WVALID	9	2	1	2
Total	175	37	10	73

  * Register:

Name	FF	LUT	Bits	Const Bits
an32Coef_load_10_reg_446	32	0	32	0
an32Coef_load_1_reg_340	32	0	32	0
an32Coef_load_2_reg_350	32	0	32	0
an32Coef_load_3_reg_360	32	0	32	0
an32Coef_load_4_reg_370	32	0	32	0
an32Coef_load_5_reg_380	32	0	32	0
an32Coef_load_6_reg_390	32	0	32	0
an32Coef_load_7_reg_400	32	0	32	0
an32Coef_load_8_reg_410	32	0	32	0
an32Coef_load_9_reg_420	32	0	32	0
an32Coef_load_reg_330	32	0	32	0
ap_CS_fsm	14	0	14	0
grp_fir_n11_maxi_Pipeline_XFER_LOOP_fu_242_ap_start_reg	1	0	1	0
lshr_ln16_cast_reg_440	31	0	31	0
pn32HPInput_read_reg_435	64	0	64	0
pn32HPOutput_read_reg_430	64	0	64	0
trunc_ln18_1_reg_451	62	0	62	0
trunc_ln30_1_reg_456	62	0	62	0
Total	650	0	650	0

- Interface

```
44 ================================================================
45 == Interface
46 ================================================================
47 * Summary:
48 +-----------------------+-----+-----+------------+-------------+-------------+
49 |       RTL Ports       | Dir | Bits|  Protocol  | Source Object|    C Type    |
50 +-----------------------+-----+-----+------------+-------------+-------------+
51 |s_axi_control_AWVALID  |   in|    1|       s_axi|       control|         array|
52 |s_axi_control_AWREADY  |  out|    1|       s_axi|       control|         array|
53 |s_axi_control_AWADDR   |   in|    7|       s_axi|       control|         array|
54 |s_axi_control_WVALID   |   in|    1|       s_axi|       control|         array|
55 |s_axi_control_WREADY   |  out|    1|       s_axi|       control|         array|
56 |s_axi_control_WDATA    |   in|   32|       s_axi|       control|         array|
57 |s_axi_control_WSTRB    |   in|    4|       s_axi|       control|         array|
58 |s_axi_control_ARVALID  |   in|    1|       s_axi|       control|         array|
59 |s_axi_control_ARREADY  |  out|    1|       s_axi|       control|         array|
60 |s_axi_control_ARADDR   |   in|    7|       s_axi|       control|         array|
61 |s_axi_control_RVALID   |  out|    1|       s_axi|       control|         array|
62 |s_axi_control_RREADY   |   in|    1|       s_axi|       control|         array|
63 |s_axi_control_RDATA    |  out|   32|       s_axi|       control|         array|
64 |s_axi_control_RRESP    |  out|    2|       s_axi|       control|         array|
65 |s_axi_control_BVALID   |  out|    1|       s_axi|       control|         array|
66 |s_axi_control_BREADY   |   in|    1|       s_axi|       control|         array|
67 |s_axi_control_BRESP    |  out|    2|       s_axi|       control|         array|
68 |ap_clk                 |   in|    1|  ap_ctrl_hs|  fir_n11_maxi|  return value|
69 |ap_rst_n               |   in|    1|  ap_ctrl_hs|  fir_n11_maxi|  return value|
70 |interrupt              |  out|    1|  ap_ctrl_hs|  fir_n11_maxi|  return value|
```

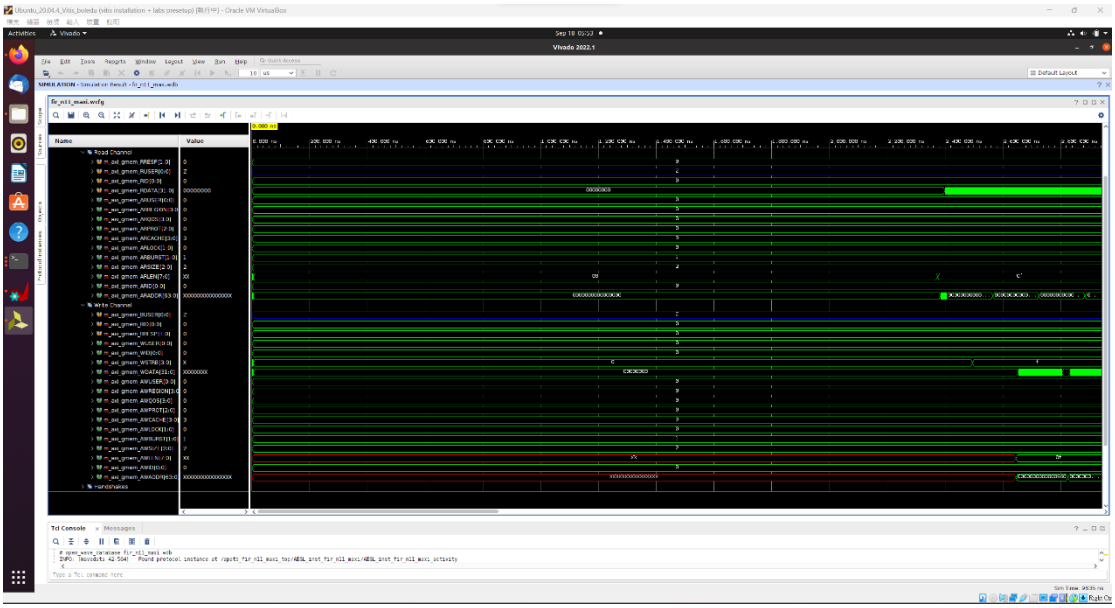
```
171 |m_axi_gmem_AWVALID     |  out|    1|       m_axi|          gmem|       pointer|
172 |m_axi_gmem_AWREADY     |   in|    1|       m_axi|          gmem|       pointer|
173 |m_axi_gmem_AWADDR      |  out|   64|       m_axi|          gmem|       pointer|
174 |m_axi_gmem_AWID        |  out|    1|       m_axi|          gmem|       pointer|
175 |m_axi_gmem_AWLEN       |  out|    8|       m_axi|          gmem|       pointer|
176 |m_axi_gmem_AWSIZE      |  out|    3|       m_axi|          gmem|       pointer|
177 |m_axi_gmem_AWBURST     |  out|    2|       m_axi|          gmem|       pointer|
178 |m_axi_gmem_AWLOCK      |  out|    2|       m_axi|          gmem|       pointer|
179 |m_axi_gmem_AWCACHE     |  out|    4|       m_axi|          gmem|       pointer|
180 |m_axi_gmem_AWPROT      |  out|    3|       m_axi|          gmem|       pointer|
181 |m_axi_gmem_AWQOS       |  out|    4|       m_axi|          gmem|       pointer|
182 |m_axi_gmem_AWREGION    |  out|    4|       m_axi|          gmem|       pointer|
183 |m_axi_gmem_AWUSER      |  out|    1|       m_axi|          gmem|       pointer|
184 |m_axi_gmem_WVALID      |  out|    1|       m_axi|          gmem|       pointer|
185 |m_axi_gmem_WREADY      |   in|    1|       m_axi|          gmem|       pointer|
186 |m_axi_gmem_WDATA       |  out|   32|       m_axi|          gmem|       pointer|
187 |m_axi_gmem_WSTRB       |  out|    4|       m_axi|          gmem|       pointer|
188 |m_axi_gmem_WLAST       |  out|    1|       m_axi|          gmem|       pointer|
189 |m_axi_gmem_WID         |  out|    1|       m_axi|          gmem|       pointer|
190 |m_axi_gmem_WUSER       |  out|    1|       m_axi|          gmem|       pointer|
191 |m_axi_gmem_ARVALID     |  out|    1|       m_axi|          gmem|       pointer|
192 |m_axi_gmem_ARREADY     |   in|    1|       m_axi|          gmem|       pointer|
193 |m_axi_gmem_ARADDR      |  out|   64|       m_axi|          gmem|       pointer|
194 |m_axi_gmem_ARID        |  out|    1|       m_axi|          gmem|       pointer|
195 |m_axi_gmem_ARLEN       |  out|    8|       m_axi|          gmem|       pointer|
196 |m_axi_gmem_ARSIZE      |  out|    3|       m_axi|          gmem|       pointer|
197 |m_axi_gmem_ARBURST     |  out|    2|       m_axi|          gmem|       pointer|
198 |m_axi_gmem_ARLOCK      |  out|    2|       m_axi|          gmem|       pointer|
199 |m_axi_gmem_ARCACHE     |  out|    4|       m_axi|          gmem|       pointer|
200 |m_axi_gmem_ARPROT      |  out|    3|       m_axi|          gmem|       pointer|
201 |m_axi_gmem_ARQOS       |  out|    4|       m_axi|          gmem|       pointer|
202 |m_axi_gmem_ARREGION    |  out|    4|       m_axi|          gmem|       pointer|
203 |m_axi_gmem_ARUSER      |  out|    1|       m_axi|          gmem|       pointer|
204 |m_axi_gmem_RVALID      |   in|    1|       m_axi|          gmem|       pointer|
205 |m_axi_gmem_RREADY      |  out|    1|       m_axi|          gmem|       pointer|
206 |m_axi_gmem_RDATA       |   in|   32|       m_axi|          gmem|       pointer|
207 |m_axi_gmem_RLAST       |   in|    1|       m_axi|          gmem|       pointer|
208 |m_axi_gmem_RID         |   in|    1|       m_axi|          gmem|       pointer|
209 |m_axi_gmem_RUSER       |   in|    1|       m_axi|          gmem|       pointer|
210 |m_axi_gmem_RRESP       |   in|    2|       m_axi|          gmem|       pointer|
211 |m_axi_gmem_BVALID      |   in|    1|       m_axi|          gmem|       pointer|
212 |m_axi_gmem_BREADY      |  out|    1|       m_axi|          gmem|       pointer|
213 |m_axi_gmem_BRESP       |   in|    2|       m_axi|          gmem|       pointer|
214 |m_axi_gmem_BID         |   in|    1|       m_axi|          gmem|       pointer|
215 |m_axi_gmem_BUSER       |   in|    1|       m_axi|          gmem|       pointer|
216 +-----------------------+-----+-----+------------+--------------+--------------+
```

- Co-simulation transcript/waveform

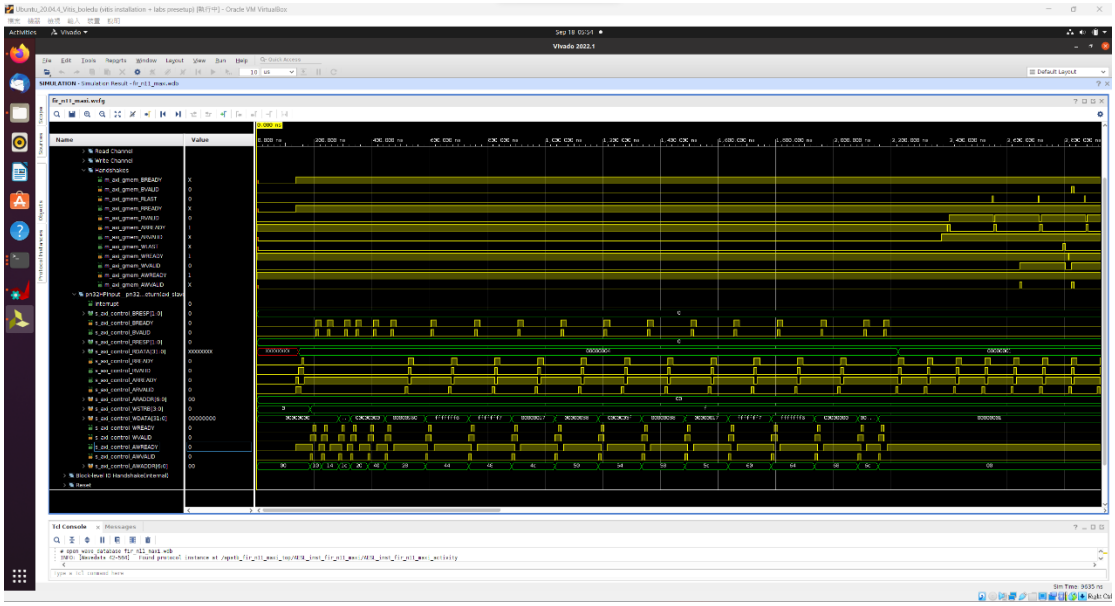
Transcript :

```
1 INFO: [SIM 2] *************** CSIM start ***************
2 INFO: [SIM 4] CSIM will launch GCC as the compiler.
3 make: 'csim.exe' is up to date.
4 >> Start test!
5 >> Comparing against output data...
6 >> Test passed!
7 ------------------------
8 INFO: [SIM 1] CSim done with 0 errors.
9 INFO: [SIM 3] *************** CSIM finish ***************
```

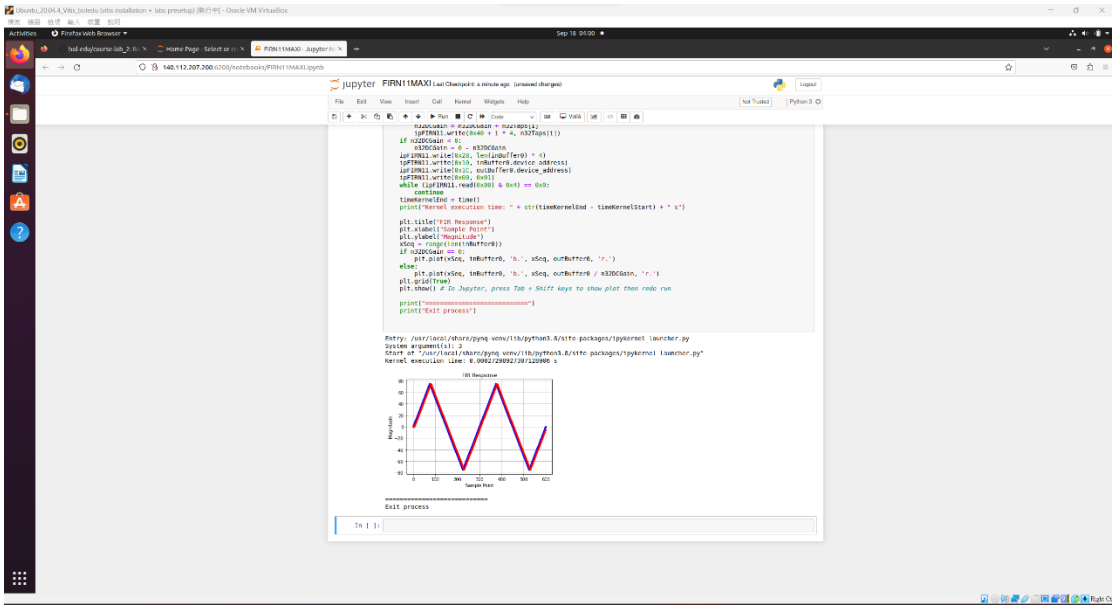
Read/write channel:



Handshake and slave signal :



- Jupyter Notebook execution results



- Screen dump -Stream
  - Performance

```
15 + Performance & Resource Estimates:
16
17    PS: '+' for module; 'o' for loop; '*' for dataflow
18    +-----------------------------------+-----+-----+---------+---------+----------+---------+------+----------+------+---------+----------+-----------+-----+
19    |              Modules              | Issue|      | Latency | Latency| Iteration|         | Trip |          |      |         |          |           |     |
20    |              & Loops              | Type | Slack| (cycles)|  (ns)  |  Latency | Interval| Count| Pipelined| BRAM |   DSP   |    FF    |    LUT    | URAM|
21    +-----------------------------------+-----+-----+---------+---------+----------+---------+------+----------+------+---------+----------+-----------+-----+
22    |+ fir_n11_strm                     |     -|  1.01|        -|        -|         -|        -|     -|        no|     -|  33 (2%)|  952 (~0%)|  1082 (~0%)|    -|
23    | + fir_n11_strm_Pipeline_XFER_LOOP |     -|  1.01|        -|        -|         -|        -|     -|        no|     -|  33 (2%)|  762 (~0%)|   825 (~0%)|    -|
24    |  o XFER_LOOP                      |    II|  7.30|        -|        -|        12|       11|     -|       yes|     -|        -|         -|           -|    -|
25    +-----------------------------------+-----+-----+---------+---------+----------+---------+------+----------+------+---------+----------+-----------+-----+
26
```

  - Utilization

```
49 ================================================================
50 == Utilization Estimates
51 ================================================================
52 * Summary:
53 +-----------------+---------+------+--------+--------+-----+
54 |       Name      | BRAM_18K|  DSP |    FF  |   LUT  | URAM|
55 +-----------------+---------+------+--------+--------+-----+
56 |DSP              |        -|     -|       -|       -|    -|
57 |Expression       |        -|     -|       0|      42|    -|
58 |FIFO             |        -|     -|       -|       -|    -|
59 |Instance         |        0|    33|     916|    1005|    0|
60 |Memory           |        -|     -|       -|       -|    -|
61 |Multiplexer      |        -|     -|       -|      35|    -|
62 |Register         |        -|     -|      36|       -|    -|
63 +-----------------+---------+------+--------+--------+-----+
64 |Total            |        0|    33|     952|    1082|    0|
65 +-----------------+---------+------+--------+--------+-----+
66 |Available        |      288|  1248|  234240|  117120|   64|
67 +-----------------+---------+------+--------+--------+-----+
68 |Utilization (%)  |        0|     2|      ~0|      ~0|    0|
69 +-----------------+---------+------+--------+--------+-----+
70
```

* Expression:

Variable Name	Operation	DSP	FF	LUT	Bitwidth P0	Bitwidth P1
ret_V_fu_171_p2	+	0	0	40	33	2
grp_fir_n11_strm_Pipeline_XFER_LOOP_fu_112_pstrmOutput_TREADY	and	0	0	2	1	1
Total		0	0	42	34	3

* Multiplexer:

Name	LUT	Input Size	Bits	Total Bits
ap_NS_fsm	26	5	1	5
pstrmInput_TREADY_int_regslice	9	2	1	2
Total	35	7	2	7

* Register:

Name	FF	LUT	Bits	Const Bits
ap_CS_fsm	4	0	4	0
grp_fir_n11_strm_Pipeline_XFER_LOOP_fu_112_ap_start_reg	1	0	1	0
tmp_reg_187	31	0	31	0
Total	36	0	36	0

■ Interface

```
================================================================
== Interface
================================================================
* Summary:
+------------------------+-----+-----+------------+----------------------+--------------+
|       RTL Ports        | Dir | Bits|  Protocol  |     Source Object    |    C Type    |
+------------------------+-----+-----+------------+----------------------+--------------+
|s_axi_control_AWVALID   |   in|    1|       s_axi|               control|         array|
|s_axi_control_AWREADY   |  out|    1|       s_axi|               control|         array|
|s_axi_control_AWADDR    |   in|    7|       s_axi|               control|         array|
|s_axi_control_WVALID    |   in|    1|       s_axi|               control|         array|
|s_axi_control_WREADY    |  out|    1|       s_axi|               control|         array|
|s_axi_control_WDATA     |   in|   32|       s_axi|               control|         array|
|s_axi_control_WSTRB     |   in|    4|       s_axi|               control|         array|
|s_axi_control_ARVALID   |   in|    1|       s_axi|               control|         array|
|s_axi_control_ARREADY   |  out|    1|       s_axi|               control|         array|
|s_axi_control_ARADDR    |   in|    7|       s_axi|               control|         array|
|s_axi_control_RVALID    |  out|    1|       s_axi|               control|         array|
|s_axi_control_RREADY    |   in|    1|       s_axi|               control|         array|
|s_axi_control_RDATA     |  out|   32|       s_axi|               control|         array|
|s_axi_control_RRESP     |  out|    2|       s_axi|               control|         array|
|s_axi_control_BVALID    |  out|    1|       s_axi|               control|         array|
|s_axi_control_BREADY    |   in|    1|       s_axi|               control|         array|
|s_axi_control_BRESP     |  out|    2|       s_axi|               control|         array|
|ap_clk                  |   in|    1|  ap_ctrl_hs|          fir_n11_strm|  return value|
|ap_rst_n                |   in|    1|  ap_ctrl_hs|          fir_n11_strm|  return value|
|interrupt               |  out|    1|  ap_ctrl_hs|          fir_n11_strm|  return value|
|pstrmInput_TDATA        |   in|   32|        axis|   pstrmInput_V_data_V|       pointer|
|pstrmInput_TVALID       |   in|    1|        axis|   pstrmInput_V_dest_V|       pointer|
|pstrmInput_TREADY       |  out|    1|        axis|   pstrmInput_V_dest_V|       pointer|
|pstrmInput_TDEST        |   in|    1|        axis|   pstrmInput_V_dest_V|       pointer|
|pstrmInput_TKEEP        |   in|    4|        axis|   pstrmInput_V_keep_V|       pointer|
|pstrmInput_TSTRB        |   in|    4|        axis|   pstrmInput_V_strb_V|       pointer|
|pstrmInput_TUSER        |   in|    1|        axis|   pstrmInput_V_user_V|       pointer|
|pstrmInput_TLAST        |   in|    1|        axis|   pstrmInput_V_last_V|       pointer|
|pstrmInput_TID          |   in|    1|        axis|     pstrmInput_V_id_V|       pointer|
|pstrmOutput_TDATA       |  out|   32|        axis|  pstrmOutput_V_data_V|       pointer|
|pstrmOutput_TVALID      |  out|    1|        axis|  pstrmOutput_V_dest_V|       pointer|
|pstrmOutput_TREADY      |   in|    1|        axis|  pstrmOutput_V_dest_V|       pointer|
|pstrmOutput_TDEST       |  out|    1|        axis|  pstrmOutput_V_dest_V|       pointer|
|pstrmOutput_TKEEP       |  out|    4|        axis|  pstrmOutput_V_keep_V|       pointer|
|pstrmOutput_TSTRB       |  out|    4|        axis|  pstrmOutput_V_strb_V|       pointer|
|pstrmOutput_TUSER       |  out|    1|        axis|  pstrmOutput_V_user_V|       pointer|
|pstrmOutput_TLAST       |  out|    1|        axis|  pstrmOutput_V_last_V|       pointer|
```

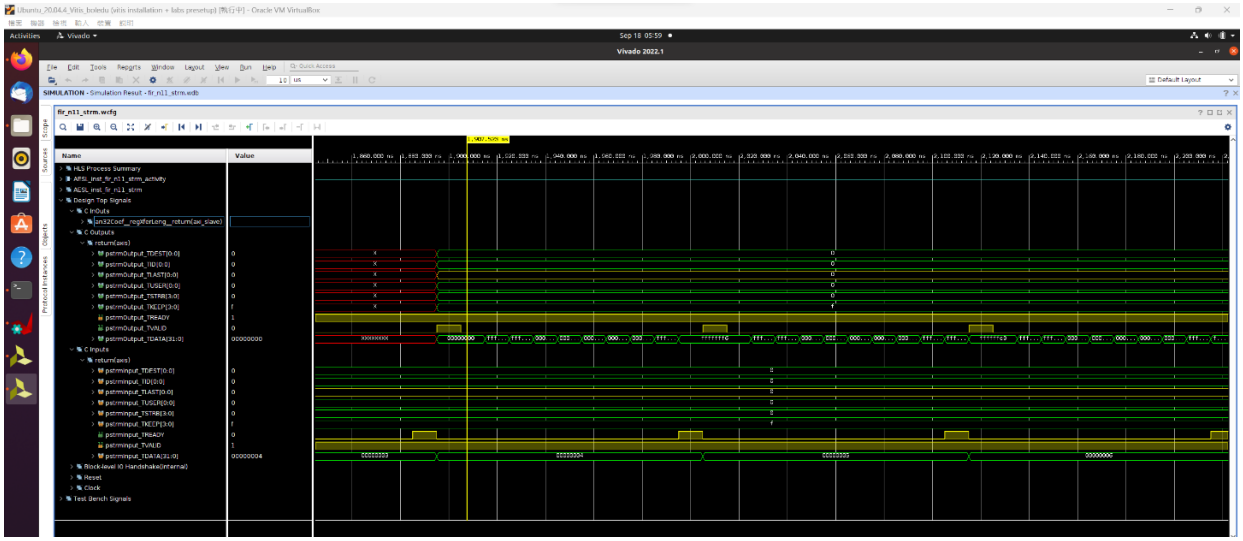
- Co-simulation transcript/waveform

transcript :

```
INFO: [SIM 2] *************** CSIM start ***************
INFO: [SIM 4] CSIM will launch GCC as the compiler.
   Compiling ../../../../hls_FIRN11Stream/FIRTester.cpp in debug mode
   Compiling ../../../../hls_FIRN11Stream/FIR.cpp in debug mode
   Generating csim.exe
>> Start test!
>> Comparing against output data...
>> Test passed!
------------------------
INFO: [SIM 1] CSim done with 0 errors.
INFO: [SIM 3] *************** CSIM finish ***************
```

C InOut :

C Input , C Output :



- Jupyter Notebook execution results