Chamarthi Phanikumar **10307044**
Electrical Engineering **M.Tech.+Ph.D.**
Indian Institute of Technology Bombay **Male**
Specialization: Power Electronics and Power Systems **DOB: 05-06-1987**

Examination	University	Institute	Year	CPI / %
Doctorate	IIT Bombay	IIT Bombay	2018	8.51
Postgraduate Specialization: Electrical Engineering				
Post Graduation	IIT Bombay	IIT Bombay	2011	8.13
Graduation	Acharya Nagarjuna	Bapatla Engineering College	2008	66.27
Intermediate/+2	Board of Intermediate Education,AP	PBPR Junior College	2004	91.40
Matriculation	Board of Secondary Education, AP	Govt. High school, Charla	2002	73.33

AREAS OF INTEREST

- High efficient Multilevel inverter topologies for medium voltage and high power applications.
- Optimized Space vector pulse width modulation techniques for Multilevel inverters.
- Transformerless Multilevel inverter topologies for grid connected solar PV applications.

DOCTORAL RESEARCH

Analysis and Control of Novel Multilevel Inverter Topologies for Grid Connected Solar PV Application
Supervisor - Prof. Vivek Agarwal, IIT Bombay**.**

- **A Dual Input Nine Level Inverter(DINLI) for 1-ϕ Grid-Connected Applications**
  - The proposed DINLI topology uses a total of seven power switches out of which three switches operate at high frequency and remaining are at low frequency.
  - The DINLI consists of reduced number of power components, lower switching and conduction losses which increase the reliability, reduces the cost and improves the overall efficiency (η≈97%).
  - Due to modularity in structure, the DINLI can be easily extended to *n*-level, 3-ϕ application
- **A New Self-Balancing 7-Level Inverter (SB7LI) with Coupled Inductors for 1-ϕ Grid Connected Solar PV Systems**
  - The SB7LI uses total eight power switches to generate seven output voltage levels and feeds high-quality power into the grid.
  - It can boost the input voltage to 1.5 times and doesn't require extra voltage balancing circuits.
  - The output filter requirements are reduced due to the presence of coupled inductors.
- **A Hybrid 9-level Inverter (H9LI) with Minimum Number of Switches for 1-ϕ Grid connected PV System with Innovative Voltage Balancing Techniques for Auxiliary Capacitor**
  - This H9LI topology requires lesser number of power switches (Ten switches per phase).
  - The voltage across the auxiliary capacitor can be balanced without any physical current sensing, unlike conventional voltage balancing techniques.
  - The H9LI offers good loss distribution among power switches and incurs zero leakage current, making it highly suitable for grid tied solar PV applications.
- **Simplified Implementation Scheme for Space Vector Pulse Width Modulation of *n*-level Inverter with On-line Computation of Optimal Switching Pulse Durations**
  - The *l-factor* approach based space vector implementation scheme is proposed to obtain generalized optimal switching pulse expressions.
  - The generalized switching pulses enable the online computation so that extensive storage of lookup table of switching states is eliminated.
  - Dynamic performance is highly improved due to an online implementation of the control.
  - Proposed modulation scheme can be implemented even on a low-cost microcontroller with limited resources, saving development and implementation costs.
- **Space Vector Control of *n*-level Dual Input Nine Level Inverter with Reduced Computation and Memory Requirements**
  - The proposed space vector scheme uses less number of equations to identify the sub-triangle which reduces the computational burden.

- It doesn't need any pre stored lookup tables for computing the on-times and for generation of the switching states. Therefore memory requirement in the DSP is very less.
- Since the requirement of look up tables of the switching states are not required the proposed scheme can be easily used for higher levels (even or odd).

Publications

- Phanikumar.Ch, Pawan. Ch and Agarwal.V, "Simplified implementation scheme for space vector pulse width modulation of the *n*-level inverter with the online computation of optimal switching pulse durations", *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 6695–6704, Nov. 2016.
- Phanikumar.Ch and Agarwal.V, "A dual input nine level inverter for 1-ϕ grid connected applications", *IEEE Trans. Ind. Electron.* , under review.
- Phanikumar. Ch and Agarwal. V, "An asymmetrical multilevel inverter with minimum number of switches for 1-ϕ grid-connected applications", *3rd Annual Southern Hemisphere Power Electronics Conference (SPEC 2017)*, under review.
- Roy.J, Phanikumar.Ch and Agarwal.V, "A hybrid 9-level inverter with a minimum number of switches for single phase grid connected solar PV system", *43rd IEEE Photovoltaic Specialist Conference (PVSC)*, 8-13 Jun. 2016, USA.
- Phanikumar. Ch and Agarwal. V,"A new couple inductor based 9-level inverter with reduced number of switches for standalone/grid connected solar PV systems", *40thIEEE PhotovoltaicSpecialistConference (PVSC)*, pp. 3094-3099, 8-13 Jun. 2014, USA.
- Phanikumar.Ch and Agarwal.V, "A nine-level inverter based grid connected solar PV system with voltage boosting", *IEEE Conference on Power Electronics, Drives and Energy Systems(PEDES)*, pp. 1-6, 16-10 Dec. 2014, India.
- Phanikumar.Ch and Agarwal.V, "Novel self-balancing single phase 7 level inverter with two coupled inductors", *IEEE Student's Technology Symposium*, pp. 313-318, 28th Feb-2nd Mar. 2014, India.
- Phanikumar.Ch, Nataraj.P and Agarwal.V, "Novel 1-ϕ multilevel current source inverter for balanced/unbalanced PV sources", *40thIEEE PhotovoltaicSpecialist Conference (PVSC)*, pp. 3090-3093, 8-13 Jun. 2014, USA.
- Phanikumar. Ch and Agarwal. V," Novel self-balancing single phase asymmetric 9 level grid connected inverter for photovoltaic applications", *Annual IEEE India Conference(INDICON)on Impact of engineering on global sustainability*, pp. 1-7, 13-15 Dec. 2013, India.
- Phanikumar.Ch and Agarwal.V, "Single phase 9-level grid connected inverter for photovoltaic applications", *4th IEEE Conference on Power Electronics for Distributed Generation Systems*, pp. 1-8, 8-11 Jul. 2013, USA.

SKILL SET

- Simulation Tools: MATLAB/Simulink, PSpice, SEQUEL
- PCB Designing Tools: KICAD
- Microcontrollers: TMS320F28069, TMS320F28335 and DSpace

RELEVANT COURSE WORK

- Power Electronics-I and Power Electronics-II
- Application of Power Electronics to Power Systems
- Circuit Simulation in Power Electronics
- Electric Drives
- Power Electronics and Power System Lab
- Restructured Power Systems
- Computer Aided Power System Analysis.

ACHIEVEMENTS AND OTHER ACTIVITIES

- Secured All India Rank **225** with **99.57** percentile among 52,246 candidates in Electrical Engineering GATE-2010.
- Volunteer in the conference **IEEE-PEDES-2014** held at IIT Bombay.
- Volunteer in the conference **NPEC-2015** held at IIT Bombay.