

Nexys 2 board tutorial

(Decoder, ISE 12.2)

Jim Duckworth, August 2010, WPI.

Digilent Adept Programming Steps added by Zoe (Zhu Fu)

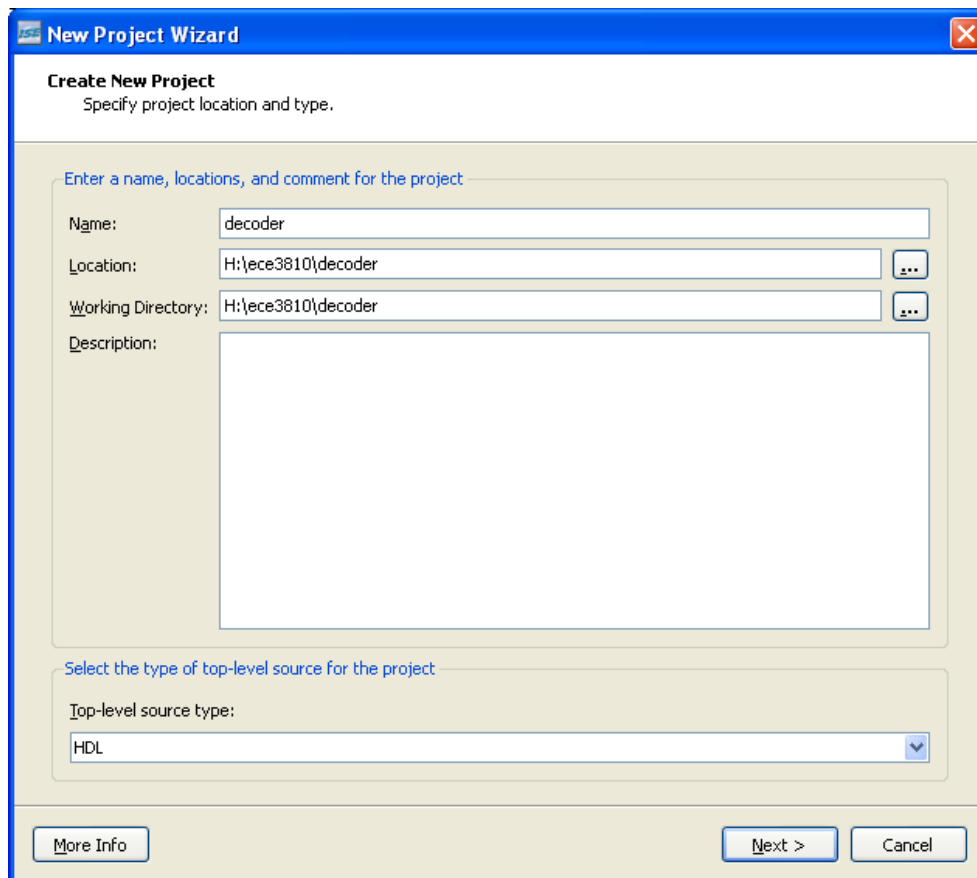
Note: you will need the Xilinx ISE Webpack installed on your computer (or you can use the department systems).

[Note you can also review Xilinx Tutorials, for example, under Design Resources: ISE Design Suite Tutorials, and ISE Design Suite Logic Edition - Quick Tour]

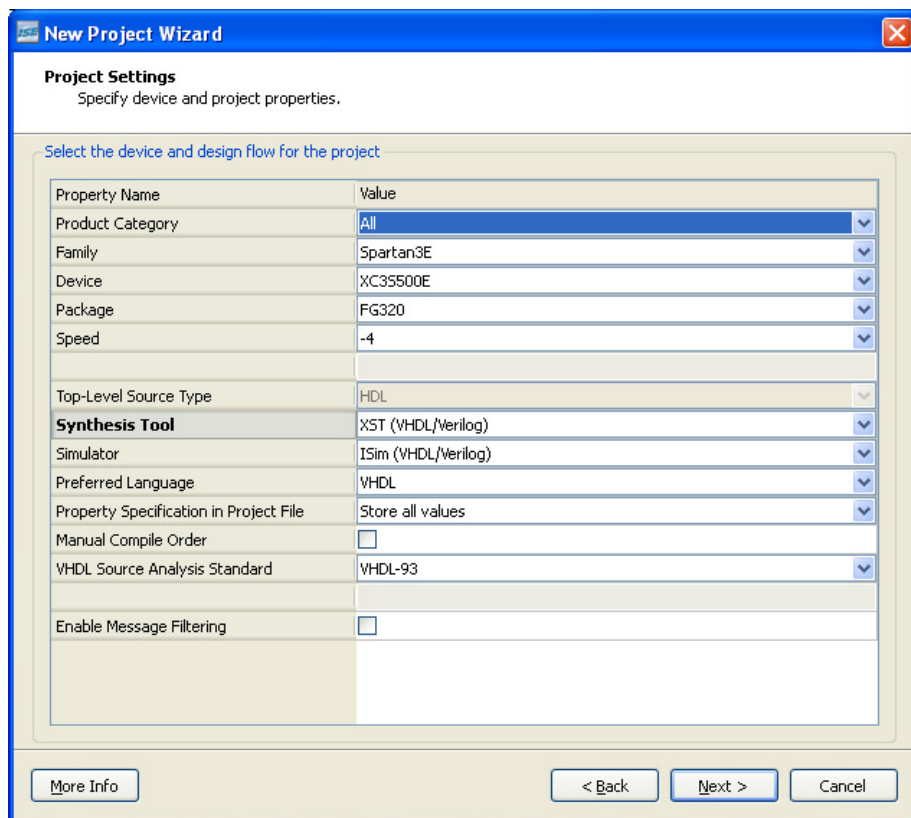
Start Xilinx ISE Design Suite,

Select **File => New Project**

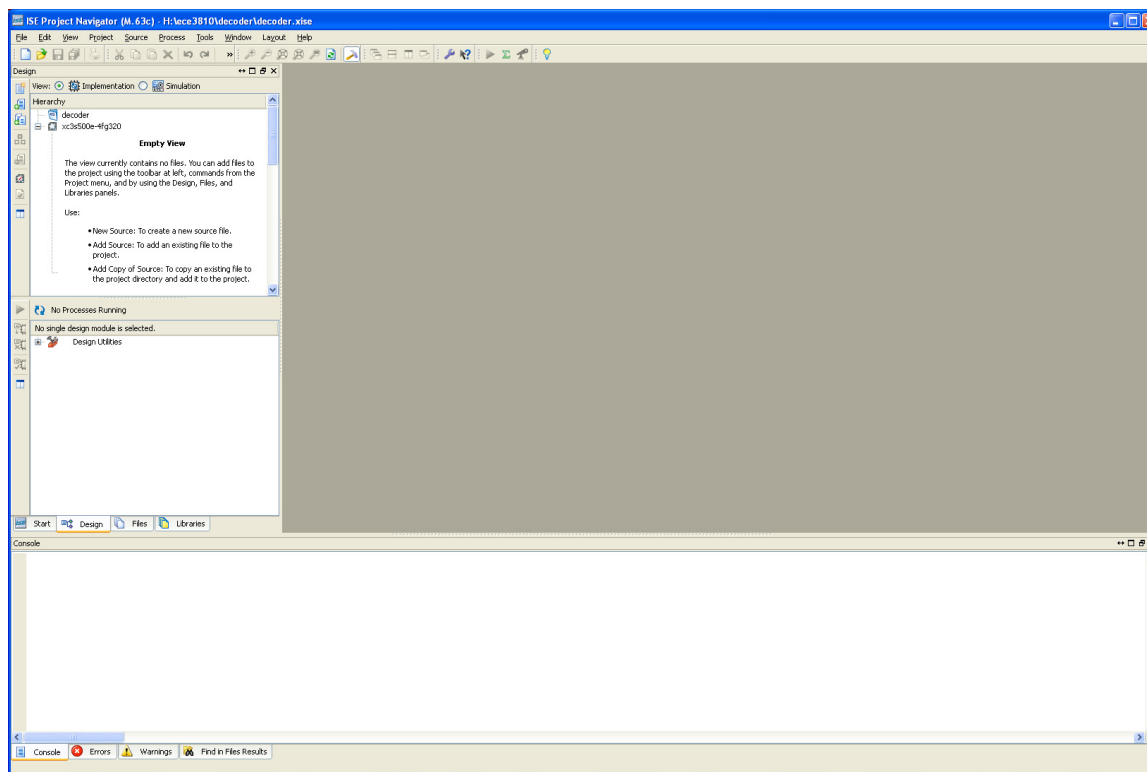
and enter "decoder" for the project name (select an appropriate location):



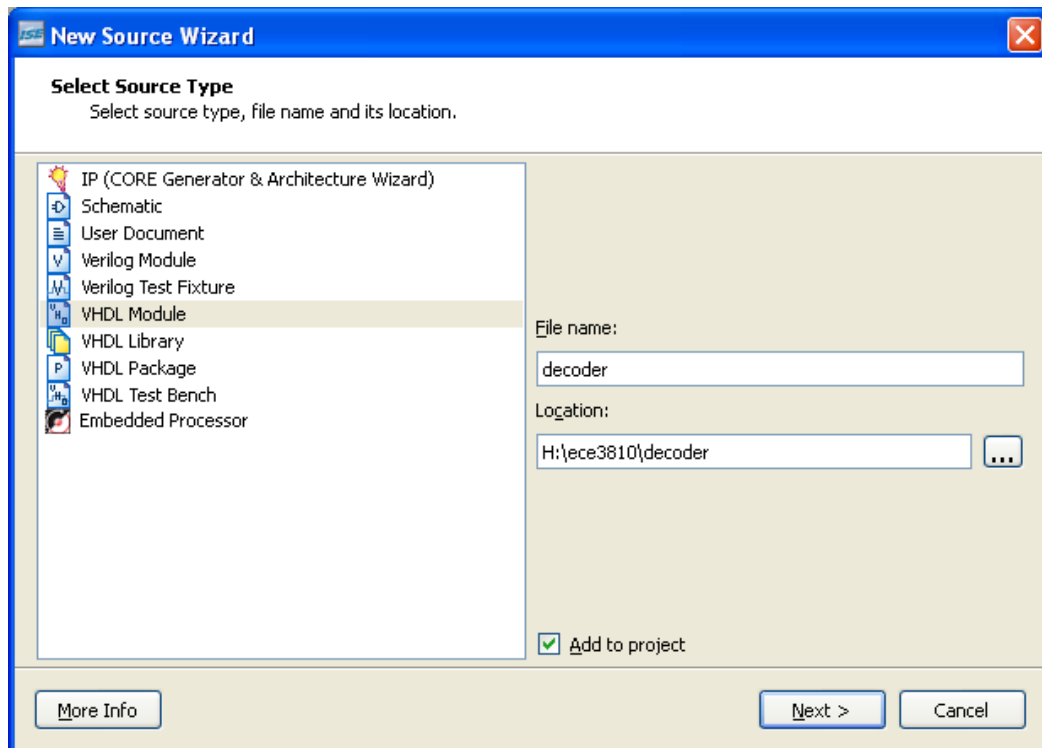
Click **Next** and carefully select the family, device, package, etc to match the FPGA on the Nexys 2 board (also select ISim for the simulator):



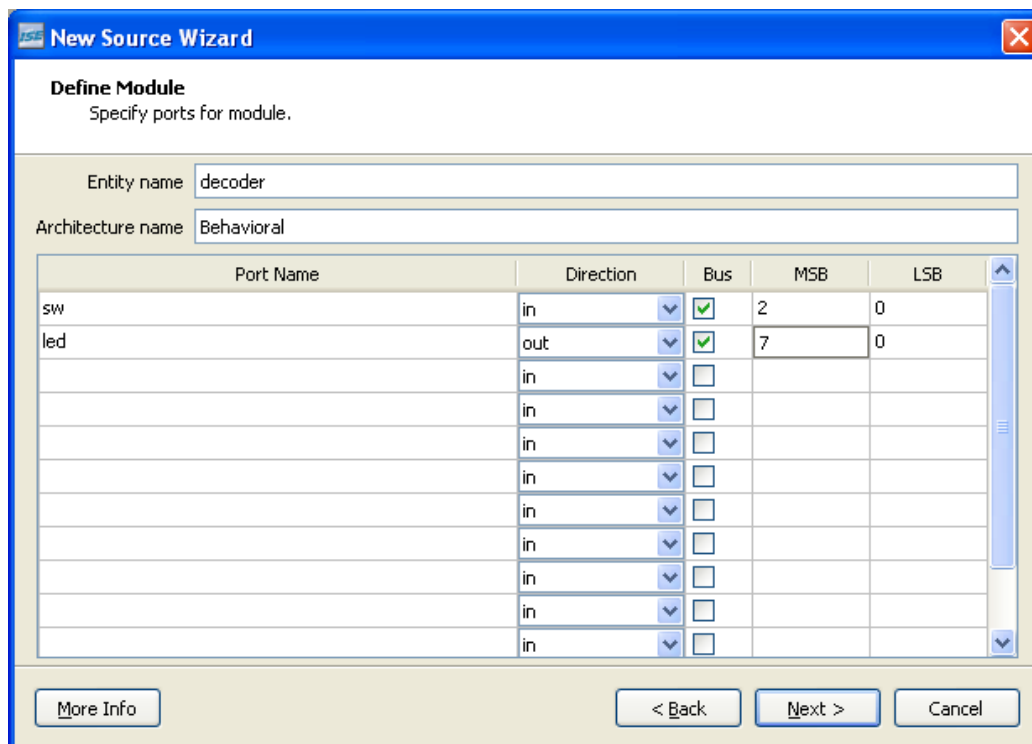
Click **Next**, and then click **Finish**



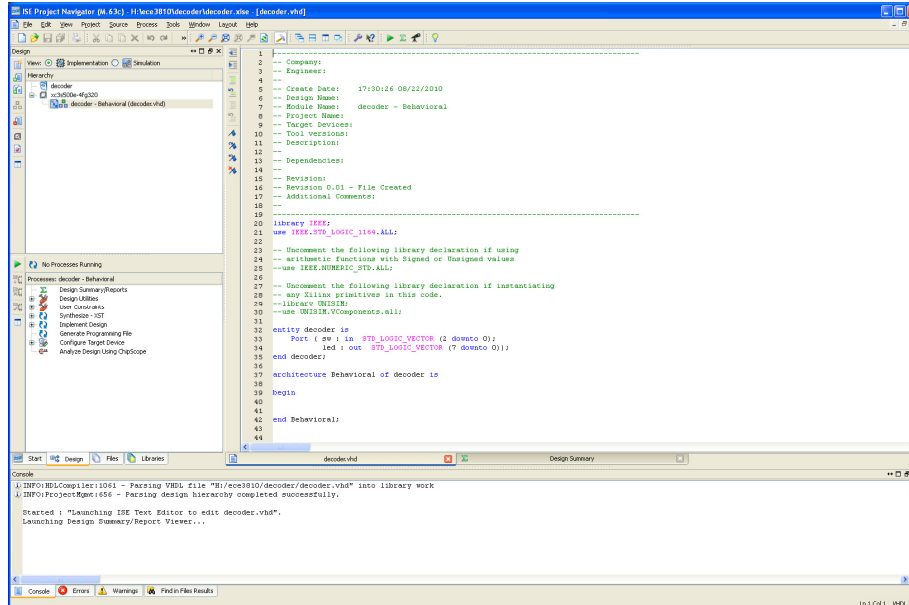
Click on **New Source** (top left icon in the Design window), select VHDL Module, and type "decoder" for name.



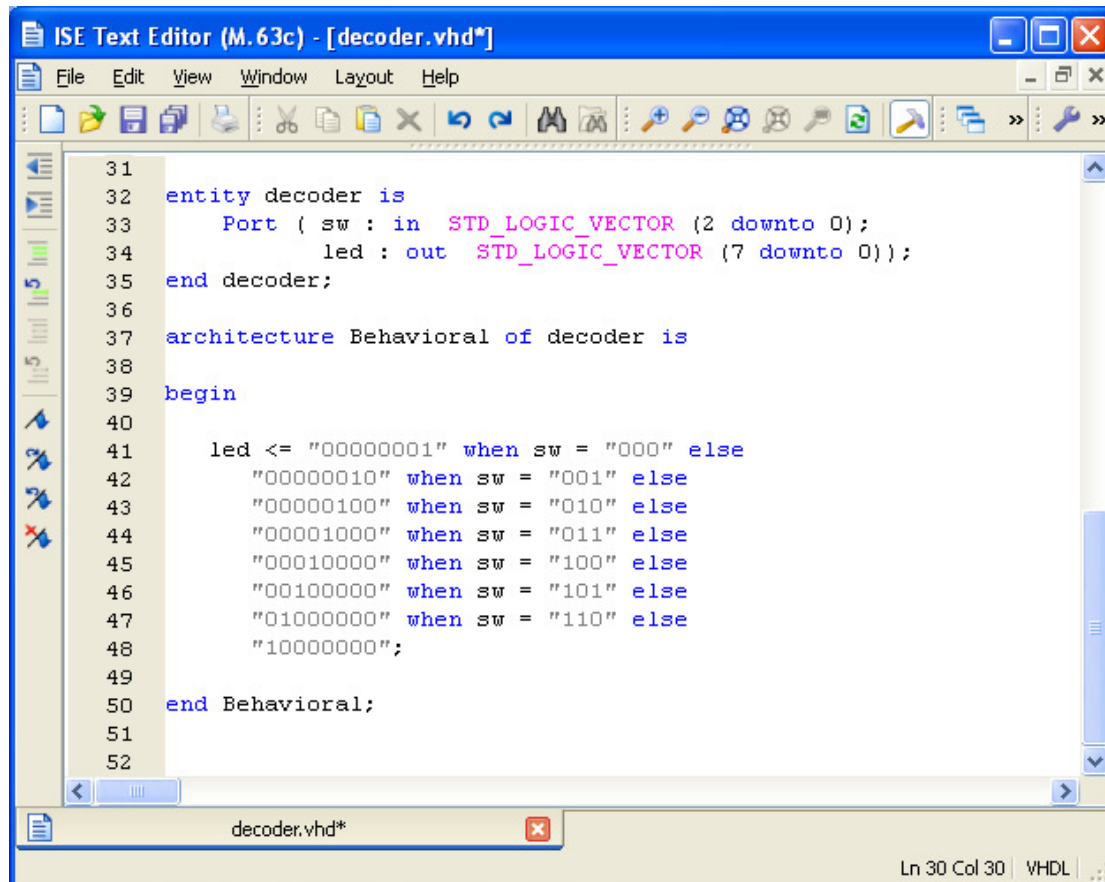
Click **Next**, and add sw and led port names, select direction, and bus size:



Click **Next**, and then **Finish**. A skeleton of your decoder VHDL source file is open for editing:



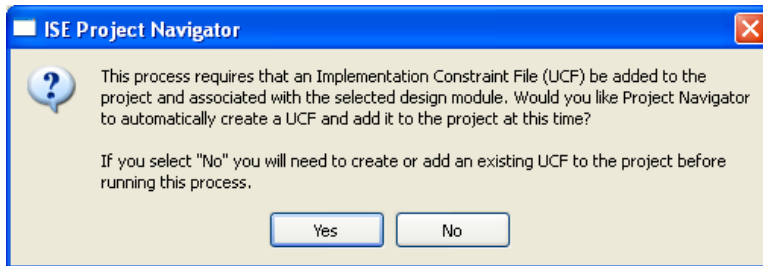
Add VHDL statements to describe the operation of the 3 to 8 decoder:



We now need to assign FPGA pins to the switches and leds so they will be connected to the correct ports on the board. This is done by creating a UCF file (User Constraints File).

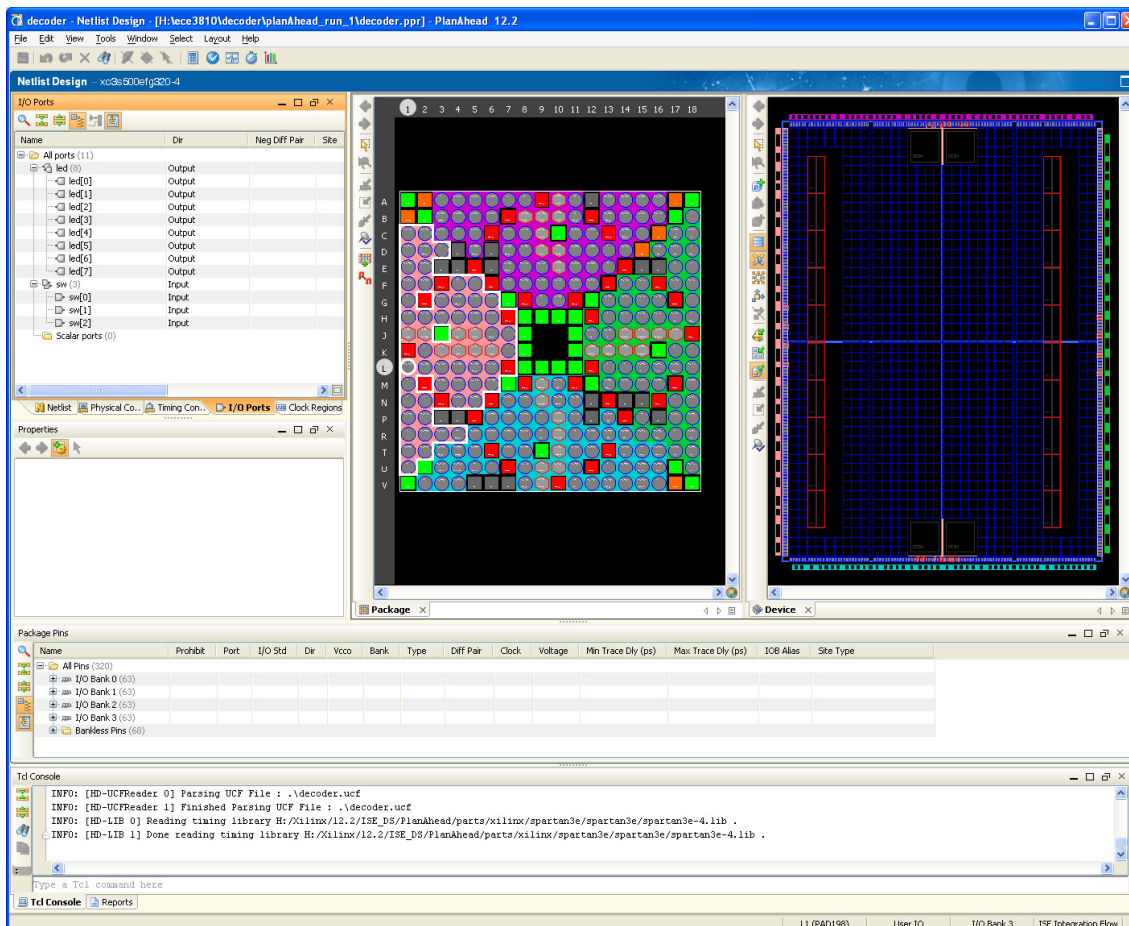
Expand the *User Constraints* process in the Processes window and double-click on the **I/O Pin Planning - Post Synthesis**.

Synthesis will run at this point (if you find errors they are probably due to syntax problems so check your source file) and eventually alert you to create a UCF file:



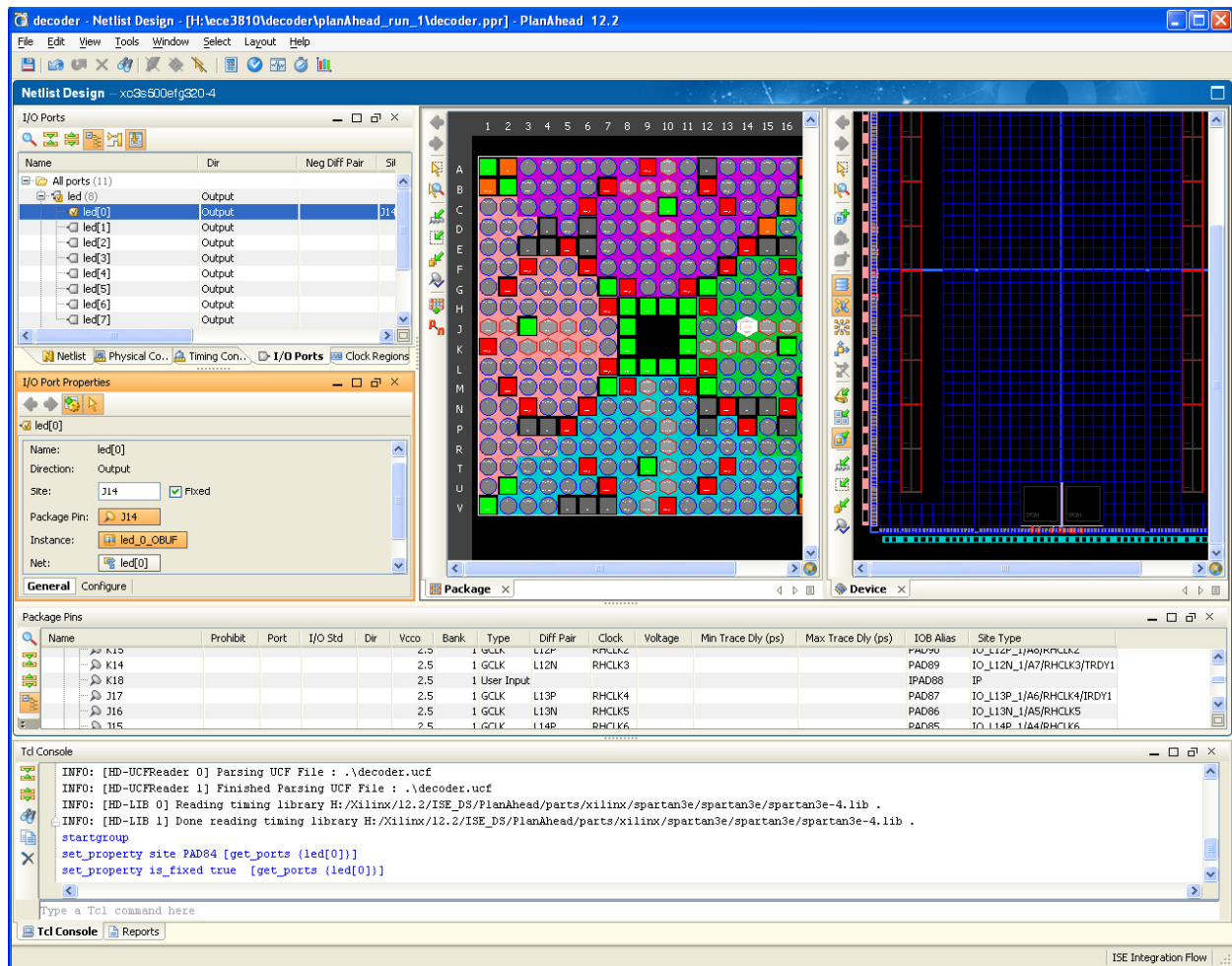
Select **Yes**

PlanAhead will now run, eventually a window will open (select the I/O ports tab and then expand the led and sw ports as shown:



Select led[0] in the I/O ports window and drag to the package pin location J14:

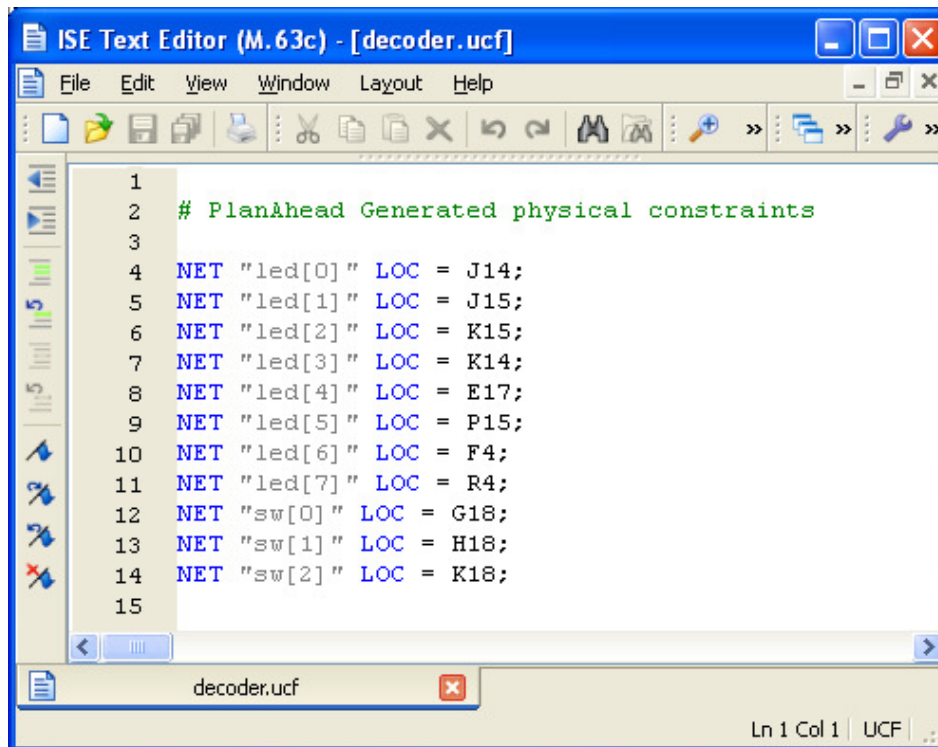
The Site box in the I/O Port Properties window should be updated (instead of dragging, you can also type the site location directly).



With reference to the Nexys2 Reference Manual complete the pin information for the rest of the led and sw ports.

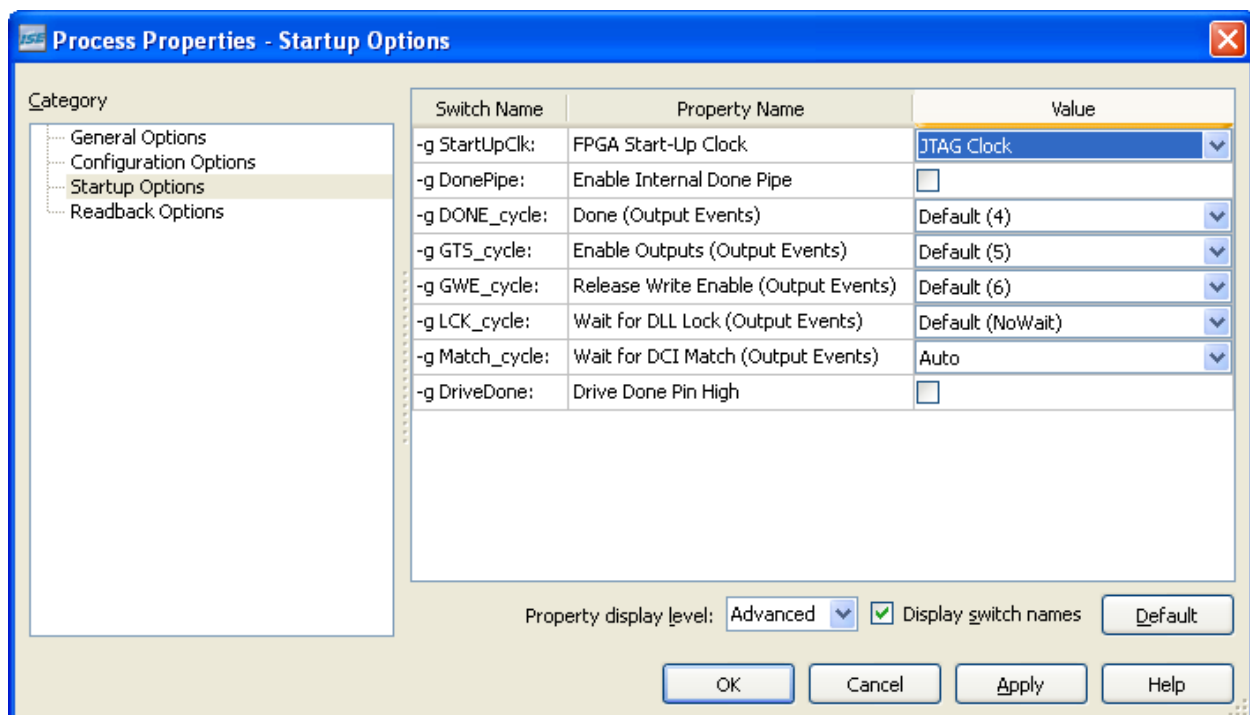
Select **File => Save Design** and exit PlanAhead.

In the Project navigator Design Hierarchy expand the decoder and you should see the new decoder.ucf file is now added. To view the UCF file, select the *decoder.ucf* and then select **Edit Constraints (Text)** in the Processes window:



We can now complete the Synthesis, Implementation, and Generate Programming File steps. Back in the design window select the decoder-Behavioral(decoder.vhd) and then *right-click* on the **Generate Programming File** button and select the Process Properties – Startup Options.

IMPORTANT: Change the default FPGA start-up Clock from CCLK to JTAG:



Click OK and then double click the Generate Programming Button.

You should eventually see a "Generate Programming File" message in the console window:

The screenshot displays the ISE Project Navigator interface. The Design Summary window is open, showing the 'Generate Programming File' button highlighted in the Design Summary pane. The console window at the bottom shows the command line and the successful completion of the programming file generation process.

decoder Project Status (08/22/2010 - 18:08:44)

Project File:	decoder.xise	Parser Errors:	No Errors
Module Name:	decoder	Implementation State:	Programming File Generated
Target Device:	xc3s500e-4fg320	Errors:	No Errors
Product Version:	ISE 12.2	Warnings:	No Warnings
Design Goal:	Balanced	Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	Timing Constraints:	
Environment:	System Settings	Final Timing Score:	0 (Timing Report)

Device Utilization Summary

Logic Utilization	Used	Available	Utilization	Note(s)
Number of 4 input LUTs	8	9,312	1%	
Number of occupied Slices	4	4,656	1%	
Number of Slices containing only related logic	4	4	100%	
Number of Slices containing unrelated logic	0	4	0%	
Total Number of 4 input LUTs	8	9,312	1%	
Number of bonded IOBs	11	232	4%	
Average Fanout of Non-Clock Nets	2.91			

Performance Summary

Final Timing Score:	0 (Setup: 0, Hold: 0)	Pinout Data:	Pinout Report
Routing Results:	All Signals Completely Routed	Clock Data:	Clock Report
Timing Constraints:			

Detailed Reports

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Sun Aug 22 17:46:25 2010	0	0	0
Translation Report	Current	Sun Aug 22 18:08:10 2010	0	0	0
Map Report	Current	Sun Aug 22 18:08:17 2010	0	0	2 Infos (2 new)
Place and Route Report	Current	Sun Aug 22 18:08:29 2010	0	0	1 Info (1 new)
Power Report					
Post-PAF Static Timing Report	Current	Sun Aug 22 18:08:33 2010	0	0	5 Infos (5 new)

Console

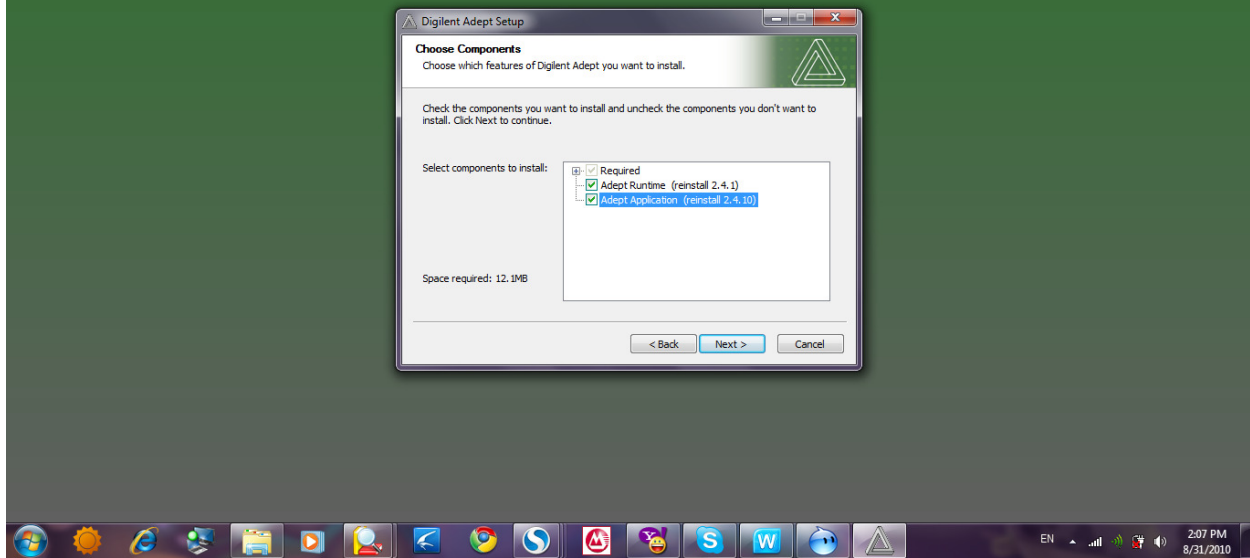
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Command Line: bitgen -intstyle ise -f decoder.ut decoder.nod
J:\INFO\WebTalk:4 - R:/ece3810/decoder/usage_statistics_webtalk.html WebTalk
report has been successfully sent to Xilinx. For additional details about this
file, please refer to the WebTalk log file at R:/ece3810/decoder/webtalk.log
WebTalk is complete.
Process "Generate Programming File" completed successfully
  
```

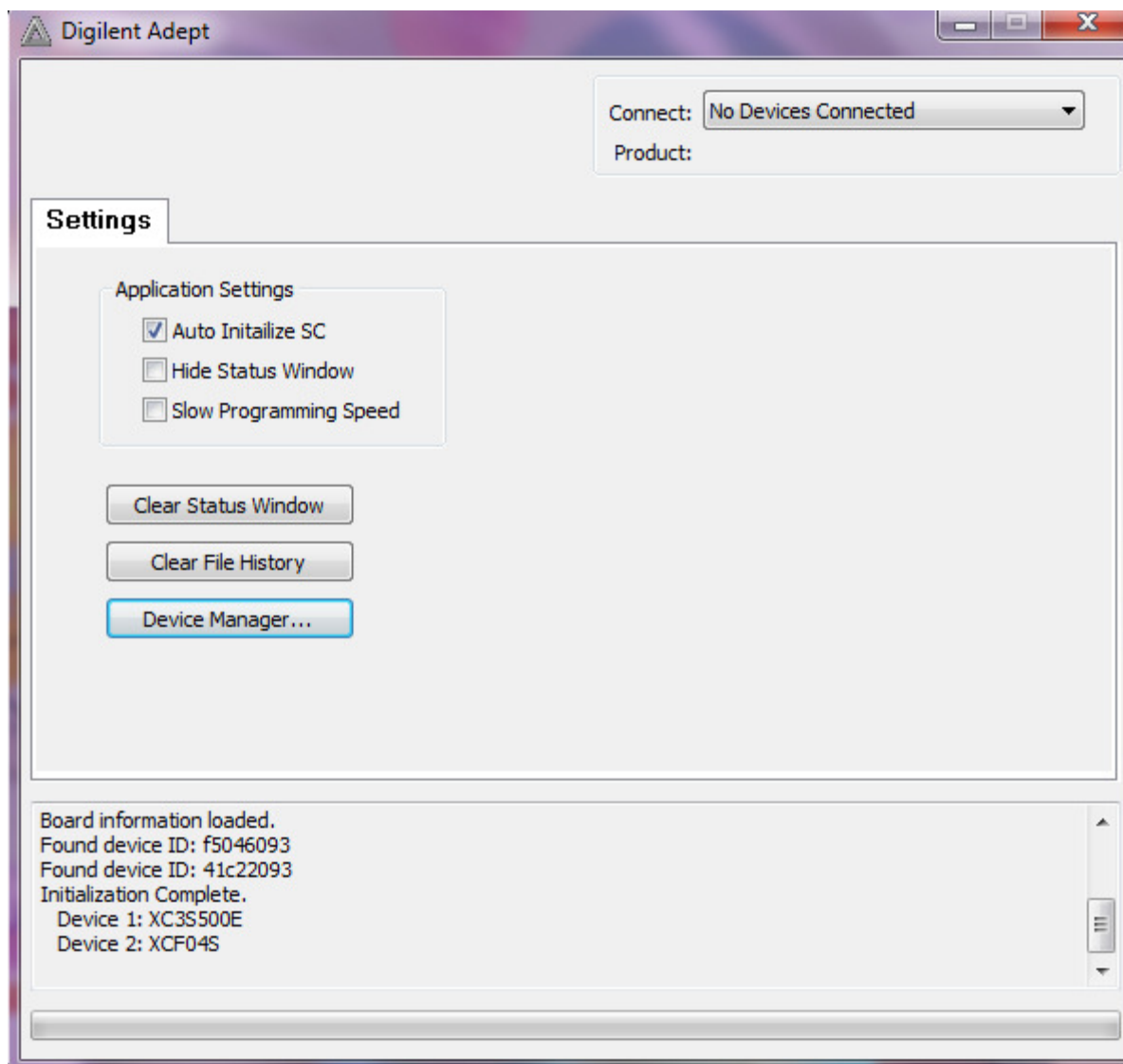
Finally, in order to program and communicate with the Nexys 2 board, you must download and install the [Digilent Adept software](#).

First, download the corresponding version of Adept software which supports the operating system of your computer.

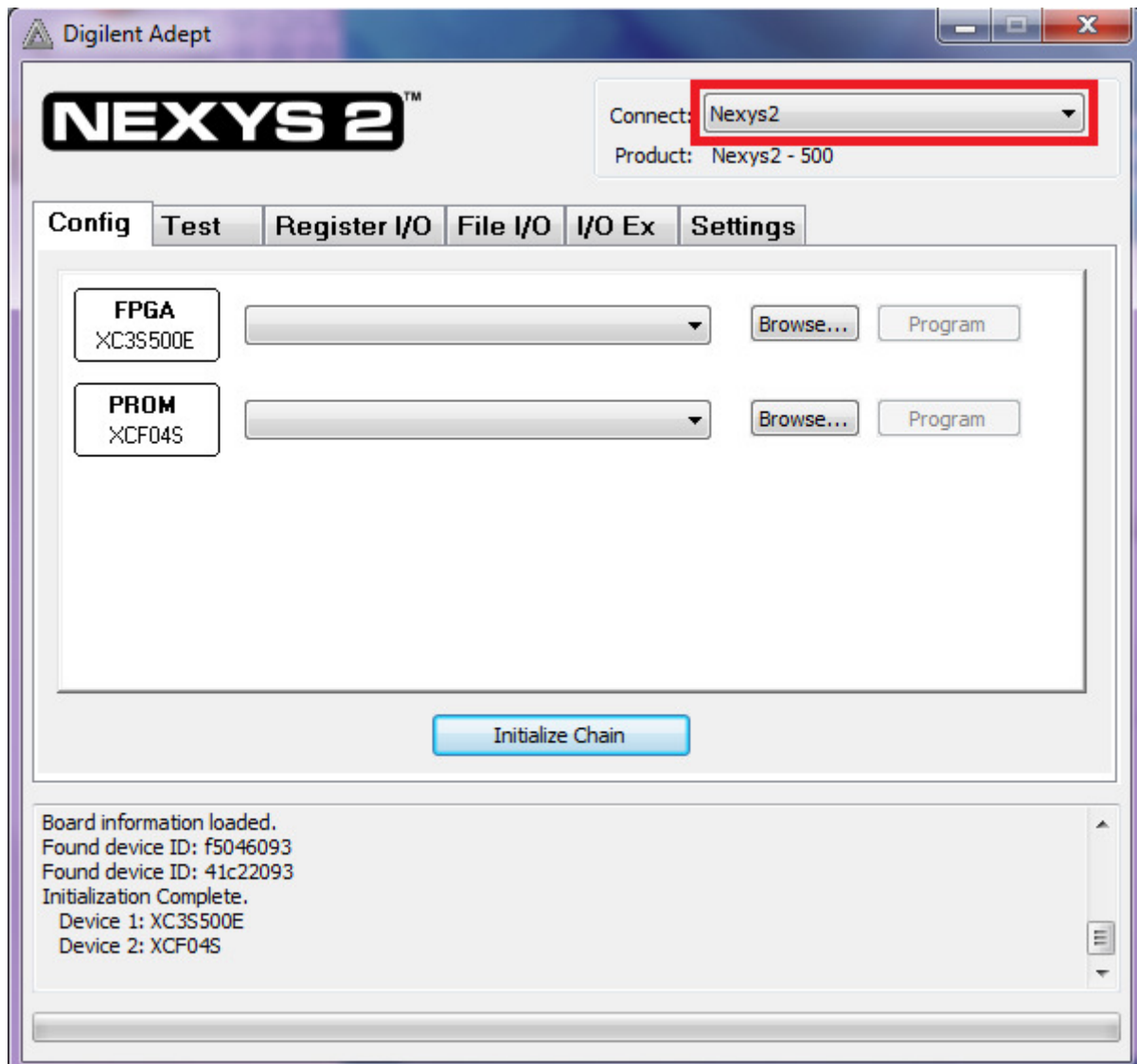
Digilent Adept Setup



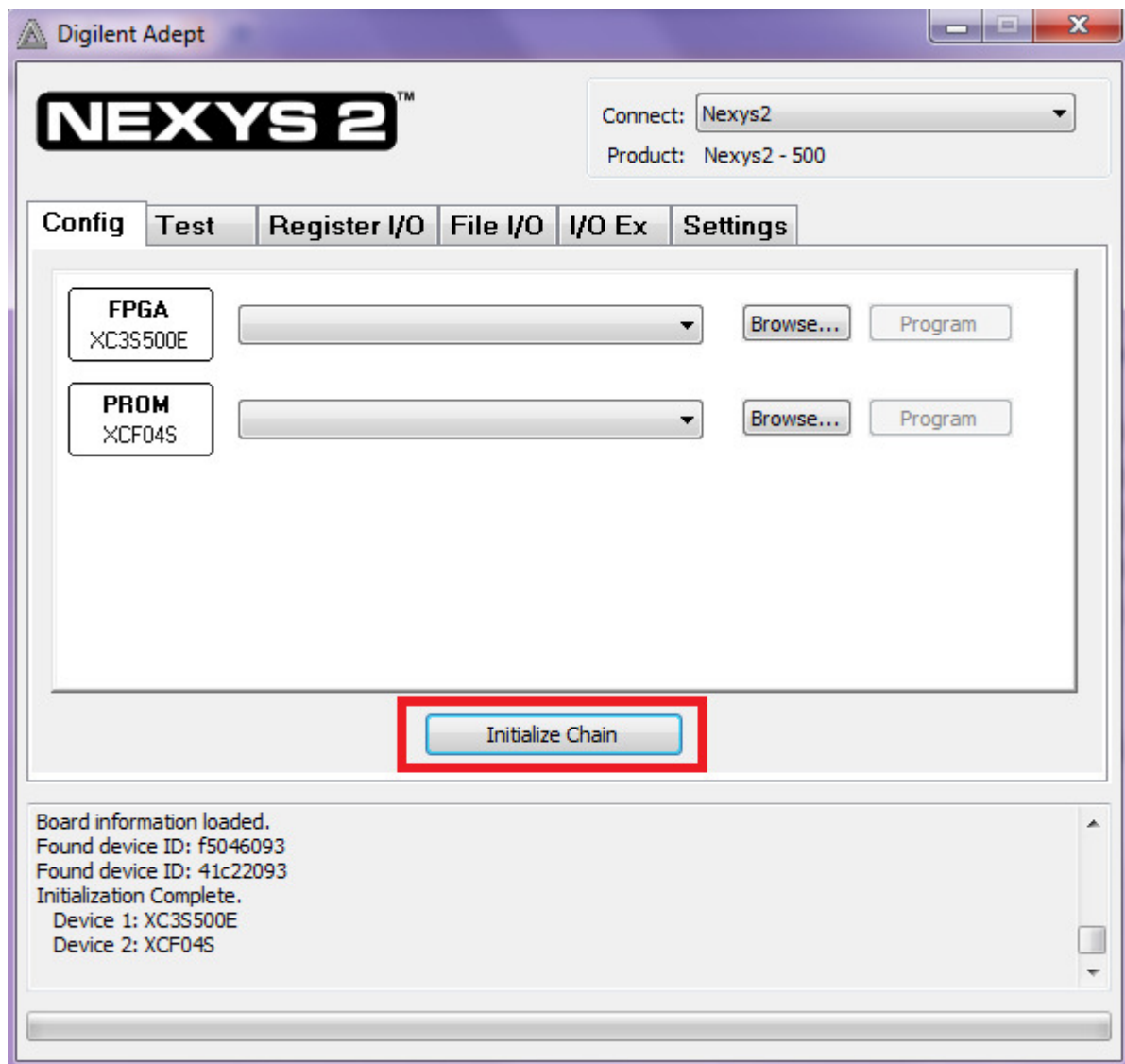
Second, install the Digilent Adept software on your computer.



Third, open Adept application after installation, a restart of your computer might be necessary. (Start > Programs > Digilent > Adept > Adept)

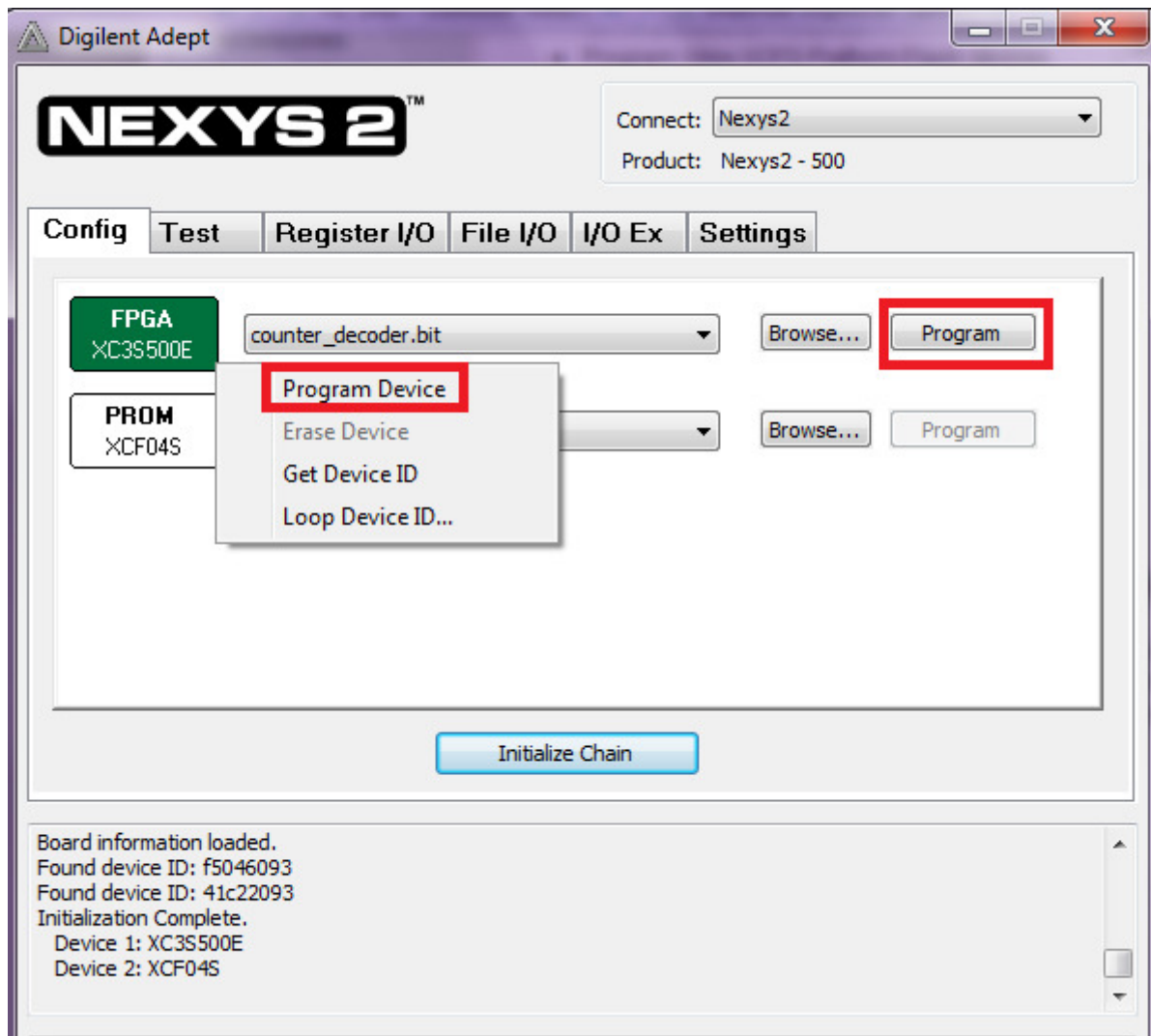


Fourth, connect your Nexys 2 board to your computer with the USB cable, if your PC is running Windows XP, you might need to wait for the operating system to recognize the board and install the USB driver for the USB port you are using. Click on the drop-down menu highlighted on the screen-shot above and select the name of the board which you are trying to communicate with, and then the Adept application should detect your board soon after.

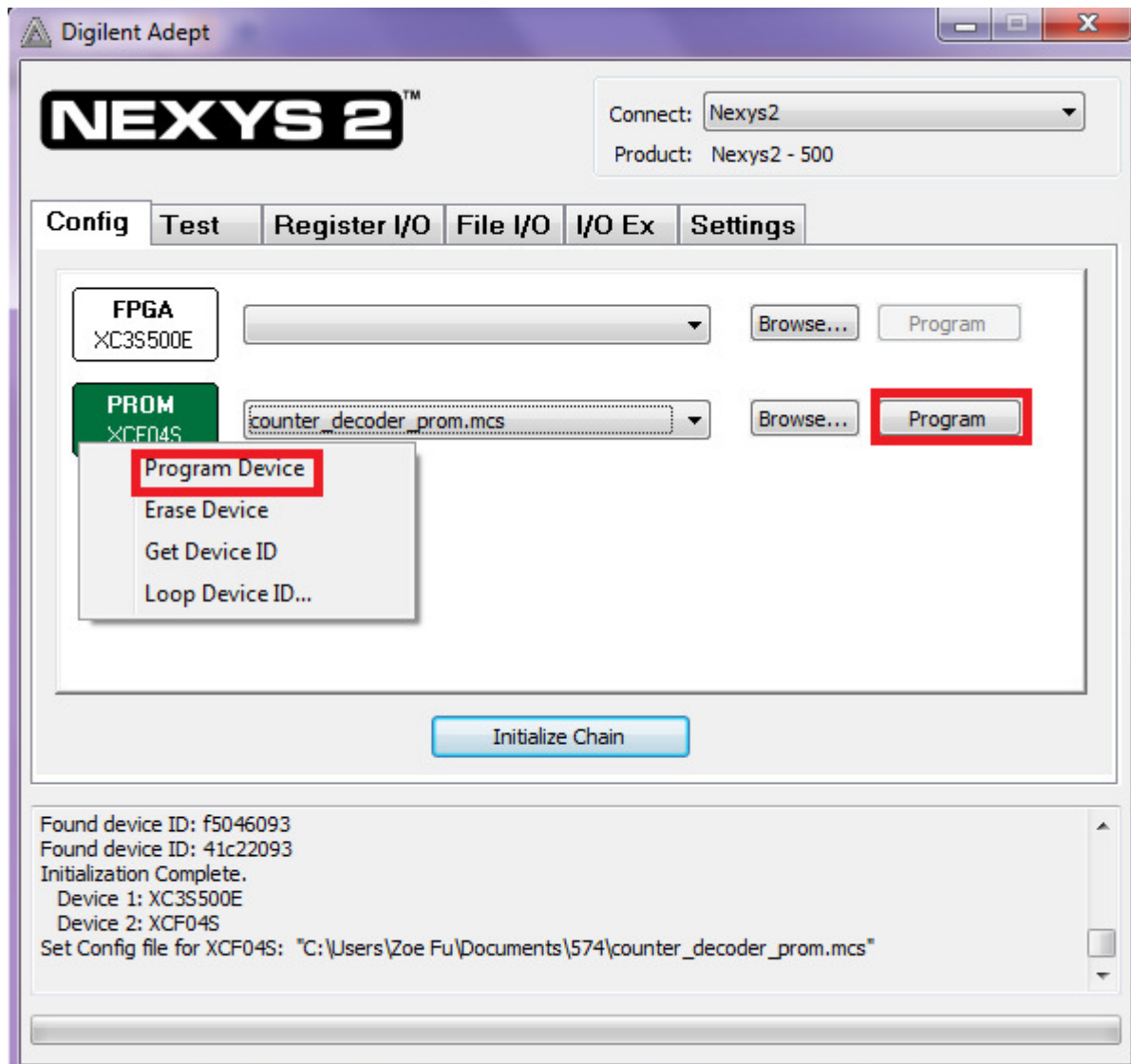


After previous steps, the chain should be initialized automatically, but you can also click on "Initialize Chain" to initialize it manually.

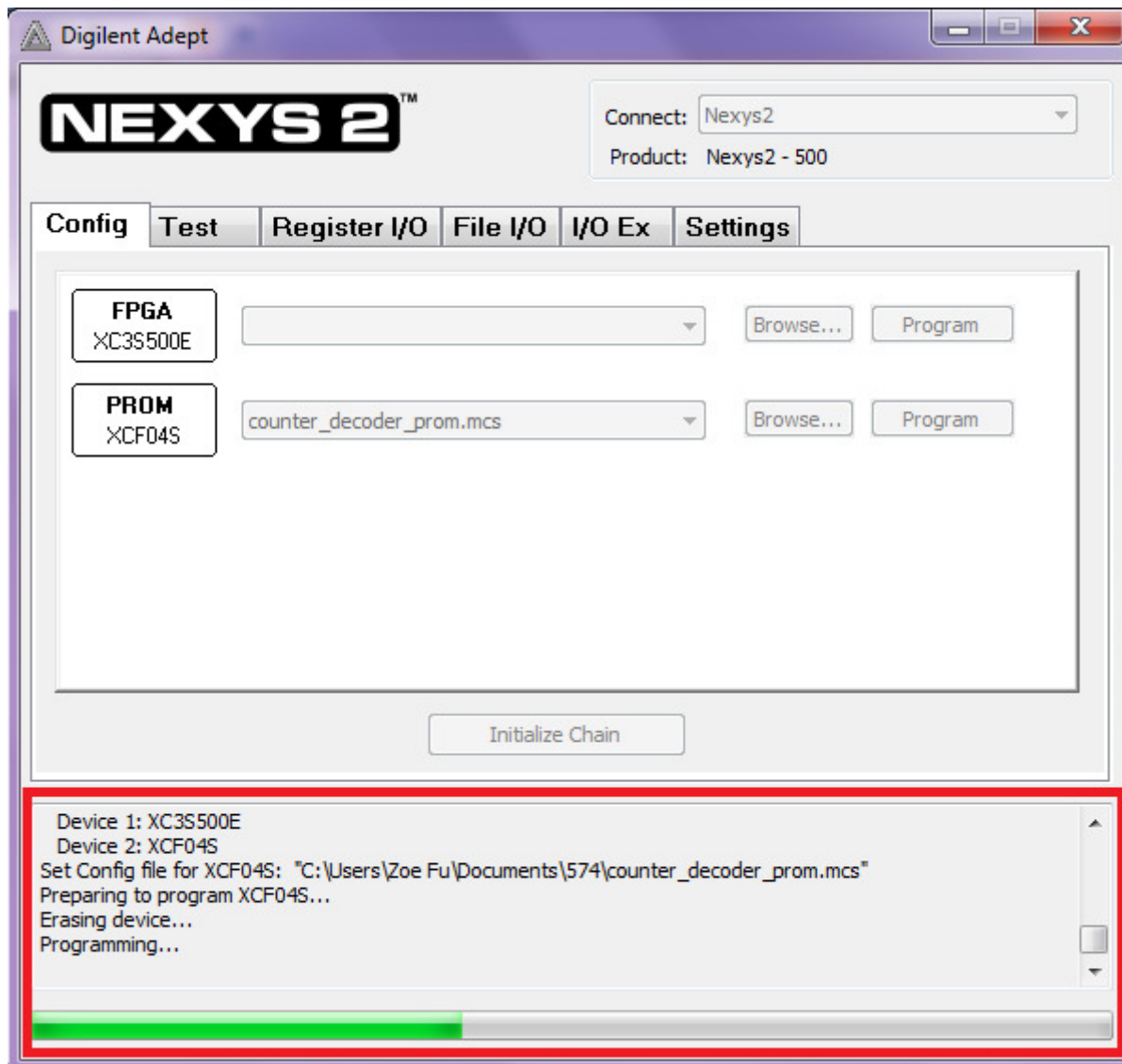
Fifth, now we are ready to program the devices!



When trying to program the FPGA, Click the Browse button nex to the FPGA device icon, select your configuration file(.bit) and click the open button. After that, program the FPGA chip by right-clicking on the FPGA device icon and select "Program Device" or simply hit the "Program" button on the right.



When trying to downloading the load to PROM, Click the Browse button nex to the PROM device icon, select your configuration file(.mcs) and click the open button. After that, program the PROM by right-clicking on the PROM device icon and select "Program Device" or simply hit the "Program" button on the right. We can also erase the PROM first before programming it.



We can check the progress of our operations in the window at the bottom of the interface.

At last, if programming successfully, we should be able to see if our projects and loads actually work fine on the board.

Advanced features or further information of Adept software in details can be found @

<http://www.digilentinc.com/Data/Documents/Tutorials/Adept%20Software%20Basic%20Tutorial.pdf>

Have fun!