Name: Samson Raj Surendra
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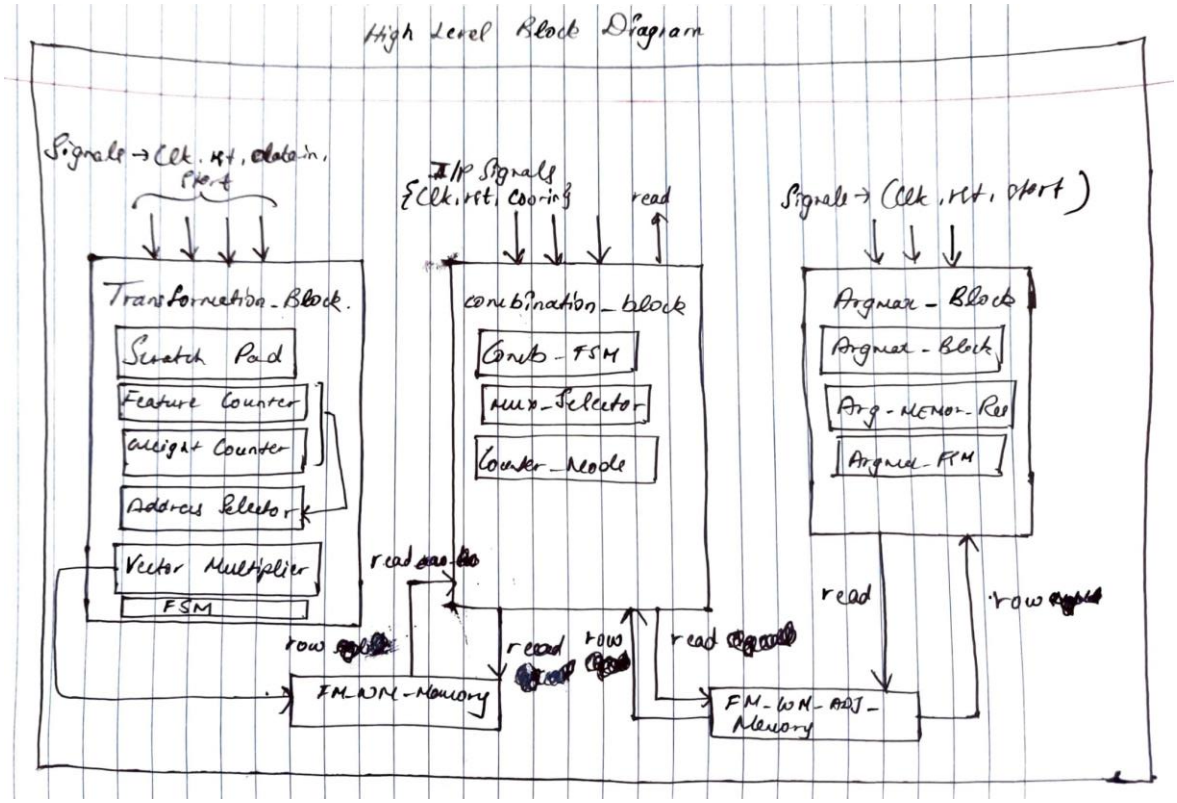
EEE 525 LAB 4
Milestone 2

1) Architecture and high-level block diagram



Initial Design Considerations:

Transform block:

- Feature matrix × Weight matrix
- Scratchpad basically stores your weight columns
- FM_WM memory stores the result of your vector multiplication
- Control FSM – state machine orchestrates the entire design by providing control signals
- Feature counter and weight counter is there is keep track of your operation

Virtual Memory Scheme Concept:

- Where all the weights and features are stored
- Read address is connected to virtual memory or actual memory
- Address 0x0 to 0xFF – weights
- Address 0x200 to 0x2FF – features
- Should generate the correct address to read the weight column and feature row
- Whenever we give an address we get a vector and at each address we will store 96, 5-bit values

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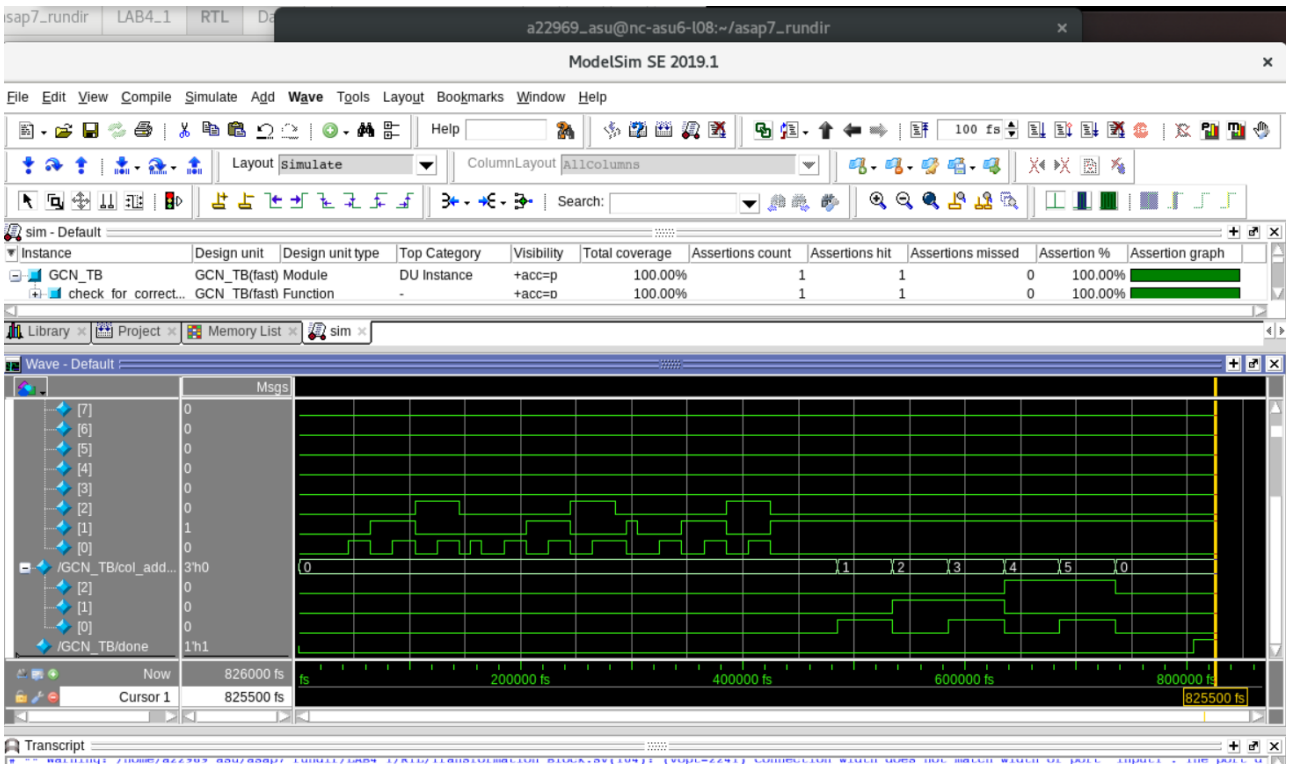
Combination Block:

- Obtained from multiplying adj matrix with the vector product of FM and WM
- Converting from coordinate format to adjancy matrix format is required to perform matrix to matrix multiplication
- We only read on coordinate column at a time
- Each column represents one edge
- We loop through entire coordinate matrix and then create the adjancy matrix
- We are also given the FM_WM_ADJ_ memory which stores the final output of the memory

Argmax Block:

- Argmax is used for node classification
- Once we have the result of 3 matrix multiplication from the combinational block, the classification is done by the Argmax function
- For FM_WM_ADJ which is a 6 × 3 matrix, each column corresponds to a class and each row corresponds to one node in our graph
- For example, in node1what is the strength of the classification for each class.
- Therefore we need to iterate through all our nodes of the adj matrix and pick the column that has the largest value
- Output will be the class that corresponds to the column we pick

Behavioral Verilog – Simulation:



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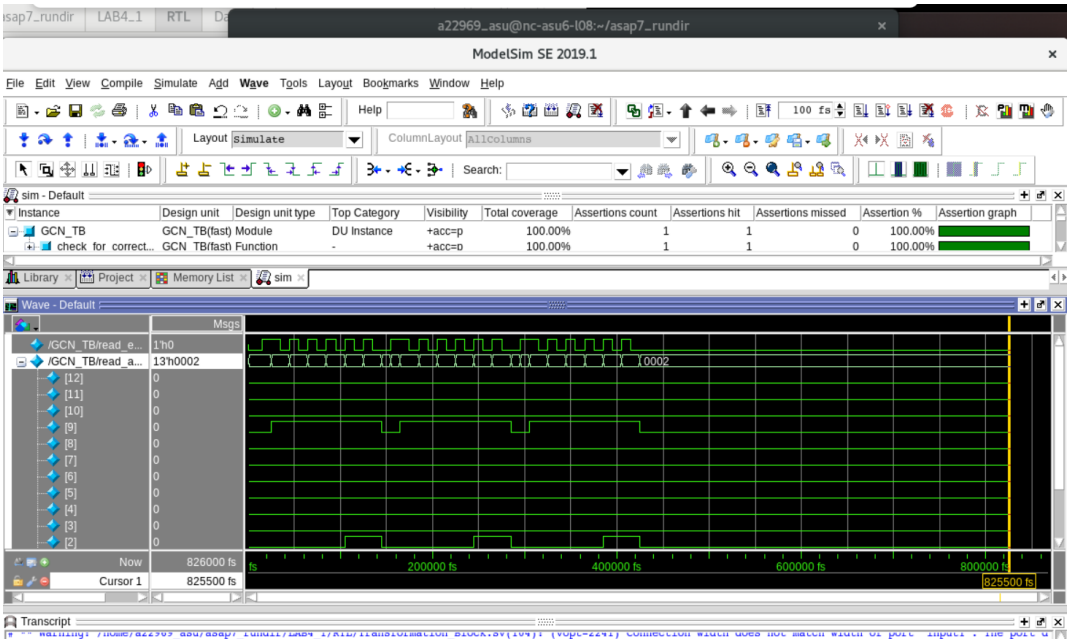
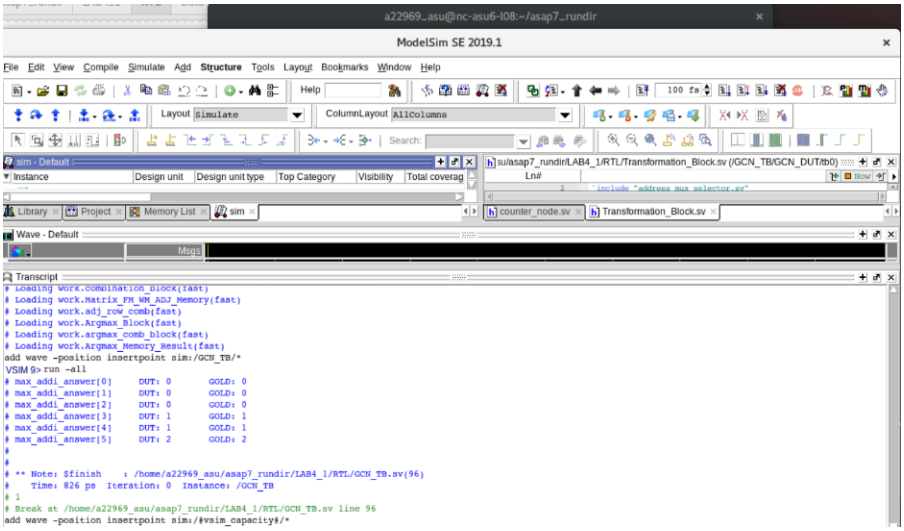
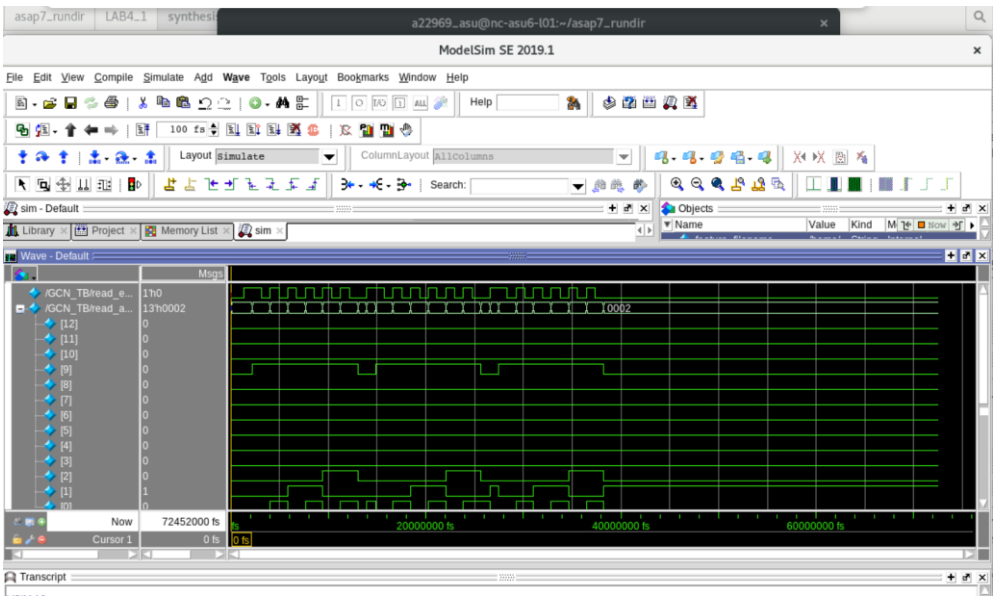




Post_Synthesis - Simulation:



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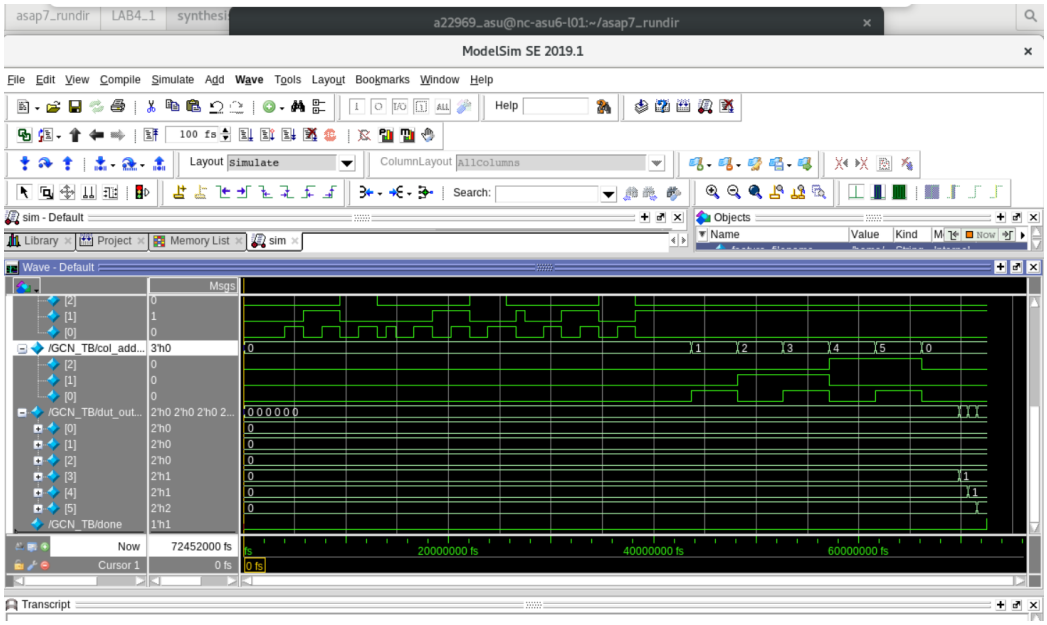
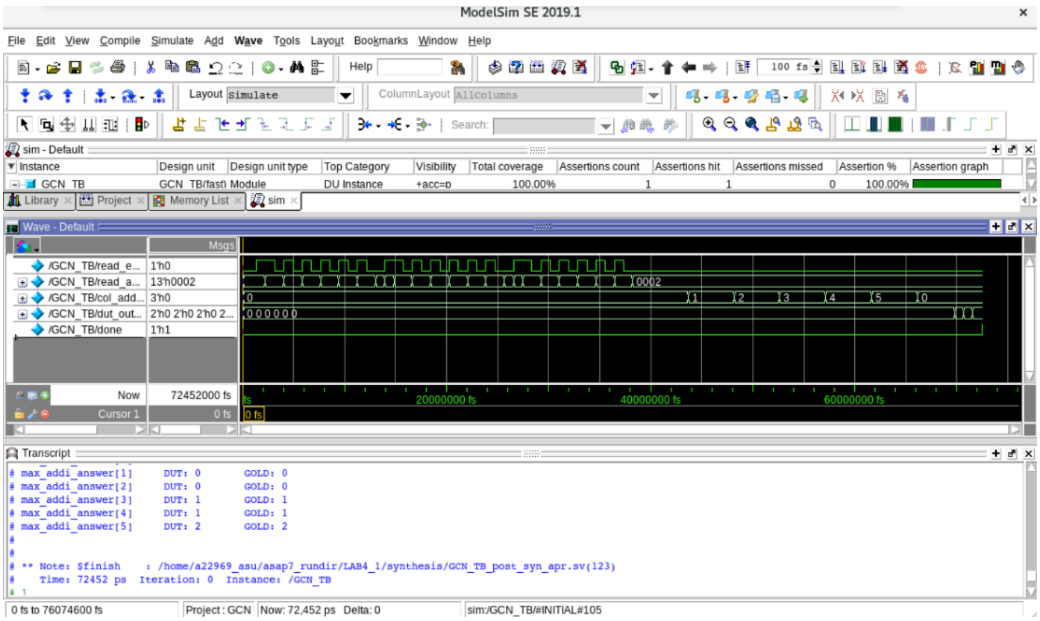
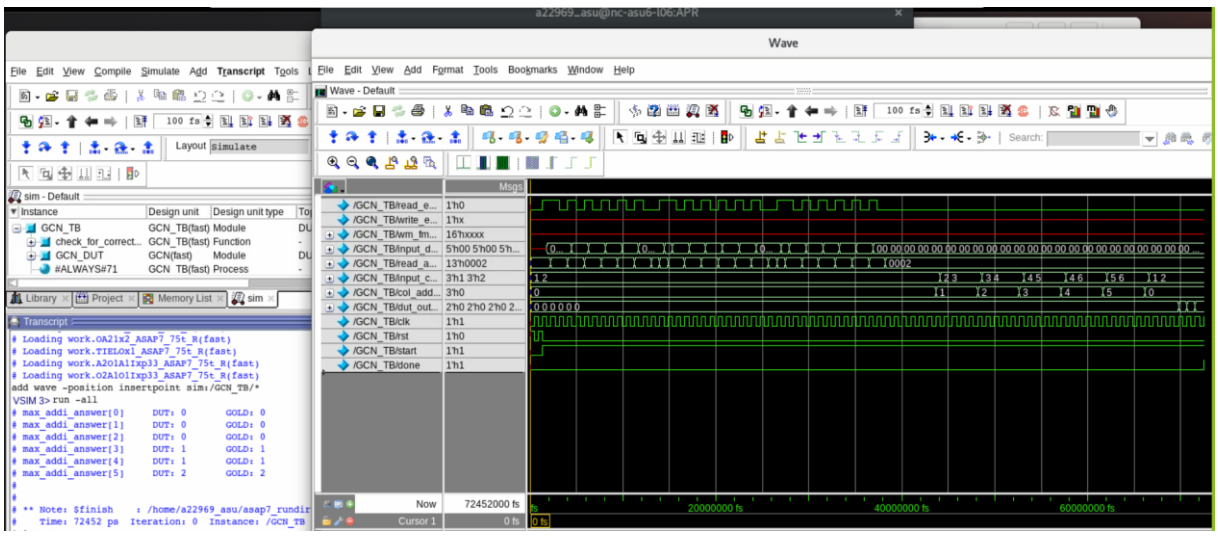




Post APR Simulation:



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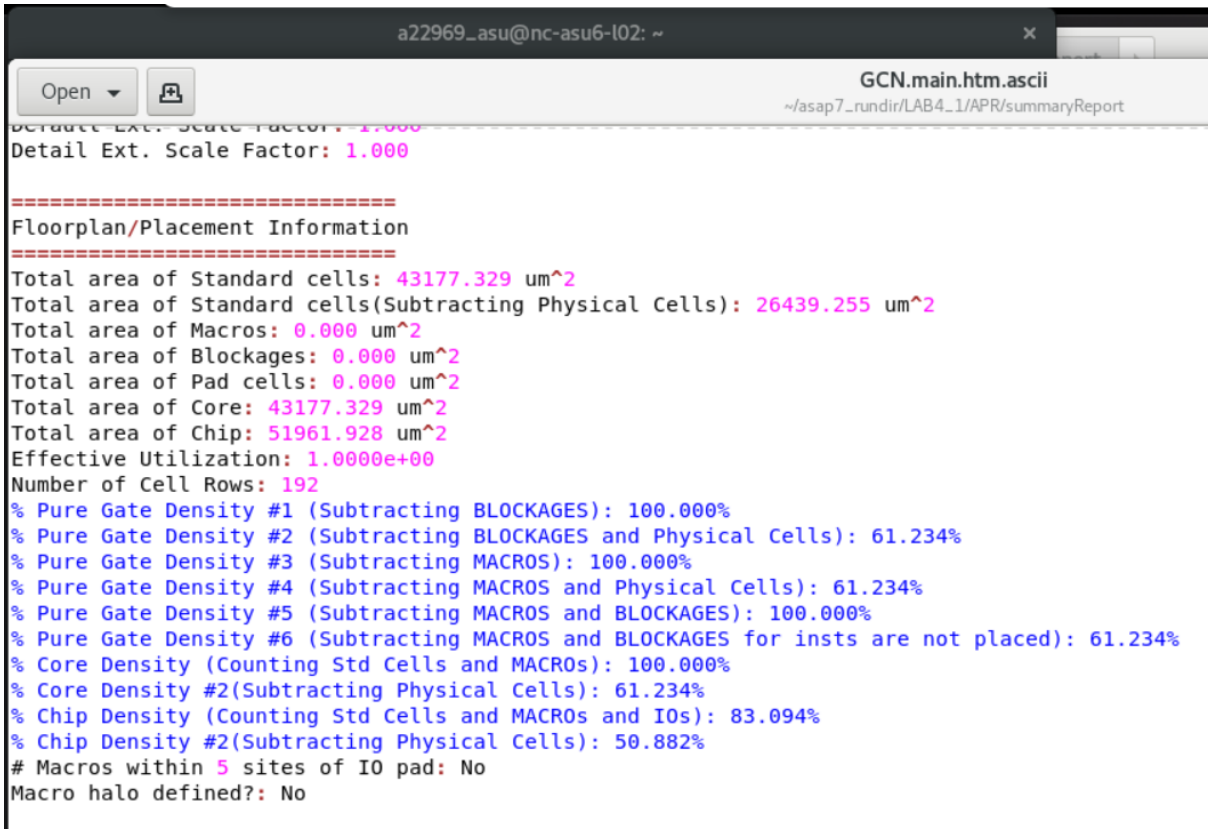
Total Latency: 72.45 ns with a clock frequency of 1111.11 MHz

Clock Period: 900 ps

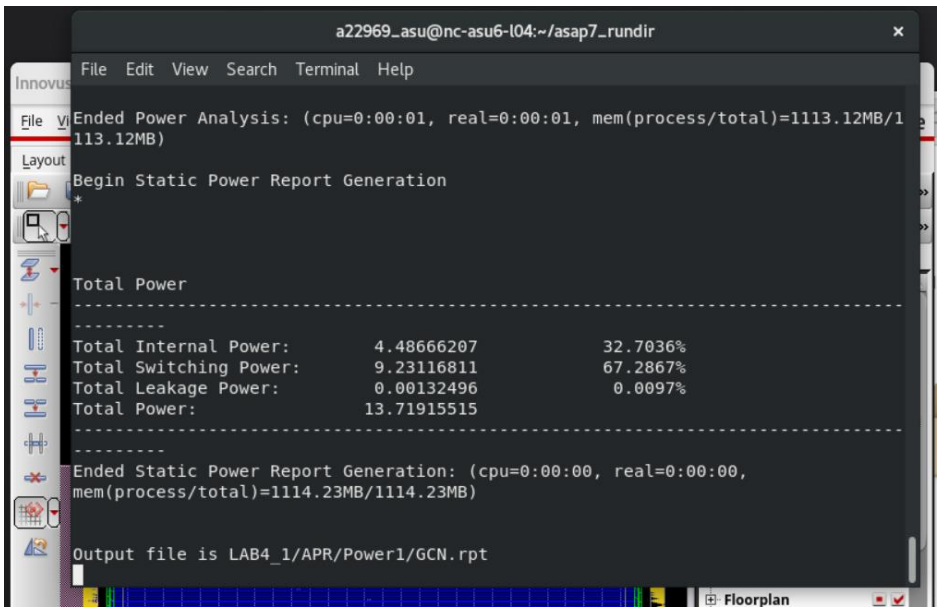
Area:

Standard Cells + Filler Cells: 0.43 mm2



Power:

Total Power = 13.71 mW



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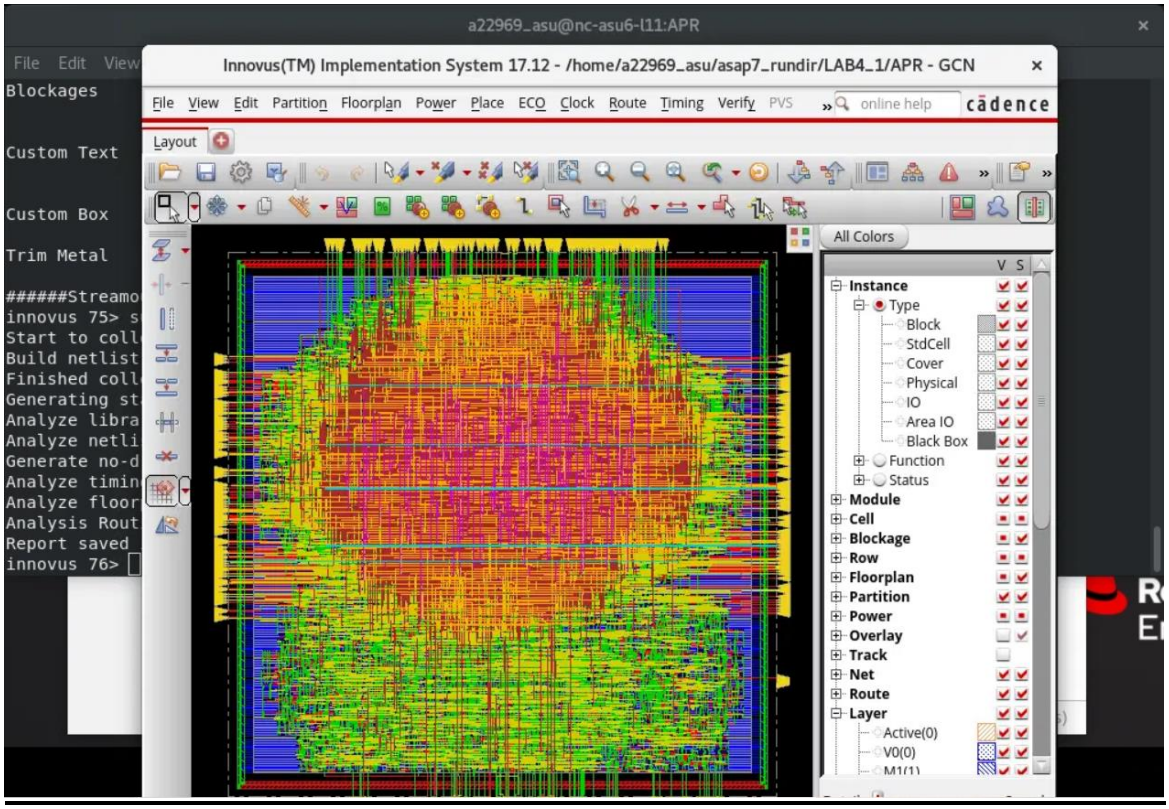
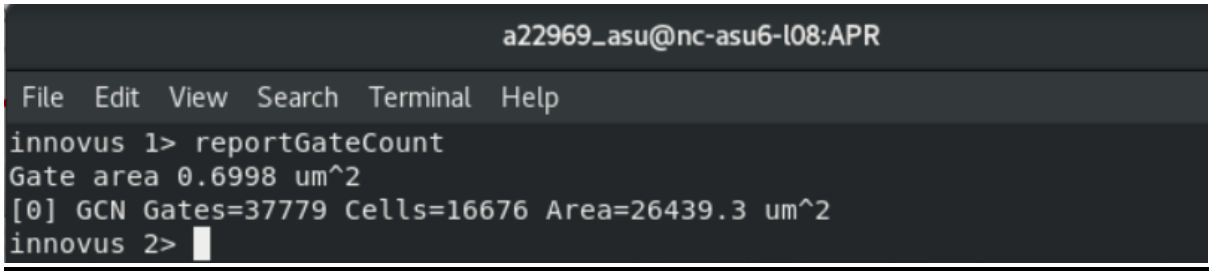
Layout – Innovus:



Innovus Density:

Number of Gates:

Gates = 37779
Cells = 16676



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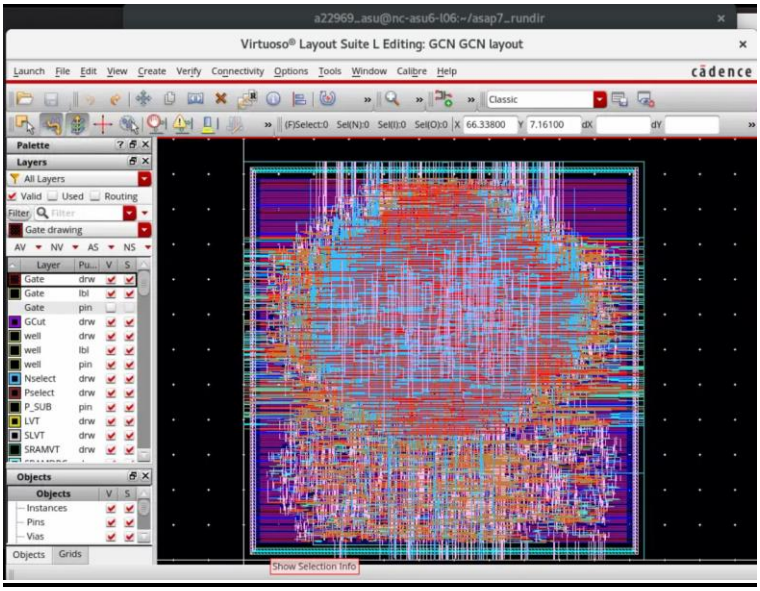
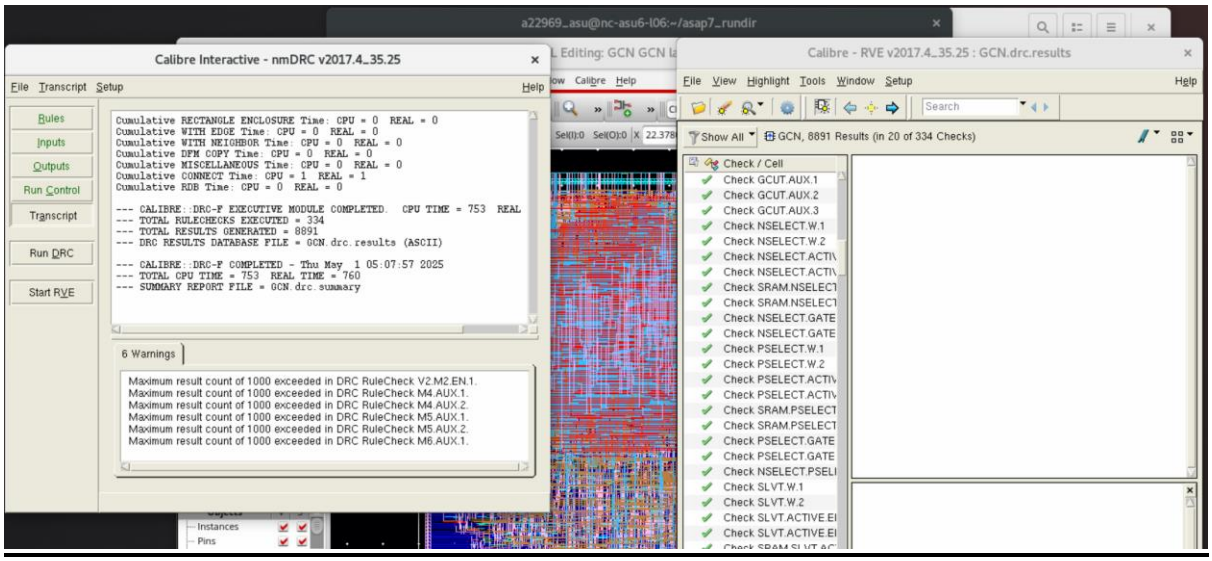
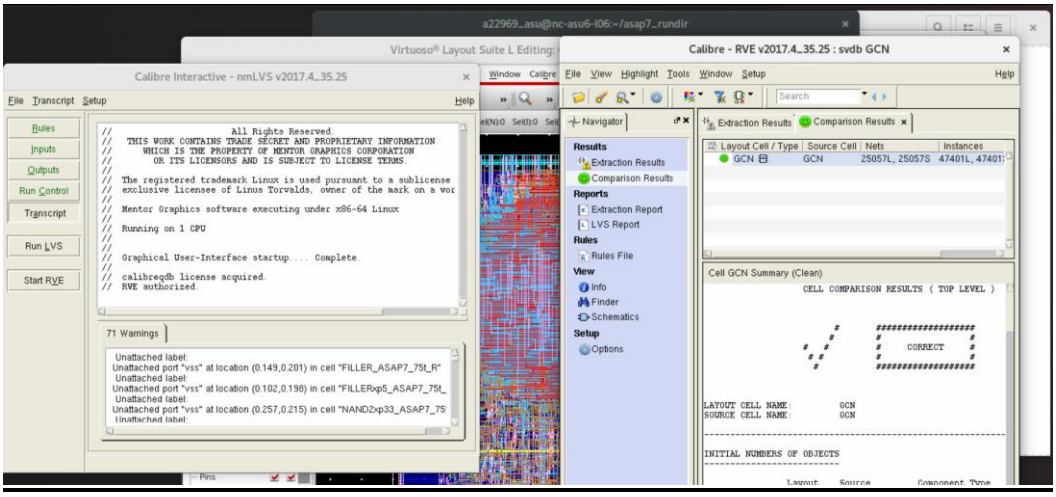
Layout – Virtuoso:



Post APR -DRC:



Post APR -LVS:



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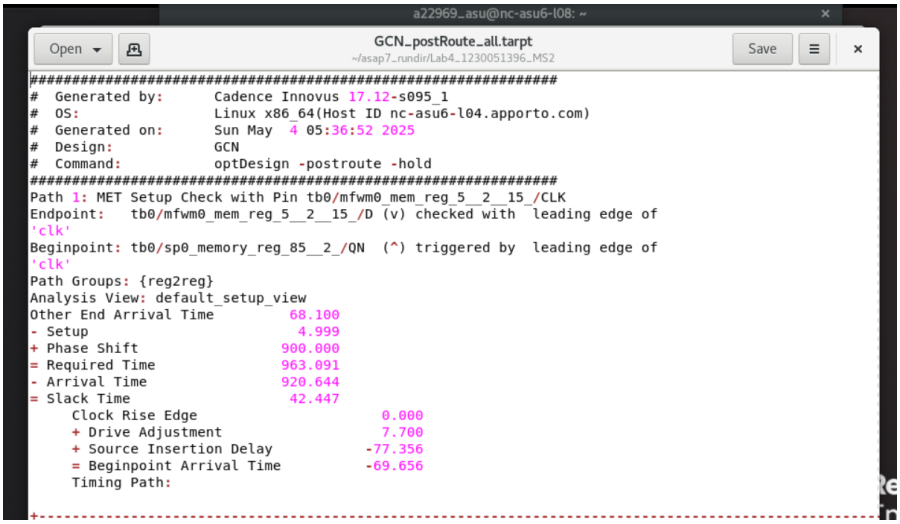
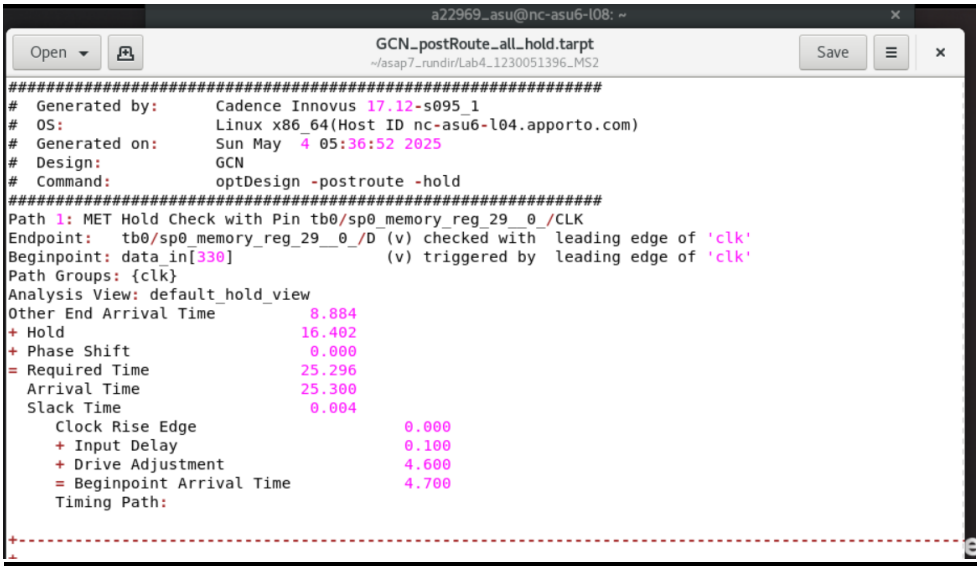
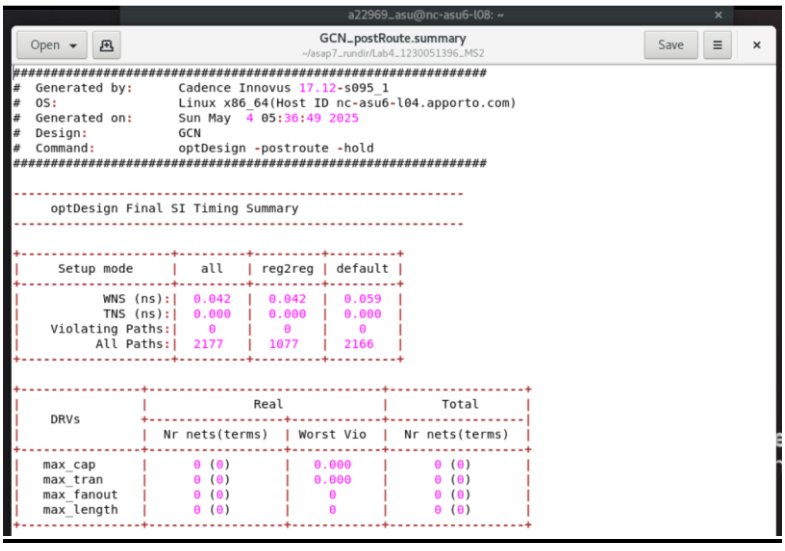
Timing Report for worstcase Setup path:



Timing Report for worstcase Hold path:



Summary Report Setup:



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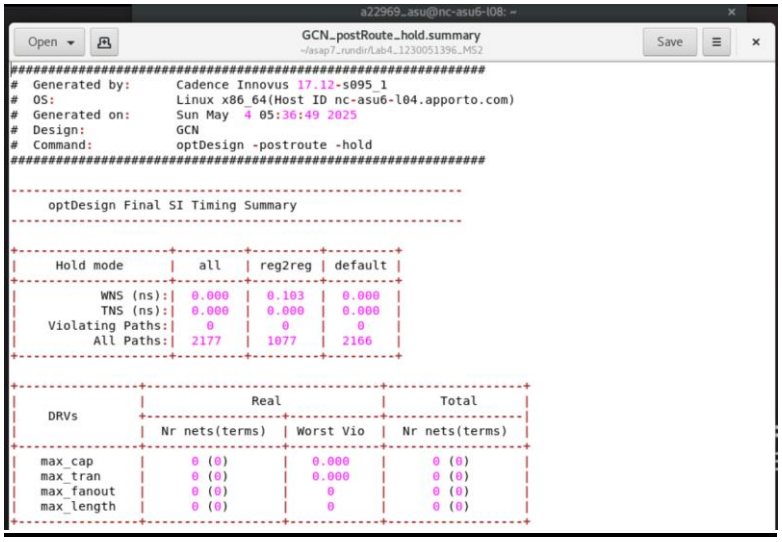
Summary Report Hold:



a22969_asu@nc-asu6-l08: ~

Open | GCN_postRoute_hold.summary ~/asap7_rundir/Lab4_1230051396_MS2 | Save

```
#################################################################
#  Generated by:      Cadence Innovus 17.12-s095_1
#  OS:                Linux x86_64(Host ID nc-asu6-l04.apporto.com)
#  Generated on:      Sun May  4 05:36:49 2025
#  Design:            GCN
#  Command:           optDesign -postroute -hold
#################################################################

------------------------------------------------------------
     optDesign Final SI Timing Summary
------------------------------------------------------------

+--------------------+--------+---------+---------+
|     Hold mode      |  all   | reg2reg | default |
+--------------------+--------+---------+---------+
|          WNS (ns):|  0.000 |  0.103  |  0.000  |
|          TNS (ns):|  0.000 |  0.000  |  0.000  |
|    Violating Paths:|    0   |    0    |    0    |
|          All Paths:|  2177  |  1077   |  2166   |
+--------------------+--------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +---------------+---------------+------------------|
|                | Nr nets(terms)|  Worst Vio    | Nr nets(terms)   |
+----------------+---------------+---------------+------------------+
|   max_cap      |      0 (0)    |    0.000      |      0 (0)       |
|   max_tran     |      0 (0)    |    0.000      |      0 (0)       |
|   max_fanout   |      0 (0)    |      0        |      0 (0)       |
|   max_length   |      0 (0)    |      0        |      0 (0)       |
+----------------+---------------+---------------+------------------+
```