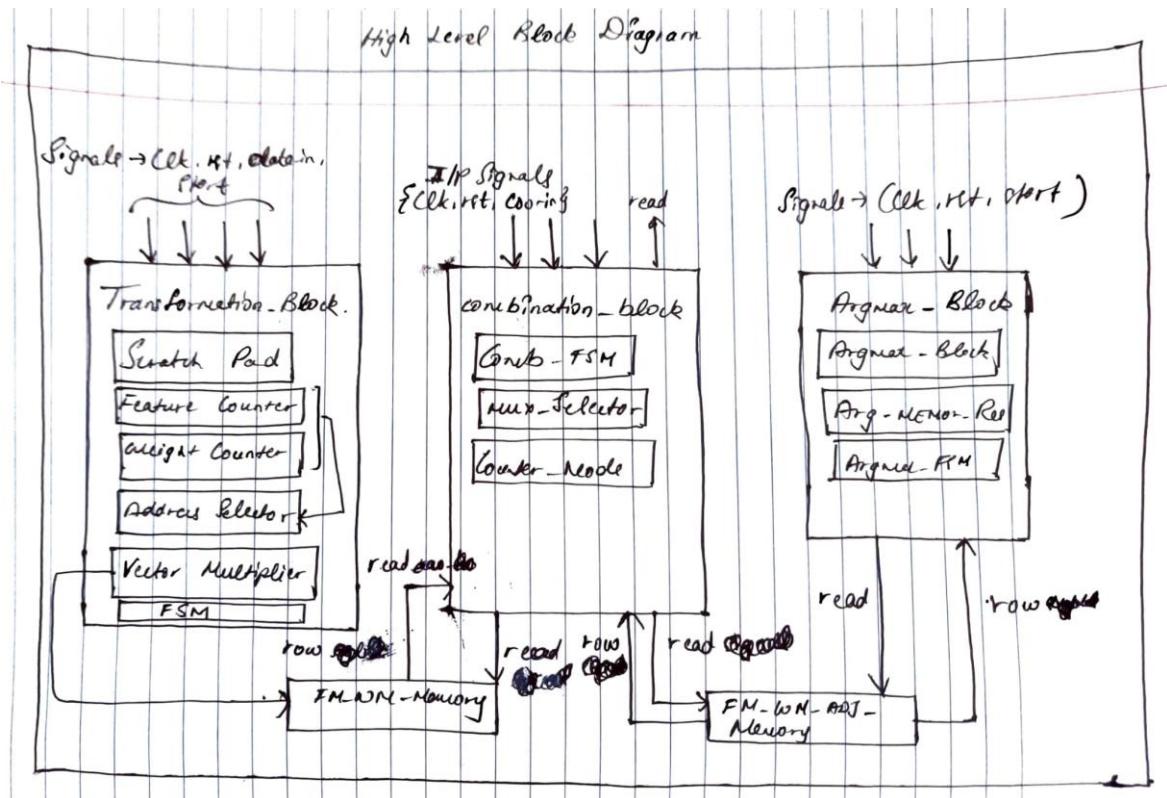


## EEE 525 LAB 4

### Milestone 2

#### 1) Architecture and high-level block diagram



#### Initial Design Considerations:

Transform block:

- Feature matrix  $\times$  Weight matrix
- Scratchpad basically stores your weight columns
- FM\_WM memory stores the result of your vector multiplication
- Control FSM – state machine orchestrates the entire design by providing control signals
- Feature counter and weight counter is there to keep track of your operation

Virtual Memory Scheme Concept:

- Where all the weights and features are stored
- Read address is connected to virtual memory or actual memory
- Address 0x0 to 0xFF – weights
- Address 0x200 to 0x2FF – features
- Should generate the correct address to read the weight column and feature row
- Whenever we give an address we get a vector and at each address we will store 96, 5-bit values

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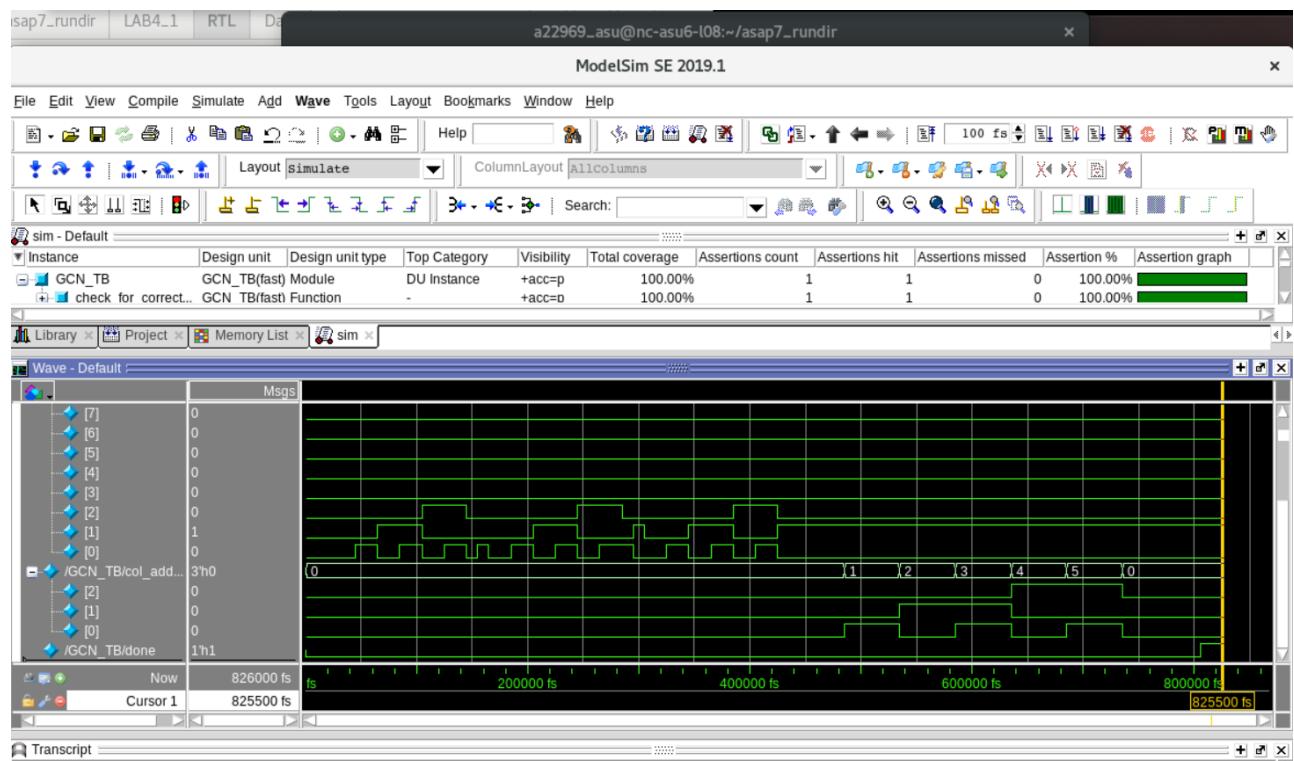
### Combination Block:

- Obtained from multiplying adj matrix with the vector product of FM and WM
- Converting from coordinate format to adjency matrix format is required to perform matrix to matrix multiplication
- We only read on coordinate column at a time
- Each column represents one edge
- We loop through entire coordinate matrix and then create the adjency matrix
- We are also given the FM\_WM\_ADJ\_ memory which stores the final output of the memory

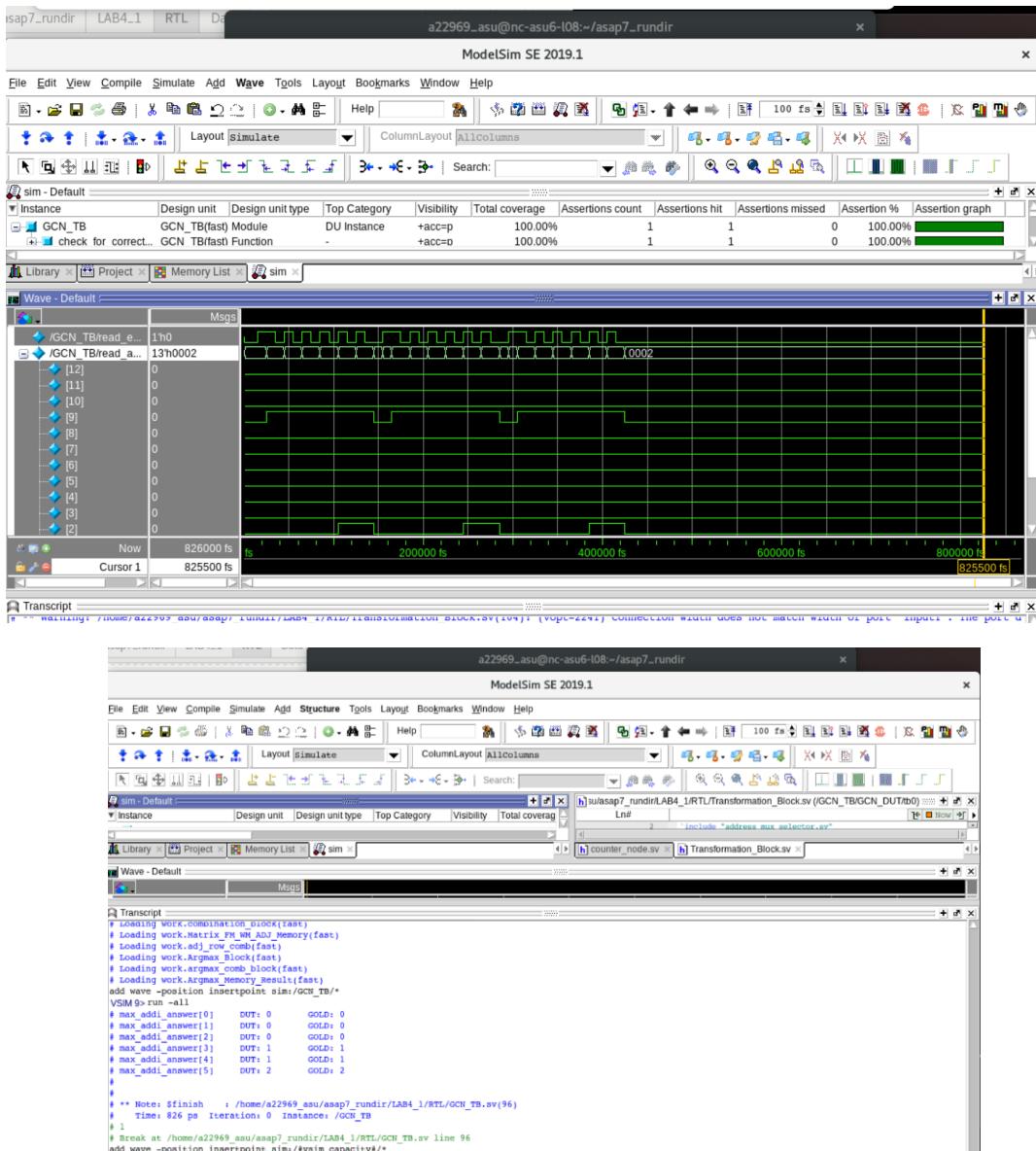
### Argmax Block:

- Argmax is used for node classification
- Once we have the result of 3 matrix multiplication from the combinational block, the classification is done by the Argmax function
- For FM\_WM\_ADJ which is a  $6 \times 3$  matrix, each column corresponds to a class and each row corresponds to one node in our graph
- For example, in node1 what is the strength of the classification for each class.
- Therefore we need to iterate through all our nodes of the adj matrix and pick the column that has the largest value
- Output will be the class that corresponds to the column we pick

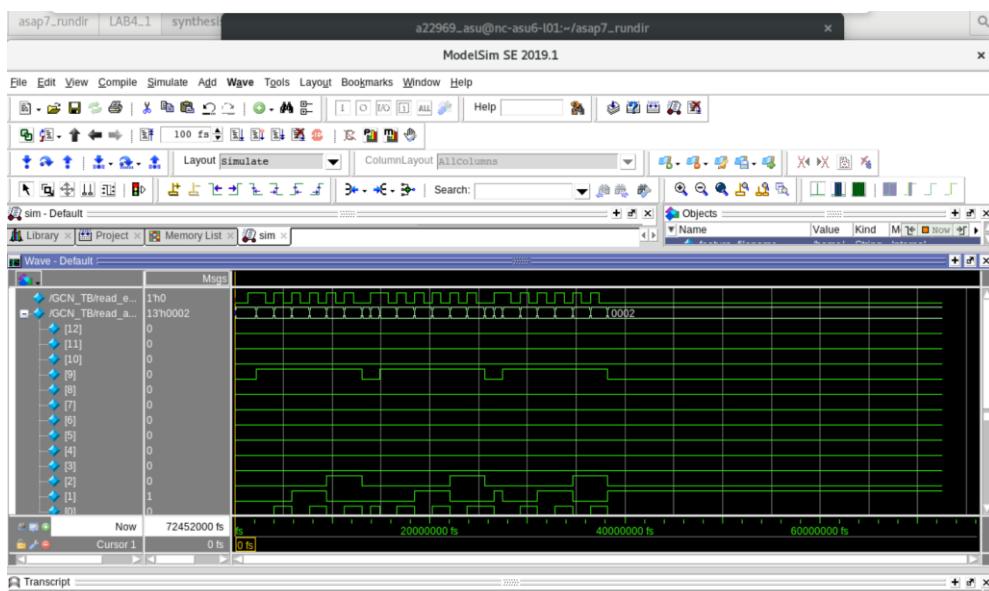
### Behavioral Verilog – Simulation:



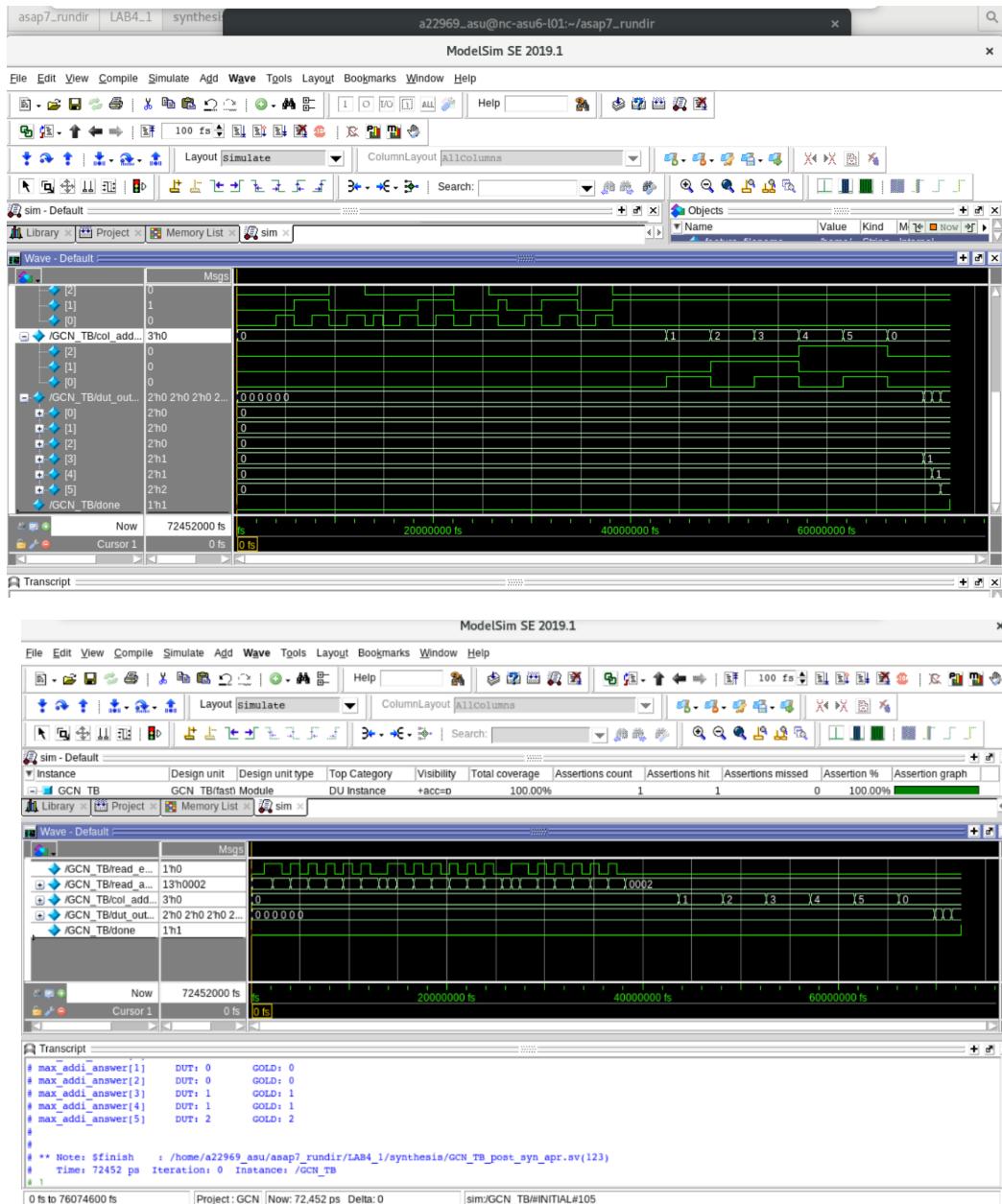
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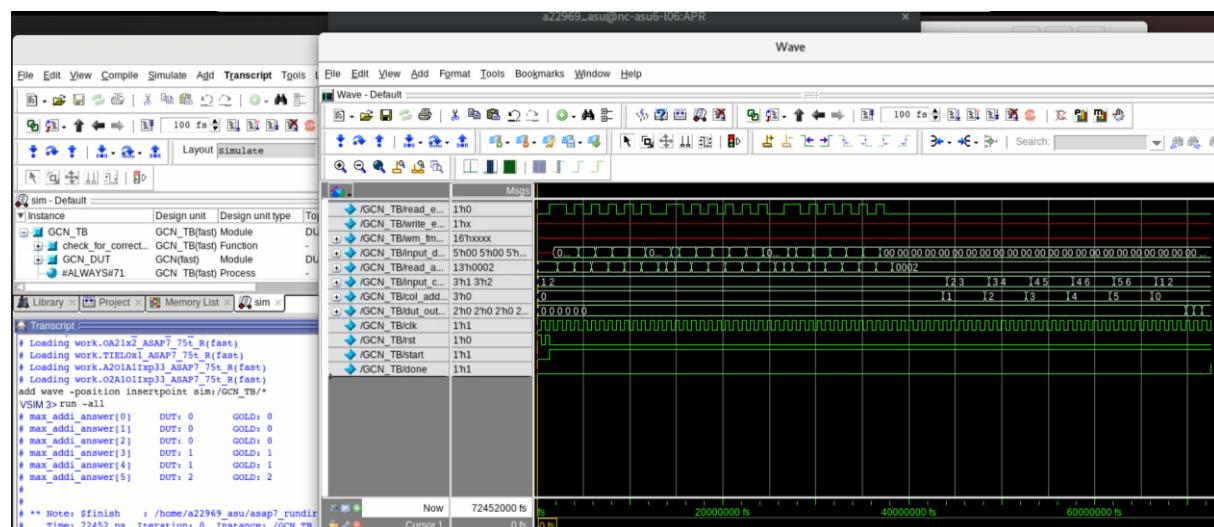
## Post Synthesis - Simulation:



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## Post APR Simulation:



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Total Latency: 72.45 ns with a clock frequency of 1111.11 MHz

Clock Period: 900 ps

### Area:

Standard Cells + Filler Cells: 0.43 mm<sup>2</sup>

```
a22969_asu@nc-asu6-l02: ~ GCN.main.htm.ascii
~/asap7_rundir/LAB4_1/APR/summaryReport

Detail Ext. Scale Factor: 1.000
Detail Ext. Scale Factor: 1.000

=====
Floorplan/Placement Information
=====
Total area of Standard cells: 43177.329 um^2
Total area of Standard cells(Subtracting Physical Cells): 26439.255 um^2
Total area of Macros: 0.000 um^2
Total area of Blockages: 0.000 um^2
Total area of Pad cells: 0.000 um^2
Total area of Core: 43177.329 um^2
Total area of Chip: 51961.928 um^2
Effective Utilization: 1.0000e+00
Number of Cell Rows: 192
% Pure Gate Density #1 (Subtracting BLOCKAGES): 100.000%
% Pure Gate Density #2 (Subtracting BLOCKAGES and Physical Cells): 61.234%
% Pure Gate Density #3 (Subtracting MACROS): 100.000%
% Pure Gate Density #4 (Subtracting MACROS and Physical Cells): 61.234%
% Pure Gate Density #5 (Subtracting MACROS and BLOCKAGES): 100.000%
% Pure Gate Density #6 (Subtracting MACROS and BLOCKAGES for insts are not placed): 61.234%
% Core Density (Counting Std Cells and MACROs): 100.000%
% Core Density #2(Subtracting Physical Cells): 61.234%
% Chip Density (Counting Std Cells and MACROs and IOs): 83.094%
% Chip Density #2(Subtracting Physical Cells): 50.882%
# Macros within 5 sites of IO pad: No
Macro halo defined?: No
```

### Power:

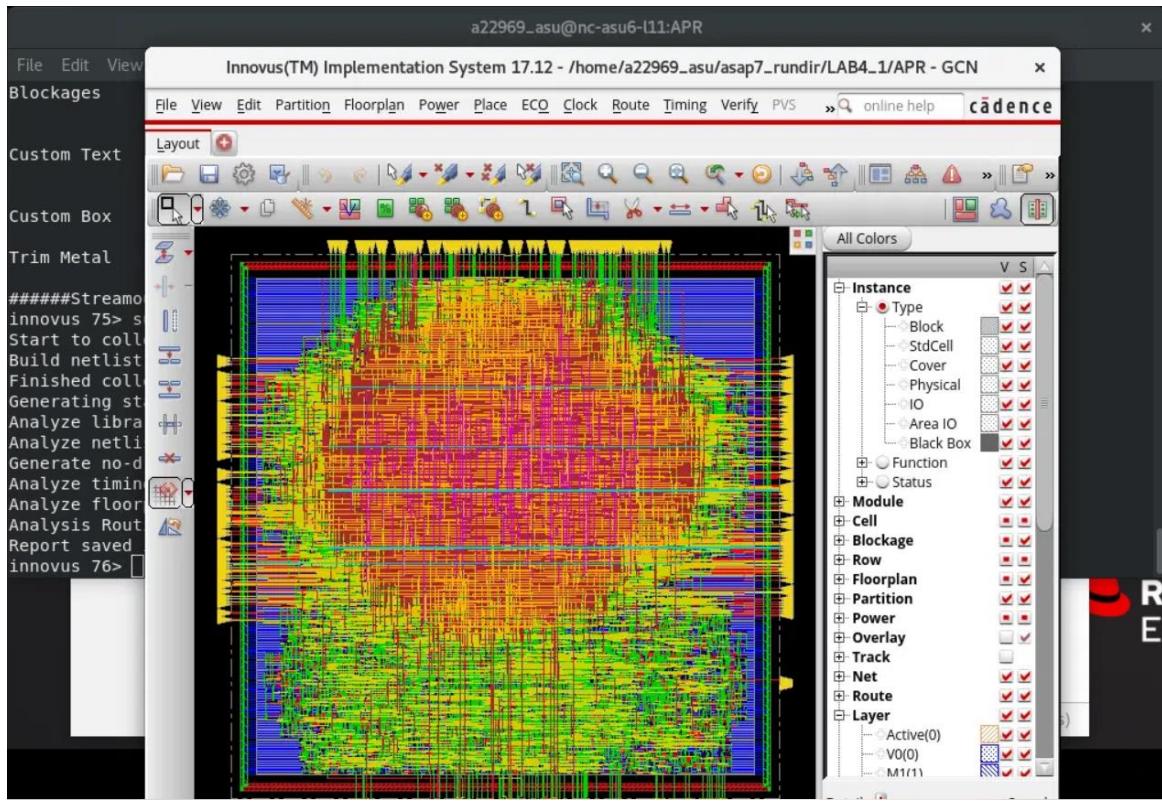
Total Power = 13.71 mW

```
a22969_asu@nc-asu6-l04:~/asap7_rundir

File Edit View Search Terminal Help
Innovus
File Ended Power Analysis: (cpu=0:00:01, real=0:00:01, mem(process/total)=1113.12MB/1113.12MB)
Layout Begin Static Power Report Generation
Total Power
-----
Total Internal Power: 4.48666207 32.7036%
Total Switching Power: 9.23116811 67.2867%
Total Leakage Power: 0.00132496 0.0097%
Total Power: 13.71915515
-----
Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,
mem(process/total)=1114.23MB/1114.23MB)
Output file is LAB4_1/APR/Power1/GCN.rpt
Floorplan
```

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### Layout – Innovus:



### Innovus Density:

```
item 17.12 - /ho a22969_asu@nc-asu6-l08:APR
GCN_postRoute.summary
~/asap7_rundir/LAB4_1/APR/timingReports
Save x

Density: 65.01%
Total number of glitch violations: 0
```

### Number of Gates:

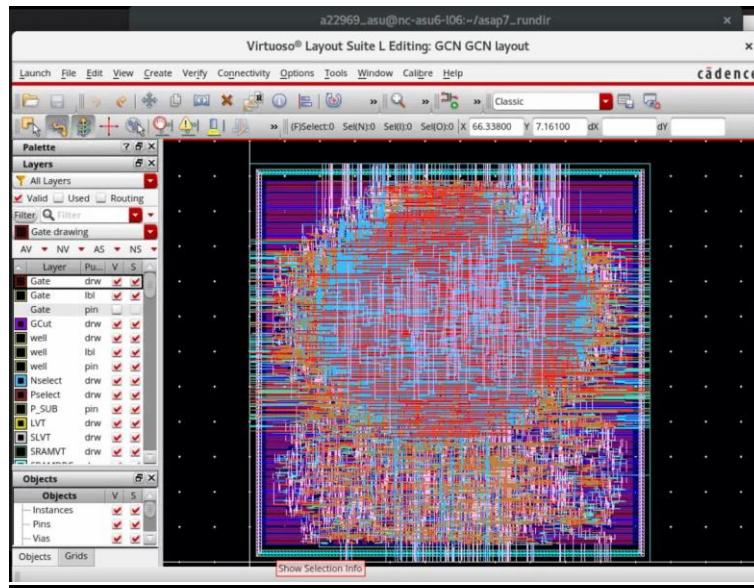
Gates = 37779

Cells = 16676

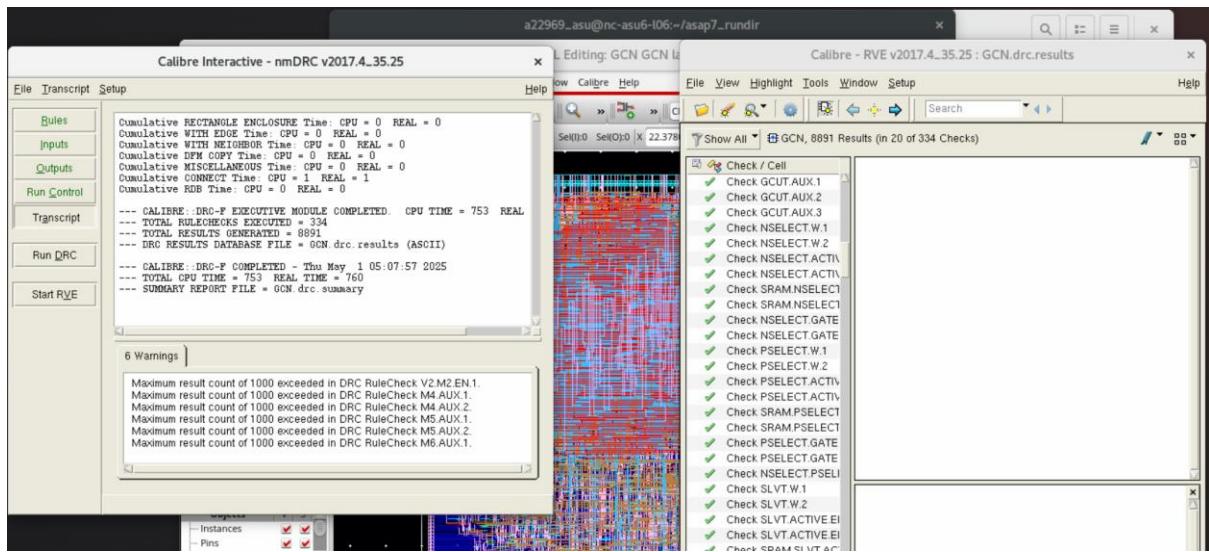
```
a22969_asu@nc-asu6-l08:APR
File Edit View Search Terminal Help
innovus 1> reportGateCount
Gate area 0.6998 um^2
[0] GCN Gates=37779 Cells=16676 Area=26439.3 um^2
innovus 2>
```

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ASU ID: 1230051396

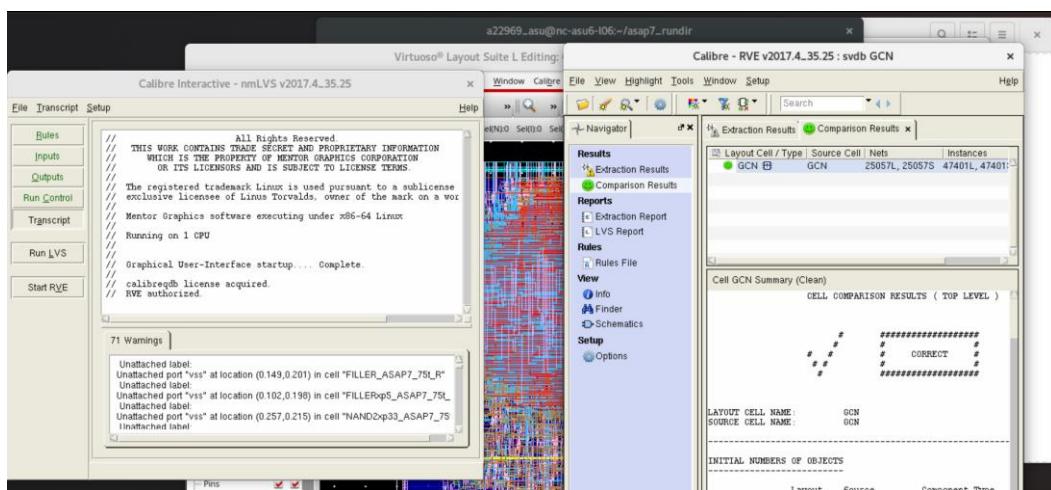
## Layout – Virtuoso:



## Post APR -DRC:



## Post APR -LVS:



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ASU ID: 1230051396

## **Timing Report for worstcase Setup path:**

```
a22969_asu@nc-asu6:~$ GCN_postRoute_all.tarp
GCN_postRoute_all.tarp
Save x
#####
# Generated by: Cadence Innovus 17.12-s095_1
# OS: Linux x86_64(Host ID nc-asu6-l04.apporto.com)
# Generated on: Sun May 4 05:36:52 2025
# Design: GCN
# Command: optDesign -postroute -hold
#####
Path 1: MET Setup Check with Pin tb0/mfwm0_mem_reg_5_2_15/_CLK
Endpoint: tb0/mfwm0_mem_reg_5_2_15/_D (v) checked with leading edge of
'clk'
Beginpoint: tb0/sp0_memory_reg_85_2/_QN (^) triggered by leading edge of
'clk'
Path Groups: {reg2reg}
Analysis View: default_setup_view
Other End Arrival Time 68.100
- Setup 4.999
+ Phase Shift 900.000
= Required Time 963.091
- Arrival Time 920.644
= Slack Time 42.447
    Clock Rise Edge 0.000
    + Drive Adjustment 7.700
    + Source Insertion Delay -77.356
    = Beginpoint Arrival Time -69.656
Timing Path:
+
```

## **Timing Report for worstcase Hold path:**

```
a22969_asu@nc-asu6-l08: ~
GCN_postRoute_all_hold.tarpt
~/asap7_rundir/Lab4_1230051396_MS2
Save x

Open
#####
# Generated by: Cadence Innovus 17.12-s095_1
# OS: Linux x86_64(Host ID nc-asu6-l04.apporto.com)
# Generated on: Sun May  4 05:36:52 2025
# Design: GCN
# Command: optDesign -postroute -hold
#####
Path 1: MET Hold Check with Pin tb0/sp0_memory_reg_29_0 /CLK
Endpoint: tb0/sp0_memory_reg_29_0/D (v) checked with leading edge of 'clk'
Beginpoint: data_in[330] (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: default_hold_view
Other End Arrival Time 8.884
+ Hold 16.402
+ Phase Shift 0.000
= Required Time 25.296
Arrival Time 25.300
Slack Time 0.004
    Clock Rise Edge 0.000
    + Input Delay 0.100
    + Drive Adjustment 4.600
    = Beginpoint Arrival Time 4.700
Timing Path:
+-----+
+
```

## **Summary Report Setup:**

Name: Samson Raj Surendra  
ASU ID: 1230051396

## Summary Report Hold:

```
a22969_asu@nc-asu6-l08: ~
GCN_postRoute_hold.summary
~/asap/_rndrlab4_1230051396.MS2

#####
# Generated by: Cadence Innovus 17.12-s095.1
# OS: Linux x86_64(Host ID nc-asu6-l04.apporto.com)
# Generated on: Sun May 4 05:36:49 2025
# Design: GCN
# Command: optDesign -postroute -hold
#####

optDesign Final SI Timing Summary

+-----+-----+-----+
| Hold mode | all | reg2reg | default |
+-----+-----+-----+
| WNS (ns): | 0.000 | 0.103 | 0.000 |
| TNS (ns): | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 2177 | 1077 | 2166 |
+-----+-----+-----+

+-----+-----+-----+
| DRVs | Real | Total |
+-----+-----+-----+
| | Nr nets(terms) | Worst Vio | Nr nets(terms) |
+-----+-----+-----+
| max_cap | 0 (0) | 0.000 | 0 (0) |
| max_tran | 0 (0) | 0.000 | 0 (0) |
| max_fanout | 0 (0) | 0 | 0 (0) |
| max_length | 0 (0) | 0 | 0 (0) |
+-----+-----+-----+
```