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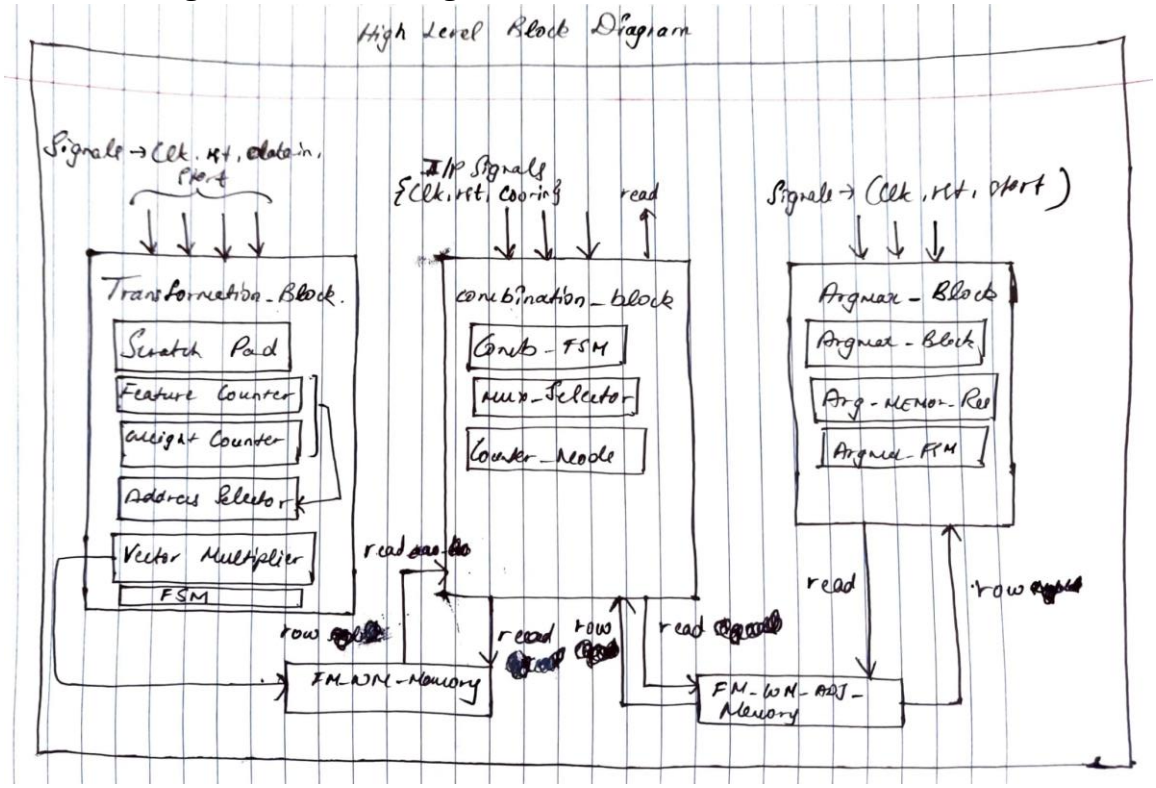
EEE 525 LAB 4
Milestone 1

Architecture and High Level Block Diagram



Initial Design Considerations:

Transform block:

- Feature matrix × Weight matrix
- Scratchpad basically stores your weight columns
- FM_WM memory stores the result of your vector multiplication
- Control FSM – state machine orchestrates the entire design by providing control signals
- Feature counter and weight counter is there is keep track of your operation

Virtual Memory Scheme Concept

- Where all the weights and features are stored
- Read address is connected to virtual memory or actual memory
- Address 0x0 to 0xFF – weights
- Address 0x200 to 0x2FF – features
- Should generate the correct address to read the weight column and feature row
- Whenever we give an address we get a vector and at each address we will store 96, 5-bit values

Combination Block

- Obtained from multiplying adj matrix with the vector product of FM and WM

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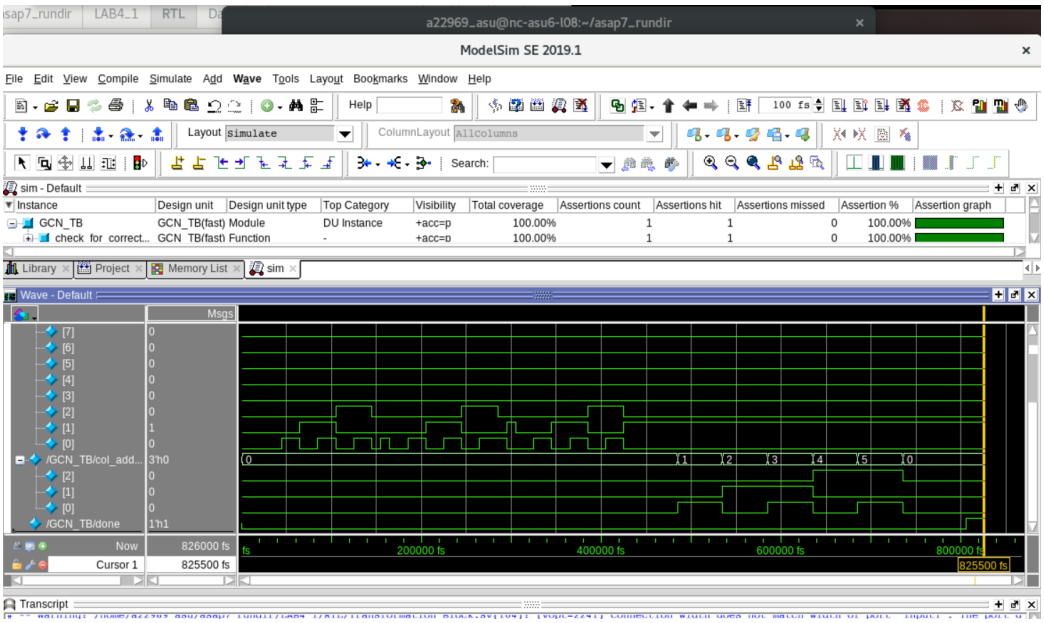
- Converting from coordinate format to adjancy matrix format is required to perform matrix to matrix multiplication
- We only read on coordinate column at a time
- Each column represents one edge
- We loop through entire coordinate matrix and then create the adjancy matrix
- We are also given the FM_WM_ADJ_ memory which stores the final output of the memory

Argmax Block

- Argmax is used for node classification
- Once we have the result of 3 matrix multiplication from the combinational block, the classification is done by the Argmax function
- For FM_WM_ADJ which is a 6 × 3 matrix, each column corresponds to a class and each row corresponds to one node in our graph
- For example, in node1what is the strength of the classification for each class.
- Therefore we need to iterate through all our nodes of the adj matrix and pick the column that has the largest value
- Output will be the class that corresponds to the column we pick

Behavioral Verilog – Simulation:



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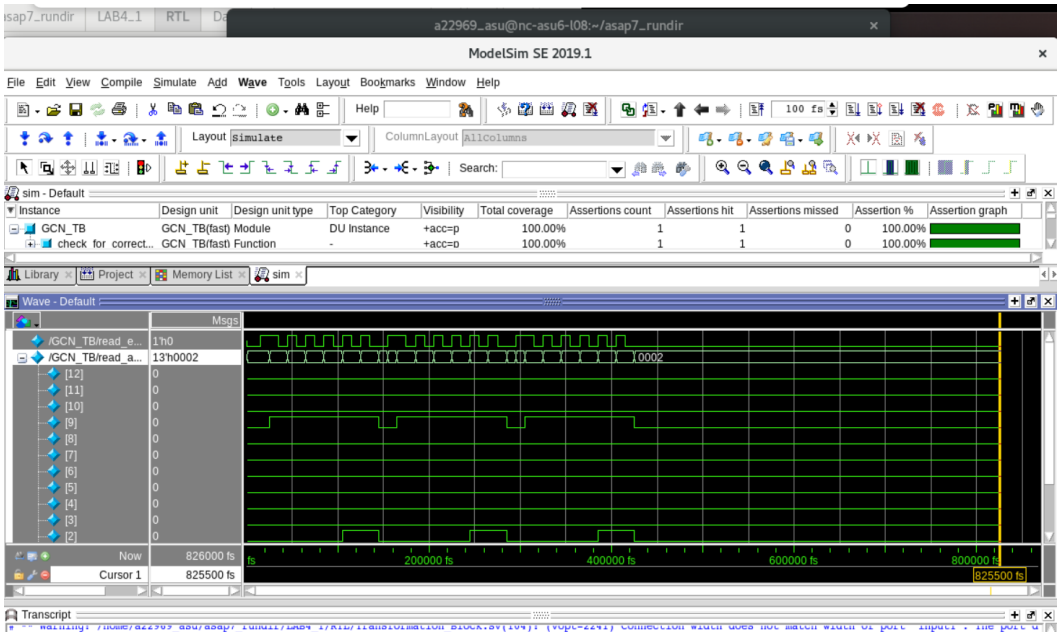
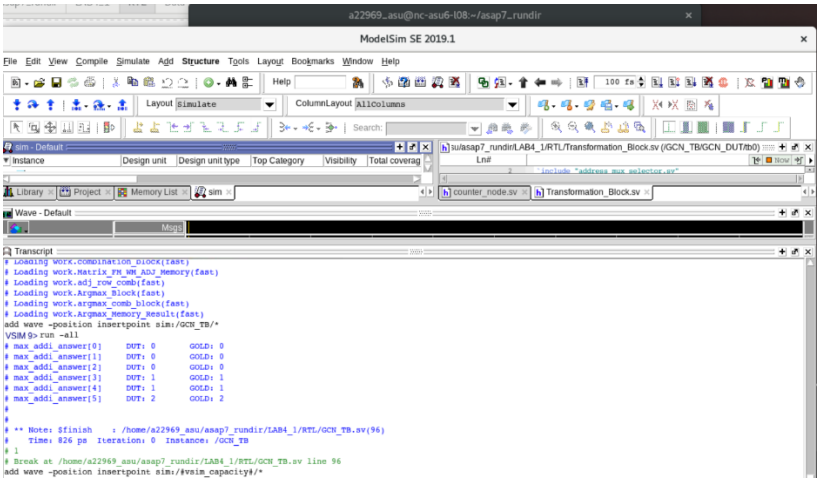
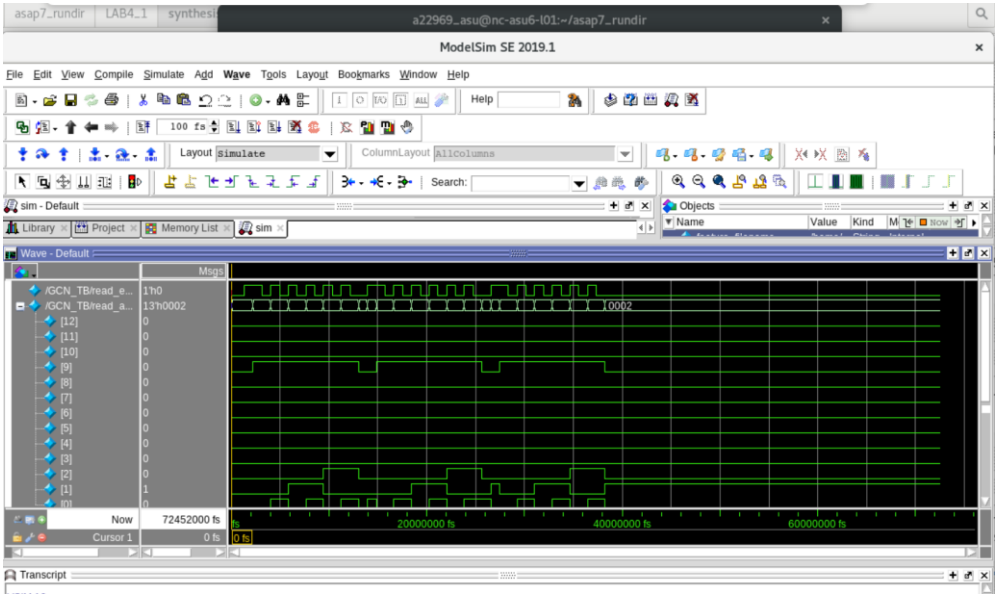




Post_Synthesis - Simulation:



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