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EEE 525 LAB 2

1. Schematic:
   a. Truth Table

Inputs		Outputs
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

   b. Schematic with visible sizing

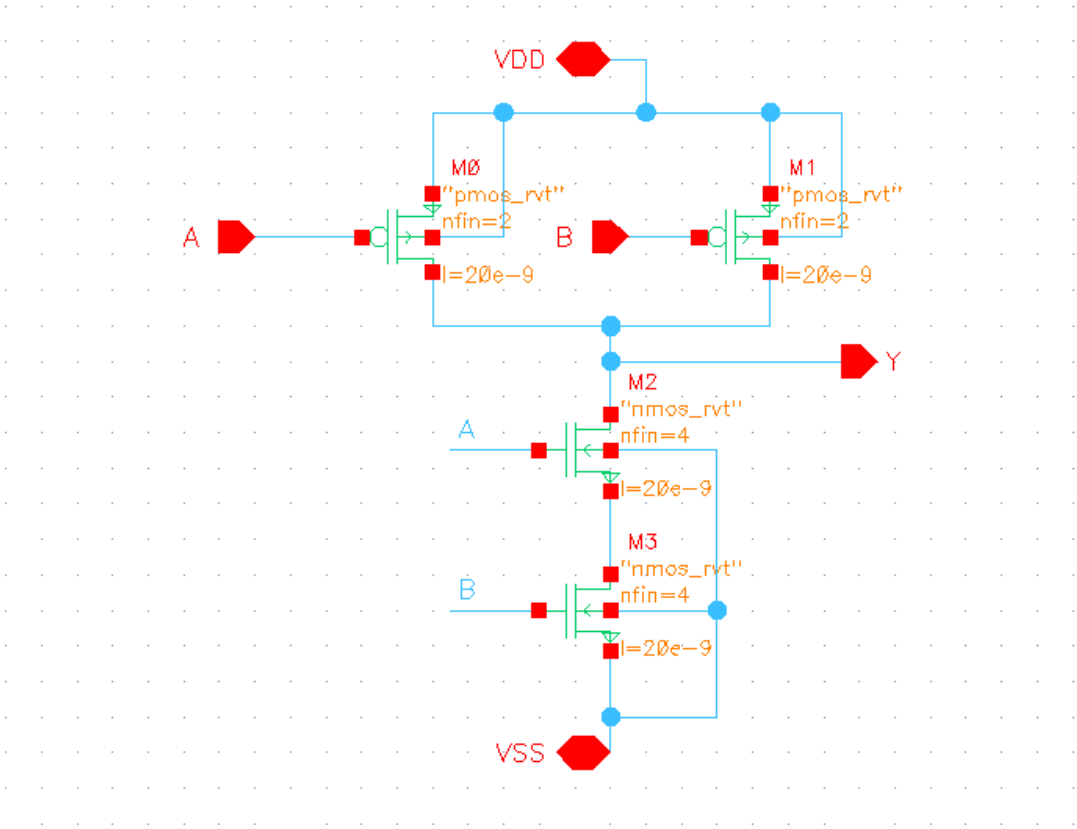

Figure 1: Schematic of NAND2xp67_ASAP7_75t_R

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c. Symbol

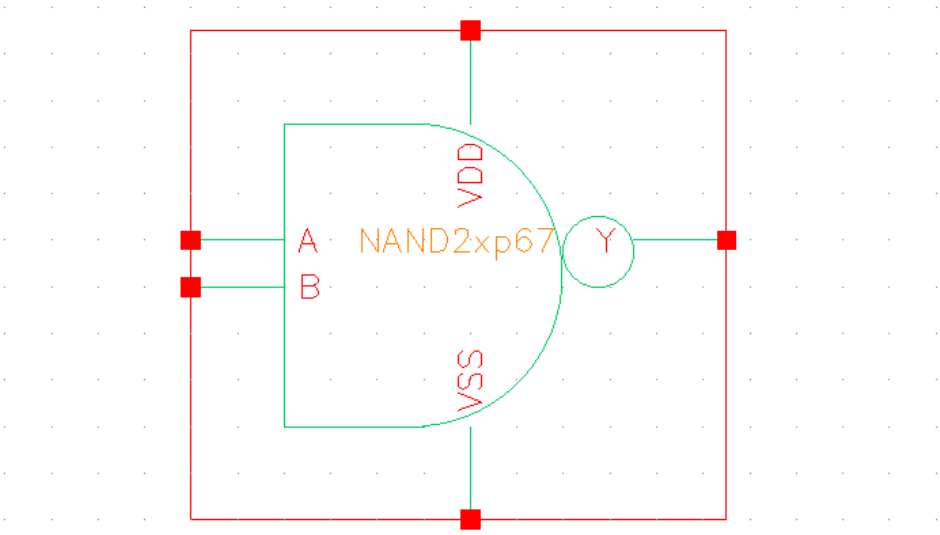

Figure 2: Symbol of NAND2xp67_ASAP7_75t_R

d. Waveform and proper functionality

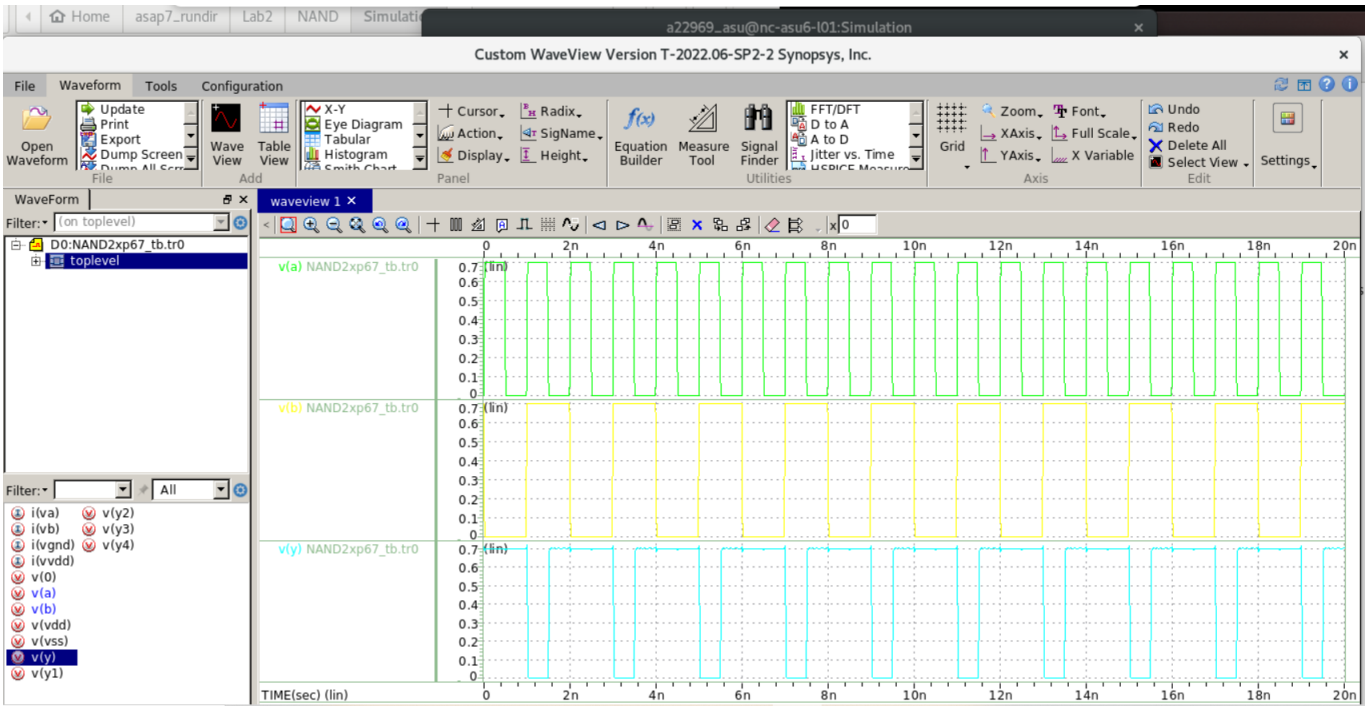

Figure 3: NAND Waveform showing functionality

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e. Testbench schematic with load

Open ~/asap7_rundir/Lab2/NAND/Simulation Save

```
.TEMP 70
.OPTION

.param pvcc=0.7
.param period1=1n
.param period2=2n
.param tr=25p
.param tf=25p
.param pw1= '(period1/2)-(tr+tf/2)'
.param pw2='(period2/2)-(tr+tf/2)'

.inc "/usr/local2/ASAP7/afs/asu.edu/class/e/e/e/eee525b/asap7/asap7PDK/models/hspice/7nm_TT.pm"

.include "NAND2xp67.sp"
.include "INVx1.sp"

X_Nand A B VDD VSS Y NAND
X_INV1 Y VDD VSS Y1 INVx1_ASAP7_75t_R
X_INV2 Y VDD VSS Y2 INVx1_ASAP7_75t_R
X_INV3 Y VDD VSS Y3 INVx1_ASAP7_75t_R
X_INV4 Y VDD VSS Y4 INVx1_ASAP7_75t_R

Vvdd VDD 0 DC=0.7
Vgnd VSS 0 DC=0

VA A 0 PULSE (0 0.7 0 tr tf pw1 period1)
VB B 0 PULSE (0.7 0 0 tr tf pw2 period2)

.TRAN 2p 20n start=0.0
.probe v(*)
.probe i(*)

.option post
.END
```

Figure 4: Testbench with Inverter Load

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2. Layout:
    a. Cell Layout Screenshot

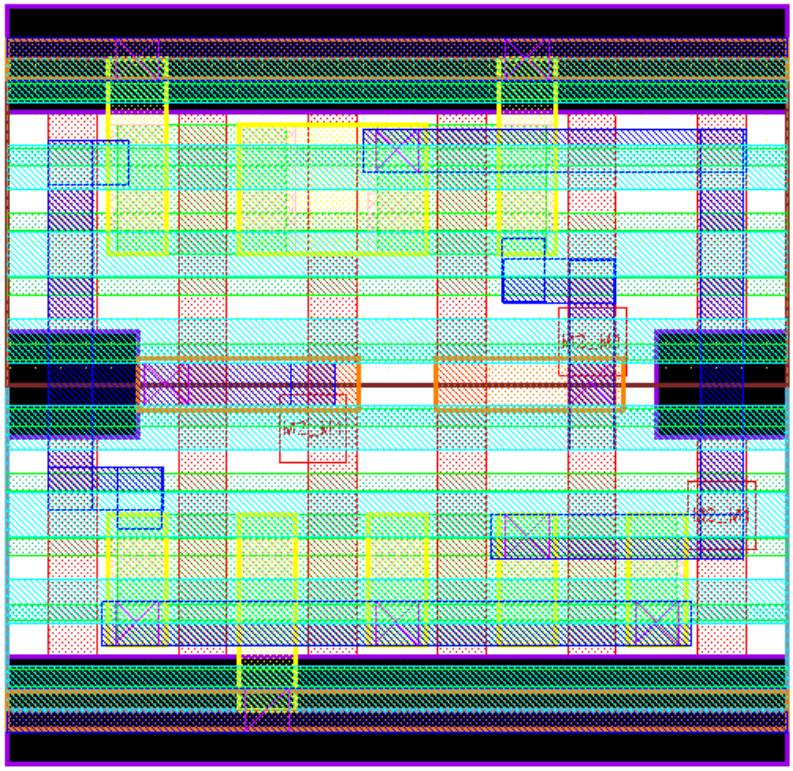

Figure 5: Layout without Tap Cell

    b. DRC and LVS screenshot

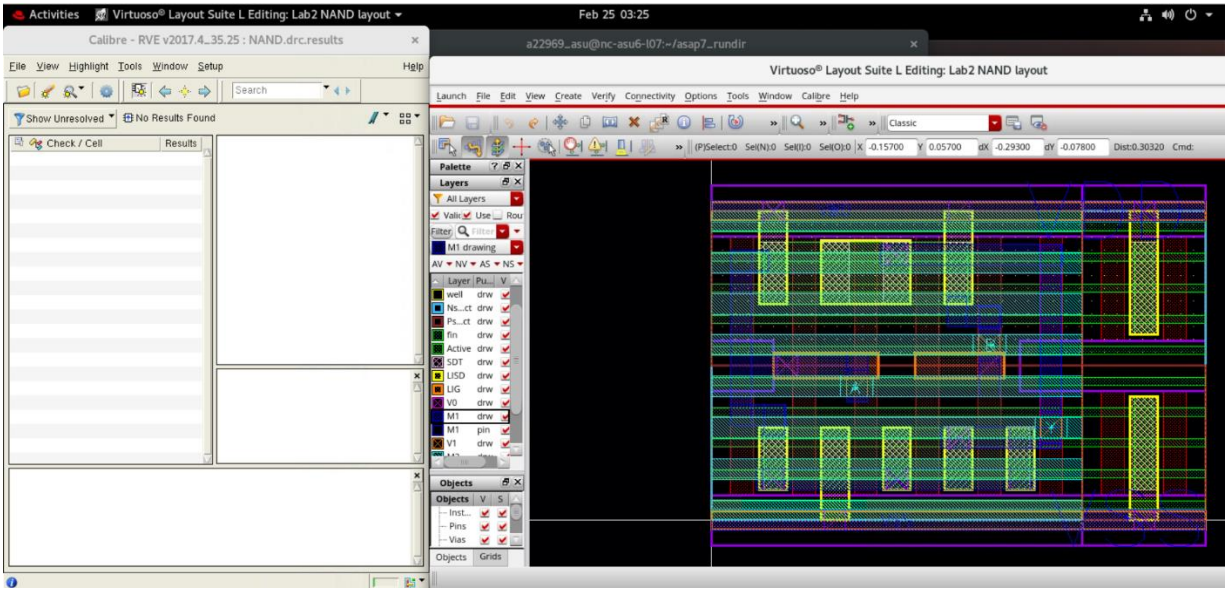

Figure 6: DRC screenshot

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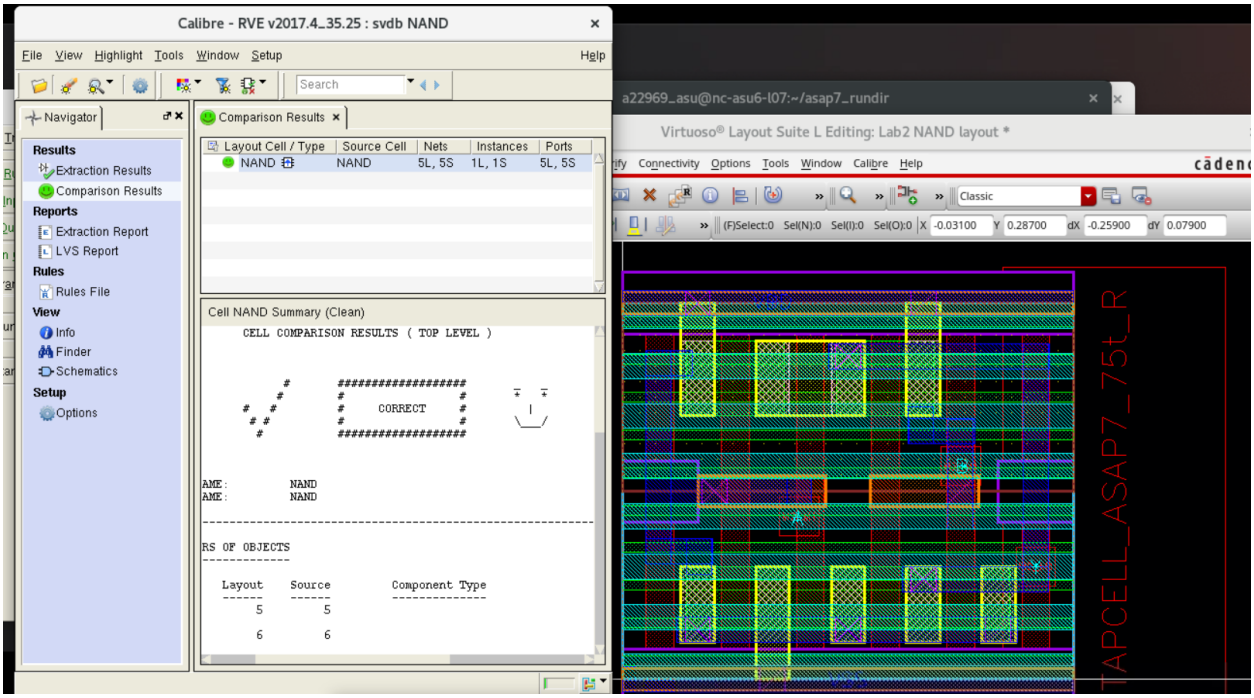

Figure 7: LVS Screenshot

c. 3x3 layout and DRC screenshot for 3x3 layout

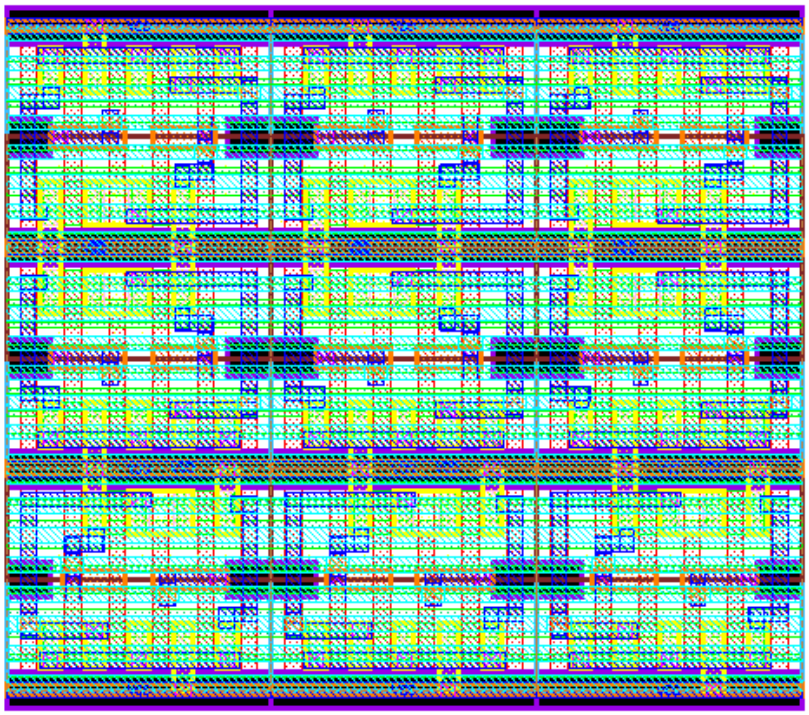

Figure 8: 3x3 Layout

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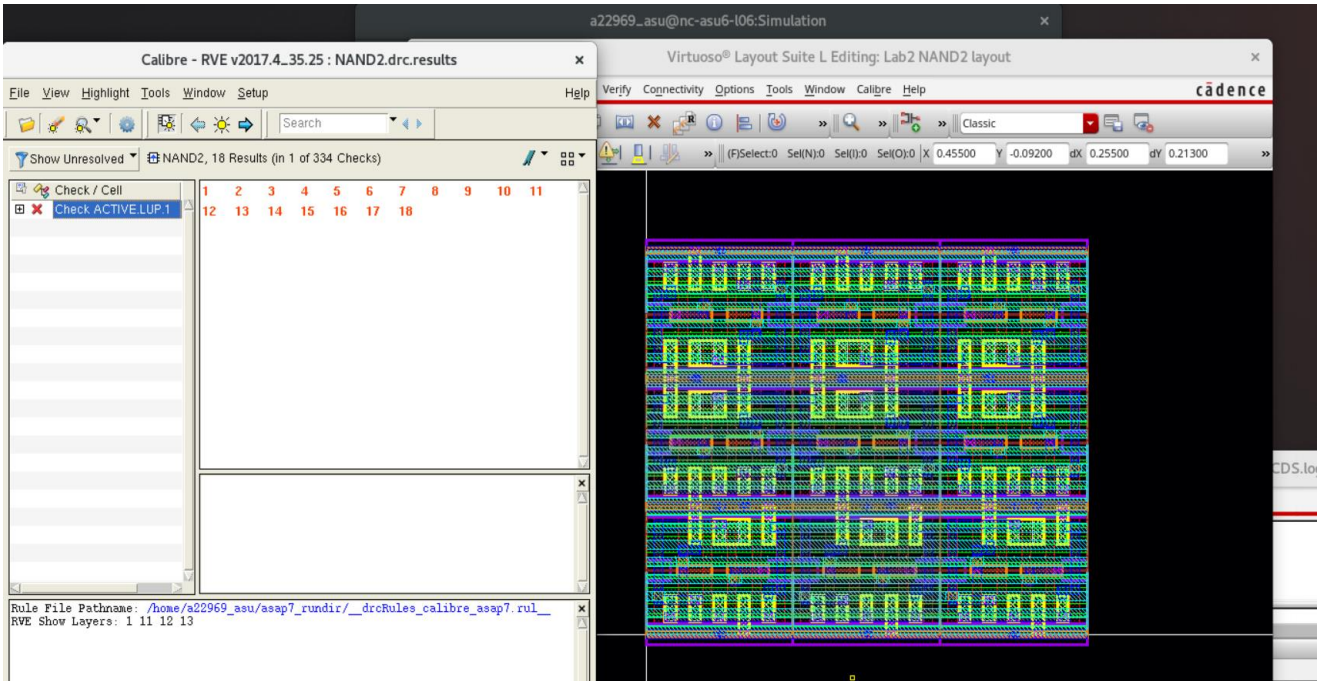

Figure 9: DRC Check for 3x3 Layout

d. Full path to your design
   Path to 2-input NAND gate
   /home/a22969_asu/asap7_rundir/Lab2/NAND
   Path to 3x3 Layout
   /home/a22969_asu/asap7_rundir/Lab2/NAND2

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3. Post Layout:
    a. Pex netlist

Open | NAND.pex.netlist | ~/asap7_rundir/Lab2/NAND/Simulation | Save

```
* Design:       NAND
* Created:      "Tue Feb 25 2025"
* Vendor:       "Mentor Graphics Corporation"
* Program:      "Calibre xACT 3D"
* Version:      "v2017.4_35.25"
* Corner Name: typical_27
* Nominal Temperature: 25C
* Circuit Temperature: 27C
*
* Integrated TICER reduction is not enabled.
* SHORT DELAY THRESHOLD: 2e-15
* Fill Mode: NG
* PEX REDUCE CC ABSOLUTE : 1
* PEX REDUCE CC RELATIVE : 0.01
* Delta transform mode : 344834

.include "NAND.pex.netlist.pex"



*
.SUBCKT NAND VDD A VSS B Y
*
* VDD VDD
* A A
* VSS VSS
* B B
* Y Y
*
*

MM3 N_MM3_d N_MM3_g N_MM3_s N_MM2@2_b nmos_rvt L=2e-08 W=5.4e-08 nfin=2
MM3@2 N_MM3@2_d N_MM3@2_g N_MM3@2_s N_MM2@2_b nmos_rvt L=2e-08 W=5.4e-08 nfin=2
MM2 N_MM2_d N_MM2_g N_MM2_s N_MM2@2_b nmos_rvt L=2e-08 W=5.4e-08 nfin=2
MM2@2 N_MM2@2_d N_MM2@2_g N_MM2@2_s N_MM2@2_b nmos_rvt L=2e-08 W=5.4e-08 nfin=2
MM0 N_MM0_d N_MM0_g N_MM0_s N_MM1_b pmos_rvt L=2e-08 W=5.4e-08 nfin=2
MM1 N_MM1_d N_MM1_g N_MM1_s N_MM1_b pmos_rvt L=2e-08 W=5.4e-08 nfin=2


.include "NAND.pex.netlist.pxi"
.ENDS
*
```

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b. Waveform and proper functionality with brief explanation

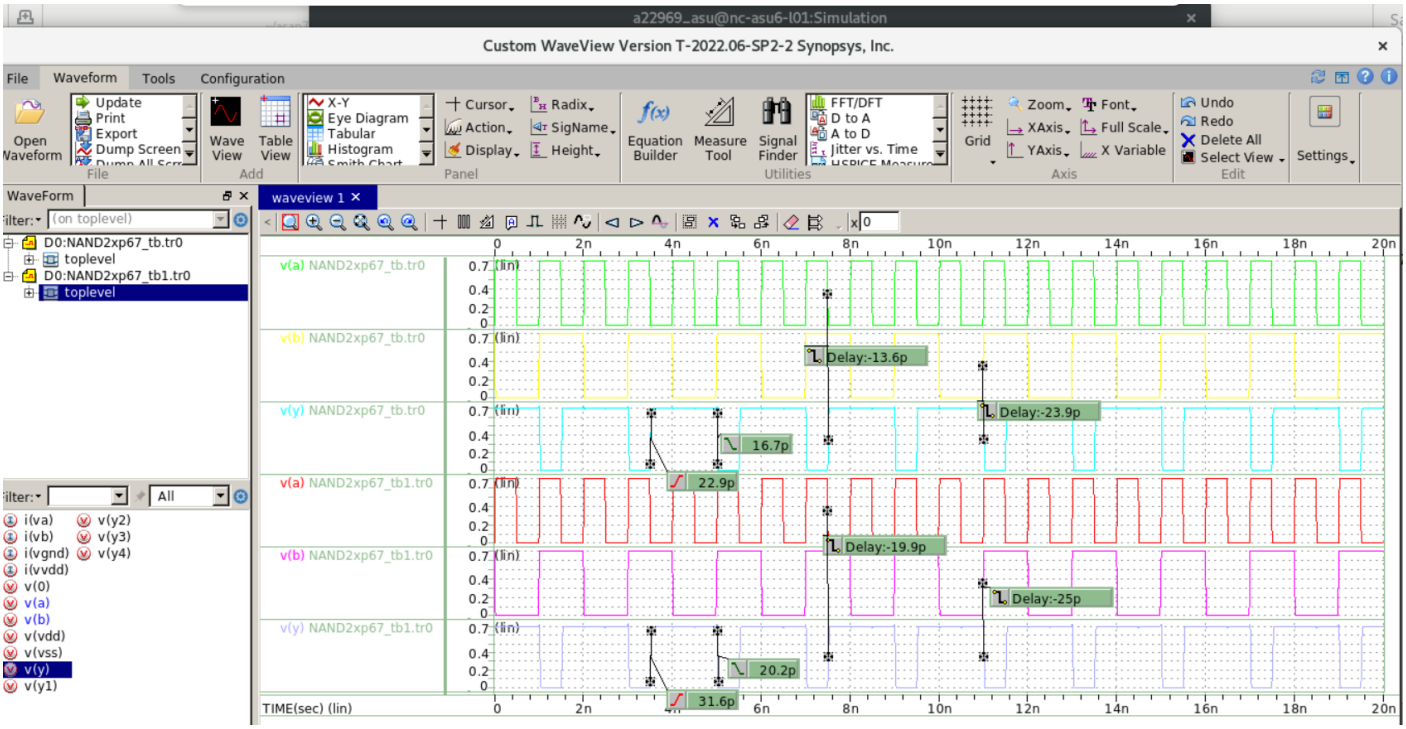

Figure 10: Waveform showing the comparison in delay and rise and fall times between pre-layout and post-layout

Note:

- From the figure above, we can see that both rise and fall times increase when moving from pre-layout to post-layout. The rise time increases from 22.9 ps to 31.6 ps, while the fall time goes from 16.7 ps to 20.2 ps.
- A similar trend is observed in delay comparisons. The delay increases from 13.6 ps to 19.9 ps (for signal 'a' to 'y') and from 23.9 ps to 25 ps.
- This happens because the pre-layout (schematic) simulation assumes ideal conditions, whereas the post-layout simulation accounts for non-idealities, including extracted parasitic resistance (R) and capacitance (C) values.