EEE 598 - Co-Design and Modelling for Advanced Semiconductor Packaging

Impact of Underfill Properties on Solder Joint Reliability

Research Question:

How do underfill mechanical properties (CTE and modulus) affect solder joint stress distribution and fatigue life under thermal cycling?

Team Members:
Archana Raj, Samson Raj, Nishchal Gowda , Pratham Panwar

Arizona State University

Methodology:
1: Thermal Modeling With & Without Underfill

Objective: Evaluate the thermal response of the package and quantify temperature distribution differences introduced by underfill.

Steps:

Geometry Creation:

Built a simplified 3D package cross-section in ANSYS Mechanical including silicon die, substrate, bumps, and optional underfill.

Material Assignment:

Assigned realistic thermal/elastic material properties (silicon, substrate, solder, and underfill).

Boundary Conditions:

Applied thermal cycling temperatures based on typical JEDEC profiles.

Simulation Cases:

Case A: Model with underfill

Case B: Model without underfill

Thermal Simulation:

Solved for temperature fields to observe how underfill improved heat spreading or altered temperature gradients.

Methodology:

2. Structural Stress Modeling of Solder Balls With and Without Underfill

Objective: Quantify stress and strain variations in solder joints when underfill is present versus absent.

Steps:

- **Detailed Ball Grid Array (BGA) Model:**
  - Constructed a fine-meshed model of solder balls between die and substrate.
- **Underfill Variation:**
  - Created **two sets** of models:
    - **With underfill**
    - **Without underfill**
- **Thermo-Mechanical Coupling:**
  - Mapped temperature loads from the thermal simulation onto the structural model.
- **Stress Analysis:**
  - Solved for:
    - Von Mises stress distribution
    - Plastic strain accumulation
    - Maximum principal stress at critical solder locations
- **Parametric Observation:**
  - Recorded stress levels under thermal cycling for:
    - Solder-only (no underfill)
    - Solder + underfill

Relevance to Semiconductor Packaging:

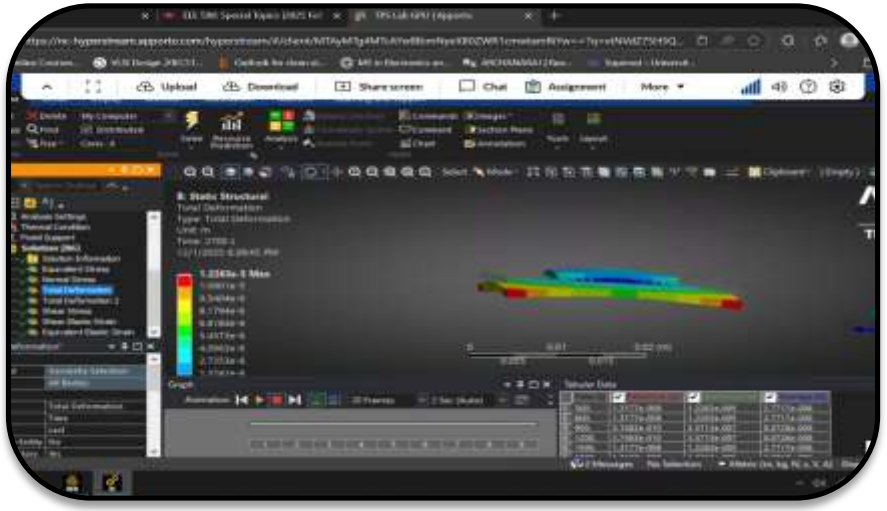
Why This Work Is Important for Packaging?

- Underfill is a *critical reliability enhancer* in flip-chip and advanced BGA packages.
- It reduces CTE mismatch between silicon and substrate, lowering mechanical stress.
- Understanding underfill behavior helps:
  - Predict solder joint fatigue earlier in design
  - Improve package lifetime and reliability
  - Guide material selection in real manufacturing
- High-density packages (chiplets, 2.5D, 3DIC) rely heavily on optimized underfill.

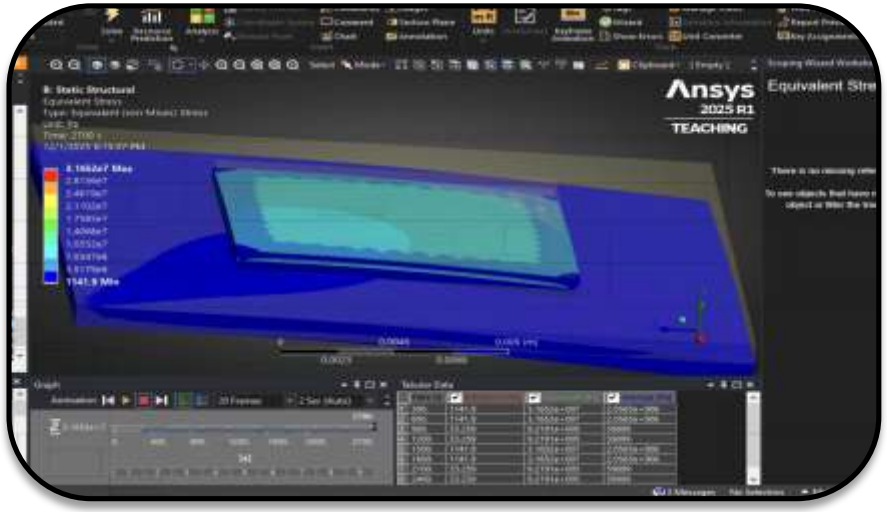
Direct Packaging Impact

- Reduces bump cracking and delamination
- Improves thermal distribution
- Enables reliable high-performance electronic systems

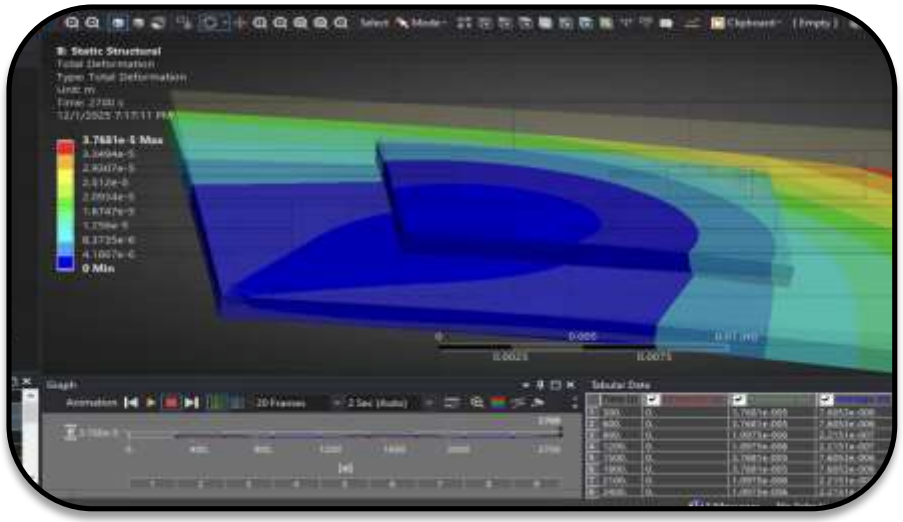
Results:



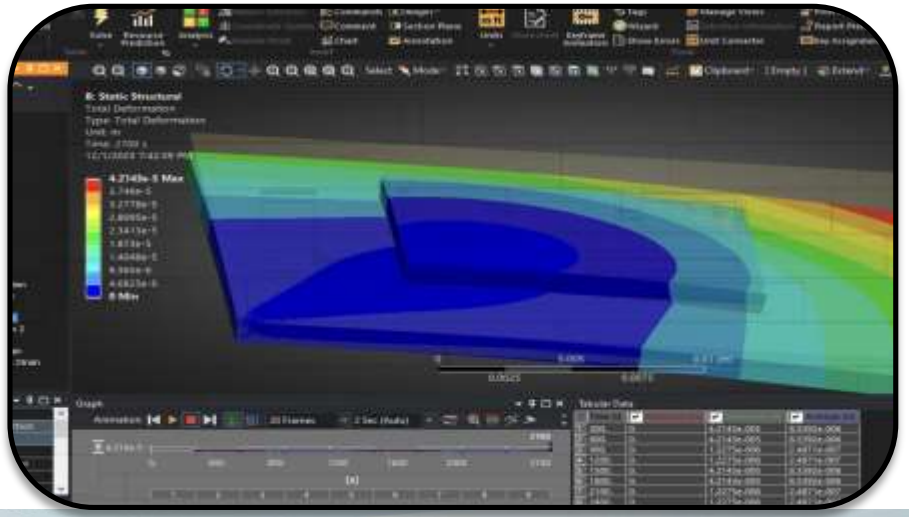
With Underfill



Without underfill



Without underfill
(best case)



Without underfill
(worst case)