# FULL ADDER IMPLEMENTATION USING DCVSL

S S V Mridula
*Pre-Final Year ECE Undergrad,*
*Vellore Institute of Technology Chennai Campus,*
*mridula.ssv2023@vitstudent.ac.in*

GitHub Repository ReadMe file

## Objective:

The objective of this project is to design and implement a 1-bit full adder using Differential Cascode Voltage Switch Logic (DCVSL) to achieve high-speed, low-power, and area-efficient operation suitable for VLSI arithmetic circuits. The project aims to demonstrate how DCVSL effectively provides both true and complementary outputs with minimal static power dissipation, improving overall circuit performance compared to conventional CMOS logic. Using open-source tools such as eSim and Ngspice, the design is simulated and analysed to validate its efficiency in terms of speed, power, and transistor count, aligning with modern low-power digital system design objectives.

## Circuit Schematic:

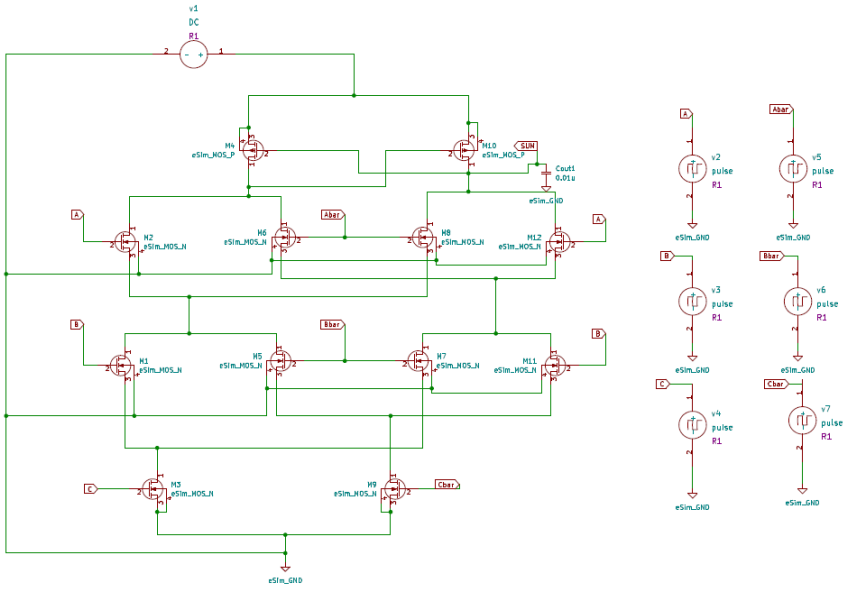


Fig 1: DCVSL SUM circuit implemented in eSim

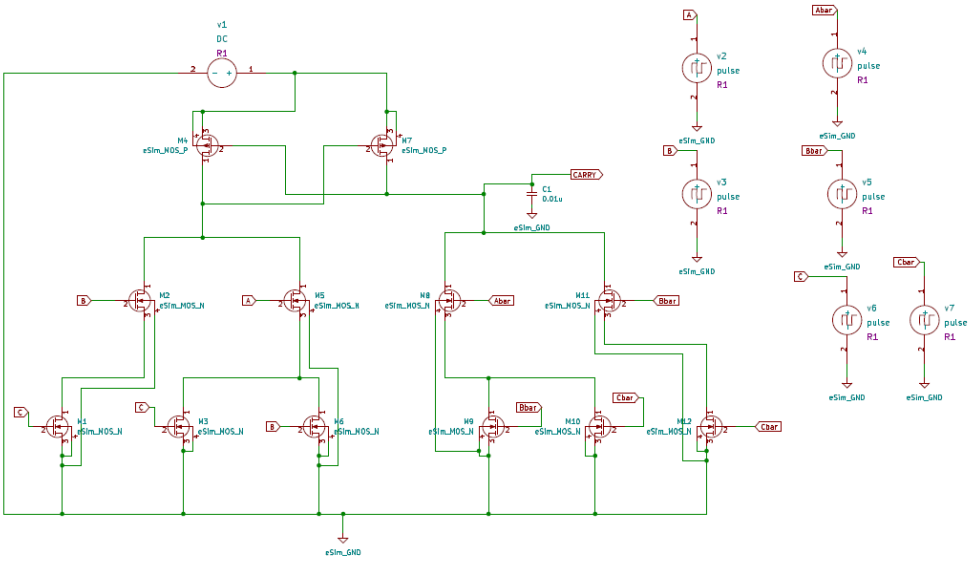


Fig 2: DCVSL CARRY circuit implemented in eSim

Additionally, a CMOS inverter subcircuit was designed and integrated in eSim to generate the complementary input signals $\overline{A}$, $\overline{B}$, and $\overline{C}$ required for the DCVSL-based full adder implementation. A load capacitance of 0.01 µF was incorporated at the output nodes of the CMOS circuits to accurately emulate the effects of parasitic capacitances and fan-out loading commonly present in practical VLSI designs. This inclusion enables a more realistic evaluation of circuit performance parameters such as propagation delay, dynamic power consumption, and output waveform integrity during switching transitions, thereby enhancing the accuracy and reliability of the simulation results.

## Simulation Results and Expected Output:

The simulation was performed using the default eSim 180 nm PMOS and NMOS models. Although the IHP-SG13G2 PDK can be included by modifying the .cir.out file generated after converting the KiCad schematic to an Ngspice file, this integration could not be successfully implemented in the current setup. The pulse voltage sources for input signals (A, B, C and their complements) were defined in the .cir.out file, and the circuit was simulated with a 1.8 V supply over a transient analysis period of 85 ms with a 10 ms step size to analyse timing and switching performance.

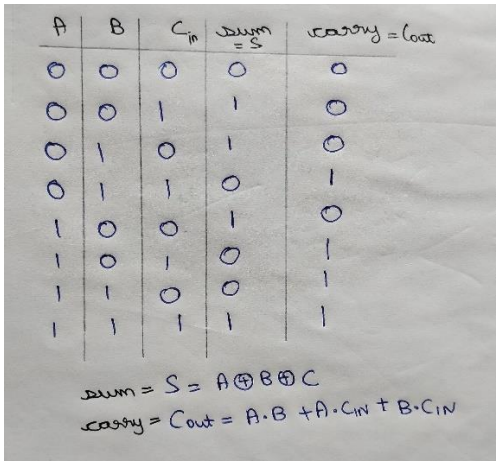


Fig 3: Truth Table of Full Adder

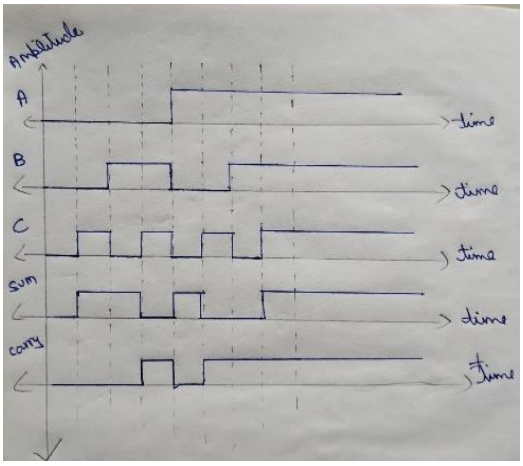


Fig 4: Expected Circuit Waveform

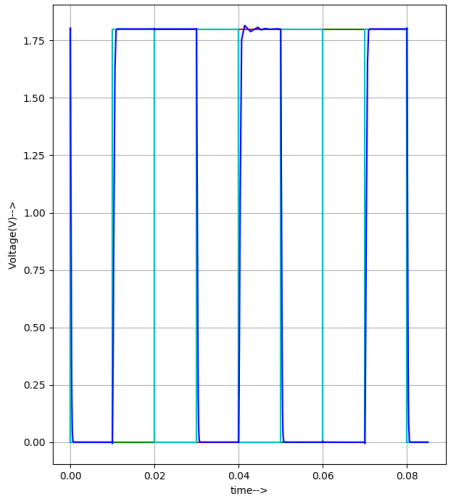


Fig 5: Output for SUM (Blue is the sum)

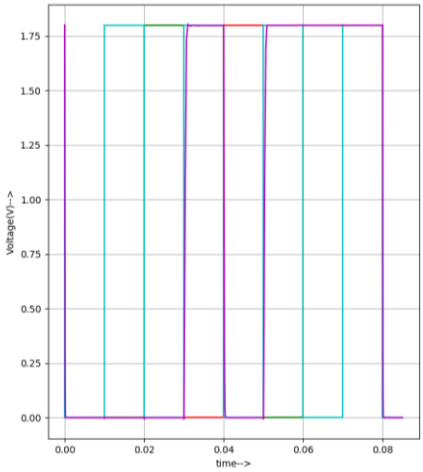


Fig 6: Output for CARRY (Pink is the sum)

The simulation output waveform obtained from eSim accurately matches the truth table of the 1-bit full adder, confirming the correct logical functionality of the designed DCVSL-based circuit. The generated sum and carry outputs followed the expected transitions for all input combinations, validating the design's accuracy and stable switching behaviour.

## Conclusion:

The 1-bit full adder using DCVSL was designed and simulated using eSim and Ngspice. While the installation and setup took some time to complete, the software provided a reliable environment for circuit design and verification. However, the integration of the IHP-SG13G2 PDK into eSim could not be successfully achieved, even after multiple attempts on a Linux system. Despite this limitation, the default 180 nm PMOS and NMOS models were effectively used, and the overall project provided valuable practical experience in circuit simulation and logic design.