01/02/2023

Open Loop Forward Converter Design

Converter Design Group Report

Jed Gawan, Hongyu YAN, Jasleen Kaur, Pengyuan SHU
DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING,
UNIVERSITY OF NOTTINGHAM

Table of Contents

1. Introduction

The main aim for the project is to design a fully controlled two switches forward converter that outputs and regulates a desired voltage. From a 230V, 50Hz AC supply, the voltage must be stepped down to 30V, 50Hz using a XFMR gate drive transformer, from which a Switch Mode Power Supply (SMPS) Forward Converter produces a regulated output. This report focuses on the development of a open loop converter. It covers the development of two main sections of the Switch Mode Power Supply (SMPS) Forward Converter: the open loop two switch forward converter and the MOSFET gate drive.

This report presents the design and simulation of a forward converter, under both ideal and non-ideal conditions. The initial calculations involved determining the necessary component values, duty cycle, and switching frequency. This in turn allowed for the calculations of important factors such as the turn ratio, output inductors, and capacitors. Values that could not be estimated directly, including the capacitors' Equivalent Series Resistance (ESR), winding numbers, and equivalent resistance, were then considered. Following these calculations, simulations of the converter were carried out under different conditions. Exploring both ideal conditions and non-ideal components, along with the effect of an AC-derived input.

The report then delves into the MOSFET Gate Drive circuit, which is crucial for providing electrical isolation between the control circuits (with low voltage and power levels) and the power MOSFETs (with high voltages and powers). The operation of the gate drive and the role of each component, such as coupling capacitors, Zener diodes, and resistors, are explored, along with their effects on the signal and the converter. The report concludes with the resultant output and a summary.

2. Calculations for the Forward Converter

2.1. Calculations in ideal conditions

Given values:

Power rating (P_{max})	50W
Input Voltage for basic testing	35Vdc
Input voltage AC (Step Down XFMR)	230Vac @ 50Hz- (30Vac isolated)
Output voltage	8Vdc
Output voltage ripple (peak to peak)	<0.1V
Load resistance at discontinuous output current threshold	R=Resistance for 15% P_{max}
Switching Frequency	75 – 105kHz

Figure 1. Specification for the forward converter

Duty cycle:

For the converter design, the duty cycle should be limited under 50% to avoid saturation of the transformer core. Thus, duty cycle has been chosen to be 30% to provide a wider range to control the output voltage.

Turns ratio:

$$V_0 = \left(\frac{N_1}{N_2}\right) dV_s \qquad \textit{Equation.1}$$

$$\frac{N_2}{N_1} = \frac{V_0}{d \cdot V_s} = \frac{8V}{0.3 \cdot 35V} = \frac{16}{21} \qquad \textit{Equation.2}$$

Switching Frequency:

From the range within the **Figure 1**, the switching frequency was selected to be 100kHz. Given the duty cycle, a higher frequency can maintain the same average output voltage whilst simultaneously reducing peak currents, output ripple and improving overall efficiency.

Output filter inductor:

Use minimum load condition to get ΔI_L:

$$I_{RMS} = \frac{P}{V} = \frac{50W \times 0.15}{8V} = 0.9375A \qquad \textit{Equation.3}$$

$$\Delta I_L = I_{peak} = \sqrt{3} I_{RMS} = 1.6238A \qquad \textit{Equation.4}$$

Voltage time area equation to find the inductance:

$$L = \frac{VTA}{\Delta I_L} = \frac{VTA}{I_{peak}} = \frac{V_0(1-d)\cdot T_{sw}}{I_{peak}} = \frac{8V \cdot 0.7 \cdot 1/100kHz}{1.6238A} = 34.487\mu H \qquad \textit{Equation.5}$$

Output filter capacitor:

Use current time area equation to find the capacitance:

$$C_0 = \frac{ITA}{\Delta V_0} = \frac{I_{RMS} \cdot \frac{T_{sw}}{2} \cdot \frac{1}{2}}{\Delta V_0} = \frac{0.9375A \cdot 5\mu s \cdot 0.5}{0.1V} = 23.4375\mu F \qquad \textit{Equation.6}$$

2.2. Calculations for non-ideal components

In terms of simulation with non-ideal components, the ESR (equivalent serial resistance) of capacitors, the DCR (DC resistance) of inductors, the resistance and forward bias voltage of diodes, the on-resistance of MOSFET, and the losses on the transformer should all be reflected on the schematic. Among all the component values, most could be found on the datasheet of their own, including the forward bias voltage of diodes, on-resistance of MOSFET, etc. The following part of this section presents the methods to calculate or estimate the equivalent component values which could not be found on the datasheet directly.

Capacitor ESR Calculation:

The capacitor ESR is dependent to the capacitance and the power dissipation factor which could be found in the datasheet.

Dissipation Factor (120Hz @ 25°C) (tan δ)	Add 0.02 per 1000µF for more than 1000µF						
	Working Voltage	10	16	25	35	63	100
	tan δ	0.2	0.17	0.15	0.12	0.1	0.08

Figure 2. Dissipation factors with different working voltages for the capacitor

The primary part of the converter is operating around 35V and the voltage across output filter is around 10V. Therefore, the dissipation factor chosen for the corresponding capacitors are 0.12 and 0.2. The ESR could be calculated using the equation below:

$$ESR = tan\sigma \cdot Xc = tan\sigma \cdot \frac{1}{2\pi fC} \qquad \textit{Equation.7}$$

The capacitors placed after the rectifier for smoothing the input voltage works at 100Hz while the capacitors at the output end of the converter are operating at 100kHz, the capacitances could hence be derived:

$$C_{output} = 0.2 \times \frac{1}{2 \times \pi \times 100k \times 23.4375\mu} = 0.014\Omega \qquad \textit{Equation.8}$$

$$C_{input} = 0.12 \times \frac{1}{2 \times \pi \times 120 \times 1000\mu} = 0.16\Omega \qquad \textit{Equation.9}$$

Main Converter transformer winding number calculation

The number of turns on the transformer is determined by the equation below (the derivation steps are skipped):

$$N = \frac{VTA}{\Delta B A_{core}} \qquad \textit{Equation.10}$$

In this equation, the cross-section area of the core is settled (97.1 mm^2) and VTA is calculated in the worst-case scenario, which refers 50% duty cycle. Although the flux density of N87 material saturates at around 500mT from the datasheet, the value of maximum flux density is chosen as 150mT to reduce the losses in the transformer and increase the efficiency. Therefore, the number of windings on the primary part of the transformer:

$$N = \frac{0.5\times35\times\frac{1}{100k}}{150\times10^{-3}\times97.1\times10^{-6}} = 12 \qquad \textit{Equation.11}$$

According to the primary and secondary turns ratio:

$$N_2 = N_1 \times \frac{16}{21} = 10 \qquad \textit{Equation.12}$$

It is found that the magnitude of the magnetising current is reasonable after calculation as well. Therefore, the numbers of turns on the transformer are settled at least 12 turns and 10 turns. 21 turns for primary coil and 16 turns for secondary coil has been chosen for the transformer design in practise, which could make the flux density lower, and thus the power loss could be lower.

Main Converter Transformer Winding Equivalent Resistance

The equivalent resistance of the windings is dependent on the length and the type of the copper wire which have been used to build the transformer. To choose the wire with correct diameter, the skin depth of the wire is found using the equation below:

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_r \mu_0}} \qquad \textit{Equation.13}$$

The following parameters are fixed for copper material:

$$\rho = 1.678 \times 10^{-8}\Omega m, f = 100kHz, \mu_r = 0.99, \mu_0 = 4\pi \times 10^{-7}$$

Thus, the skin depth is found to be **0.206mm** at 100kHz for copper.

For the main converter transformer, any current density between $2 - 8A/mm^2$ is considered reasonable and the current through the transformer is also dependent on the resistance of the load. Thus, for safety reason, the thickest wire (20AWG) is chosen which has an effective cross-sectional area of 0.39 mm^2 (considering skin depth). The equivalent resistance of the windings on the transformer could hence be calculated as the type of the wire and the number of turns has been chosen. The following calculations show the method to estimate the resistance:

$$R_{primary} = N_1 \pi D \cdot R_{wire} = 0.015\Omega \qquad \textit{Equation.14}$$

$$R_{secondary=}N_2 \pi D \cdot R_{wire} = 0.012\Omega \qquad \textit{Equation.15}$$

Winding Number of the Output Filter Inductor

As the inductance was calculated to be $34.57\mu H$, the winding number of the inductor could be given as the following equation:

$$N = \sqrt{\frac{gL}{\mu_0 A_{core}}} = \sqrt{\frac{0.5mm\times34.57\mu H}{4\pi\times10^{-7}H\cdot m^{-1}\times97.1mm^2}} = 11.9 \qquad \textit{Equation.16}$$

Thus, we pick N=12 as the winding number of output inductor.

Inductor DC Resistance

The wire of 0.81mm diameter has been chosen for winding. The resistance could be given to be:

$$R_L = \rho_{cu}\frac{L_{cu}}{A_{cu}} = \rho_{cu} \times \frac{2N\pi r_{core}}{\pi {r_{wire}}^2} = 1.72 \times 10^{-8}\Omega m \times \frac{24\cdot5.56mm}{(0.405mm)^2} = 0.014\Omega \qquad \textit{Equation.17}$$

3. Simulations Results under ideal conditions

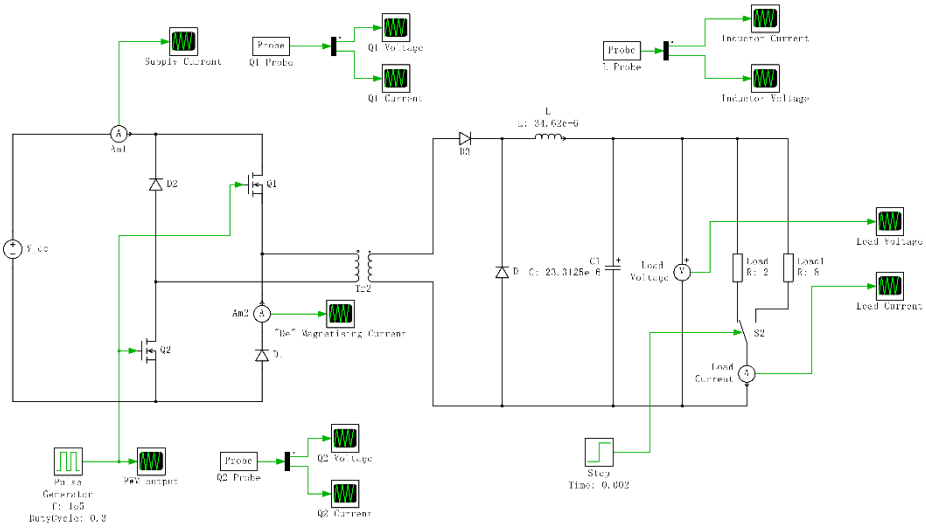

Figure 3. Ideal schematic with 35V DC input

Simulation Settings

The simulation time was set to 0.005s and the max step size was set to 1×10^{-6} to ensure the accuracy of the simulation result. Two loads with different resistances were connected to a switch at the output end of the circuit. The step-input-driven switch would jump to the load with higher resistance from the load with lower resistance at 2ms to simulate the change of load in real working conditions. The pulse generator that used for driving MOSFET has been set to 100kHz with the duty cycle of 0.3, and its high-level voltage has been set to be 15V in the simulation.

Results & Observations

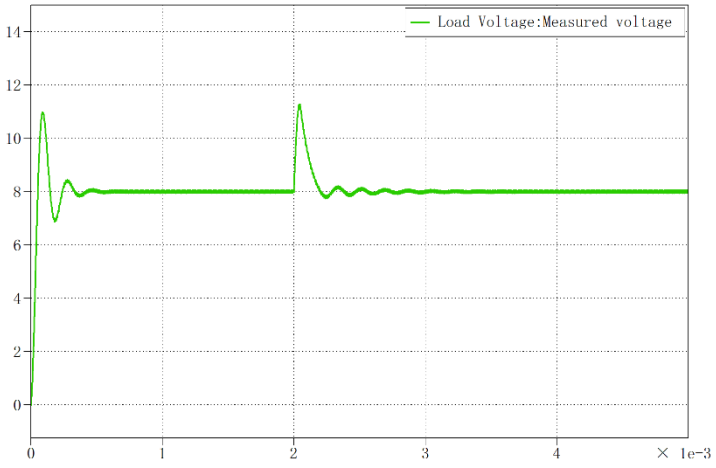

Figure 4. Simulation result of ideal conditions

It can be observed that there are generally two significant overshoots in the plot, where t=0s and t=2ms respectively. The output load is 2Ω initially and has been changed to 8Ω after 2ms. Before and after the change of load, the output voltage would be 8V in steady state, though it is apparent that the change of load causes the overshoot. Comparing these two overshoots, the second one takes longer time than the first one to steady, which might because the change in resistance changes the time constant of the RLC circuit. The cause of the overshoot could be there is no feedback loop in the system to implement feedback control, so the system is merely an open loop system. Moreover, the output voltage contains ripple of $5\mu V$ (peak-to-peak, much smaller than the minimum requirement),

which might be caused by the charging and discharging of the capacitor under high switching frequency.

4. Simulation results with non-ideal components

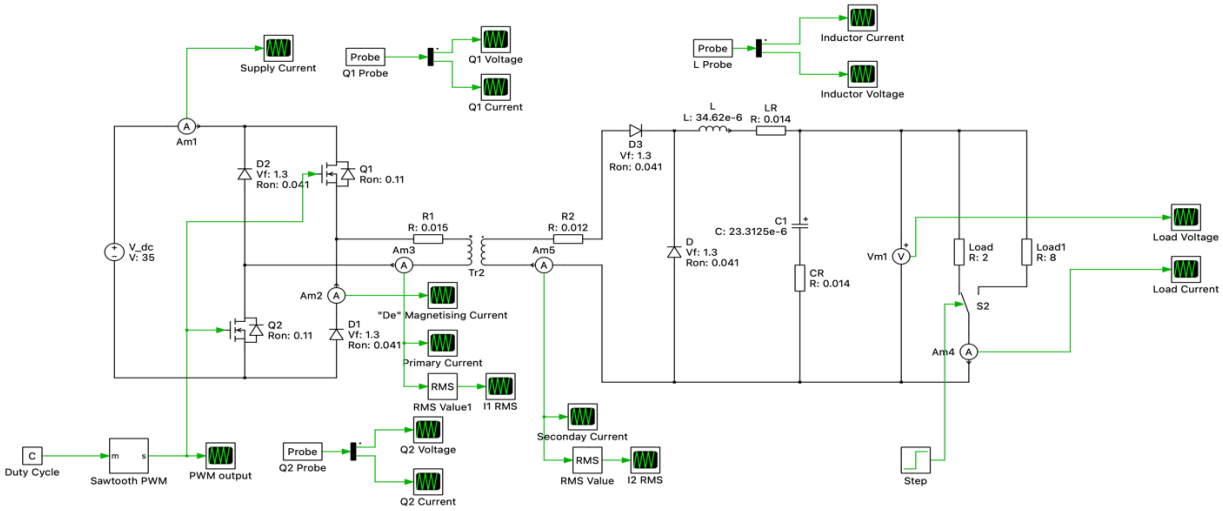

Figure 5. Non-ideal schematic with 35V DC input

Simulation Settings

The simulation settings of the non-ideal circuit were identical to the ideal circuit except the changes in component values as shown in the schematic above.

Results & Observations

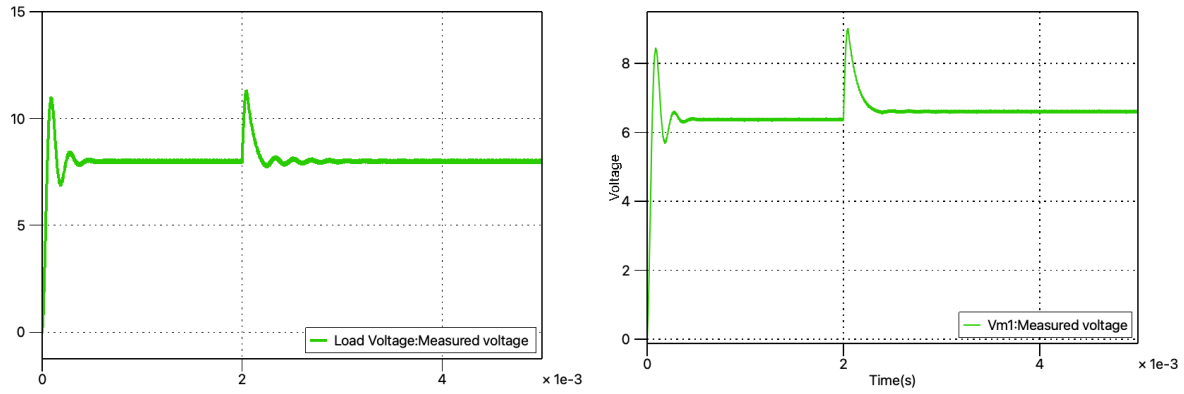

Figure 6. Ideal (left) and non-ideal (right) output voltage

Two major differences could be found by comparing the output voltage plot of ideal and non-ideal simulations. The first point is that the stable voltage on the load of non-ideal simulation is smaller than that of the ideal simulation. The second point is that in non-ideal simulation, the steady state voltage across a larger resistance load is higher than the voltage across a smaller resistance load.

The possible explanation to the first difference is that after taken the forward bias voltage on the diodes and the equivalent serial resistances into consideration, there would be voltage drops on every circuit component while the input voltage remains the same, which results in a relatively lower output voltage in the non-ideal simulation. In terms of the second difference, the changes in the voltage level are seemed caused by the difference in the load resistance, however, it is the difference in current which directly leads to the result. The larger load resistance would lead to a smaller current in both primary part and the secondary part of the converter. As the power rating of the converter and the

turns ration on the transformer are consistent, the voltage drop across the components would hence be smaller when the current flowing in the circuit became smaller, thus, the steady state voltage across the load would be higher when a larger resistance load is applied to the circuit.

The peak-to-peak value of the ripples at the steady state voltage is around 0.08V, smaller than 0.1V that minimum required. The ripples in the steady state voltage are mainly caused by the charging and discharging process of the capacitor, therefore, the peak-to-peak value could be further reduced by using a capacitor with larger capacitance in the circuit. However, the feasibility of using a very large capacitor on the PCB is doubtful mainly due to the limited space on the board, and larger capacitance could make the output voltage response slower.

Besides the observations on the output end of the converter, another simulation result that could guide the future practice is the current magnitude on the transformer. The RMS value of the current directly determines the heat losses of the converter while the current value has an inverse linear relationship with the load resistance, it is important to keep the current density on the wires at a safety region. In the case of copper wires, this figure should be around or below 5A per square millimeter according to the instructions while the thickest wire in the lab only has a cross sectional area of 0.39mm^2 after considering the skin depth which has been calculated previously. The figures below are the RMS current values on the secondary winding under a smaller load (2Ω) and a larger load (8Ω).

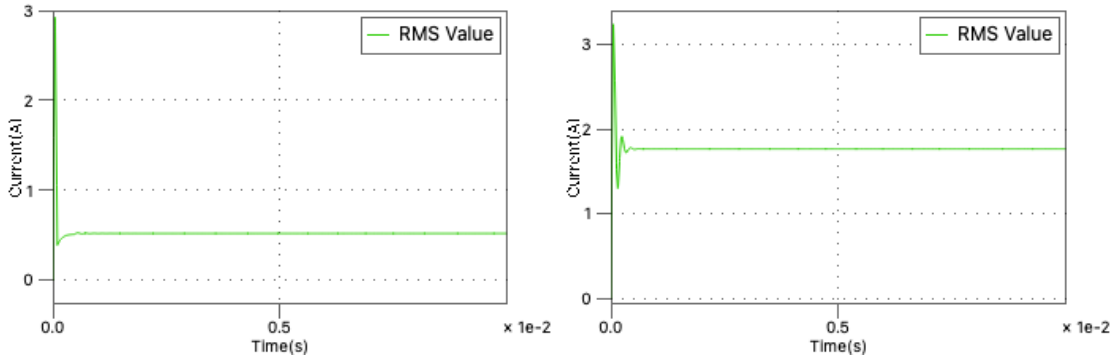

Figure 7. RMS current value on secondary winding under 8Ω (left) and 2Ω (right) load

The current value is roughly at 0.5A under larger load and 1.8A under smaller load, which give an instructional idea on wire type selection in practice.

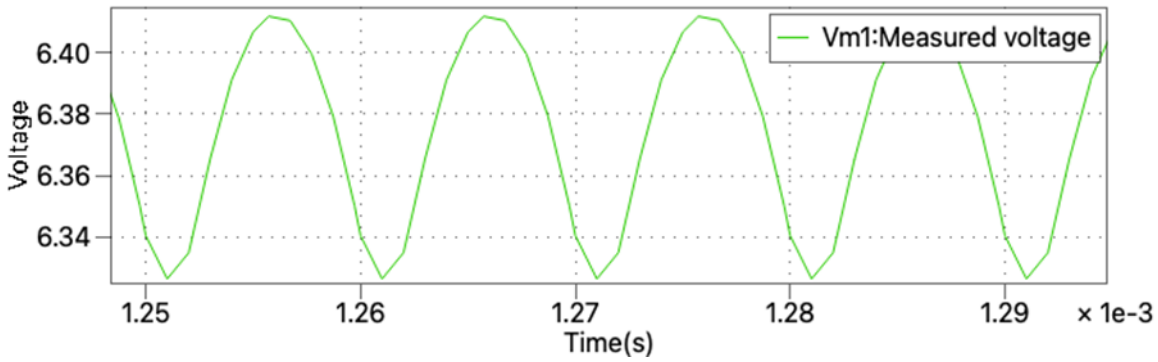

Figure 8. Ripples at steady state voltage

5. Simulation Results with AC derived input

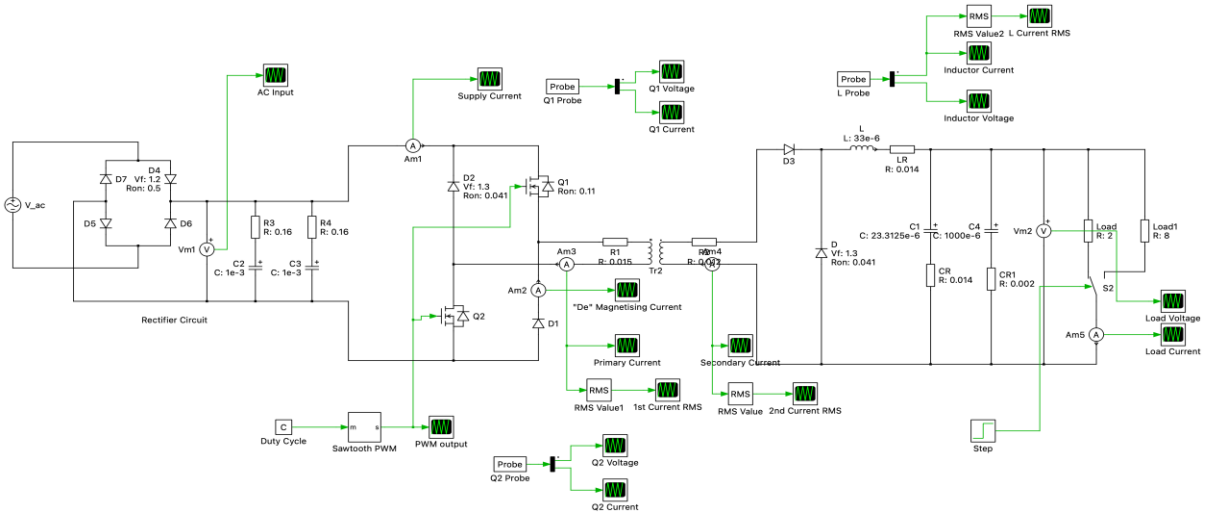

Figure 9. Non-ideal schematic with AC input

Simulation Settings

The simulation time was increased to 0.2s to obtain the stable wave forms, the rest of settings were identical to the non-ideal circuit except the changes in circuit layout and component values as shown in the schematic above.

Results & Observations

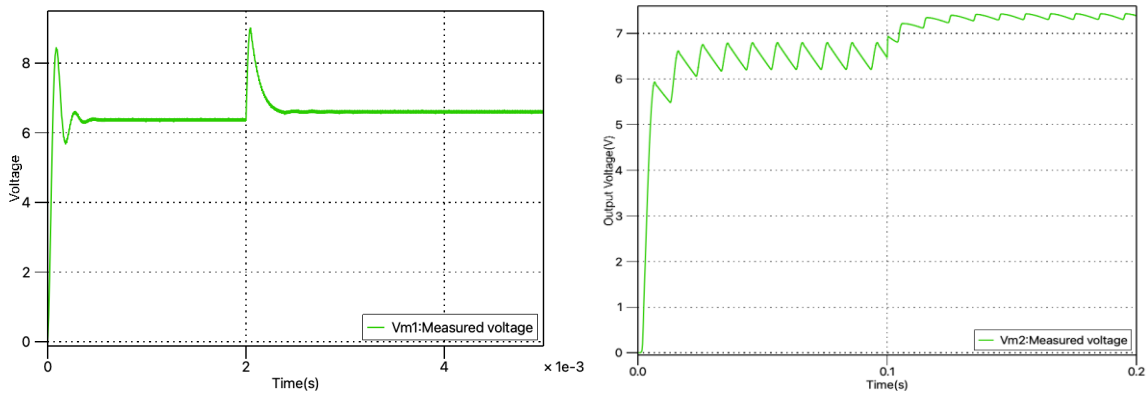

Figure 10. Non-ideal (left) and non-ideal with AC input (right) output voltage

It is observed from the figure above that the ripples in the output voltage (not referring to the big ripples caused by the AC input) is around 0.005V, significant smaller than that in the non-ideal simulation. This change is due to a relatively large capacitor 'CR1' added into the circuit to filter the high frequency noises. Besides the capacitance value, the ESR value also has a noticeable impact on the ripple. In general, the larger the ESR resistance, the larger the ripples in the output voltage. The reason for this could be that the output voltage ripple is proportional to the load current, so the load current decreases, the output voltage ripple would also decrease.

The capacitors in this circuit are mainly used as bypass capacitors to filter the ripples in the rectified AC signal which has a frequency of 100Hz since the input AC signal is at 50Hz. Therefore, the 'noise' in the input signal is considered at 100Hz which requires a significant larger capacitor to filter it out. However, this solution is non-realistic as it is mentioned before, two bypass filters C2 and C3 are placed

in parallel after the rectifier to obtain a reasonable output waveform from the rectifier, the rest of the jobs are left to the control loop which would be applied on the converter in the future.

The second difference found in Figure 10 is that the average output voltage at steady state in AC simulation is higher than that in non-ideal simulation. The main reason of this difference is that the magnitude of the input AC signal was set to 42.42V whose RMS value equals to 35V as the simulation before. However, the reading on the voltmeter across the rectifier is found to be higher than 35V dc as shown in Figure 11, which results in a higher output voltage than the simulations using 35Vdc input. The working principle of bypass filters, the relation between the capacitances and input wave form have been further revealed through this observation, it is found that with the increase of the capacitance, the upper extreme of the ripples would remain the same while the lower extreme of the ripple increase, hence narrowing the ripple. In the real case, this would not be a major problem since the output voltage would be dynamically adjusted.

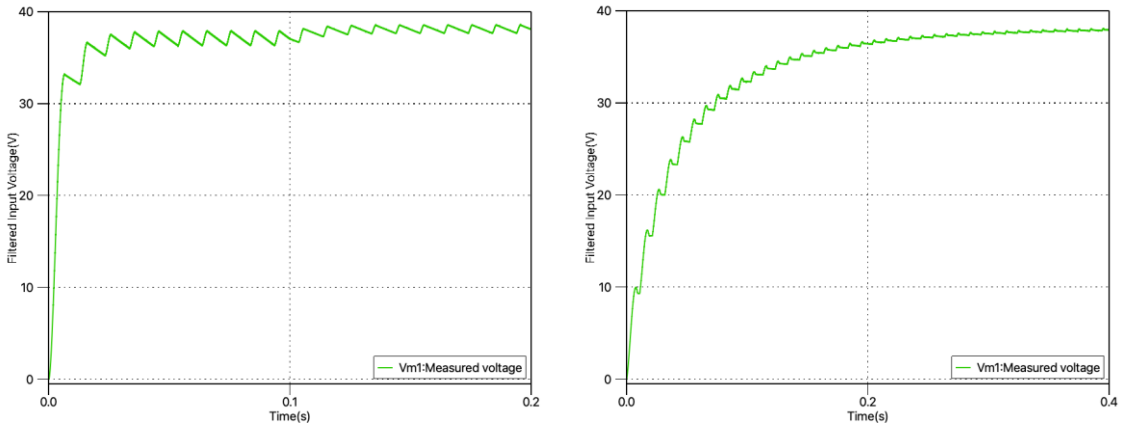

Figure 11. Filter AC input via 2uF capacitor (left) and 20uF capacitor (right)

The two figures above present the input wave forms to the converter with different bypass capacitors. In general, the ripples in the input voltage would increase with the decrease of the bypass capacitors' capacitance while the time consumed to the steady state would decrease.

6. Gate Drive Circuit

The gate driver circuit is a critical component in the power electronics converter, providing electrical isolation between the control and power sections for safety and reliable operation. **Figure 12** depicts the circuit schematic, with MOSFETs represented as capacitors. The circuit components are carefully selected and arranged to ensure efficient operation of the MOSFETs as power switches. The next section explains the circuit operation in detail, discussing the purpose of each component.

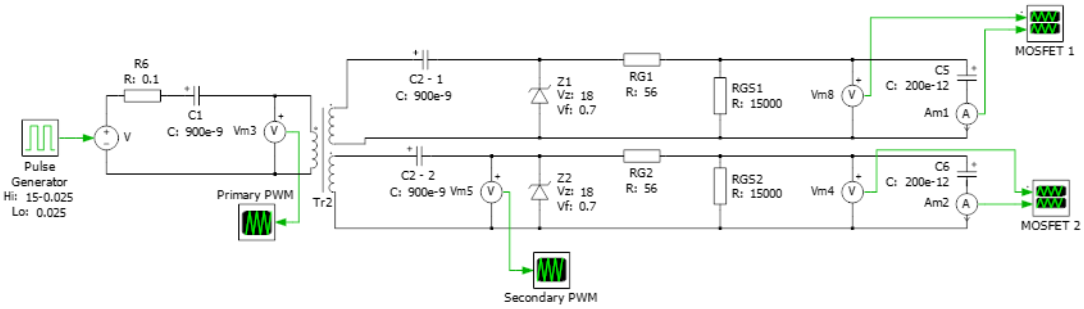

Figure 12. Schematic of the Gate Driver Circuit

The gate driver circuit utilized a 100 kHz square wave input signal with a peak voltage of 15V to control the MOSFET power switches, which required an input voltage between 12V and 15V. To prevent the

transformer from becoming saturated by the input signal's DC components, a coupling capacitor (C1) was used to block the DC components. Without C1, signal distortion and potential transformer damage could occur due to a duty cycle-dependent voltage across the transformer windings. Although C1 caused a signal shift with peaks of 10.5V and -4.5V, its relatively large value was necessary to effectively block DC and prevent signal distortion caused by voltage drop. If the C1 value was chose too small, the impedance of the capacitor would be large, so that the AC component might not be fully conducted, which would cause higher power loss. Additional that the DC component might not be fully blocked, which could cause saturation of the transformer. If the C1 value was chose too large, the impedance would be small and thus the current would be large, and this would also cause the saturation of the transformer.

The signal then enters a unity transformer, which provides galvanic isolation and protection between the control and power sections of the converter. The transformer in the gate drive circuit helps to ensure reliable and safe operation of high-power switching devices by allowing a safe signal transfer. Low leakage inductance was needed in the transformer to prevent time delays that could reduce system performance and reliability. Trifilar winding was employed to achieve this.

The second coupling capacitor restores voltage drop and maintains voltage levels of 15V and 0V, while the Zener diode protects the MOSFET from overloaded conditions by clamping the voltage at a safe level. The Zener diode with a breakdown voltage of 18V mitigates the risk of voltage levels rising above the MOSFET's voltage rating of 20V during turn-on and turn-off. A voltage of 18V was used to provide an additional safety margin, considering the MOSFET's maximum gate-source voltage of 20V and its requirement of only 12V-15V to operate.

The MOSFETs were represented with capacitors, C5 and C6, because the gate terminal of a MOSFET behaves like a capacitor, and it has to be charged and discharged through a resistor in order to turn the MOSFET on and off. The gate capacitance is typically much larger than other capacitances in the circuit, which is why it is represented separately as a capacitor. Representing the MOSFETs as capacitors, C5 and C6, allowed for accurate simulation of the gate capacitance and circuit behaviour.

The gate resistor, Rg, was responsible for charging and discharging the gate capacitance within the MOSFET which meant choosing a correct value for it was mandatory. Since, a small value of the gate resistor, caused the gate capacitor to charge faster increasing the turn on speed and thus decreasing the power losses. However, it can cause excessive current to flow into the gate at turn on, which can potentially damage the MOSFET. Hence, a suitable value balancing the current limit and turn-on speed was chosen.

The gate source resistor, Rgs, was a necessary component responsible for removing the charge stored by the parasitic capacitances, C5 and C6, between the gate and the source. Without this resistor, the MOSFET becomes unpredictable and may have floating voltages due to parasitic interference and noise. Since it was responsible for the removal of charge, its value was dependent on the time constant, which meant that a large Rgs would increase the switching times leading to higher power dissipations and thus thermal losses. From a selection of the correct components a voltage output with peak of approximately 14.3V and -0.7V were produced, as shown in **Figure 13**. With the voltage drops in the peaks caused by the Zener diode in forward mode.

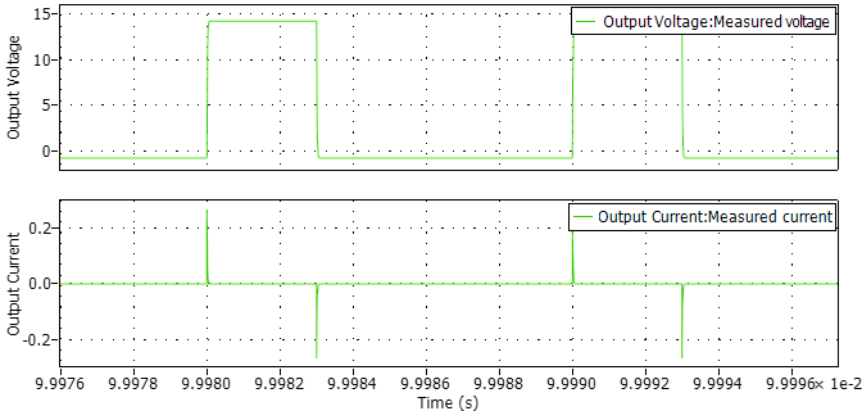

Figure 13. Output voltage and current of the gate drive.

7. Summary

In conclusion, the selection of duty cycle and frequency at 30% and 100kHz, respectively, provided optimised efficiency and switching losses. Calculations were made for various components, including the output filter inductor and capacitor, and values were obtained for non-ideal conditions, considering the forward bias voltage on diodes and ESRs.

Multiple simulations were carried out, including two loads with different resistances, 2Ω and 8Ω, and the results within ideal conditions demonstrated that the output voltage was steady at 8V in both cases, with overshoots caused by changes in the load. The simulations also showed that the output voltage contained a ripple much lower, 5μV, than the requirement of 0.1V. However, under non-ideal conditions, the stable voltage was lower than 8V due to voltage drops in the components. The voltage level was higher in the high resistance case since larger load resistance led to smaller currents and, thus, lower voltage drops in each component. The peak-to-peak value of ripple at steady state was 0.08V, which was smaller than the required 0.1V, the possibility to reduce this ripple was limited by the space availability on the PCB.

In terms of the AC derived input, the simulation ran for a longer time due to the larger capacitor applied to the circuit. The major differences compared to non-ideal simulation were the results of changing DC source to AC. The output voltage was found to be larger than non-ideal simulation at around 10%. However, also showcasing that the ripples within the output voltage was much lower at 0.005V due to the addition of the large capacitor CR1 which also resulted in the ripples becoming smaller for a larger load.

It was seen that the gate driver circuit played a critical role in the proper functioning of the MOSFETs. The circuit components were carefully selected and arranged to enable efficient operation of the MOSFETs. The use of coupling capacitors, a unity transformer, and Zener diode to provide reliable and safe operation of high-power switching devices, while the proper selection of gate resistors and gate-source resistors aids in reducing power losses, limiting current flow into the gate, and removing charge stored by the parasitic capacitance.