University of Nottingham
UK | CHINA | MALAYSIA

Department of Electrical and Electronic Engineering

EEEE2046 Energy Project: Viva 2022/23

General Guidance (Read me first!!!)

This document contains a list of 25 questions, covering four main subject areas that you will have encountered and studied during the Energy project. In the viva, your Assessor will use 6 of these questions, picked at random, to form the basis for the interview. The Assessor will then discuss your response to the main question so that you can demonstrate your level and depth of understanding of the topic. This will form the basis of the assessment. It is therefore essential that you do not just learn an answer for each question – but that you know an answer and can explain it in a discussion including supplementary questions.

This viva is worth 40% of the Energy project, which is a significant proportion of the marks, and will test your understanding of all the tasks undertaken. Although we will aim to make the atmosphere as relaxed as possible on the day - you must prepare for this viva the same way you would for an exam.

The questions:

A. Components

1. Explain why the ESR (Equivalent Series Resistance) of the electrolytic capacitors used in the project is important.
2. Why is it that we don't need to consider the low frequency input voltage ripple when we design the output filter of the Forward Converter?
3. When operating from the transformer derived DC input- why does the input capacitor DC voltage reduce when we have the lowest resistance (highest power) load attached.
4. Why does the PWM chip (and the other ICs in the circuit) need a decoupling capacitor?
5. Why have we decided to use Ferrite in all the magnetic components considered except for the input transformer which is made of silicon steel?
6. Why might it be better to wind the magnetic components with multiple strands rather than a single wire of equivalent (approximately) cross sectional area?
7. Since it is stated in the gate drive transformer document that a Ferrite toroid is a good option for winding small components- why don't we use a toroidal Ferrite core for the output filter inductor?
8. The PWM IC (UC3524) has a sawtooth generator which has an offset of 0.8V- why is it that we don't need to worry about this in the closed loop system using either a Type 1 or Type 3 controller?

B. Forward Converter

1. In the original specification document, a switching frequency of 75-150 kHz is defined. What are the implications (benefits/drawbacks) of operating at these two extremes?
2. Why is the duty cycle of the isolated forward converter limited to <0.5?
3. What would happen to the current in the MOSFETs if the main transformer (not the input transformer) was saturated? Why does this happen?

C. MOSFET Gate Drives

1. Why is it that we cannot simulate the gate drives driving an actual MOSFET in PLECS? How could we get around this and verify the basic operation of the gate drive circuit?

C. MOSFET Gate Drives (Continued)

2. For the gate drive circuit used in the project-. What is the purpose of C1? Why is it important that C1 is not too large?
3. Why do we use a Zener diode rather than a standard diode in the gate drive circuit?
4. Why do we need a gate driver chip such as the TC4425A? Why can't we drive the MOSFETs directly from the UC3524 PWM IC?
5. Why is isolation needed in the gate drive circuit? Since we're driving both MOSFETs with the same demand (i.e. they are driven to switch on and off at the same time) why can't we use a single gate drive circuit for both?
6. For the gate drive transformer- does it matter how you wind the three windings onto the toroidal core?

D. Control

1. Why is feedback important for power supply control?
2. The control transfer functions are implemented using Operational Amplifiers- what alternative might the project have used? How would this be approached?
3. What is the purpose of the "integrator" part of the controller/compensator transfer function (Both type 1 and Type 3)?
4. Why is it important to achieve a reasonable phase margin in the design? What would be an appropriate Phase Margin? Why is this?
5. Why should we be careful when having a low Gain or Phase Margin?
6. Why is it important to not have significant open loop gain at the converter switching frequency?
7. What effect does the output filter capacitor ESR (Equivalent Series Resistance) have on the Bode plots of the forward converter?
8. Why is important to have a reasonably high open loop gain at 100Hz in the converter circuit from the labs?

Marking Scheme

The students will need to answer 6 questions from above- supplementary/follow-up questions should be used to ensure that they have not memorised an answer and that they therefore understand what they have said.

After you have finished each question, mark the response out of five in the spreadsheet according to the following mark scheme.

0- Failure to answer, or incorrect

1- Poorly answered showing limited understanding

2- Basic concept understanding demonstrated

3- Understood but unable to answer supplementary questions

4- Well understood but follow-up in supplemental questions incomplete

5- Clearly well understood and handled main and supplementary questions

Al Watson

March 2023