My duty cycle looks like is saturating – is this a problem?

Maybe Yes and maybe No – there probably 4 reasons why you might see the duty cycle calculation limiting at 45% (assuming you set it to 45%).

[1] **The duty cycle limits for many switching cycles in steady state** – particularly when the load is high (R is small at the output). You notice dips in the output voltage when the D limits. This due to the value of N2/N1 on the transformer being too small (assuming everything else is OK with the model – for example, is the AC input voltage correct?). Is it a problem – **YES** – does it need fixing **YES**.

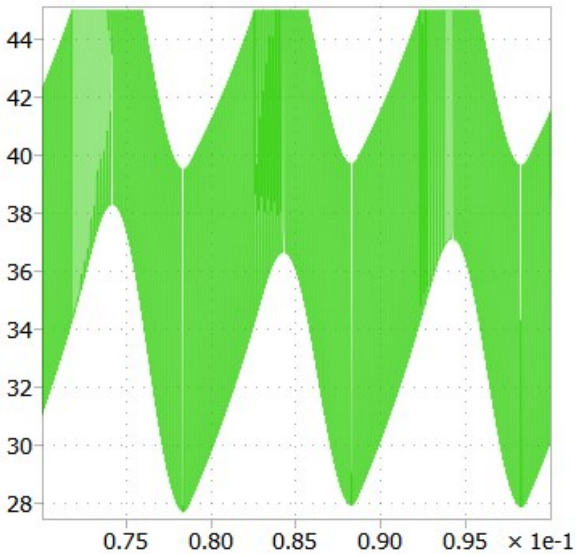
[2] **The duty cycle hits the limit when the simulation starts up** but after that when it gets to steady state it is OK. Is it a problem – **NO** – does it need fixing – **NO**. What the simulation does at start up and what will happen in the lab are totally different – the simulation is not representing any sort of reality here so you should not worry about what it is showing. In the lab you will have a separate switch for the AC supply and a separate switch for the power supply that is powering your electronics – you will not switch them at exactly the same time – and even if you did that are all sorts of transient effects in the lab power supply and in the 50Hz transformer that you simulation model does not include – so at start up the simulation model is not representing reality - the results are "fiction" – you can ignore them! Always think about whether your model is modelling something realistic!

However, if you want to "fix" this problem so the results look "nicer" you can do what a real power supply would do and multiply the output of the error amplifier by a ramp that goes from zero to unity at start-up so that the control is gradually introduced. You can set the ramp time at something sensible by looking at how long the transient is and by making it a reasonable amount longer than that. If you do this, you need to make sure the error amplifier output does not go to a crazy value at start-up (think about why it might do this!) – so you need to be using the amplifier model with limits and have set them sensibly (the supply rails for the op-amps on the control PCB are 0V and +5V – so that should give you a good idea).

Alternatively, you can use the "initialisation" feature of PLECS which allows you to start a new simulation with the conditions at the end of a previous one to remove the start-up transient completely. I will leave you to find that feature.

[3] **The duty cycle hits the limit during load transients** – for example when you change the load from 25% to 100% or the other way, but it works fine in steady-state. Is it a problem – **NO** – does it need fixing – **NO.** Most controllers saturate (hit the limits) during large transients – provided it recovers as the transient proceeds – it is not a problem – it is perfectly normal operation.

[4] **The duty cycle has a lot of "noise" on it and it hits the limit once per switching cycle –** for parts of the operation – usually at full load**.** Your calculated duty cycle looks something like this:



Is it a problem? – **well not really** provided your output voltage is stable. This effect is caused by the controller amplifying the 100kHz ripple at the output of the converter – you have all the information and knowledge to calculate how big the 100kHz ripple will be at the output of your controller. If you look at the inputs to the comparator – you will see that at the instants where the waveforms cross and the pulse is produced, it is not limiting, and the duty cycle is not at the limit. **Could it be a problem**? – if you have this situation it means you are close to the point where all the assumptions we made in deriving the model and doing the control design (all the discussion about "averaging") is close to not being valid. If you push it too far the system may become unstable if the ripple on the duty cycle signal gets so large that it may cross the triangular wave more than once in each cycle. Also remember that the simulation is an approximation and something that is "just stable" in the simulation may be unstable in the lab. **Do you need to fix it**? – that is an engineering decision – if the ripple is very big at the duty cycle input – you may consider playing safe and changing your control design to reduce it – or you could make a change to reduce the ripple at the converter output. I will leave you to think about those 2 possibilities.

Jon Clare