KiCad Design Explanation

Track width and thickness:

Main converter circuit:

The table below shows the design requirements of the main converter:

Vin	Vout	P
35V	8V	50W

The average current in the primary part and second part could be derived using the formula: I=P/V

Hence the estimated average current flowing in the main converter is listed in the table below:

Iin	Iout
1.43A	6.35A

In the PCS design, considering the power losses across the components, the input power would be roughly 20% higher than the output power, the primary part track is hence designed to have the capability to deliver 2A current. The secondary part track is designed to have a 7A current tolerance. Therefore, the designed track parameters:

	Primary	Secondary
Width(mm)	0.78	4.39
Thickness(mm)	0.035	0.035

Gate driver circuit:

There are three factors affecting the choice of track width. Firstly, the peak output current from the MOSFET gate driver(4.5A). Secondly, the secondary and the tertiary windings are connected to PWM_COM_A and PWM_COM_B nets, which deliver a 2A current. Thirdly, the gate driver circuit is a high-frequency circuit, which would be **very demanding on the low inductance of the tracks.**

From the inductance calculation formula, the length of the track has the greatest impact on the inductance, followed by track width. Therefore, the gate driver circuit footprints are arranged compactly and the width of the tracks are set to 4.5mm.

Capacitor Location

- U39>>**bypass capacitor**(the smaller capacitance one), placed close to voltage source, to eliminate high frequency noise from the voltage source.
- U37>>**decoupling capacitor**(the larger capacitance one), placed close to IC circuit, to reduce the impact of the varying voltage levels on the IC circuit. A relatively larger capacitance is chosen because it is the energy-storing feature that we need.

General Considerations:

- 45-degree corner: every corner in this design is 45-degree, to reduce the possibility of radiated Electromagnetic Interference (EMI), which has a great impact on high frequency circuits.
- Input ports are placed on the left side of the board, output ports are placed on the right side of the board for convenience.
- There is a reasonable clearance(distance) between the power converter circuit and the control circuit, to reduce possible interference.
- All GND pins are connected to a filled zone at the back of board to reduce electrical noise and interference through ground loops.

Thermal Management

- Heatsinks are attached on two MOSFETs and two diodes on the converter output end, where large current flows.
- Multiple thermal vias are placed under the 4-diode-rectifier and the MOSFET Driver to increase heat convection.

Testpoints:

Unit Reference	Testing Property
U1(TP1)	Rectifier PWM output
U3(TP2)	MOSFET1 Vgs
U7(TP3)	MOSFET2 Vgs
U9(TP4)	Converter primary current
U10(TP5)	Converter transformer output current

Warnings Explanation

- ‘Silkscreen clipped by solder mask’: Caused by silkscreen layer overlap with solder pad, has no impact on the function of the circuit, could be ignored.