EEEE2046 Energy Project: PWM Generation and MOSFET Gate Drive Circuit

1.0 Introduction

As part of the Energy project, you will be required to control and drive MOSFETs in the main part of the Forward Converter circuit. This requires two elements: A Pulse Width Modulation (PWM) Generator and a MOSFET Gate Drive Circuit.

2.0 Pulse Width Modulation

Most switching power converters rely on some form of PWM in order to regulate and control the output voltage/current of the circuit. There are many methods of generating PWM signals- microcontrollers (similar to the one used in the Electronics Project), digital circuits, analogue circuits, dedicated ICs or a combination of these can be used. In the Energy Project, you will use a PWM IC to generate the PWM, which controls the operation of the MOSFETs.

You should be familiar with the basic concept of PWM from your EEEE2045 lectures. The basic use for PWM in a Switch Mode Power Supply (SMPS) is simple: by varying the on and off time the MOSFETs, you can control the energy flow through the power supply and in turn regulate the output voltage at its desired level. Figure 1 shows a PWM signal. In most applications the switching frequency, and therefore the switching period (T_{sw}), is constant and the duty cycle (ratio of on time to the switching period) is varied. Some applications utilise a variable switching frequency, but these are not covered in either of the 2nd year modules.

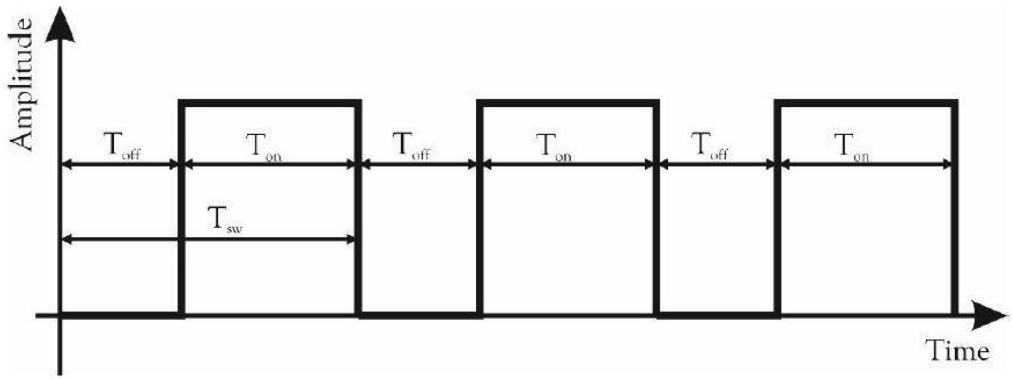

Figure 1: PWM signal with fixed switching frequency

In this module, we will be using a PWM IC to generate the desired switching waveforms. There is a huge range of PWM ICs available- we have chosen a simple one, the UC3524. Upon studying this chip, you may find that it has many peripherals- error amplifiers etc. These could be used to implement the control scheme of the SMPS but are not used in this module (we us external op-amp circuits instead).

In objective one of the project, you should have operated a simulation of the converter in “open loop” mode. This means that there is no feedback or “closed loop” control in the circuit (we add this in objective 5). This means that we set the duty cycle manually rather than having it automatically

varied by a control circuit. This is the mode that we will test the basic circuit operation with before looking at closed loop control.

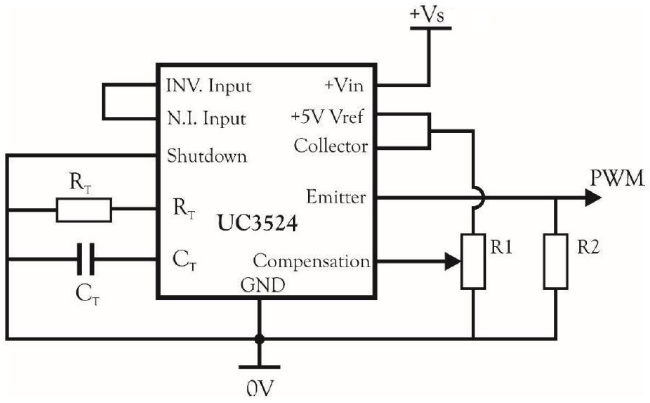

Figure 2: Basic configuration of UC3524 IC for open loop PWM operation

The UC3524 chip can be used as an open loop PWM generator with which we can manually vary the duty cycle. This configuration will be used to test your practical converter once it has been built (objective 4). The setup of the chip for open loop operation is shown in figure 2. You need to look at the data sheet for this IC in order to select the correct component values to achieve the required switching frequency and duty cycle for testing the converter circuit.

3.0 MOSFET Gate Drive Circuit

One aspect of power electronics is the interfacing of the control part of the converter circuit to the power part of the circuit. An important part of this takes the relatively low voltage and current output of a control circuit and amplifies it to produce the higher voltage and current, required to drive the power switching device, in this case a MOSFET. Since, for many power devices, the device pin that we drive is called the “Gate”, this class of circuit is commonly called a “Gate Drive Circuit”.

Control circuits typically have logic level or low voltage (3-5V) outputs and are designed for driving a few mA into the next part of the circuit. Unfortunately, this means that they are not suitable for driving power MOSFETs directly. The gate drive circuit, which is connected between the control circuit and the MOSFET, acts as an amplifier.

For a MOSFET, the device is turned on and off by charging and discharging the gate-source capacitance. A voltage, V_{gs}, is applied by the gate drive circuit to the gate-source capacitance to turn the MOSFET on, and a zero V_{gs} voltage is used to turn it off. Although power MOSFETs have a relatively low threshold voltage (the voltage that begins to turn them on), they require 12-15V to fully switch on. Applying lower voltages increases the MOSFETS “on state” resistance (R_{DS}) and therefore increases the conduction loss of the device, decreasing the efficiency of the SMPS. It should be noted that a voltage above 20V for V_{gs} will destroy the MOSFET. As a result, some protection is usually put in the gate drive circuit to clamp V_{gs} at a maximum of around 18V.

Another source of loss in the MOSFET is switching loss (see EEEE2045). This increases when the gate-source capacitance is charged slowly. As a result, it is desirable to charge this capacitance as quickly as possible. However, driving a MOSFET too quickly can create interference and other undesirable behaviour in neighbouring circuits. A “gate resistor” (see below) is used to control the rate of the charge and discharge the gate-source capacitance.

An example of a MOSFET gate-source voltage and gate current during switching is shown in figure 3. Note the pulses of current that are used to charge and discharge the gate-source capacitance. These currents have a peak of several Amps- thus justifying the need for an amplifier (Gate Drive Circuit).

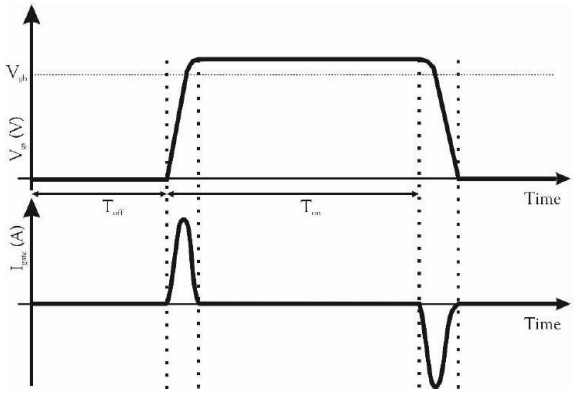

Figure 3: Typical Gate Source voltage and gate current waveforms for a MOSFET being switched on and off

The gate drive for this project must be able to drive two devices simultaneously. However, the source pins of the MOSFETs are not commonly connected. The upper MOSFET source pin is connected to the transformer primary winding and the lower MOSFET source pin is connected to the DC input (See Appendix A). In order to turn both of the MOSFETs on, their gate-source capacitance must be charged. The connection of the MOSFET source pins to different nodes in the circuit means we cannot drive them with a single gate drive. The usual solution is to use isolated gate drive circuits. These can be connected between the gate and source of the MOSFET and 'float' along with any changes in the source potential and maintain the correct potential, V_{gs}.

Figure 4 is a schematic for a simple power circuit, with a similar issue to the power stage of the forward converter and includes an isolated gate driver able to drive both devices simultaneously. Note that similar to our Forward Converter, the source pins of the two MOSFETS are connected to different points in the circuit. This circuit can be used to test the functionally of the gate drive and PWM circuits (figure 2). The gate drive circuit is based on a "positive clamp" and "DC restore" circuit. To build and test this circuit you will need to determine various component values as well as design and build the transformer, T1. For design of this approach for this transformer see the document "Gate Drive Transformer Considerations" on Moodle.

R1 is termed the "gate resistor" and is a very important component in gate drive circuits. It is this resistor which determines the peak current flowing in the gate and hence the switching transition time (and therefore the switching loss of the circuit). Selection of the gate resistor is challenging, and an initial 'guess' is often made and then fine-tuned by experiment and switching tests. The reason for this is that the possible rate of device switching is influenced by many factors which are difficult to consider at the design stage e.g. component layout, stray inductance, parasitic capacitances, EMI & EMC requirements.

An initial 'guess' for R1 in this circuit, based on experience, is 50Ω.

C1 "AC couples" the transformer and gate driver IC. The considerations in determining C1 are:

1) C1 must not be 'too' small. Think about it's impedance- how might a small capacitor effect circuit operation?
2) C1 must not be 'too' large. This can lead to saturation of the transformer, T1. Think about how this happens. As rough guide, based on experience with the circuit, C1 is <1000nF.

D1 is selected to protect the gate from over voltage spikes (mentioned above).

R2 is a “pull down” resistor. Its main function is to stop the gate-source capacitance charging “parasitically” if the gate drive circuit becomes disconnected. There are two time constants to consider in selecting R2: the discharge time constant of the gate capacitance and the time constant formed with C2 and R1. As a guide, based on experience, R2 is >10kΩ.

C2 is selected to maintain V_{gs} >> V_{th} for the whole on period and forms a time constant with R1 and R2 during the positive half cycle.

The operation of this circuit is a function of all these components- some trial and error (and simulation!) may be needed.

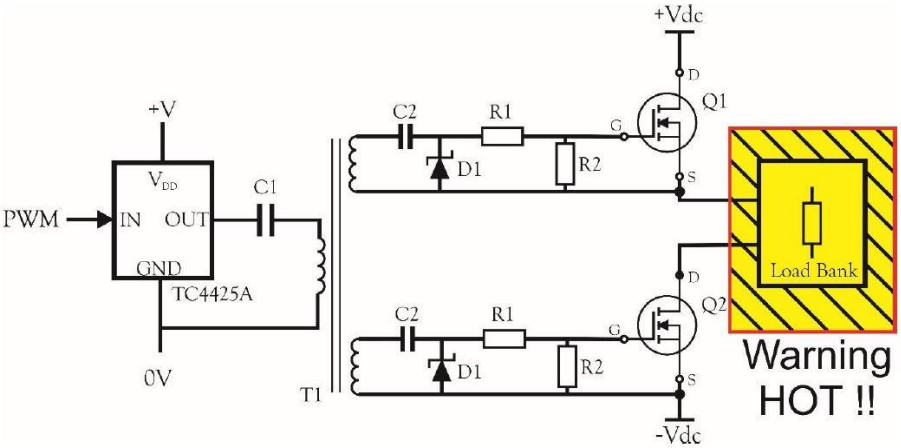

Figure 4: Dual Gate Drive Circuit with test load

It should be noted that the “load” circuit in figure 4, although useful for basic testing, is far from perfect. Inductance in the wire connecting the two MOSFETS, and inductance associated with the construction of the resistors can cause the voltage across the MOSFETs to “ring” when switching (think about why this happens- see EEEE2045 notes). This ringing should not be significant enough to damage the MOSFETs, if Vdc is not chosen to be too large.

Appendix A: 2 Switch Forward Converter Circuit Diagram

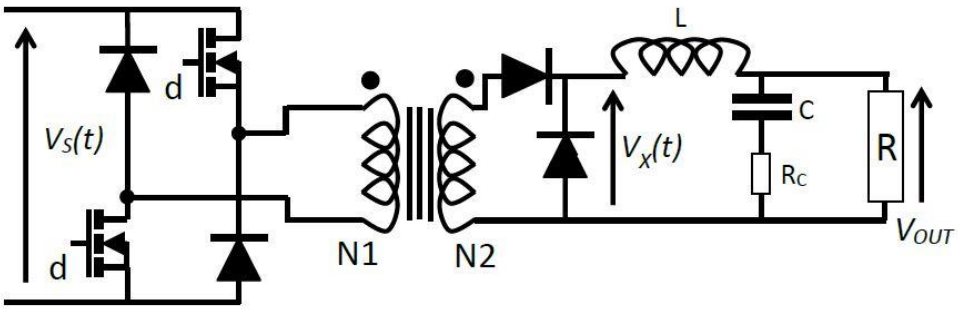

Figure A1: Two Switch Isolated Forward Converter Circuit

Updated: Al Watson, January 2023