University of Nottingham
Electrical and Electronic Engineering

Coursework 2: Switching Simulation

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0. Error Fixes in Coursework 1

0.1 Saturation and Anti-Windup Fixing

In Coursework 1, a 'Saturation' module has been added to restrict the output of current controller within the range from $-251.61\sqrt{2}\,V$ to $251.61\sqrt{2}\,V$, and an 'Anti-windup' has been added to the 'integrator' of the PI controller. However, the 'Saturation and Anti-windup' modules should not be added because it would bring temporary uncontrollability to the system. The fixed current controller verification schematic is shown in **Figure 0.1** below.

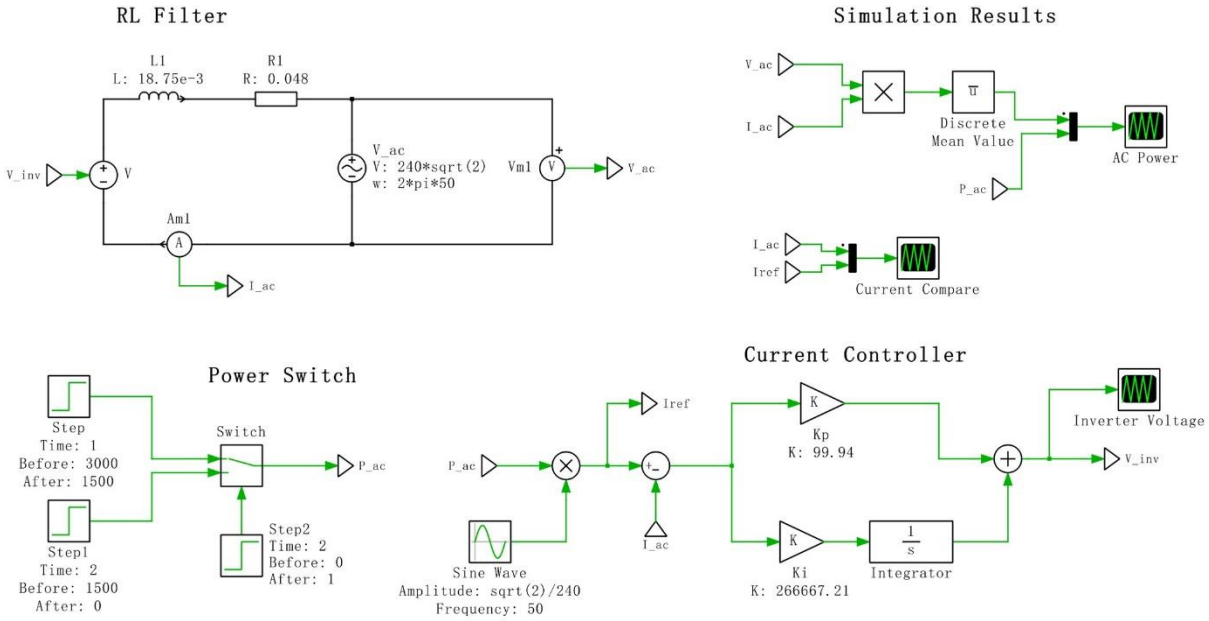

Figure 0.1 Fixed Current Controller Verification Schematic

0.2 Lag Compensator Fixing

In Coursework 1, the derivation of lag compensator's transfer function is incorrect. It should be based on the closed loop transfer function, instead of the open loop transfer function. The fixed procedure is presented in following:

The expression of 'Lag Compensator' could be expressed by:

$$G_{lag}(s) = \frac{k(s+z)}{s+p}, |z| > |p| \qquad \textit{Eqn.0.1}$$

The open loop transfer function could be given by:

$$G_o(s) = G_{lc}(s) \cdot G_D(s) = \frac{62.83k(s+z)}{s(s+p)}, |z| > |p| \qquad \textit{Eqn.0.2}$$

The closed loop transfer function could be given by:

$$G_{cl}(s) = \frac{G_o(s)}{1+G_o(s)} = \frac{62.83k(s+z)}{s(s+p)+62.83k(s+z)} = \frac{62.83k(s+z)}{s^2+(p+62.83k)s+62.83kz} \qquad \textit{Eqn.0.3}$$

Thus, combining the general transfer function of 2nd order system (*Eqn.2.6* in Coursework 1) to the above closed loop transfer function (*Eqn.4.8* in Coursework 1):

$$2\zeta\omega_n = p + 62.83k,\ \omega_n^2 = 62.83kz \qquad \textit{Eqn.0.4}$$

The natural frequency of outer loop (voltage controller) should be at least 1/10 of the natural frequency of inner loop (current controller), because the response of outer control loop should be slower than the inner control loop. Thus, the natural frequency ω_n of voltage controller should be $377.124\ \text{rad/s}$. Assuming the value of 'k' is 8, the values of 'p' and 'z' of $G_{lag}(s)$ could be given by:

$$p = 30.61,\ z = 282.95 \qquad \textit{Eqn.0.5}$$

Overall, the transfer function of 'Lag Compensator' could be expressed by:

$$G_{lc}(s) = \frac{8(s+282.95)}{s+30.61} \qquad \textit{Eqn.0.6}$$

The verification schematic is shown in **Figure 0.2** below.

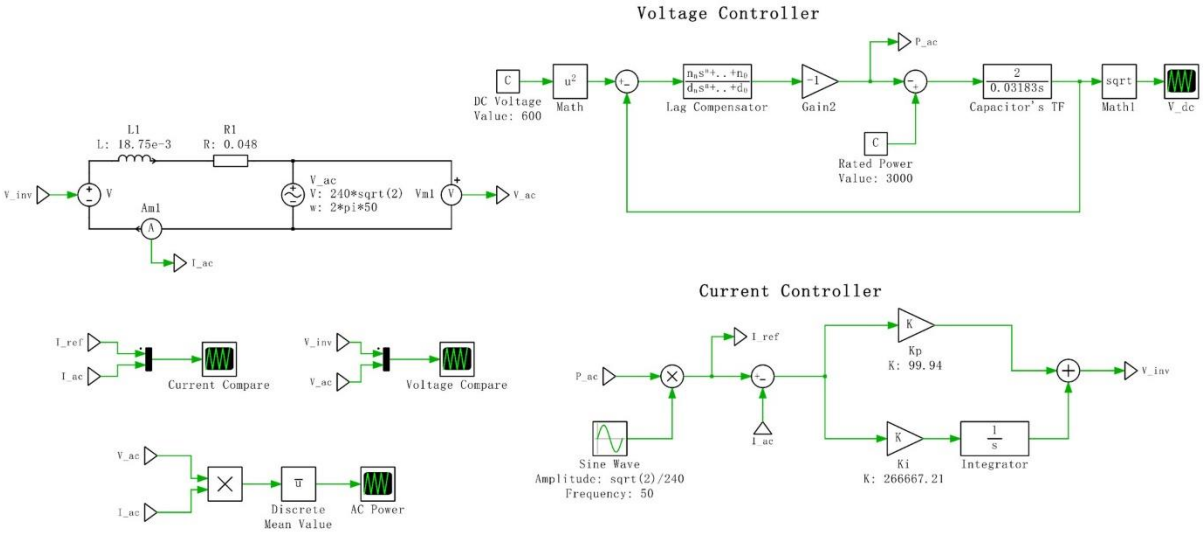

Figure 0.2 Verification Schematic of Lag Compensator

The AC output power is presented in **Figure 0.3** below. It can be observed that the power is stabilized at 3 kW in 0.04 seconds.

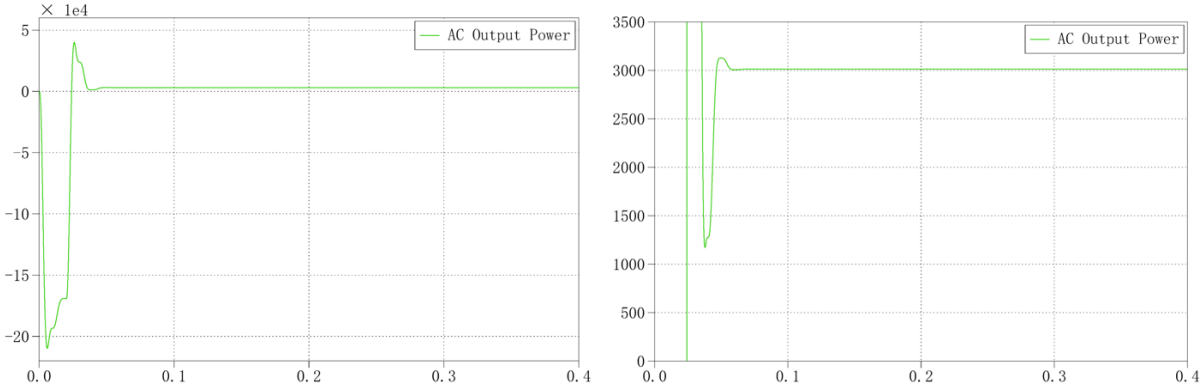

Figure 0.3 AC Power (left: full view, right: zoomed into 0 to 3 kW)

The AC current and voltage after the power stabilized are also presented in **Figure 0.4** below, both of which are performed as expected.

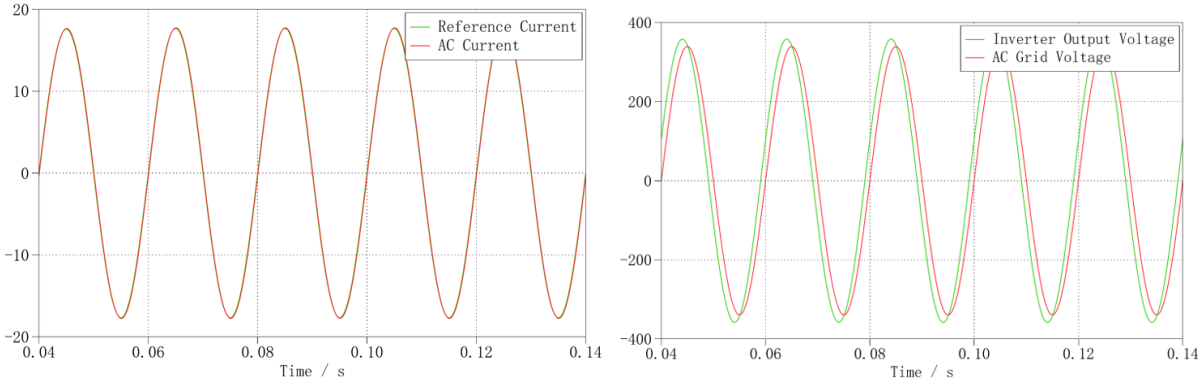

Figure 0.4 AC Current (left) and AC Voltage (right)

1. Switching Model

1.1 Construction and PWM Implementation

The construction of full switching model is shown in **Figure 1.1** below.

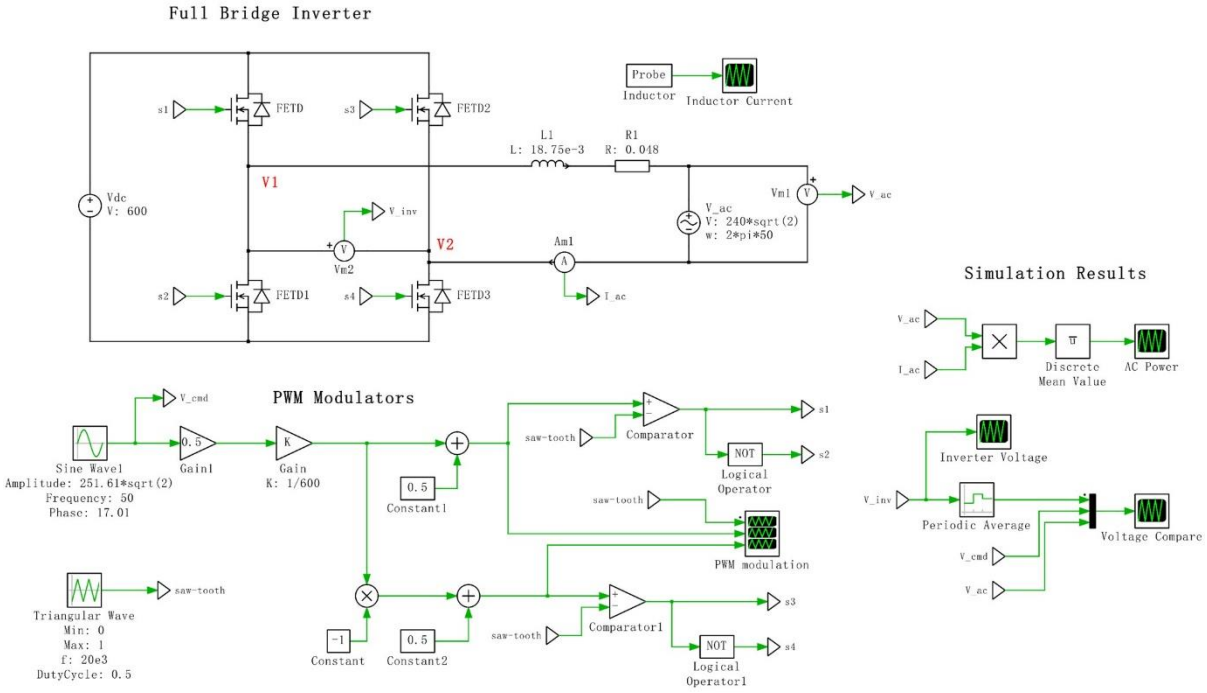

Figure 1.1 The construction of full switching model

The modulation of PWM is completed by two comparators, each of which takes two inputs: a reference signal (20 kHz triangle wave) and a control signal (50 Hz sine wave). The expression of sine wave is given by the *Eqn.1.8* in Coursework 1, whose RMS amplitude is 251.61 V and phase shift is 17.01°. When voltage at the positive pin (+) of comparator is greater than the voltage at the negative pin (-), the comparator output is high (1), and vice versa. In addition, the PWM wave of 's1' and 's2' is complementary, and the same is true for 's3' and 's4'. This is because the switch sets 's1 and s2' or 's3 and s4' cannot be in the 'ON' state at the same time, otherwise it will cause a short circuit in the DC power supply. The sine wave given to the lower PWM modulator in **Figure 1.1** is inverted compared to the upper one, which is shown in **Figure 1.2**.

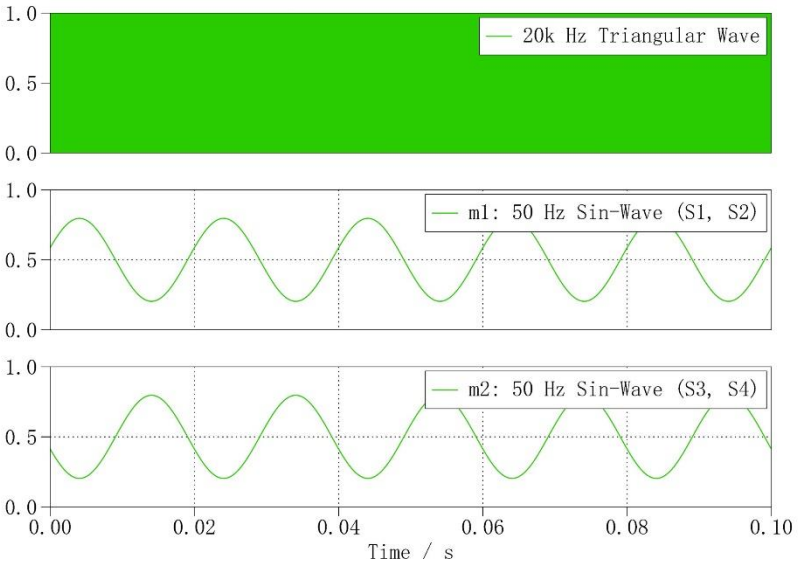

Figure 1.2 20 kHz Triangular Wave, 50 Hz Sine Wave (m1), and Inverted Sine Wave (m2)

The expression of sine wave 'm1' and 'm2' could be given by:

$$m_1(t) = 0.5 + \frac{251.61\sqrt{2}}{2\times600} \cdot \sin(2\pi 50t + 17.01°) \quad \textit{Eqn.1.1}$$

$$m_2(t) = 0.5 - \frac{251.61\sqrt{2}}{2\times600} \cdot \sin(2\pi 50t + 17.01°) \quad \textit{Eqn.1.2}$$

Thus, the voltage between 'V1' and 'V2' in **Figure 1.1** can be given by:

$$V_{12}(t) = 600 \cdot (m_1(t) - m_2(t)) = 251.61\sqrt{2} \cdot \sin(2\pi 50t + 17.01°) \quad \textit{Eqn.1.3}$$

The result given above is the same as *Eqn.1.8* in Coursework 1, which means the pre-modulated signal is as expected. The modulated signal is shown in **Figure 1.3**.

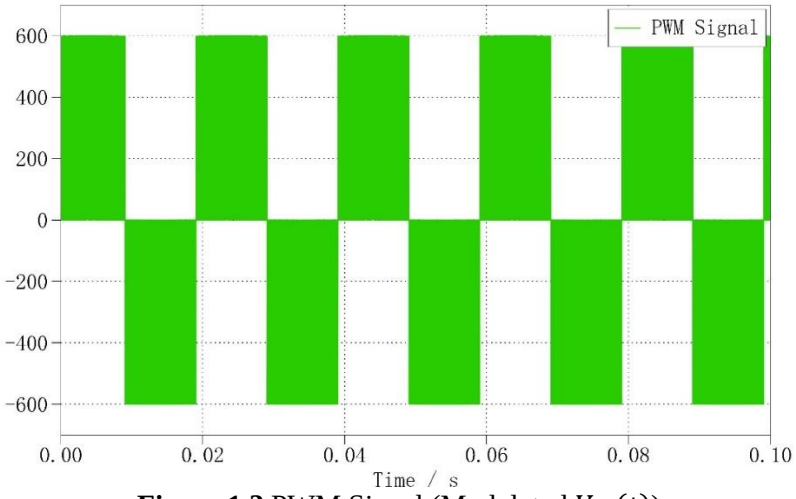

Figure 1.3 PWM Signal (Modulated $V_{12}(t)$)

In frequency domain, the 50 Hz harmonics and switching harmonics are shown in **Figure 1.4**.

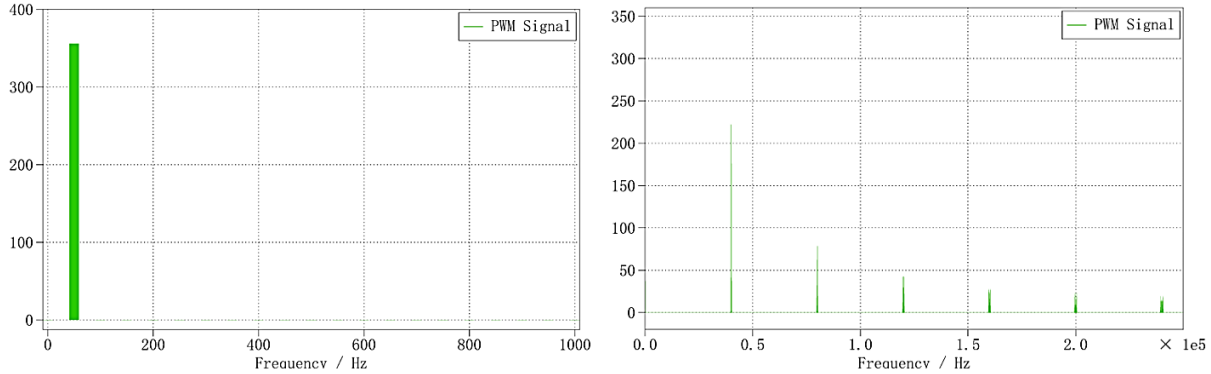

Figure 1.4 50 Hz Harmonics (left) and Switching Harmonics (right) at Frequency Domain

The amplitude of 50 Hz harmonics is measured to be 355.83 V, which is quite close to the amplitude of $V_{12}(t)$ signal ($251.61\sqrt{2}\,V$). This result indicates that the $V_{12}(t)$ signal has been successfully modulated to the PWM signal. Due to the switching of IGBT, the PWM signal also contains high frequency harmonics (multiples of 40 kHz). It can be seen from **Figure 1.4** (right) that the base harmonics is 40 kHz, which is twice of the switching frequency (20 kHz). The explanation for this could be the period for both the switch (upper and lower) to complete a full cycle is actually half of the 20 kHz frequency period.

Zoom in the 40k Hz and 80 kHz harmonics, it can be seen that the harmonics are symmetrical to the target frequency, as shown in **Figure 1.5** below. The symmetrical nature of the harmonics could be caused by the high-frequency triangular carrier wave is compared against a low-frequency modulating signal to generate the PWM. Because the triangular wave is

symmetrical and repetitive, the resulting PWM pulses are generated in a pattern that is also symmetrical over each cycle of the modulating signal.

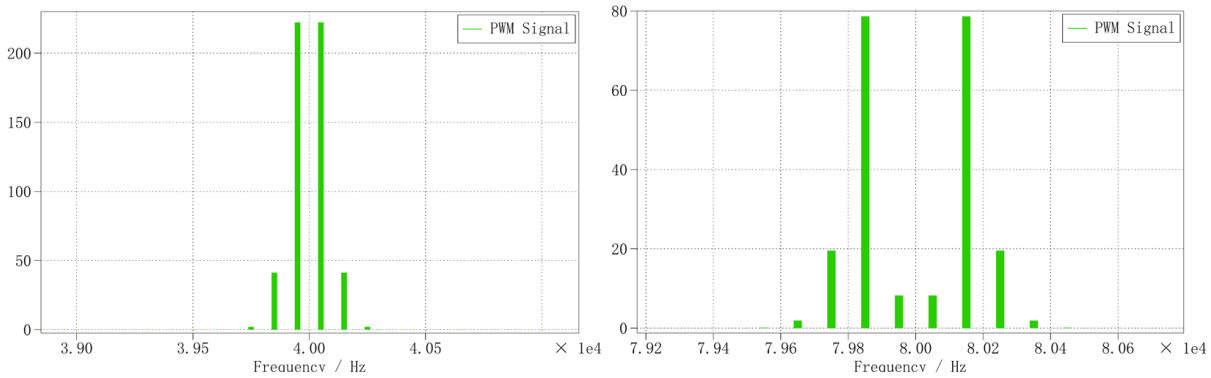

Figure 1.5 Switching Harmonics of PWM (left: 40 kHz, right: 80 kHz)

The comparation of periodic averaged (average time: 1e-4 s) PWM signal, AC command voltage signal, and AC grid voltage signal are presented in **Figure 1.6**.

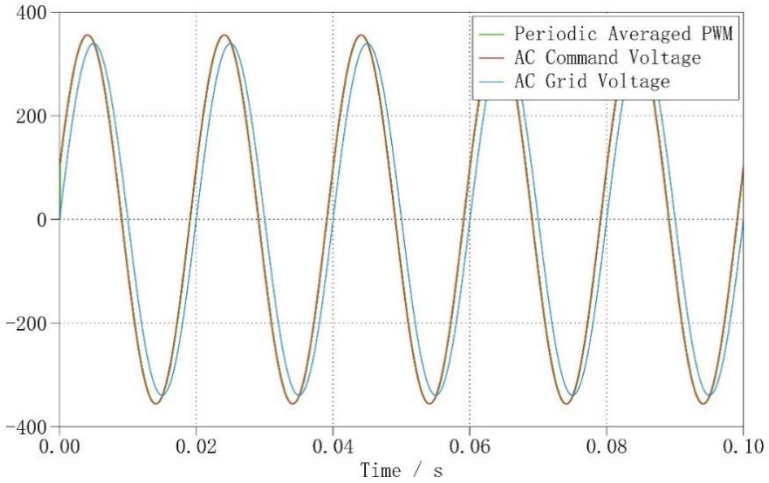

Figure 1.6 Periodic Averaged PWM Signal, AC Command Voltage, and AC Grid Voltage

It can be observed that the waveform of periodic averaged PWM is highly similar to the waveform of AC command voltage sent as input of PWM modulator, which means the design of PWM modulator meets the requirement and fully functional. In frequency domain, the 50 Hz harmonics of above three waveforms are presented in **Figure 1.7**.

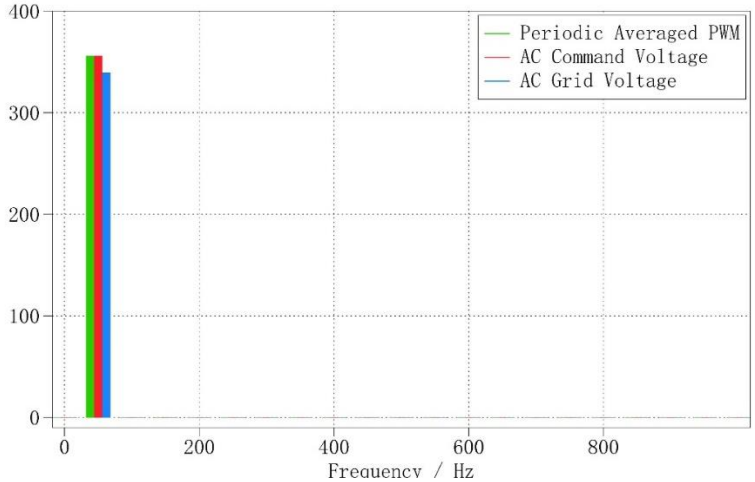

Figure 1.7 50 Hz Harmonics at Frequency Domain

The amplitude of PWM and grid voltage are measured to be 355.8 V and 339.4 V respectively, quite close to the predicted $251.61\sqrt{2}$ and $240\sqrt{2}$, which means the PWM is working as intended. One dominant limitation of this simulation model is that the 'dead time' can be ignored. However, inappropriate settling of 'dead time' might lead to signal distortion, or even short circuit and component breakdown in practical applications.

1.2 Verification of Power Exchange

The power exchanged from inverter to AC grid is shown in **Figure 1.8** below. The response shows no significant overshoot, and it stabilizes at 3 kW in about 0.02 s.

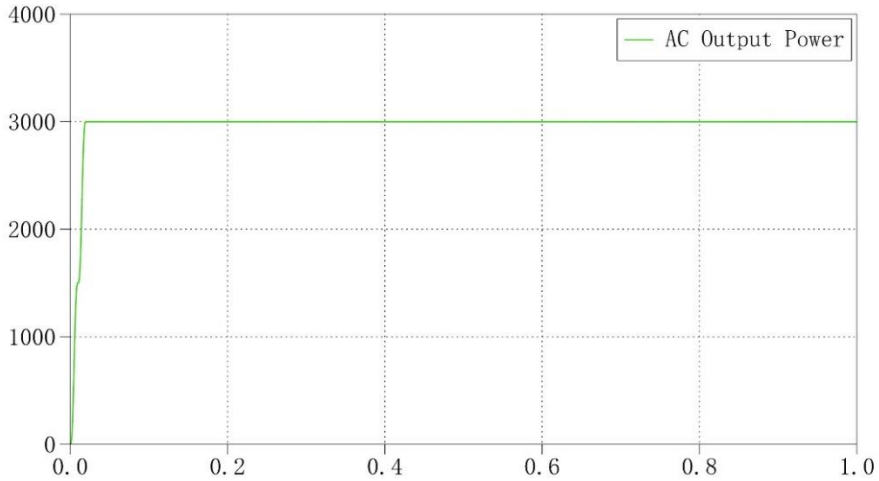

Figure 1.8 Power exchanged from inverter to AC grid

1.3 Verification of Inductor Design

The schematic to verify the inductor design is shown in **Figure 1.9**.

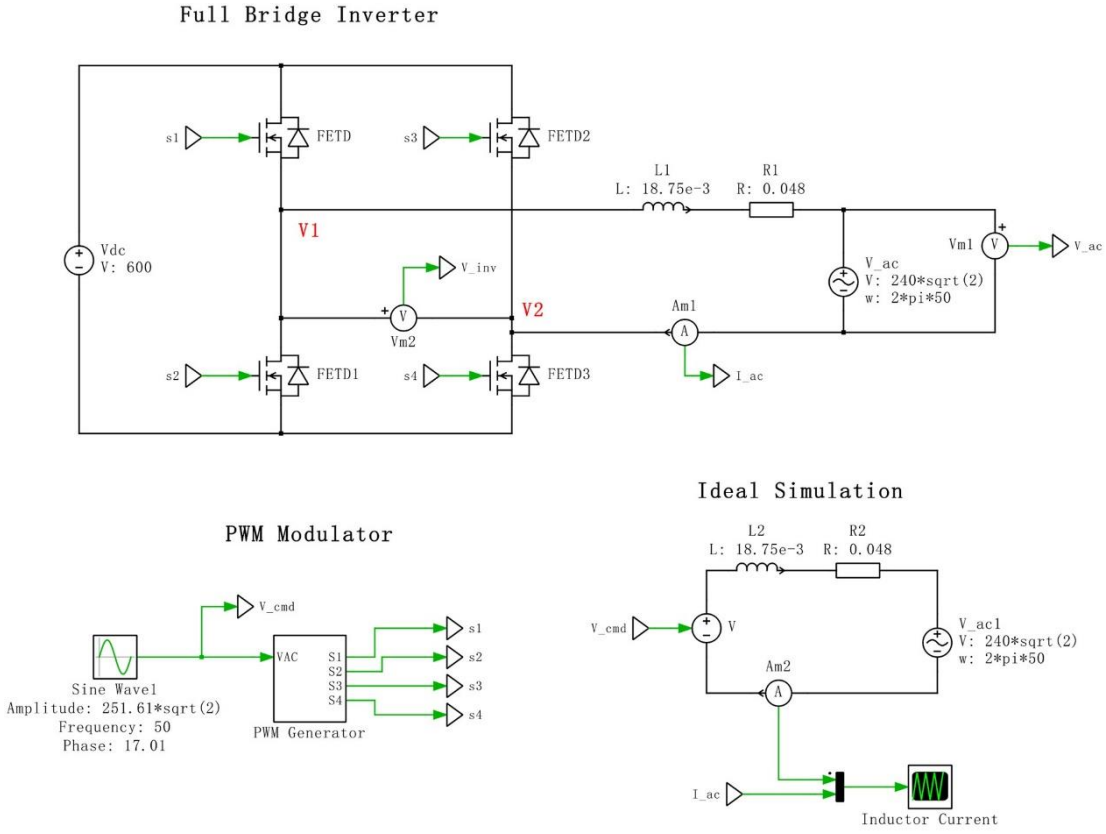

Figure 1.9 Schematic to Verify the Inductor Design

The current of inductor is shown in **Figure 1.10** below. It can be observed that the peak value of inductor current (in inverter) is $12.5\sqrt{2}\,A$, and its waveform is very consistent with the ideal waveform, which all indicate that the result aligned with the prediction.

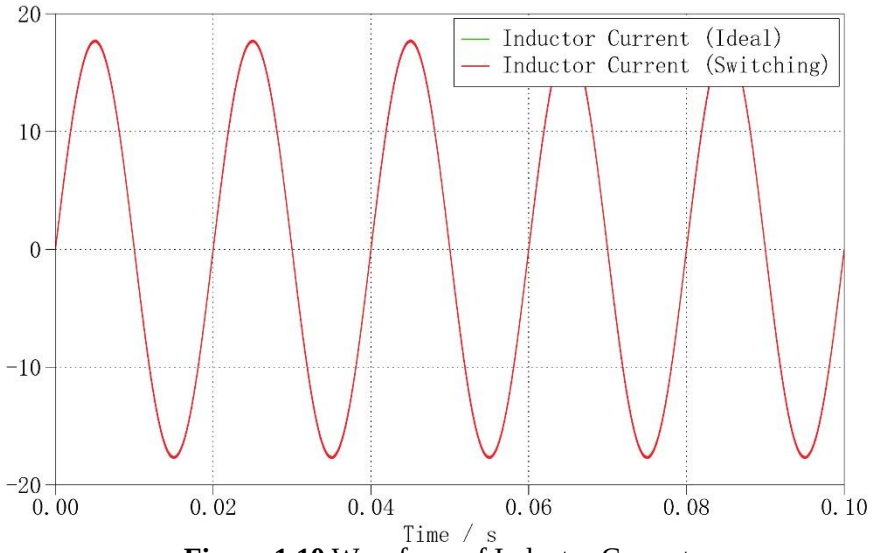

Figure 1.10 Waveform of Inductor Current

According to *Eqn.1.2* that used to calculate the inductance in Coursework 1, the maximum ripple would occur at half of the DC voltage, which is 300 V. Zooming in the ripple there, which is shown in **Figure 1.11**.

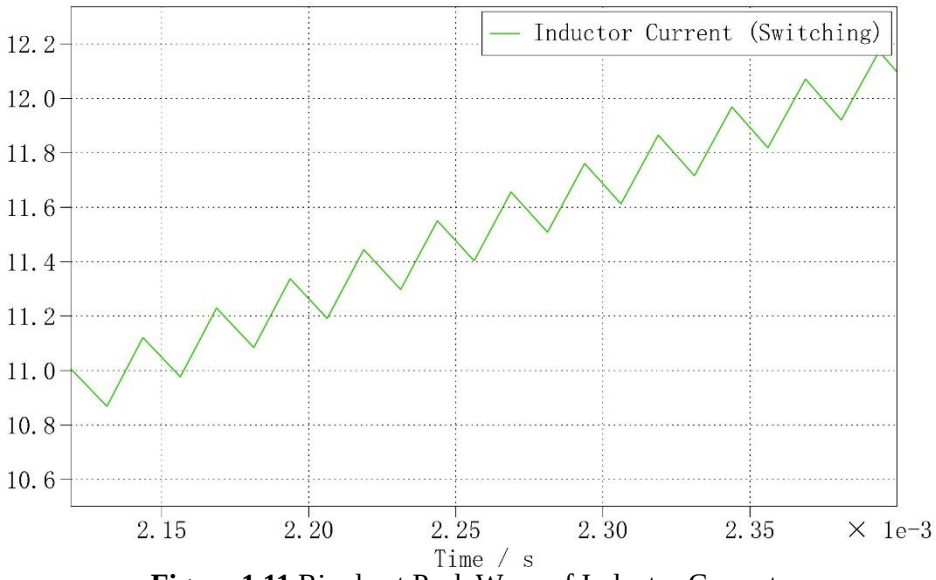

Figure 1.11 Ripple at Peak Wave of Inductor Current

According to the measurement of cursor, the maximum ripple (peak-peak) is about 0.147 A, which meets the design specification that current ripple is less than 0.2 A.

2. Current Controller

The settling time of current controller is set to be 1.5 ms, thus its transfer function is same with the one in Coursework 1. The schematic of full switching model with current controller is shown in **Figure 2.1** below.

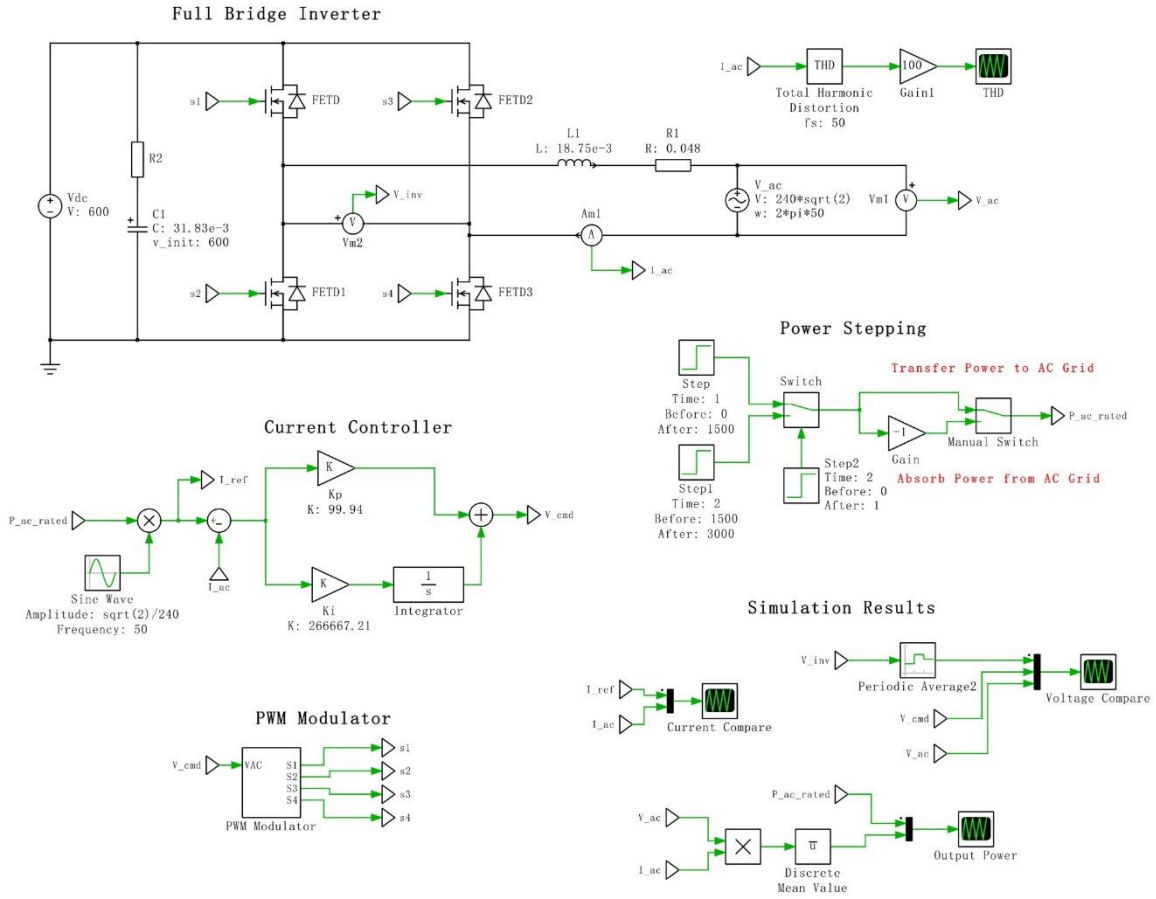

Figure 2.1 Switching Model with Current Controller and Power Stepping

The 'PWM Modulator' is given in **Figure 2.2** below.

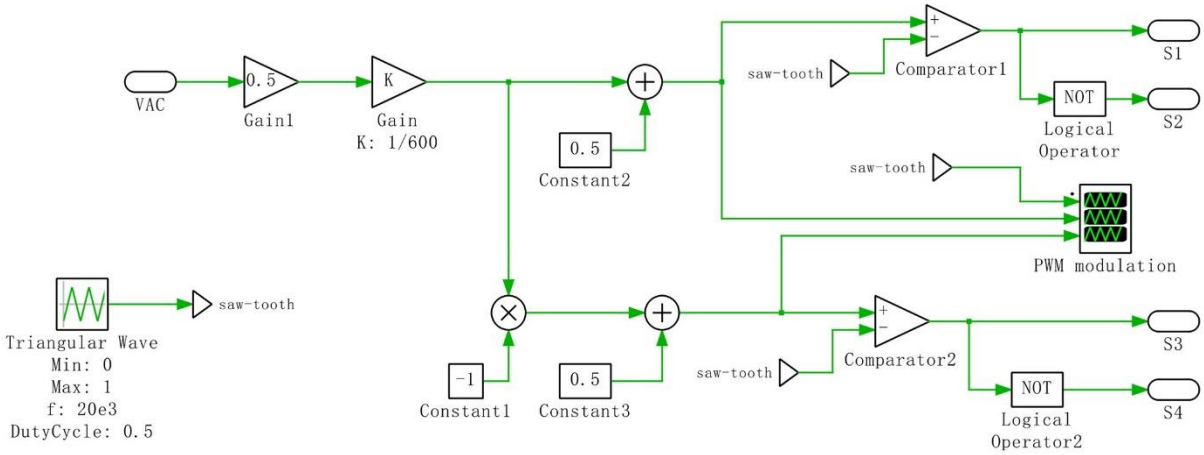

Figure 2.2 PWM Modulator Subsystem

The value of DC-link capacitor is 31.83 mF, according to the result given in *Eqn.3.1* in Coursework 1. Given the power stepping from zero to half of the rated power (1.5 kW), and then from 1.5 kW to 3 kW, the result is presented in **Figure 2.3**.

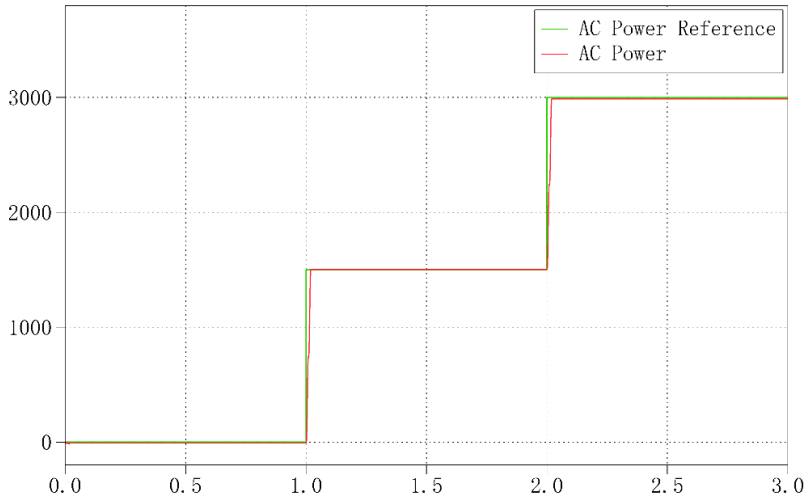

Figure 2.3 Transfer Power (0 to P/2 to P) to AC Grid

Modifying the reference AC power stepping to negative values, the inverter could be proven having the ability to absorb power from AC grid. The result is presented in **Figure 2.4**.

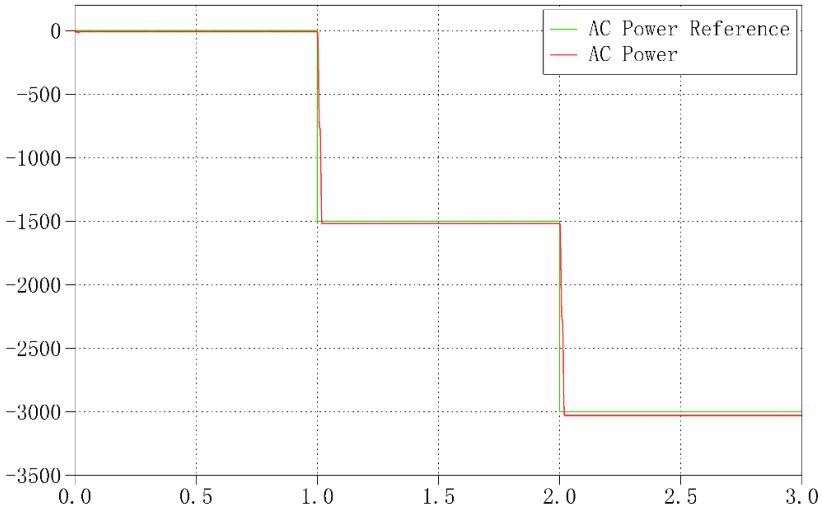

Figure 2.4 Absorb Power (0 to -P/2 to -P) from AC Grid

Changed the time interval of power stepping (0 to P/2 to P) from 1 s to 0.1 s to better demonstrate the transient state of AC current, the result is presented in **Figure 2.5** below.

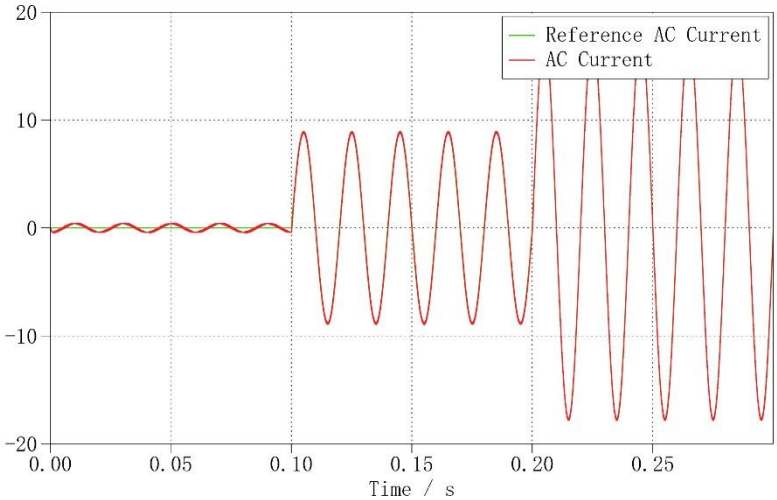

Figure 2.5 Transient State of AC Grid Current and Reference Current (0 to P/2 to P)

In the case of absorbing power from AC grid to inverter, the AC current would be inverted when applying the power stepping of '0 to -P/2 to -P'. The result of is presented in **Figure 2.6**.

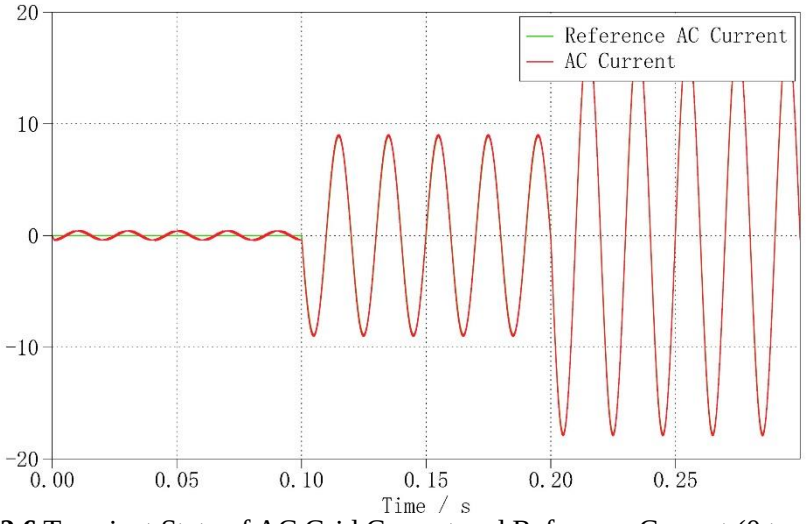

Figure 2.6 Transient State of AC Grid Current and Reference Current (0 to -P/2 to -P)

Total Harmonic Distortion (THD) measurement is used to analyse the harmonics of AC current. It indicates how much the waveform deviates from the ideal sinusoidal waveform due to the presence of harmonics. A lower THD value means the signal is closer to a pure sine wave, indicating better quality and less distortion. In addition, THD is usually expressed as a percentage of the total signal. In the schematic shown in **Figure 2.2**, a '100' gain is added to present THD in percentage scale.

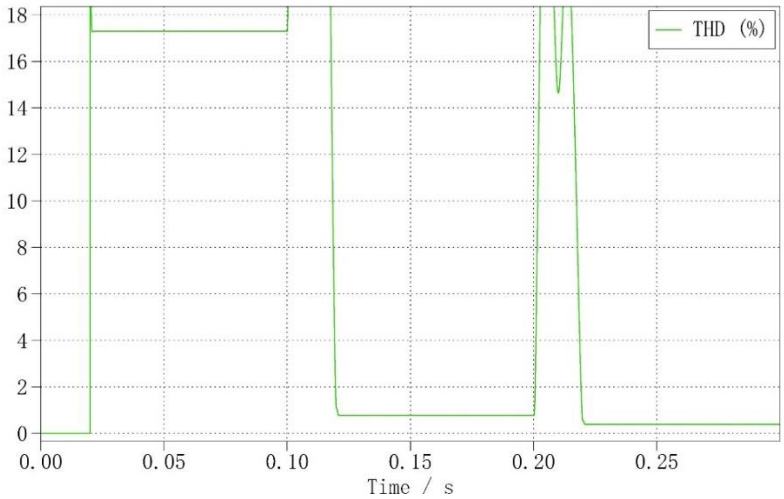

Figure 2.7 Total Harmonic Distortion of AC Current

When the rated power is zero, the value of THD is 17.27%, indicating poor quality of signal and large distortion. When the rated power is 1.5 kW and 3 kW, the THD is 0.77% and 0.39% respectively, which indicates very good quality of signal and little distortion.

3. Capacitor Implementation and Voltage Controller

3.1 Voltage Controller Design

The settling time of voltage controller should be at least 10 times larger than the settling time of current controller (1.5 ms). Assuming the settling time for voltage controller is 150 ms, the damping ratio ζ and natural frequency ω_n can be given by:

$$t_s = \frac{4}{\zeta \omega_n} = 150\, ms \;\Rightarrow\; \zeta = 0.707, \omega_n = 37.7124\, rad/s \qquad \textit{Eqn.3.1}$$

Then, according to the *Eqn.4.2* in Coursework 1, the values of PI controller's parameter could be given by:

$$K_P = C\zeta\omega_n = 0.8487,\ K_I = \frac{C\omega_n^2}{2} = 22.6347 \qquad \textit{Eqn.3.2}$$

Thus, the voltage controller could be given by:

$$G_C(s) = \frac{0.8487s+22.6347}{s} \qquad \textit{Eqn.3.3}$$

3.2 Verification in MATLAB

Setting the settling time to less than 150 ms, damping ratio larger than 0.707, and natural frequency to at least 37.7124 rad/s, the root locus of voltage controller is shown in **Figure 3.1**.

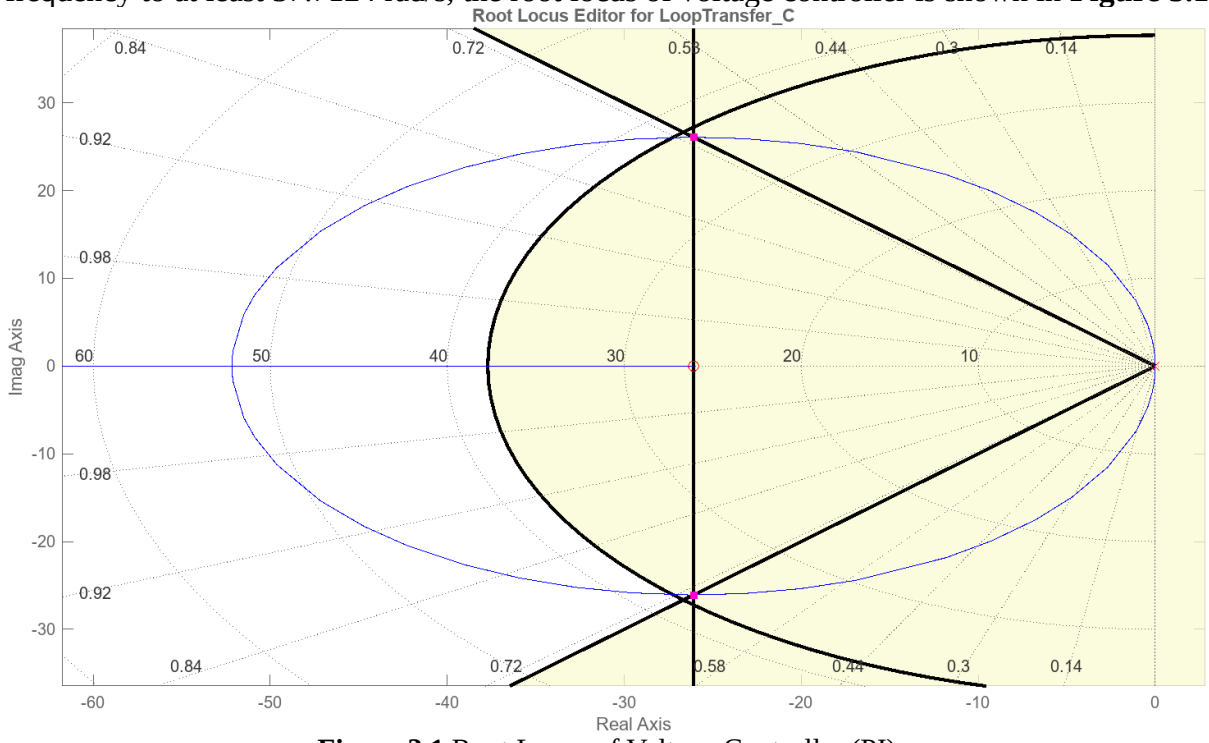

Figure 3.1 Root Locus of Voltage Controller (PI)

The transfer function of PI controller is given as following in MATLAB.

$$G_C(s) = \frac{0.82937(s+26.08)}{s} = \frac{0.82937s+21.63}{s} \qquad \textit{Eqn.3.4}$$

The result above is quite similar to the Eqn.3.3, which means the design of voltage controller can meet the requirements.

3.3 Verification Schematic

The verification schematic of voltage controller and capacitor implementation is presented in **Figure 3.2** below. The DC voltage source is replaced by a current source in parallel with a capacitor. A 'Manual Switch' is used to switch between constant current and stepping current. As the DC voltage is set to 600 V, to implement 'Power Stepping' of '0 to 1.5 kW to 3 kW', the 'Current Stepping' should be set to '0 to 2.5 A to 5 A'. The power transferred to AC grid can be approximated to the input power of DC source, if the power loss in resistor is not considered.

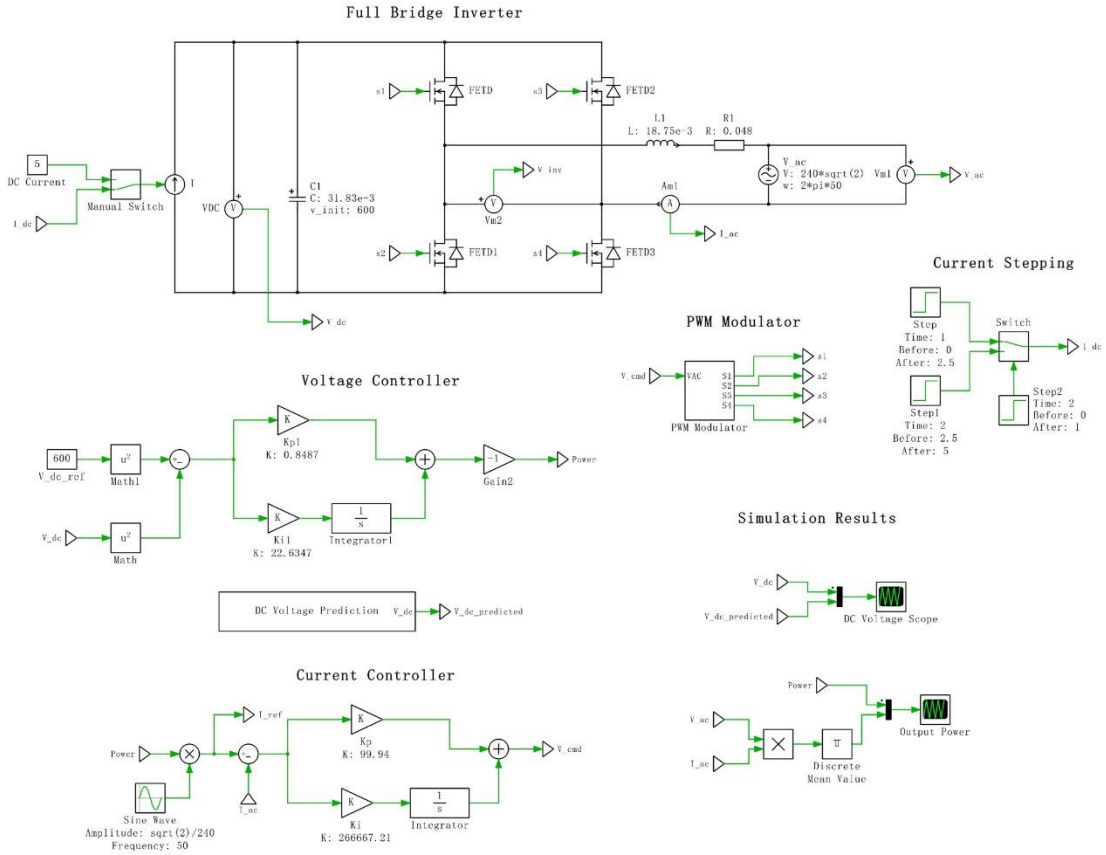

Figure 3.2 Verification Schematic of Voltage Controller and Capacitor Implementation

The 'DC Voltage Prediction' module is shown in **Figure 3.3**, the capacitor is represented in transfer function form.

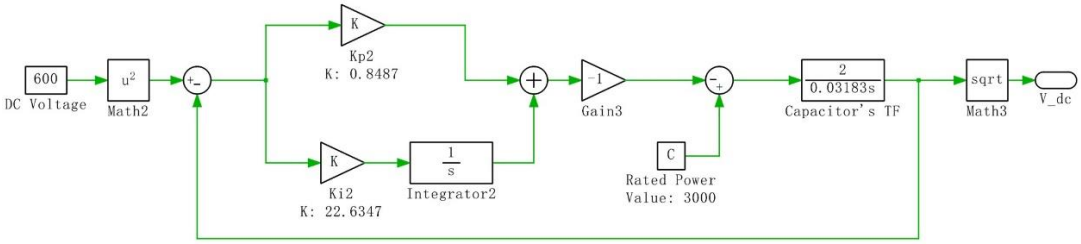

Figure 3.3 The 'DC Voltage Prediction' Module

When selecting the value of current source to be 5 A, the DC voltage across the capacitor (initial voltage is set to 600V) is shown in **Figure 3.4** below.

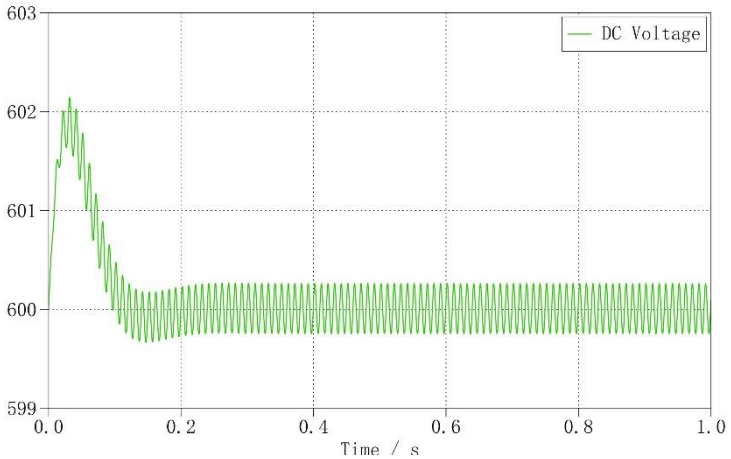

Figure 3.4 DC Voltage across the Capacitor

Comparation of predicted DC voltage and measured DC voltage is presented in **Figure 3.5**.

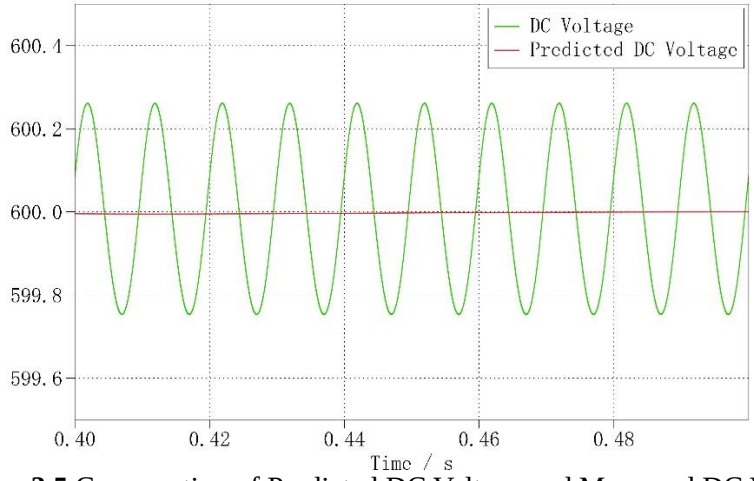

Figure 3.5 Comparation of Predicted DC Voltage and Measured DC Voltage

The ripple of DC voltage is measured to be less than 0.5 V and averaged voltage would be stabilized at 600 V, which meets the design requirements. After switching the 'Manual Switch' to current stepping, the transient state of DC voltage is presented in **Figure 3.6** below.

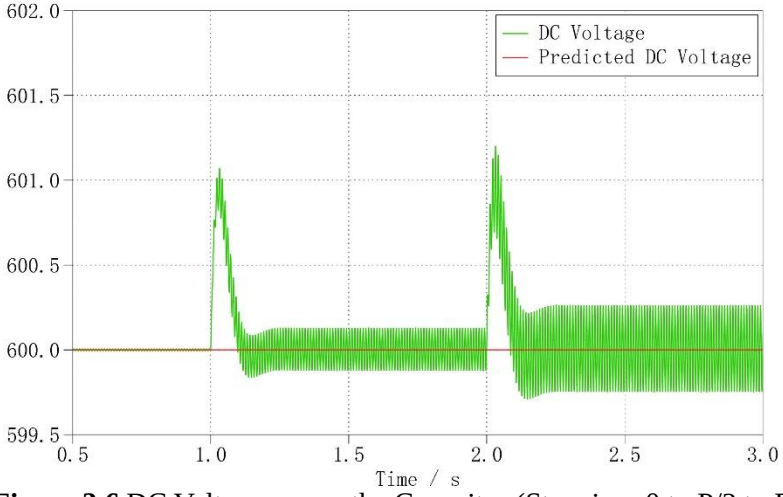

Figure 3.6 DC Voltage across the Capacitor (Stepping: 0 to P/2 to P)

Although the DC voltage would be temporarily unstable after stepping, it is still stabilized at 600 V. The AC power stepping is shown in **Figure 3.7** below.

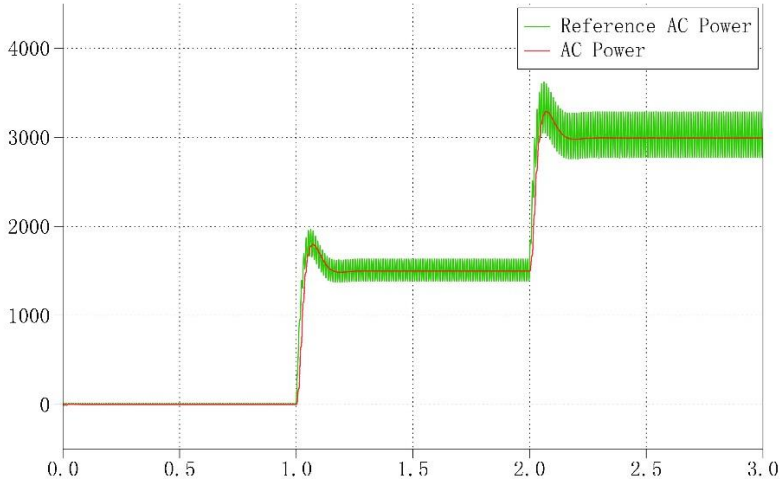

Figure 3.7 AC Power Stepping (0 to P/2 to P)

When the reference power is 1.5 kW, the cursor's measurement of AC power is 1497.49 W, and when the reference power is 3 kW, the AC power is measured to be 2991.86 W. Both of them contains a 'steady state error' compared to the reference, which could be caused by the power loss in the resistor (0.25% P).

3.4 Alternative: Lag Compensator

Set the settling time of lag compensator to 150 ms, the design specifications are given in *Eqn.3.1*, which is damping ratio $\zeta = 0.707$ and natural frequency $\omega_n = 37.7124\ rad/s$. The 'p' and 'z' can be expressed by:

$$p = 2\zeta\omega_n - 62.83k,\ \ z = \frac{\omega_n^2}{62.83k} \qquad \textit{Eqn.3.5}$$

Assuming the value of 'k' is 0.8, the values of 'p' and 'z' of $G_{lag}(s)$ could be given by:

$$p = 3.061,\ \ z = 28.295 \qquad \textit{Eqn.3.6}$$

Overall, the transfer function of 'Lag Compensator' could be expressed by:

$$G_{lc}(s) = \frac{k(s+z)}{s+p} = \frac{0.8(s+28.295)}{s+3.061} \qquad \textit{Eqn.3.7}$$

Setting the settling time to less than 150 ms, damping ratio larger than 0.707, and natural frequency to at least 37.7124 rad/s, the root locus of voltage controller is shown in **Figure 3.8**.

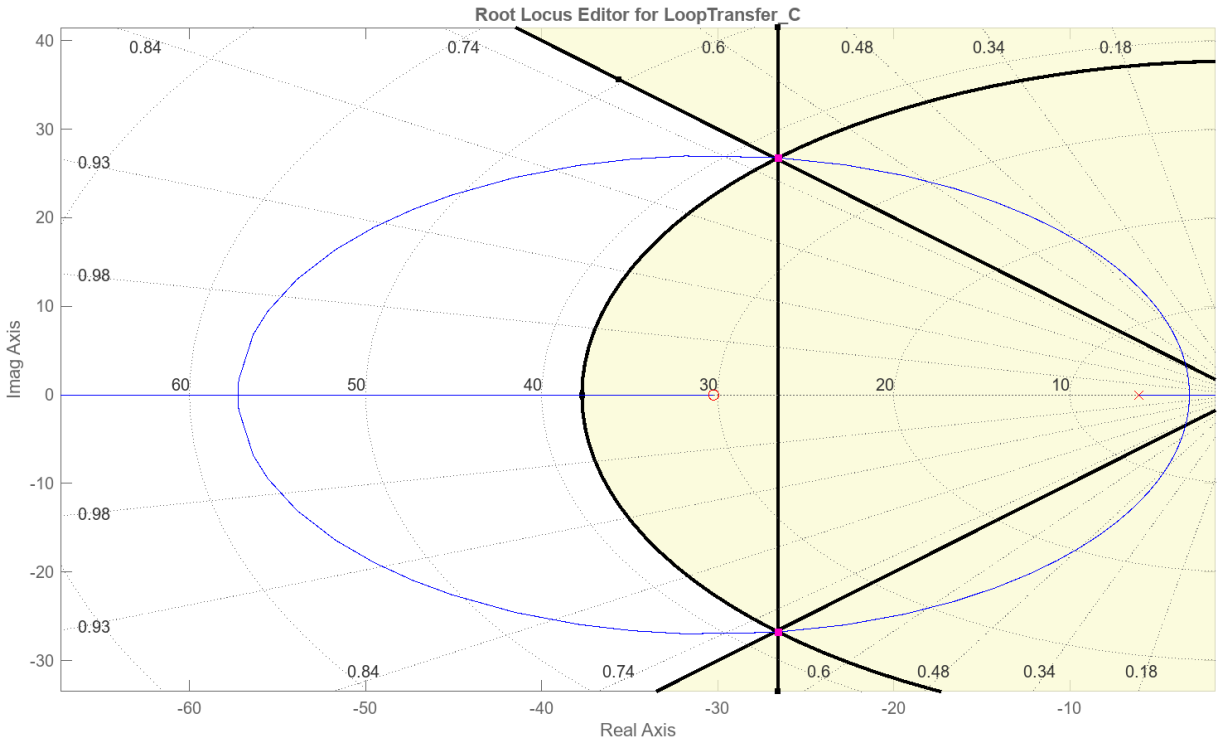

Figure 3.8 Root Locus of Lag Compensator

The transfer function of lag compensator is given as following in MATLAB.

$$G_{lag}(s) = \frac{0.74878(s+30.23)}{s+6.079} \qquad \textit{Eqn.3.8}$$

Replaced the PI controller with the transfer function of lag compensator in voltage controller. The simulation results of DC voltage and AC power are similar to **Figure 3.6** and **Figure 3.7**.

3.5 Controller Designed with Different Settling Time

In previous section, voltage controller is designed based on the settling time of 150 ms, which is 100 times of the settling time used in current controller design (1.5 ms). There is a general rule that the settling time of outer control loop (voltage controller) should be at least ten times of inner control loop (current controller), so 15 ms settling time and 1500 ms settling time might also can be considered in voltage controller design. Assuming the PI controller is used, the transfer function of '15 ms settling time design' and '1500 ms settling time design' can be expressed by:

$$G_{C\_15ms}(s) = \frac{8.487s+2263.47}{s} \qquad Eqn.3.9$$

$$G_{C\_1500ms}(s) = \frac{0.08487s+0.226347}{s} \qquad Eqn.3.10$$

Changed the time interval of stepping in **Figure 3.2** to 3 seconds, the power responses are presented in **Figure 3.9** below.

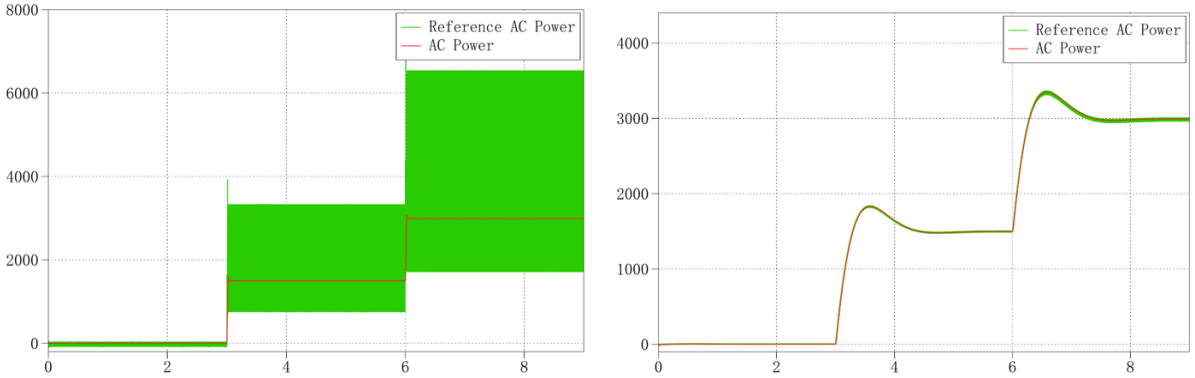

Figure 3.9 Power Stepping of '15 ms design' and '1500 ms design'

Compare to the result shown in **Figure 3.7**, the voltage controller designed based on '15 ms settling time' contains much more severe oscillations in reference power, but much less overshoot in transferred AC power. The instability of this system could be due to the response speed of voltage controller (outer control loop) is too fast to leave time for current controller (inner control loop) to stabilize.

The voltage controller designed based on '1500 ms settling time' contains less ripple compared to result shown in **Figure 3.7**, but it takes much longer time to stabilize, which could be due to the response speed of voltage controller is too slow. In addition, the response also contains larger overshoot.

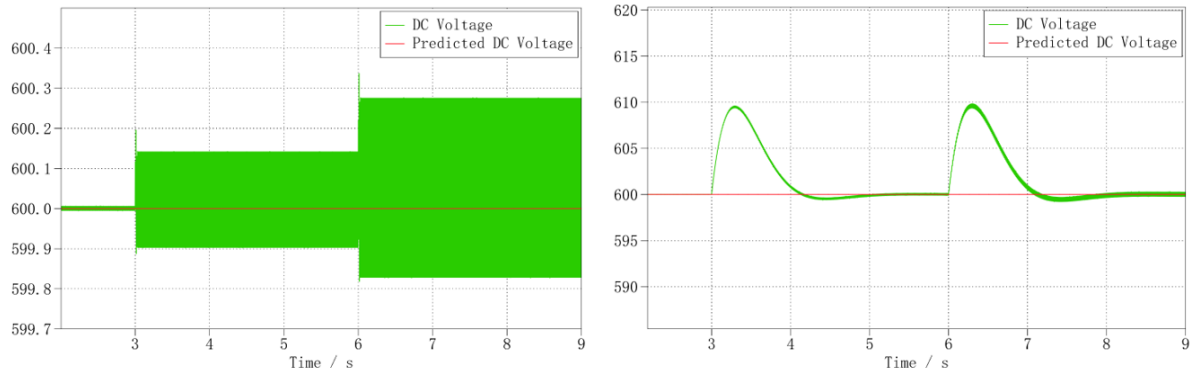

Figure 3.10 DC Voltage of '15 ms design' and '1500 ms design'

The transient state of DC voltage is presented in **Figure 3.10**. In conclusion, the controller with larger settling time contains larger overshoot and slower speed of response.