Average Design, Modelling and Control of Full Bridge Inverter

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1. LR Filter Design

1.1 Parameter Calculation

The RL filter should be developed first before the controller design. To obtain the value of inductor, the maximum current ripple across the inductor should be identified first. As the frequency of the inverter's output voltage is $2f_s$, the maximum switching 'ON' time would be $\frac{T_s}{4}$, when the duty cycle can be approximated by 0.5. The expression of current ripple could be given by:

$$\Delta I = \frac{V_{DC}}{2} \cdot \frac{1}{L} \cdot \frac{T_s}{4} = 0.2\ A \qquad Eqn.1.1$$

Thus, the value of inductor L could be calculated by:

$$L = \frac{V_{DC}}{8 f_s \Delta I} = \frac{600V}{8 \cdot 20\ kHz \cdot 0.2\ A} = 18.75\ mH \qquad Eqn.1.2$$

In realistic, the inductor has parasitic resistance, which will cause loss within it.

$$P_{loss} = 0.25\%P = I_{L(RMS)}^2 R = 7.5\ W \qquad Eqn.1.3$$

$$I_{L(RMS)} = \frac{P}{V_{L(RMS)}} = \frac{3000\ W}{240\ V} = 12.5\ A \qquad Eqn.1.4$$

Thus, the value of the parasitic resistance could be given by:

$$R = \frac{P_{loss}}{I_{L(RMS)}^2} = \frac{7.5\ W}{(12.5\ A)^2} = 0.048\ \Omega \qquad Eqn.1.5$$

The simplified schematic diagram and phasor diagram are shown in the **Figure 1.1** below.

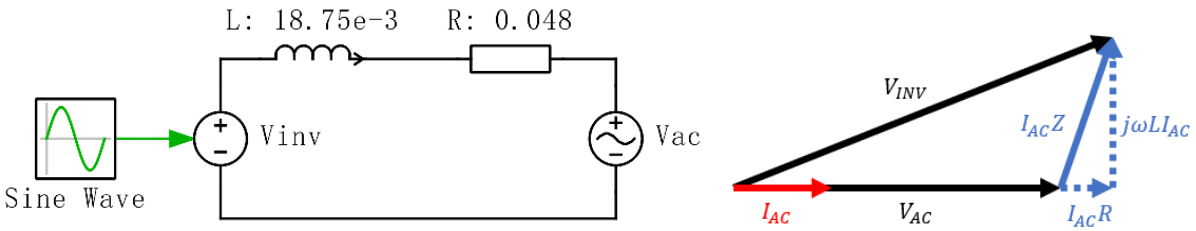

Figure 1.1 Simplified Schematic and Phasor Diagram

The phasor expression of RL impedance Z could be given by:

$$Z = R + j\omega L = 0.048 + 5.89j = 5.89\Omega\angle 89.53° \qquad Eqn.1.6$$

Thus, the phasor expression of inverter output voltage V_{INV} could be given by:

$$\widetilde{V_{INV}} = \widetilde{V_{AC}} + I_{AC}\tilde{Z} = 240V\angle 0° + 12.5A\angle 0° \cdot 5.89\Omega\angle 89.53° \qquad Eqn.1.7$$

$$\widetilde{V_{INV}} = 251.61\ V\angle 17.01° \qquad Eqn.1.8$$

1.2 Verification in PLECS

Verifying the above parameters in simulation, the schematic is shown in **Figure 1.2** below.

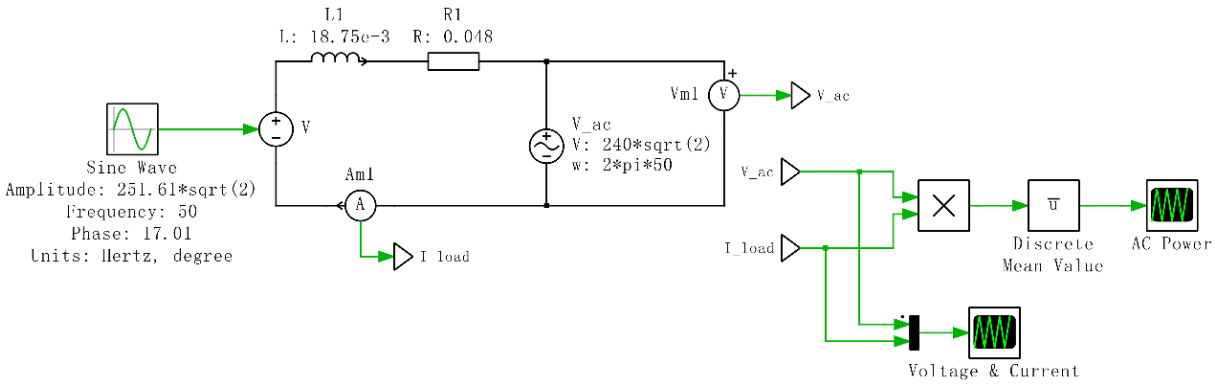

Figure 1.2 Verification Circuit of RL Filter

A 'Discrete Mean Value' module has been used to obtain the averaged AC power, the 'sample time' has been set to be 0.0002 and 'number of samples' has been set to be 100 to ensure the fundamental frequency is 50 Hz. The waveform output power to the AC grid is shown in **Figure 1.3**, and the waveform of AC voltage and current are shown in **Figure 1.4**.

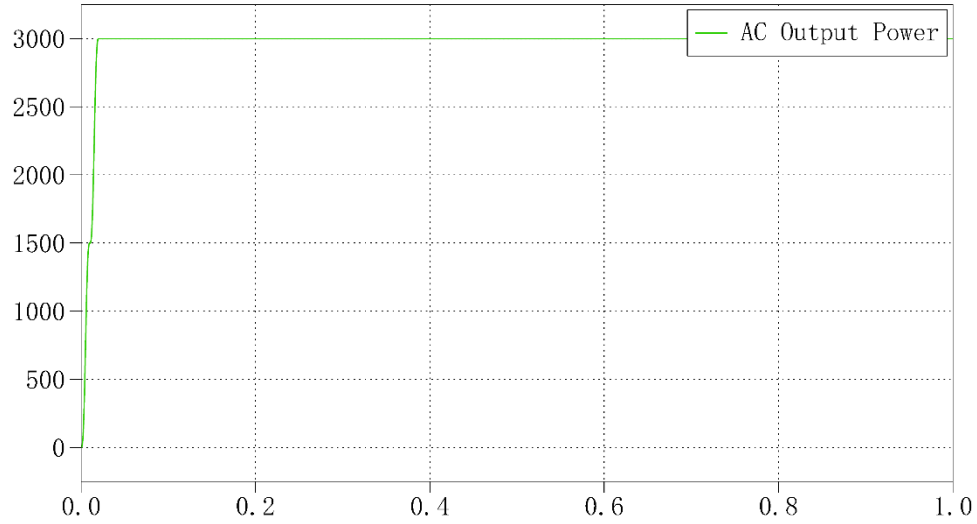

Figure 1.3 Waveform of AC Output Power (to the grid)

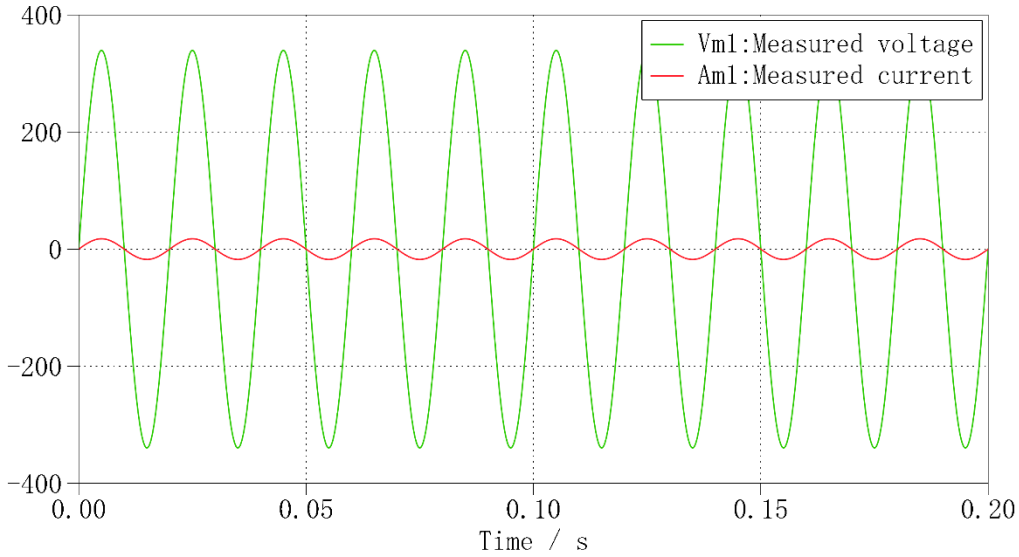

Figure 1.4 Waveform of AC Voltage and Current

It can be observed from **Figure 1.3** that the cursor reading of the AC output power at steady state is 2998.96 W, which is quite closed to the required 3 kW. The reason for the power reading is slightly lower than 3 kW could be due to the decimal rounding error of calculated inverter output voltage V_{INV}. In addition, the cursor reading of AC voltage and current in **Figure 1.4** are 339.411 V and 17.6722 A respectively, which is almost equal to the required voltage peak of $240\sqrt{2}\,V$ and current peak of $12.5\sqrt{2}\,A$.

2. Current Controller Design

2.1 Parameter Calculation

According to the required settling time of inverter t_s, specification of controller design could be given in *Eqn.2.1*, where the damping ratio ζ determines the degree of overshoot in a step response, and natural frequency ω_n determines the speed of response.

$$t_s = \frac{4}{\zeta\omega_n} = 1.5\,ms \;\Rightarrow\; \zeta = 0.707, \omega_n = 3771.24\,rad/s \qquad \textit{Eqn.2.1}$$

The transfer function of RL filter $G_F(s)$ could be given by:

$$G_F(s) = \frac{1}{Ls+R} \qquad \textit{Eqn.2.2}$$

It can be seen that the RL filter is a 1st order type 0 plant, so PI controller could be used as the current controller. The transfer function of current controller could be given by:

$$G_c(s) = \frac{K_P(s+a)}{s}\ \left(a = \frac{K_I}{K_P}\right) \qquad \textit{Eqn.2.3}$$

The control diagram could be represented in **Figure 2.1** below.

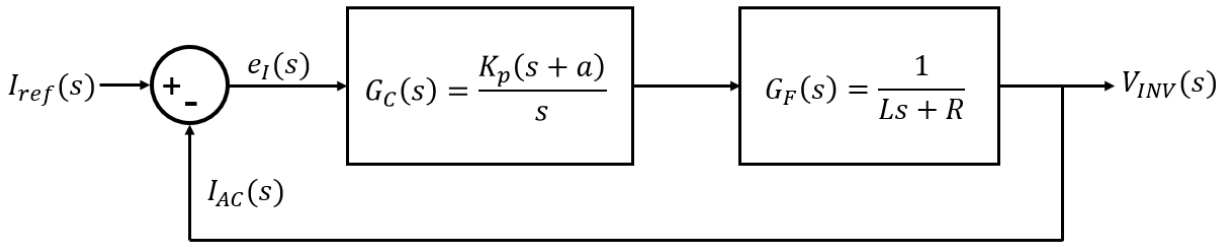

Figure 2.1 Control Diagram of Current Controller (Closed Loop)

The open loop transfer function could be given by:

$$G_o(s) = G_C(s)\cdot G_F(s) = \frac{K_P(s+a)}{s}\cdot\frac{1}{Ls+R} = \frac{K_P(s+a)}{Ls^2+Rs} \qquad \textit{Eqn.2.4}$$

Thus, the expression of the above closed loop system could be represented by:

$$G_{cl}(s) = \frac{Go(s)}{1+Go(s)} = \frac{\frac{K_p}{L}(s+a)}{s^2+\frac{R+K_P}{L}s+\frac{K_P\cdot a}{L}}\ \left(a = \frac{K_I}{K_P}\right) \qquad \textit{Eqn.2.5}$$

As the general transfer function of 2nd order system could be represented by:

$$G(s) = \frac{\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2} \qquad \textit{Eqn.2.6}$$

Comparing *Eqn.2.5* and *Eqn.2.6*, expression of PI controller's parameter (K_P and K_I) could be

obtained as below.

$$K_P = 2\zeta\omega_n L - R,\ K_I = \omega_n^2 L \qquad Eqn.2.7$$

According to the design specification identified in *Eqn.2.1,* the values of PI controller's parameter could be given by:

$$K_P = 2\zeta\omega_n L - R = 99.94,\ K_I = \omega_n^2 L = 266667.21 \qquad Eqn.2.8$$

Thus, the current controller could be given by:

$$G_C(s) = \frac{99.94(s+2668.27)}{s} \qquad Eqn.2.9$$

2.2 Verification in MATLAB

Use 'sisotool' in MATLAB to verify the current controller parameters, the procedure could be divided into four steps:

1. Enter the transfer function of the plant as parameter of 'sisotool'.
2. Add an integrator and a real zero to form a PI controller.
3. Specify the design specifications (damping ratio, natural frequency, settling time).
4. Move the zeros and poles to obtain the transfer function of designed controller.

Then, the root locus of the current controller could be given, which is shown in **Figure 2.2** below.

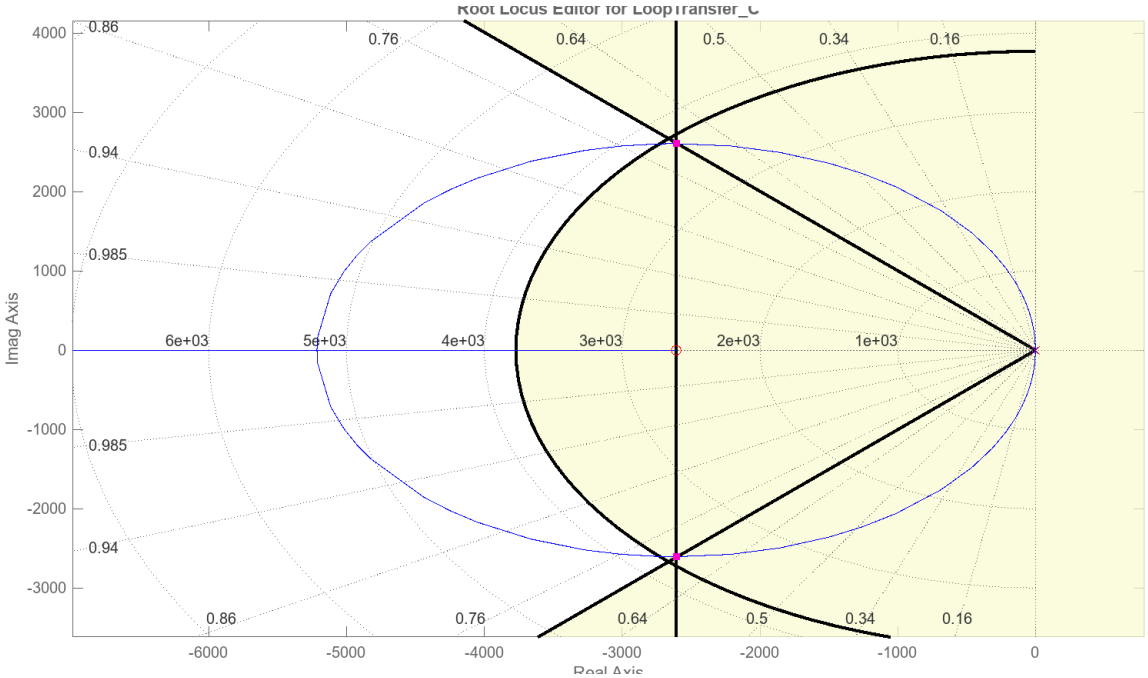

Figure 2.2 Root Locus of the Designed Current Controller

According to the result in MATLAB, the transfer function of current controller could be expressed by following equation, whose value is quite close to the calculated parameters.

$$G_C(s) = \frac{97.748(s+2608)}{s} \qquad Eqn.2.10$$

The step response of current controller is shown in the **Figure 2.3**, which meets the design requirement of settled within 1.5 ms.

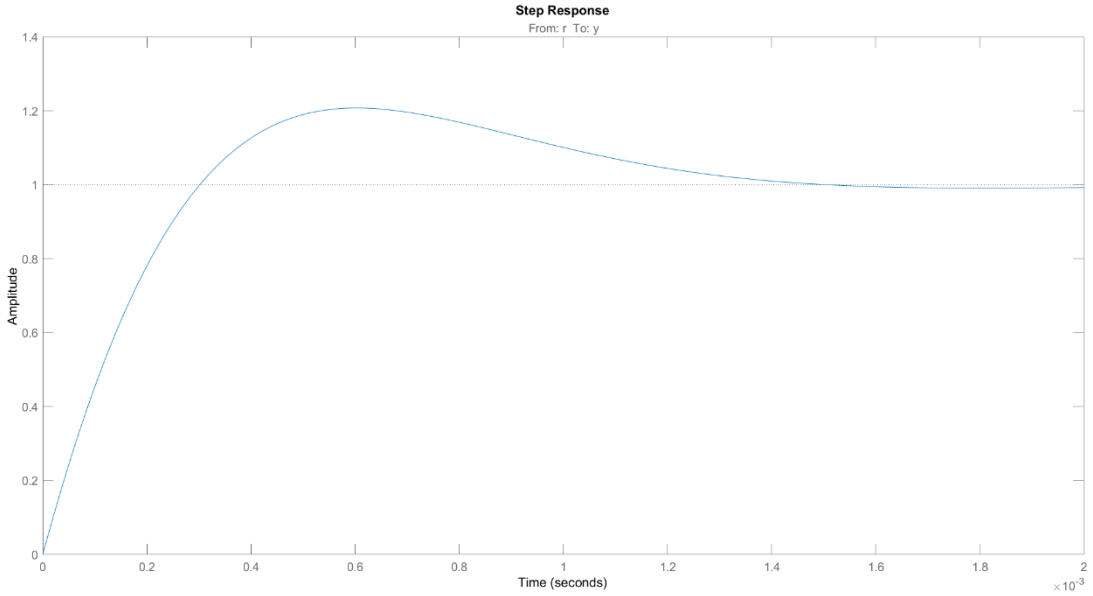

Figure 2.3 Step Response of Current Controller

2.3 Verification in PLECS

To verify the performance of current controller, the inverter was tested under different power levels, ranging from 1 kW to 3kW. The overall testing schematic of current controller is shown in **Figure 2.4** below.

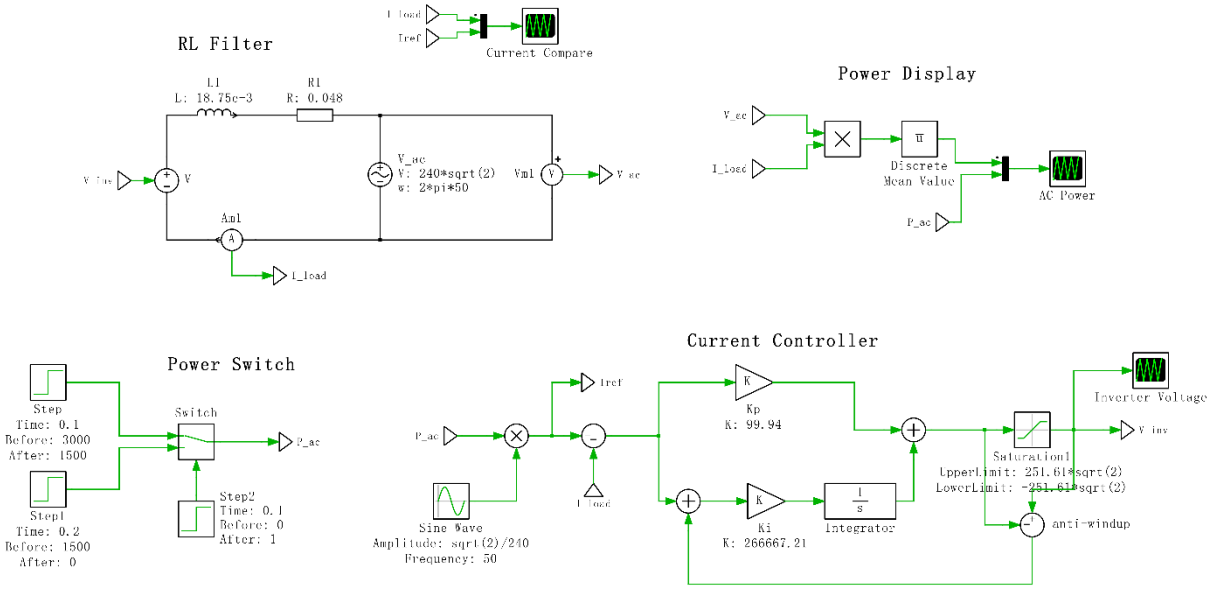

Figure 2.4. Verification Circuit of Current Controller

The RMS value of reference current I_{ref} is derived from the rated power P divided by the AC voltage RMS value (240 V). The difference value between I_{ref} and AC current I_{AC} can be referred as 'error', which is also the input of current controller. A 'saturation' module is used to set limit to the output (the inverter voltage, limited within $-251.61\sqrt{2}\,V$ to $251.61\sqrt{2}\,V$). A 'anti-windup' feedback loop is also added to the integrator to prevent closed-loop instability. The waveform of reference power and AC output power are compared in **Figure 2.5** below.

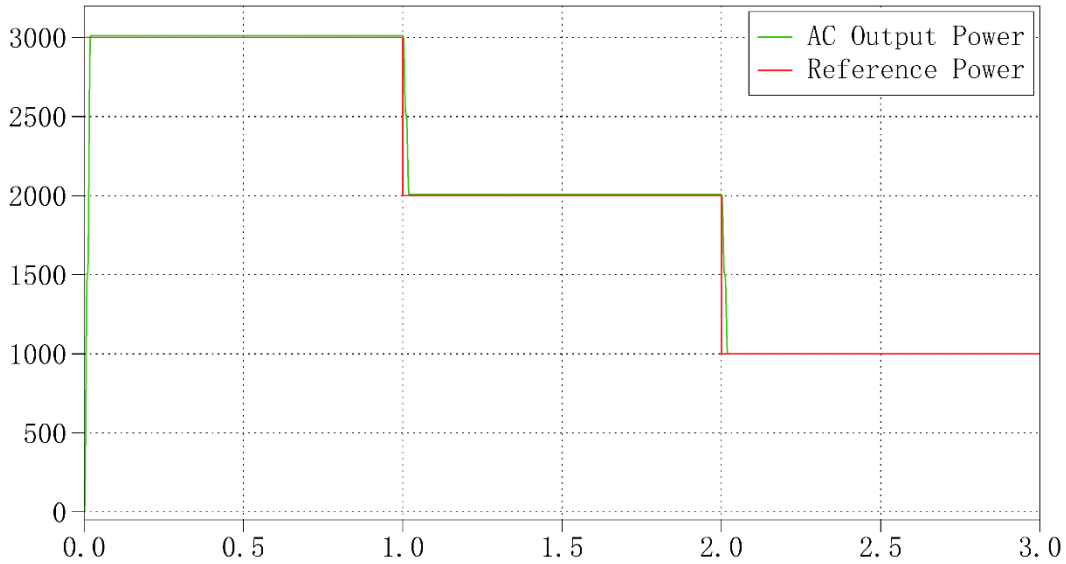

Figure 2.5 Comparison between Reference Power and AC Output Power

It can be seen that the AC output power fitting well with different reference power without significant overshoot, which means the inverter can operate at different power levels, and the current controller has a good performance in speed of response and suppressing overshoot. In addition, the waveforms of AC current are also fitting well with the reference current. The results are presented in **Figure 2.6**.

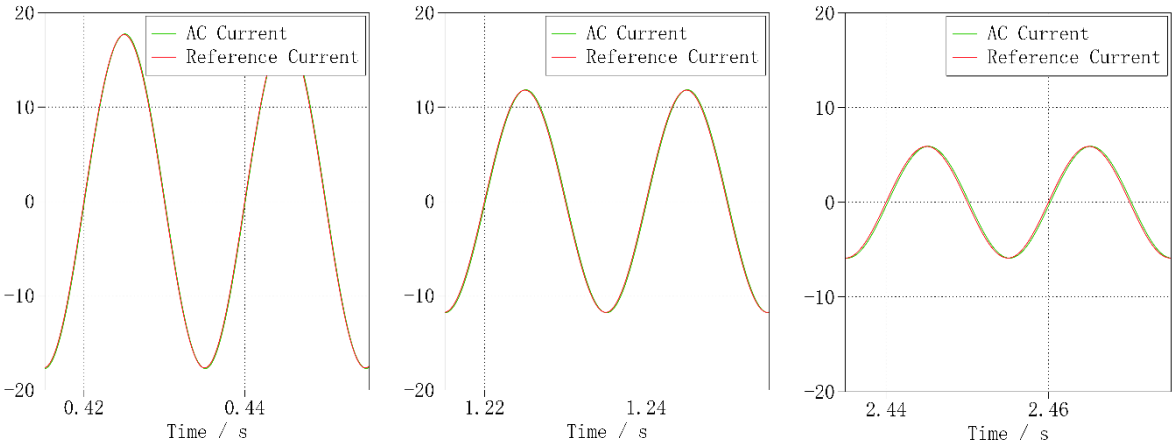

Figure 2.6 Waveforms of AC Current under 3 kW, 2 kW, 1 kW Power Level

The inverter is required to be bi-directional, which means it can transmit power as well as absorb power. From the result in **Figure 2.5**, it is clear that the inverter has the ability to transmit power. By modifying the reference power to negative values, the inverter would be proven having the ability to absorb power. The result is presented in **Figure 2.7**.

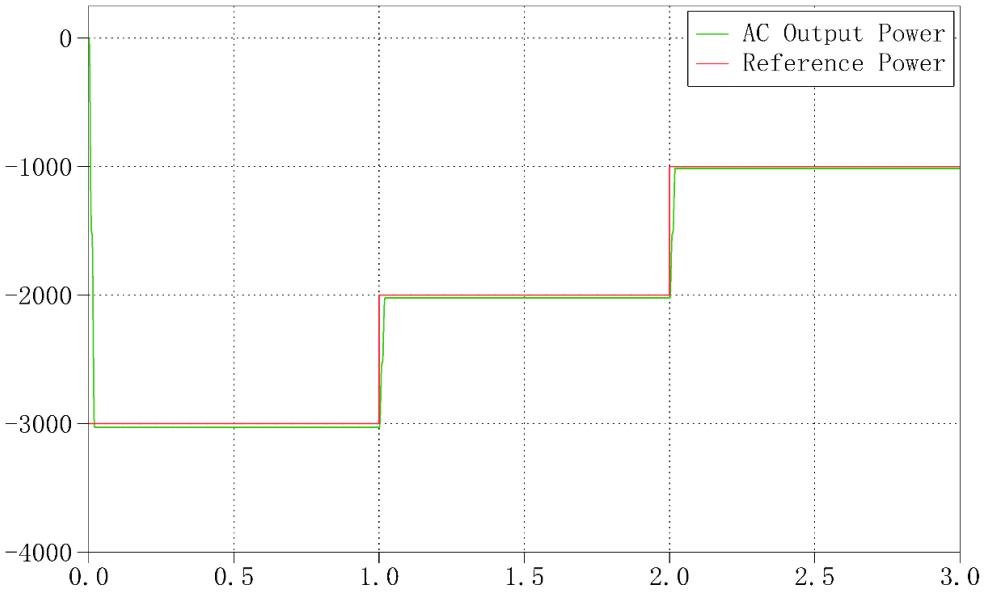

Figure 2.7 Comparison between Negative Reference Power and AC Output Power

The AC output power fitting well with different negative reference power, which means the inverter can also absorb power from AC grid.

3. DC-Link Capacitor Design

3.1 Parameter Calculation

In reality, A DC-Link capacitor is needed to decouple the DC and AC circuit. The value of DC-Link capacitance could be given by:

$$C = \frac{\hat{V}\hat{I}}{4\omega V_{DC} V_{DC(peak)}^{ripple}} = \frac{240\sqrt{2}\,V \cdot 12.5\sqrt{2}\,A}{4 \cdot 2\pi \cdot 50Hz \cdot 600V \cdot 0.25V} = 31.83\,mF \qquad Eqn.3.1$$

The energy stored in the capacitor could be given by:

$$E_C = \frac{1}{2}CV_{DC}^2 \;\Rightarrow\; V_{DC}^2 = \frac{2}{C}E_C = \frac{2}{sC}P_C \qquad Eqn.3.2$$

The power flows from DC source to capacitor and AC grid, which can be represented by:

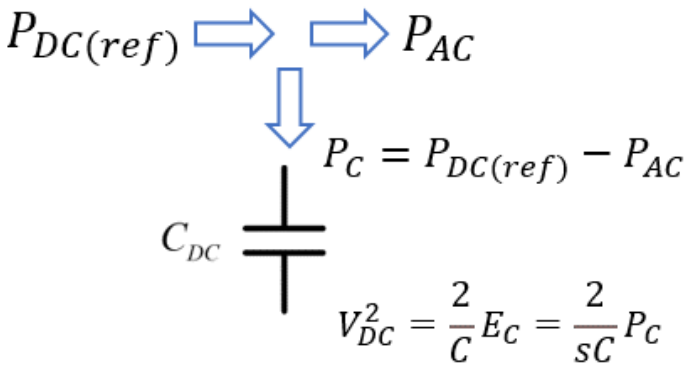

Figure 3.1 Power Flow within Inverter

3.2 Control Diagram

The open loop control diagram of DC-Link capacitor could be represented by:

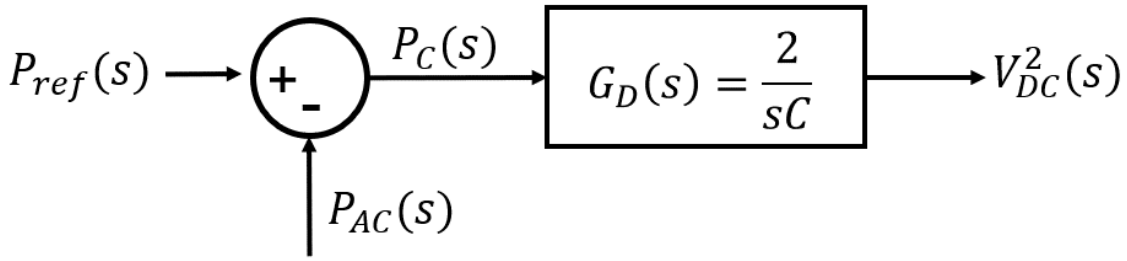

Figure 3.2 Open Loop Control Diagram of DC-Link Capacitor

The reason why the DC-Link capacitor should be kept in transfer function form is that the DC voltage source and the full bridge inverter is represented by a 'Sine Wave Generator' controlled voltage source, while the capacitor should be placed between the DC source and the inverter.

4. Voltage Controller Design

4.1 Parameter Calculation

A voltage controller should be added to keep the voltage across the capacitor to be constant, so the closed loop control diagram could be represented by:

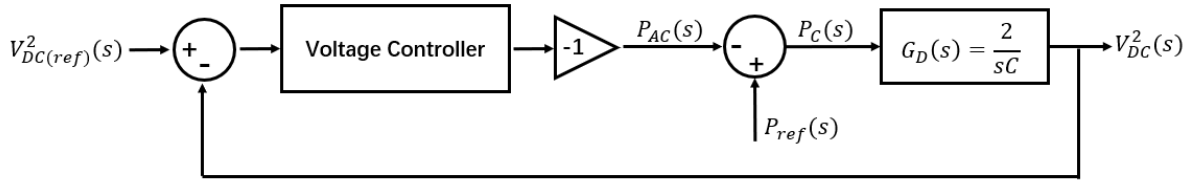

Figure 4.1 Closed Loop Control Diagram of DC-Link Capacitor

The difference between $V_{DC(ref)}^2$ and V_{DC}^2 can be referred as 'error'. The reasons for adding a negative unity gain after the voltage controller are:

1. The capacitor needs to be charged when the 'error' is positive, so that $P_C = P_{ref} + P_{AC}$.
2. The capacitor needs to be discharged when the 'error' is negative, so that $P_C = P_{ref} - P_{AC}$.

The transfer function of the plant (capacitor) is a 1st order system, if still apply the PI controller to the plant, the open loop transfer function would be given by:

$$G_o(s) = G_V(s) \cdot G_D(s) = \frac{K_P(s+a)}{s} \cdot \frac{2}{sC} \qquad \textit{Eqn.4.1}$$

Thus, the closed loop transfer function could be given by:

$$G_{cl}(s) = \frac{Go(s)}{1+G_O(s)} = \frac{2K_P(s+a)}{Cs^2+2K_Ps+2K_Pa} \qquad \textit{Eqn.4.2}$$

The expression above can also fit in the general transfer function of 2nd order system, which has been mentioned in *Eqn.2.6.* Thus, the parameters of PI controller could be given by:

$$K_P = C\zeta\omega_n = 84.87,\ K_I = \frac{C\omega_n^2}{2} = 226347.13 \qquad \textit{Eqn.4.3}$$

Thus, the voltage controller could be given by:

$$G_C(s) = \frac{84.87(s+2666.99)}{s} \qquad \textit{Eqn.4.4}$$

4.2 Verification in MATLAB

Following the same procedure in designing the current controller in MATLAB, the root locus of the voltage controller is shown in **Figure 4.2**.

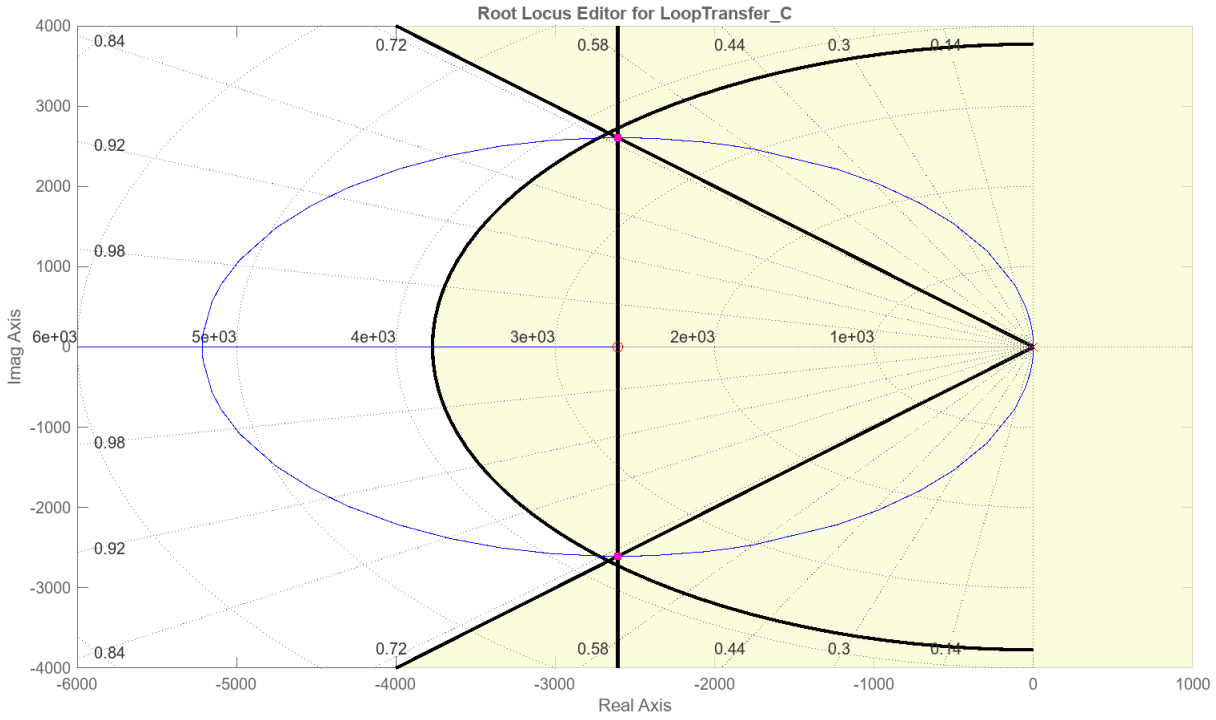

Figure 4.2 Root Locus of the Voltage Controller

According to the result in MATLAB, the transfer function of voltage controller could be expressed by *Eqn.4.5*, whose value is quite close to the calculated parameters.

$$G_C(s) = \frac{83.01(s+2608)}{s} \qquad Eqn.4.5$$

The step response is given in **Figure 4.3**, which meets the requirement of settled within 1.5 ms.

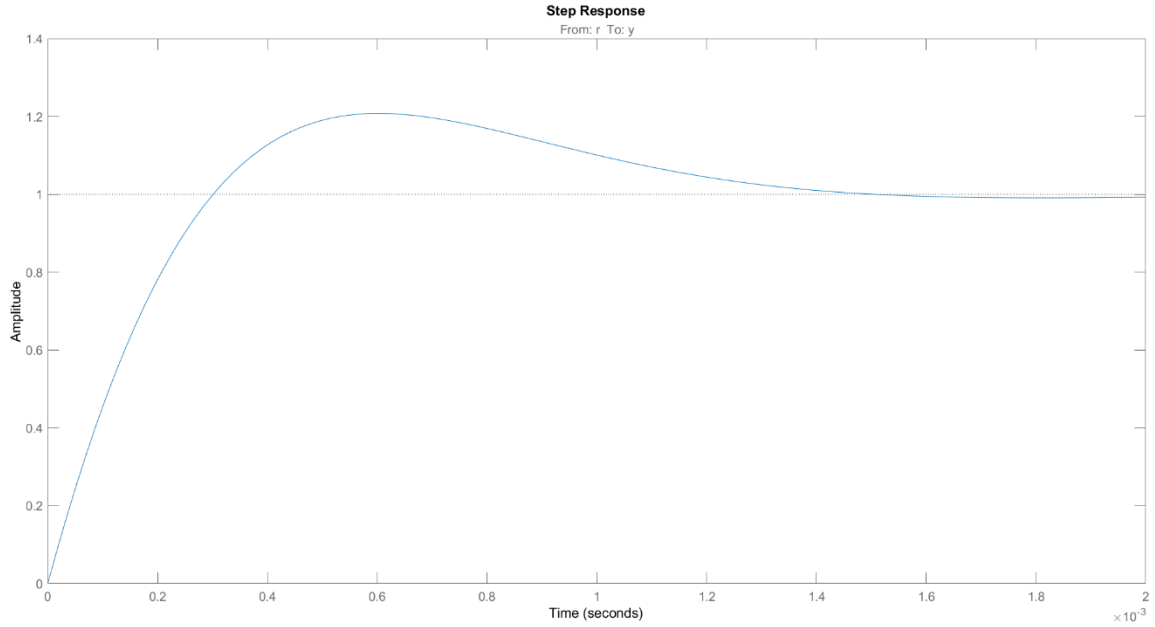

Figure 4.3 Step Response of Voltage Controller

4.3 Control Diagram

So far, the overall flow control is completed. The overall control diagram could be given in **Figure 4.4**, where the inner loop is current controller, and the outer loop is the voltage controller.

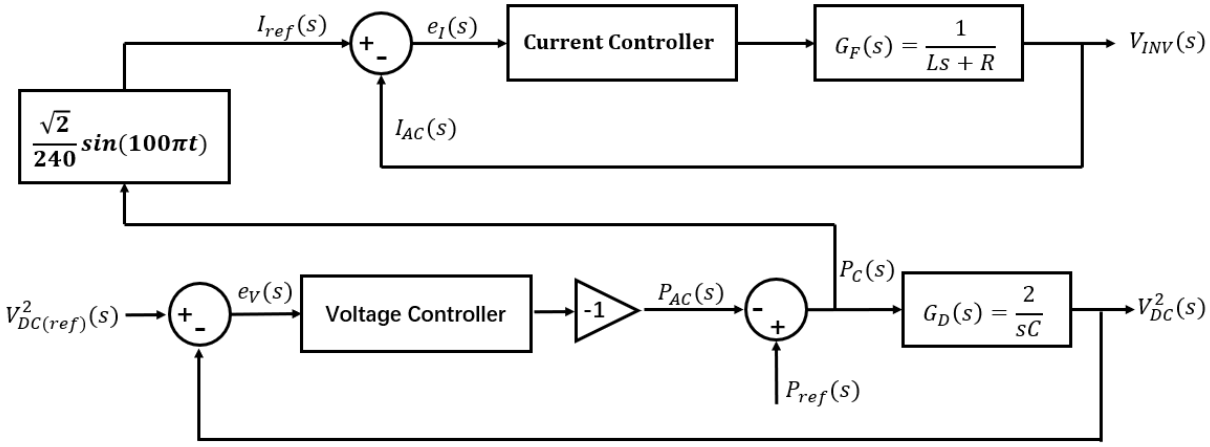

Figure 4.4 Overall Control Diagram

4.4 Verification in PLECS

To verify the performance of voltage controller, which is cascaded with the current controller, the testing schematic could be given by:

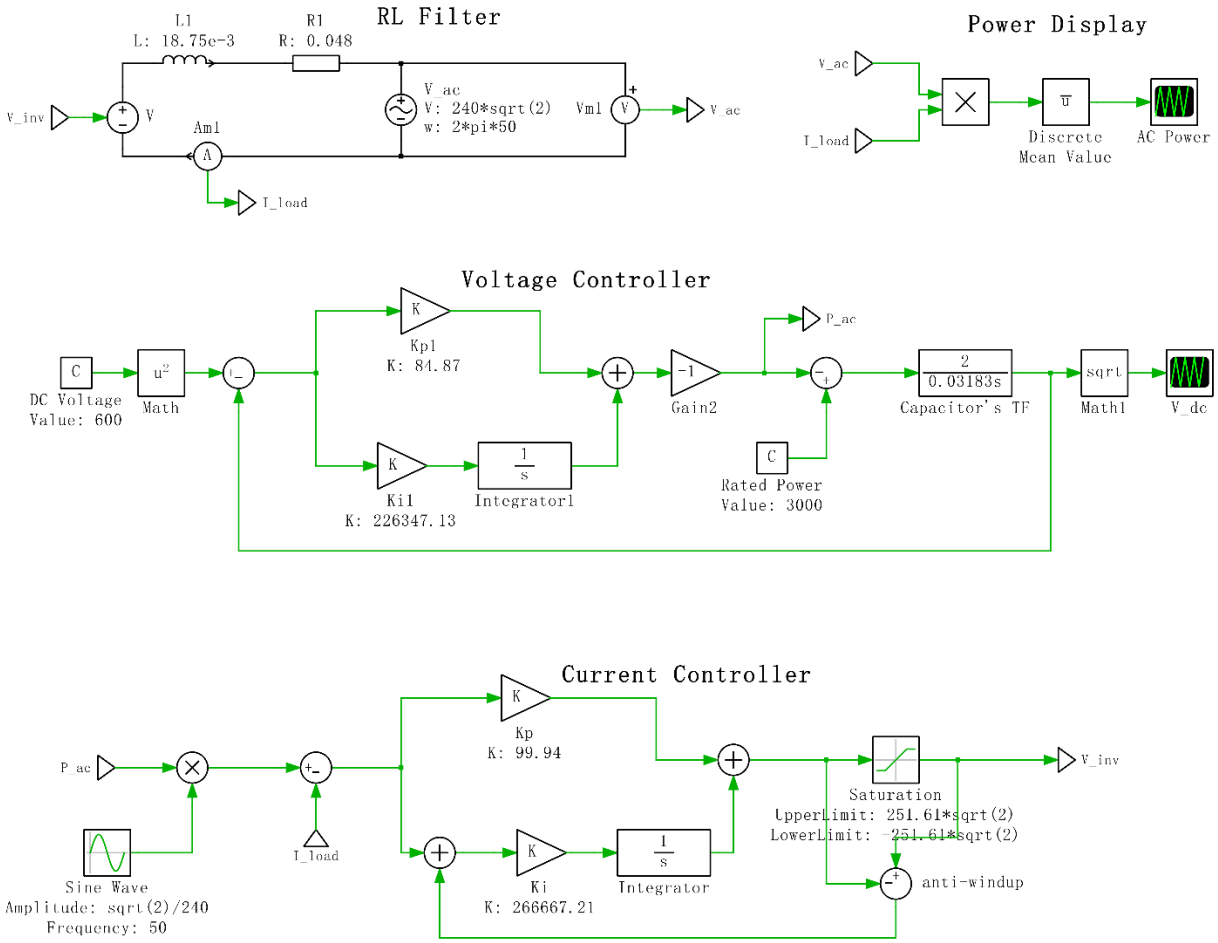

Figure 4.5 Overall Verification Schematic

The waveform of voltage across the capacitor is presented in **Figure 4.6** below.

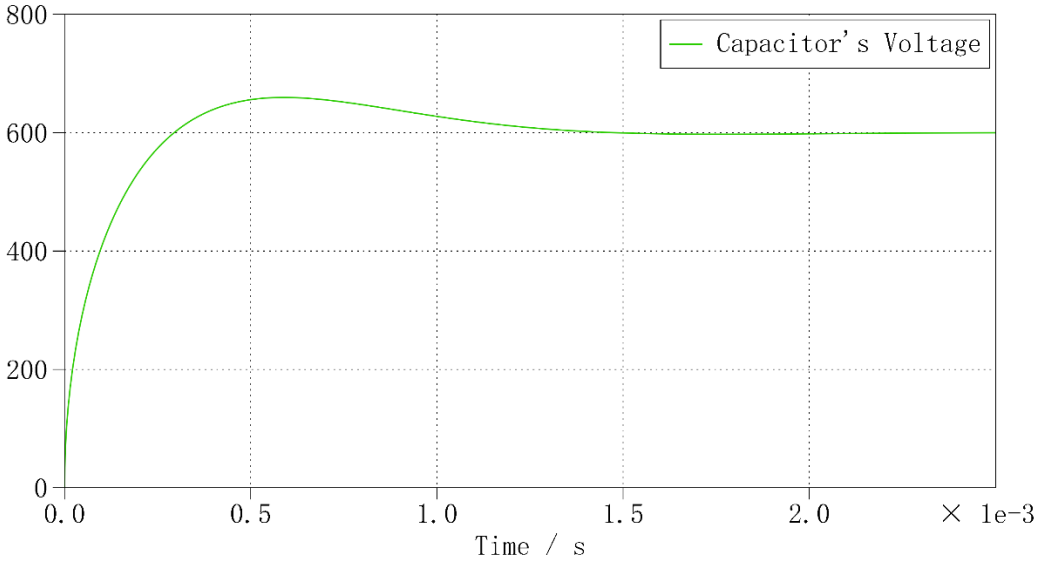

Figure 4.6 Voltage across the DC-Link Capacitor

The waveform of AC output power is presented in **Figure 4.7** below.

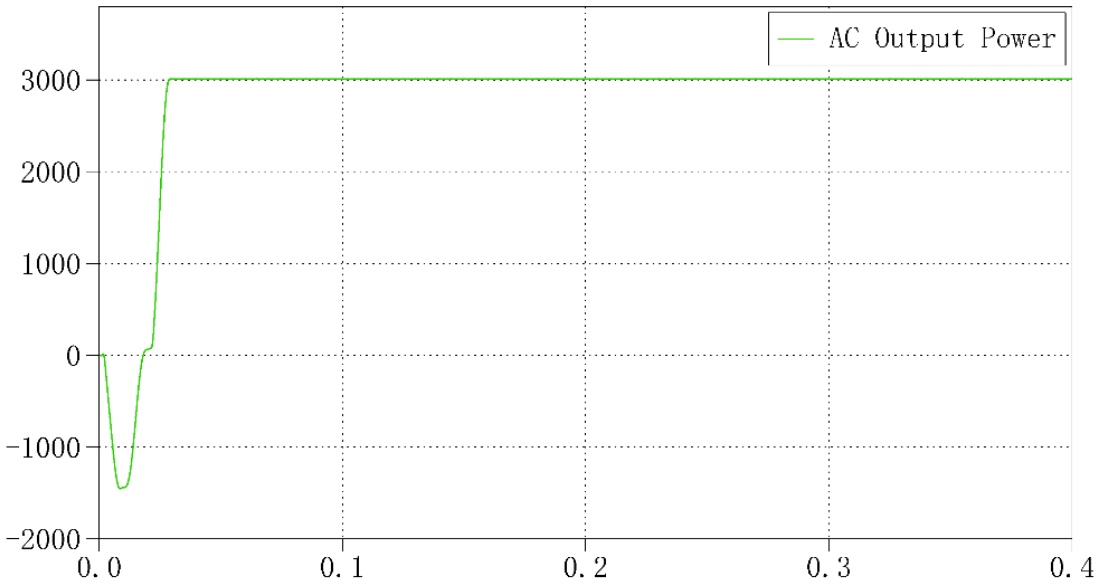

Figure 4.7 AC Output Power of Completed Schematic

It can be observed from **Figure 4.6** that the overshoot can reach up to about 660 V, which is approximately 10% of the steady state voltage (600 V). The initial voltage of capacitor is 0 V, and it takes about 1.5 ms (required settling time) to charge to achieve 600 V, which can prove that the designed voltage controller has a good performance in speed of response. The reason why there is a negative shoot in **Figure 4.7** at initial state could be due to the charging process of the capacitor, which might bring a very large positive 'error' to the voltage controller and thus caused a negative shoot at initial state. The 'error' of square of DC voltage is shown in **Figure 4.8**.

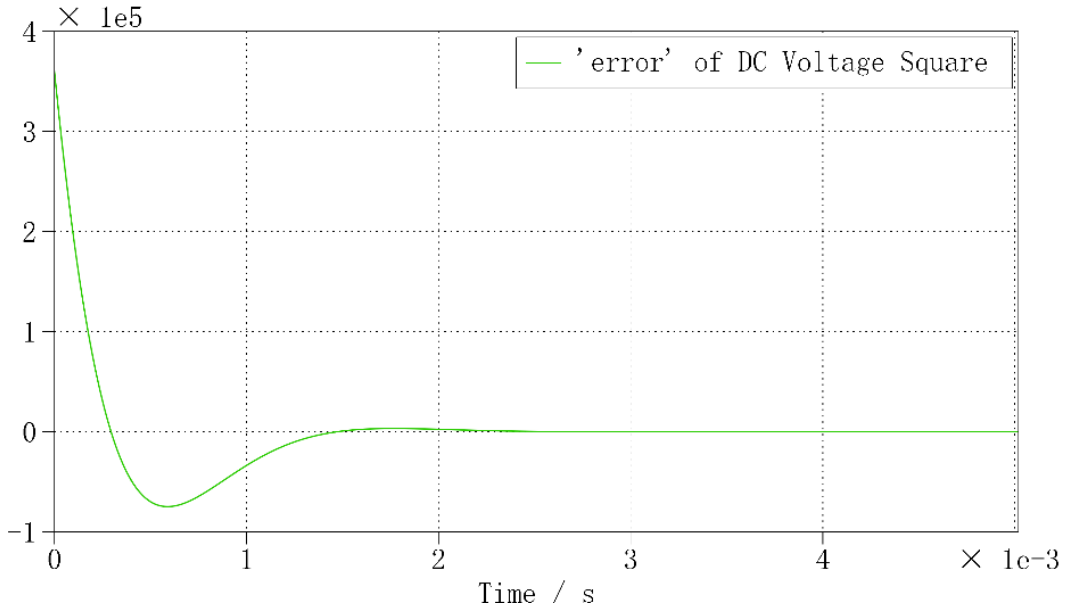

Figure 4.8 Waveform of 'error' of DC Voltage Square

After the AC output power in **Figure 4.7** steadied, the cursor reading of the output power is about 3011.1 W, which is a bit higher than the expected 3000 W. The reason for this could be the phase of inverter voltage has been delayed by PI controller by approximately $0.06°$. To verify this, changed the phase of inverter voltage to $17.08°$ and run the simulation schematic in **Figure 1.2** again, the cursor reading of steady state power would be 3010.9 W, which is quite near to the result in **Figure 4.8**.

4.5 An Alternative Design of Controller

Alternatively, a 'Lag Compensator' could be used as the voltage controller. The expression of 'Lag Compensator' could be expressed by:

$$G_{lag}(s) = \frac{k(s+z)}{s+p}, |z| > |p| \qquad Eqn.4.6$$

The open loop transfer function could be given by:

$$G_o(s) = G_{lc}(s) \cdot G_D(s) = \frac{62.83k(s+z)}{s(s+p)}, |z| > |p| \qquad Eqn.4.7$$

The closed loop transfer function could be given by:

$$G_{cl}(s) = \frac{G_o(s)}{1+G_o(s)} = \frac{62.83k(s+z)}{s(s+p)+62.83k(s+z)} = \frac{62.83k(s+z)}{s^2+(p+62.83k)s+62.83kz} \qquad Eqn.4.8$$

Thus, combining the general transfer function of 2nd order system (*Eqn.2.6*) to the above closed loop transfer function (*Eqn.4.8*),

$$2\zeta\omega_n = p + 62.83k,\ \omega_n^2 = 62.83kz \qquad Eqn.4.9$$

The natural frequency of outer loop (voltage controller) should be at least 1/10 of the natural frequency of inner loop (current controller), so the natural frequency ω_n of voltage controller should be $377.124\ \text{rad/s}$.

Assuming the value of 'k' is 8, the values of 'p' and 'z' of $G_{lag}(s)$ could be given by:

$$p = 30.61,\ z = 282.95 \qquad \textit{Eqn.4.11}$$

Overall, the transfer function of 'Lag Compensator' could be expressed by:

$$G_{lc}(s) = \frac{8(s+282.95)}{s+30.61} \qquad \textit{Eqn.4.12}$$

4.6 Verification of Lag Compensator in PLECS

Replaced the PI voltage controller by the above Lag Compensator, the schematic of voltage controller now became:

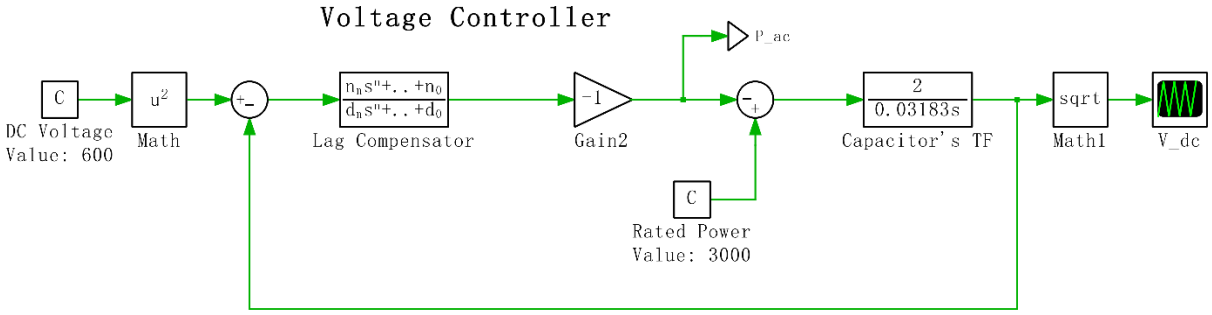

Figure 4.9 Voltage Controller with Lag Compensator

The waveform of voltage across the capacitor is presented in **Figure 4.10** below, which is quite similar to the result shown in **Figure 4.6**. It can be observed from **Figure 4.10** that takes about 1.5 ms (required settling time) to achieve steady state voltage, which can prove that the designed controller has a good performance in speed of response.

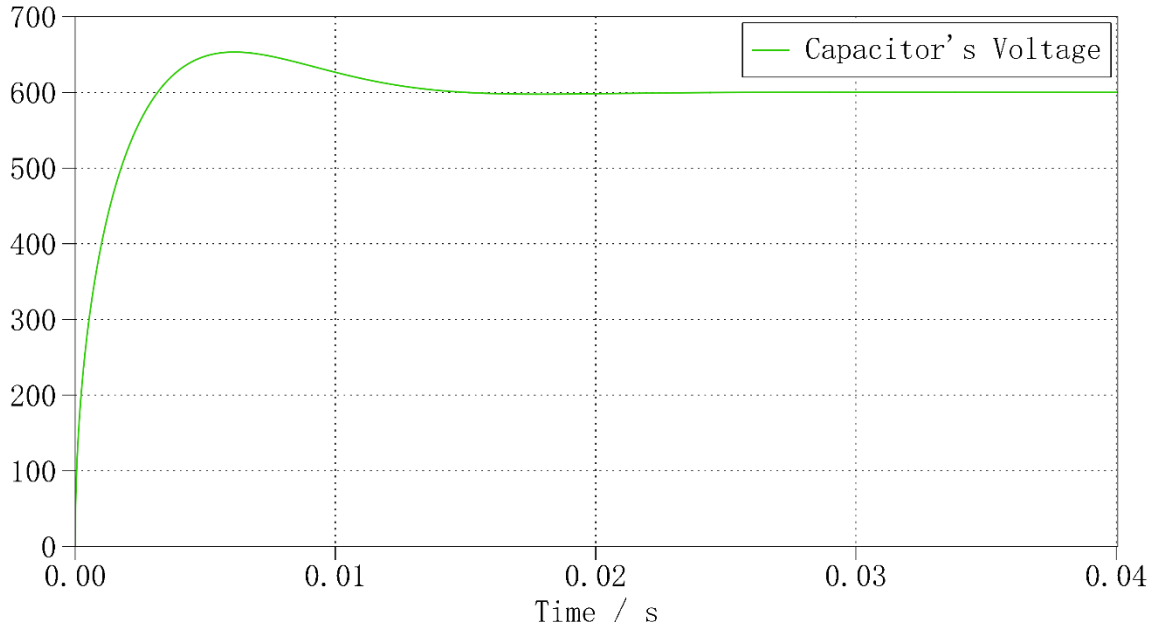

Figure 4.10 Voltage across the DC-Link Capacitor

The waveform of AC output power is presented in **Figure 4.11** below, which is quite similar to the result shown in **Figure 4.7**.

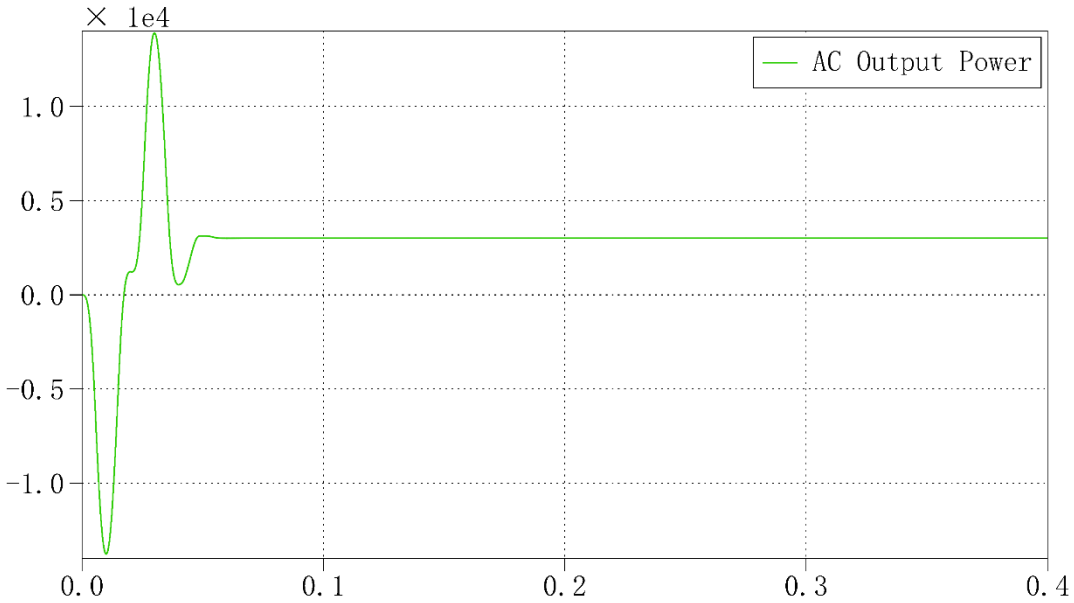

Figure 4.11 AC output power Waveform when applying the Lag Compensator

The same reason exists for the negative shoot at initial state, which is caused by the charging process of capacitor. The power transmits to the AC grid at steady state is about 3011.1 W, which is also a bit higher than the expected 3000 W. The reason for this could be the phase of inverter voltage has been delayed by the Lag Compensator. In conclusion, the overall controller design meets the specifications.