EEEE3001

Final Year Individual Project Dissertation

Diode Clamped Inverter for Vehicle AC Machine Drive

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**Abstract**

**Chapter 1: Introduction**

* 1. **Background and Summary of Literature Review**
     1. **Introduction to PMSM**

Permanent Magnet Synchronous Machines (PMSMs) are a class of electric motors that utilize permanent magnets embedded in the surface of the motor's rotor. This design is fundamental in creating a magnetic field that synchronizes with the rotating magnetic field of the stator. Efficiency is one of the distinguishing characteristics of PMSMs; the permanent magnets provide a steady magnetic field without the stator current, which is normally needed in other kinds of motors to maintain the field via the rotor windings.

The PMSM stands out for its high-power density, which is the amount of power generated per unit volume of the motor. This feature is particularly beneficial in the applications where space and weight are constrained, such as in automotive or aerospace industries. Another advantage of PMSMs is their high operational efficiency throughout a wide range of speeds and loads. This adaptability is complemented by their remarkable torque-to-weight ratio, which allows them to produce more torque per unit of motor weight than many other motor types. Moreover, PMSMs are also noted for their quiet operation and low maintenance requirements due to the lack of brushes and slide rings, which are prone to wear and strain.

The PMSM's torque generation capability is a direct consequence of the electromagnetic interaction between the stator's rotating magnetic field and the rotor's permanent magnets. This interaction produces torque that is precisely controllable, which is why PMSMs are ideal candidates for variable speed and position control applications.

* + 1. **Introduction to Diode Clamped Inverter**

The diode clamped inverters, also known as Neutral Point Clamped (NPC) inverters, can convert direct current (DC) to alternating current (AC) in a variety of applications. They are characterized by their multilevel output, which can generate voltage waveforms with steps at several voltage levels, not just the two levels produced by traditional two-level inverters. This ability to approximate sinusoidal waveforms more closely results in lower total harmonic distortion (THD). Due to their superior waveform quality, these types of inverters are commonly used as the drives for high frequency motors [1]. This intrinsic feature enables it to generate high-frequency AC voltages for the PMSM with significantly less harmonic distortion, and thus, the pulsations caused by these harmonics is significantly reduced.

In the three-phase diode clamped inverter topology, each phase leg includes several power semiconductor switches (could be MOSFET or IGBT) and clamping diodes. The clamping diodes are critical components that allow the inverter to maintain the voltage balance of the DC-link capacitors during operation, thereby ensuring the generation of the desired multi-level AC waveform. In this project, a three-phase three-level diode clamped inverter is used as the drive of PMSM motor, the topology is shown in the Figure 1.1 below. Three-level means each phase of the inverter can generate three different levels of voltage, which are , 0V, and .

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**Figure 1.1** Topology of Three-Phase Three-Level Diode Clamped Inverter

* + 1. **Field-Oriented Control (FOC)**

Field-Oriented Control (FOC), also known as vector control, is an advanced method of motor control that treats the electric motor as a controllable entity in two orthogonal components [2, 3]. This control technique allows for separate control of the magnetic flux and torque in AC machines (such as PMSM), by aligning the reference frame of the control system with the vector space of the motor’s magnetic field. Essentially, FOC decouples the PMSM's torque and magnetic flux into two independent variables that can be controlled as if the motor were a direct current (DC) motor.

* + 1. **Review of Existing Technologies and Developments**

Inverter technology has advanced significantly, especially in the area of electric vehicle (EV) propulsion. Innovations in semiconductor materials, such as Silicon Carbide (SiC) and Gallium Nitride (GaN), have been critical in spawning a new generation of inverters. These new inverters offer increased power densities and efficiency, as well as the extraordinary ability to perform optimally at high frequencies and temperatures. The consequence is a significant reduction in the physical bulk and weight of inverter systems, as well as an increase in their dependability and operational lifespan.

Meanwhile, for control algorithm, there is also a technique called sensorless control, which eliminate the need for physical sensors in the motor by using estimators and observers to infer the rotor position. However, due to the complexity of algorithm, and issue of robustness, it would not be covered in this report.

* 1. **Aims and Objectives**

The aim of this project is to achieve current and speed control of the PMSM motor (300V, BSM90N-175) through a three-phase three-level diode clamped inverter in PLECS and in reality. The inverter is controlled by TI’s F28379D Launchpad. For safety concerns, only low power situation (2kW) would be considered.

The project can be divided into following stages:

**Stage 1: Initial Simulation of FOC in PLECS**

**Aim:**

Create a mathematical model of PMSM motor in PLECS, and implement FOC in PLECS to verify the minimum acceptable capacitance of the DC-link capacitors.

**Objectives:**

* Work out the mathematical model of BSM90N-175 motor.
* Learn the working principles of Field-Oriented Control, build the continuous control model in PLECS.
* Change the target torque current to verify the performance of the two DC-link capacitors with calculated capacitance value, then work out the minimum acceptable value of capacitance and find the most suitable capacitor on the market.

**Stage 2: Hardware Design in KiCad and Manufacturing**

**Aim:**

Design a four-layer printed circuit board (PCB) for the three-phase three-level diode clamped inverter, as well as design a two-layer PCB for the control board (F28379D Launchpad) and its peripherals.

**Objectives:**

* Selection of components, build bill-of-materials (BOM) lists for purchasing.
* Schematic of the control board and the board of diode clamped inverter in KiCad, which includes gate drive circuit, ADC sampling circuit, connectors, etc.
* PCB layout in KiCad.

**Stage 3: Controller Design in PLECS and MATLAB**

**Aim:**

Design the continuous PI controller of speed, DC voltage balancing, and d-axis and q-axis current in MATLAB, convert them to discrete controllers and test in PLECS.

**Objectives:**

* Transfer functions of these continuous PI controllers from the “sisotool” in MATLAB.
* Convert the continuous PI controllers to discrete PI controllers.
* Test the discrete PI controller in PLECS.
* Convert the function blocks to “c-script” blocks in PLECS.

**Stage 4: Software Design in Code Composer Studio (CCS)**

**Aim:**

Convert the control algorithm and overall logic in PLECS file to C code that can be built and loaded on TMS320F28379D micro-controller, then test the program in real PMSM motor to verify the current and speed control.

**Objectives:**

* Configurate the environment of CCS, including file search path, library search path, predefined symbols, optimization configurations, etc.
* Construction of CCS program, which includes ADC sampling, motor encoder decoding, PI controller implementation, timer interruption, SPWM generation, etc.
* Test the program in real BSM90N-175 motor (supplied by 300 V battery) with the two PCBs to verify the speed and current control.

**Chapter 2: Simulation and Controller Design**

***2.1* Specifications of Tool Choice**

PLECS (Piecewise Linear Electrical Circuit Simulation) is chosen to be the tool of circuit simulation. It is a better choice than MATLAB in simulating electrical circuits for following reasons:

* PLECS can offer faster simulation times due to its optimized solvers.
* PLECS can offer real-time simulation capabilities for hardware-in-the-loop (HIL) testing. This feature is useful for testing the control logic on actual hardware before deployment.
* PLECS provides integrated thermal modelling, which enables the simulation of temperature-dependent behaviours of components and systems.

However, PLECS is not a suitable tool for controller design. For PI controller design, a tool named “sisotool” in MATLAB is used, which is an interactive graphical user interface (GUI) tool for designing and analysing single-input, single-output (SISO) control systems. It offers a variety of plotting functions, including bode plots, root locus, and step response plots, which are essential for understanding the frequency and time domain characteristics of the system.

***2.2* PMSM Motor Modelling**

The model is chosen to be ABB’s BSM90N-175. The electrical and mechanical parameters of this motor are shown in **Table 2.1** below.

**Table 2.1** Parameters of BSM90N-175 Model

|  |  |
| --- | --- |
| Rated Speed (at 300 V) | 4000 rpm |
| Torque Constant | 0.853 Nm/amp |
| Stator Resistance | 1.24 ohms |
| Stator Inductance | 4.15 mH |
| Pole Pairs | 4 |
| Inertia | 3.389 Kg- |

The electrical model of PMSM in PLECS is modelled by:

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**Figure 2.1** Electrical Model of PMSM in PLECS (left: d-axis; right: q-axis)

The stator flux linkages are given by:

*Eqn.2.1*

*Eqn.2.2*

where the symbol represents the constant flux linkage, the symbol and represent stator inductance in d-axis and q-axis.

The three-phase stator currents are transformed to the two-dimensional rotating reference dq-frame, which converts an AC system into an equivalent DC system. This enables the use of traditional PI controllers with zero steady-state error. According to **Figure 2.1**, the stator voltage in d-axis and q-axis are given by:

*Eqn.2.3*

*Eqn.2.4*

Due to the AC motor is a synchronous machine with surface-mounted magnets and no saliency, flux lines are distributed evenly around the stator, which means that the motor's inductance measured in the direction of the d-axis and the q-axis will be the same. Thus:

*Eqn.2.5*

This equality leads to a simplified Field-Oriented Control algorithm, because the current-regulating controller does not have to compensate for differences in inductance in different orientations of the rotor. As they are equal, and can be represented by . Thus, *Eqn.2.3* and *Eqn.2.4* can be rearranged as:

*Eqn.2.6*

*Eqn.2.7*

where the electrical rotor speed .

Moreover, according to the manual of PLECS, electromagnetic torque and mechanical rotor speed of PMSM model in PLECS are given by:

*Eqn.2.8*

*Eqn.2.9*

*Eqn.2.10*

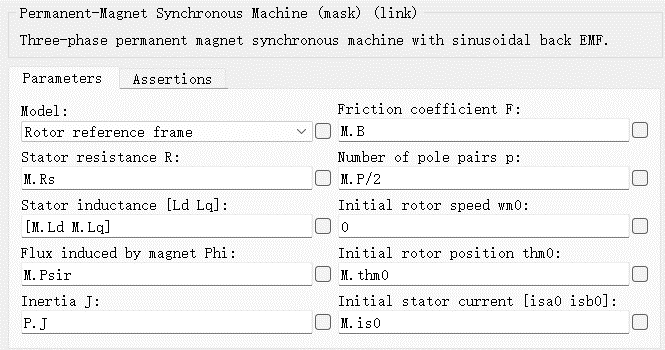
where the symbol represents the friction coefficient.

The configurations of initialising PMSM in PLECS are presented in **Figure 2.2** and **Figure 2.3** below, whose data are referred from the datasheet of BSM90N-175 motor. The model of PMSM is chosen to be “Rotor reference frame”, as it can decouple the motor’s flux and torque. In addition, the friction coefficient is assumed to be 0.01 Nm/(rad/s).

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**Figure 2.2** C-Code for Simulation Parameter Initialization in PLECS



**Figure 2.3** Configurations of PMSM Model in PLECS

***2.3* Field-Oriented Control (FOC)**

Field-Oriented Control is a control technique used in variable frequency drives to control the torque (and thus speed and position) of three-phase AC electric motors by controlling the current components independently. The essence of this algorithm is to decompose the stator currents into two orthogonal components that can be controlled separately: one aligns with the rotor's magnetic field (direct axis, or d-axis), and the other is perpendicular to it (quadrature axis, or q-axis). This decomposition allows the control system to adjust the torque and magnetic flux of the motor independently, like DC motor, which is easier to control because torque is directly controlled by armature current.

The procedures of FOC are demonstrated as follows:

1. Sample the phase currents of PMSM and get , , and .
2. Convert , , to , via Clarke Transformation.
3. Convert , to , via Park Transformation.
4. Calculate the errors between measured , and target , , enter the errors to two PI controllers and get control voltage , .
5. Convert , to , via Inverse Park Transformation.
6. Convert , to , , via Inverse Clarke Transformation, and enter the three-phase voltage to Sinusoidal Pulse Width Modulation (SPWM) module to output PWM for each gate according to the position of rotor. Another alternative is using , to synthetic voltage space vector and enter the Space Vector PWM (SVPWM) module to obtain PWM for each gate.
7. Repeat above procedure in switching frequency.

The control diagram of FOC is shown in **Figure 2.4** below.

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**Figure 2.4** Control Diagram of FOC

**Clarke Transformation**

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**Figure 2.5** ABC-Frame and Frame

The first step of Clarke Transformation is projection:

*Eqn.2.11*

*Eqn.2.12*

Thus, the relationship of , , and , can be expressed by:

*Eqn.2.13*

The second step is to convert *Eqn.2.13* to scaled version. According to Kirchhoff's current law, the sum of , , should be zero:

*Eqn.2.14*

Assume , then , the value of and would be:

*Eqn.2.15*

Although the vector and are overlapped, the projection of and make them not equal. Therefore, to make them equal, the *Eqn.2.13* should be scaled by 2/3.

*Eqn.2.16*

According to *Eqn.2.14*, , which means does not need to be sampled. and could be expressed by:

*Eqn.2.17*

*Eqn.2.18*

**Inverse Park Transformation**

Rearrange the *Eqn.2.14*, *Eqn.2.17* and *Eqn.2.18*, phase current , , could be given by:

*Eqn.2.19*

*Eqn.2.20*

*Eqn.2.21*

**Park Transformation**



**Figure 2.6** Frame and dq-Frame

The symbol represents the electrical angle of rotor, which equals the result of number of pole pairs multiplied by mechanical rotor angle. The relationship of , and , can be given by:

*Eqn.2.22*

*Eqn.2.23*

*Eqn.2.24*

**Inverse Clarke Transformation**

Rearrange *Eqn.2.22*:

*Eqn.2.25*

Then and can be given by:

*Eqn.2.26*

*Eqn.2.27*

***2.4* Topology Overview and Control Diagram**

Each phase of the inverter contains four IGBTs (with diode) to control the voltage level between S2 and S3 by switching. The other two diodes in each phase help in maintaining the voltage balance across the two DC-link capacitors.

The truth table of switching is presented in **Table 2.2** below.

**Table 2.2** Truth Table of Phase Voltage

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Phase Voltage** | **S1** | **S2** | **S3** | **S4** |
|  | 1 | 1 | 0 | 0 |
| **0** | 0 | 1 | 1 | 0 |
|  | 0 | 0 | 1 | 1 |

It can be observed from the **Figure 1.1** that there are two DC-link capacitors between DC voltage source and IGBT bridges. The two capacitors are not only used for dividing the DC voltage, but also act as a decoupling element between the power supply (which may include batteries, photovoltaic arrays, or rectifiers) and the inverter. It helps to minimize the injection of harmonics back into the power source and also reduces the harmonic content in the output AC waveform.

The controller takes the 2-phase current and PMSM motor’s angle and speed as input, and output the PWMs for each IGBT in the inverter. The controller contains three closed control loops: the current control loop contains two parallel loops (d-axis and q-axis), and speed control loop is in series with the q-axis current control loop. The current loop can also be referred as the torque loop because the torque of PMSM motor is proportional to its stator current. This is where the FOC algorithm can be applied, combined with the PI controllers to control the three-phase current and voltage to generate target torque according to the position of the rotor.

The main topology of the circuit for simulation in the PLECS is shown in **Figure 2.7** below.

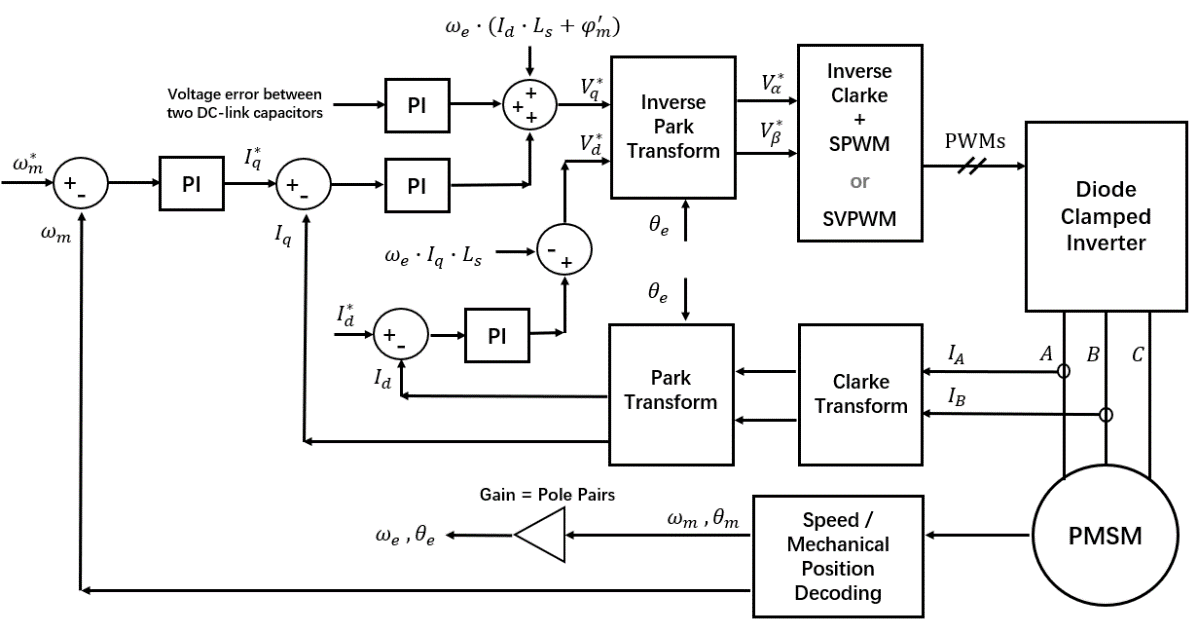
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**Figure 2.7** Main Topology of Simulation

The 20k ohms resistors that connected in parallel with the DC-link capacitors can help balance the voltage across each capacitor. Moreover, when the system is turned off, the capacitors can hold a charge for a significant amount of time. The resistors provide a discharge path for the stored energy, ensuring that the capacitors discharge safely and relatively quickly, which is important for maintenance and safety reasons.

According to *Eqn.2.6* and *Eqn.2.7*, the transformation from the three-phase to the dq-frame brings cross-coupling between the d-axis and the q-axis, which have to be considered in the controller structure. Therefore, the overall control diagram is shown in the **Figure 2.8** below.

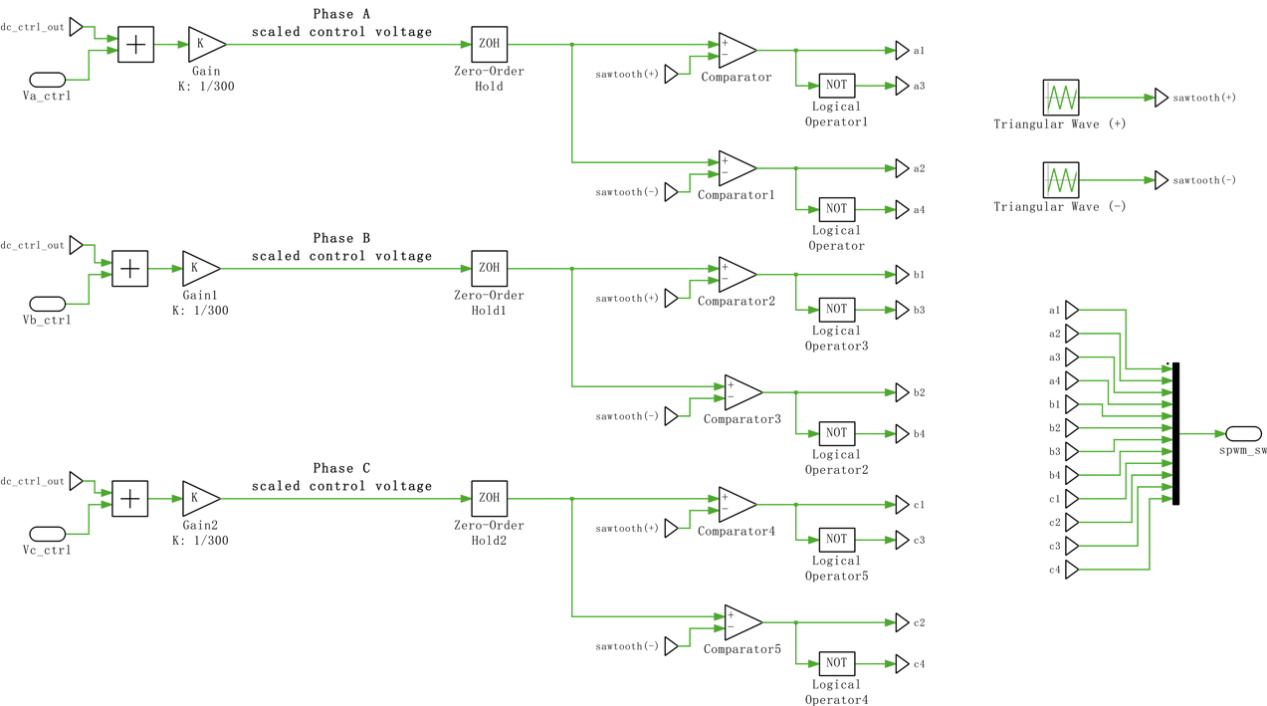


**Figure 2.8** Overall Control Diagram

***2.5* SPWM and SVPWM**

**2.5.1 Sinusoidal PWM (SPWM)**

The basic idea behind SPWM is to control the output voltage by modulating the width of the pulses based on a sinusoidal reference signal. The resulting PWM waveform effectively modulates the average voltage over time to approximate a sinusoidal AC output from a DC input. The three-phase SPWM is constructed as **Figure 2.9** in the simulation.



**Figure 2.9** Three-Phase SPWM in Simulation

The negative carrier is set to be flipped rather than shifted, and the carrier frequency is set to be 10 kHz (switching frequency). A “Zero-Order Hold” module is added to each phase to convert continuous control voltage to discrete. The waveform of the Symmetrical PWM (3-Level) module is presented in **Figure 2.10**.

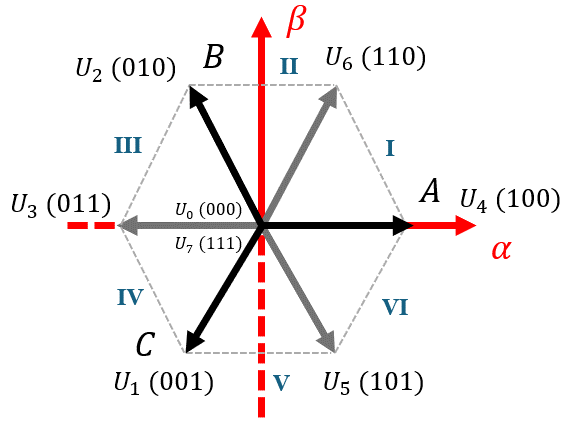
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**Figure 2.10** Symmetrical PWM (3-Level) Waveform

**2.5.2 Space Vector PWM (SVPWM)**

Another method to generate PWMs for each gate of inverter is Space Vector PWM (SVPWM). Compared to SPWM, the SVPWM is often favoured for its higher voltage utilization rate and lower THD (Total Harmonic Distortion) in the motor current (thus less noise and heat). It treats the three-phase voltages as a two-dimensional vector space, and utilizes the vector space of the inverter more efficiently by calculating the switching states that will produce the desired voltage vector closest to the ideal circular locus of the motor phase voltages. In this space, the possible voltage vectors that can be applied to the motor form a hexagon, which is shown in **Figure 2.11** below.



**Figure 2.11** Frame of SVPWM (Not for Three-Level)

The left digit of the three-digits represents the status of phase A, the middle digit represents the status of phase B, and the right digit represents the status of phase C. , ,are vectors synthesized from vectors in phase A, B, C. and represent zero vectors. These vectors divide the hexagon into six sectors (I to VI). The principle of SVPWM is to use these eight vectors (including two zero vectors) as base vectors to compound reference voltage vector.

According to the inductor volt-second balance principle, the average value of voltage applied across an ideal inductor must be zero. Therefore, the relationship between the reference voltage vector and two adjacent voltage vectors (, ) in each sector can be given as follows. For example, and in Sector I; and in Sector II, etc.

*Eqn.2.28*

After discretization, it is equivalent to the following equations:

*Eqn.2.29*

*Eqn.2.30*

*Eqn.2.31*

The symbol represents one period of PWM, which is in this case. The symbol represents the two zero vectors, which could be or . Proper placement of zero vectors can make the switching of the space voltage vector smoother. Duty cycles of , , could be given by dividing their conducting time (, , ) by , and they would be denoted as , , in the following:

*Eqn.2.32*

*Eqn.2.33*

*Eqn.2.34*

The symbol represents the sector number. Then, the three-phase voltage , *,*  could be expressed by , , . To have symmetrical PWM, the distribution of zero vector to and can be given by:

*Eqn.2.35*

The next step is to design the sequence of switching for three-phase. Due to the IGBTs have switching loss, it is essential to reduce the switching times of IGBT in sequence design. According to a method named “Seven-Segments SVPWM Sequence”, the sequence for each sector could be designed as shown in **Table 2.3**.

**Table 2.3** Seven-Segment SVPWM Sequence

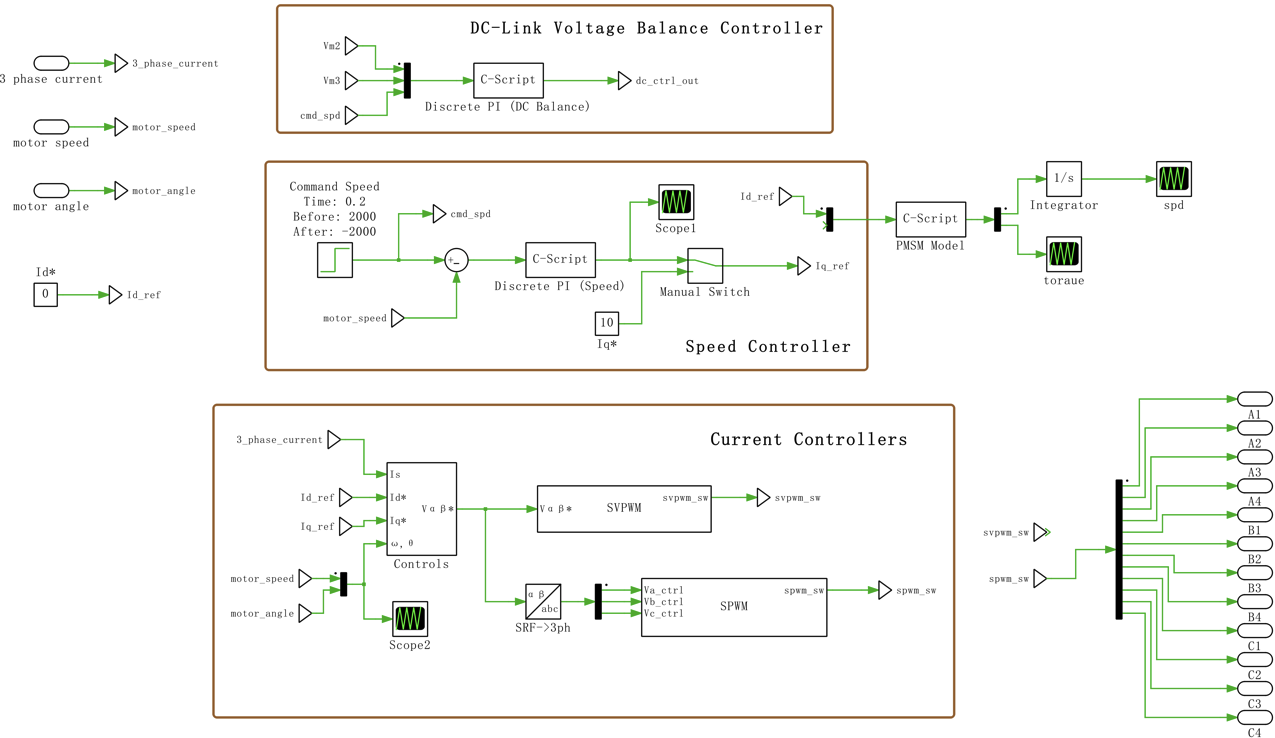
|  |  |
| --- | --- |
| **Sector** | **Sequence** |
| **I** | 0-4-6-7-7-6-4-0 |
| **II** | 0-2-6-7-7-6-2-0 |
| **III** | 0-2-3-7-7-3-2-0 |
| **IV** | 0-1-3-7-7-3-1-0 |
| **V** | 0-1-5-7-7-5-1-0 |
| **VI** | 0-4-5-7-7-5-4-0 |

The above derivation demonstrates the working principles of SVPWM. However, it is only for the case when each phase of the inverter contains two switching devices, so there are only two status (0 and 1) in each phase. For three-level inverter, there are three status (-1, 0, 1) in each phase, and the sequence design would be more complex than **Table 2.3**. Considering the complexity of algorithm, a “Space Vector PWM” module is used in PLECS simulation, and the SVPWM is not considered in the deployment to MCU.

***2.6* Design of Controllers**

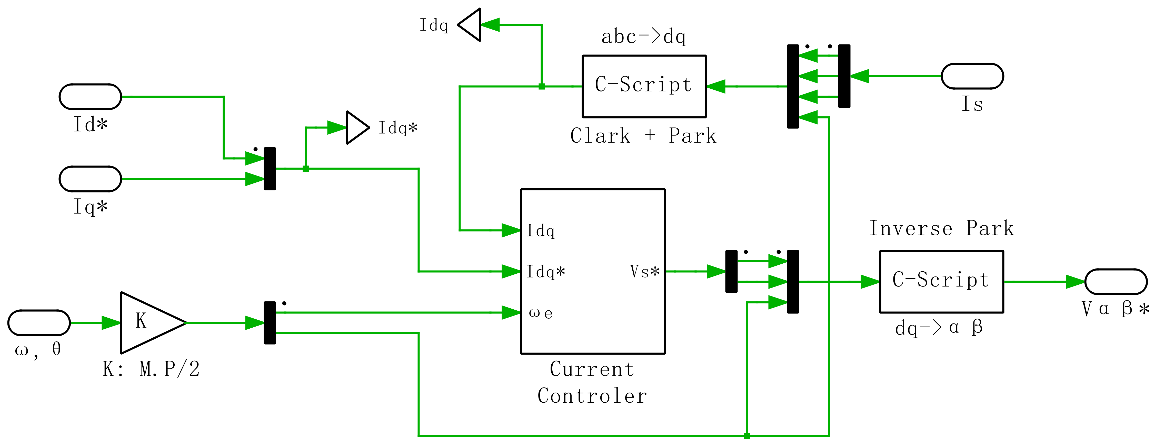
**2.6.1 Schematic of Controllers in Simulation**

The schematic of controllers is presented in **Figure 2.12** below.

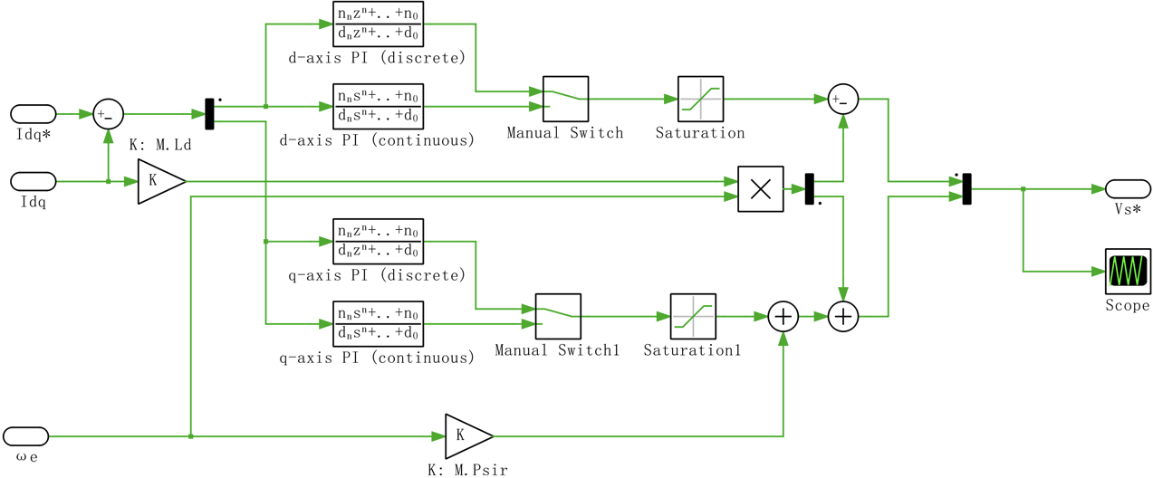


**Figure 2.12** Schematic of Controllers in PLECS

According to the control diagram shown in **Figure 2.8**, the schematics of current controllers (sub-systems) are designed as follows (presented in **Figure 2.13** and **Figure 2.14** below).



**Figure 2.13** Current Controller Sub-System 1: Frame Transformation



**Figure 2.14** Current Controller Sub-System 2: PI Controllers

**2.6.2 Current Controller**

According to the *Eqn.2.5*, the stator inductance of d-axis and q-axis are equal. Thus, the transfer function of plant (electrical system) should be identical, which can be expressed as:

*Eqn.2.36*

It can be seen that the is a 1st order plant, so PI controller could be used as the current controller. The transfer function of current controller could be given by:

*Eqn.2.37*

The control diagram could be represented in **Figure 2.15** below.

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**Figure 2.15** Control Diagram of Current Controller (d-axis or q-axis)

The open loop transfer function could be given by:

*Eqn.2.38*

Thus, the expression of the above closed loop system could be represented by:

*Eqn.2.39*

As the general transfer function of 2nd order system could be represented by:

*Eqn.2.40*

Comparing *Eqn.2.39* and *Eqn.2.40*, expression of PI controller’s parameter ( and ) could be obtained as below.

*Eqn.2.41*

Assume the settling time of the system is 10 ms, specification of controller design could be given in *Eqn.2.42*, where the damping ratio determines the degree of overshoot in a step response, and natural frequency determines the speed of response.

*Eqn.2.42*

Thus, the value of is given to be 2.08 and the is given to be 1328.40, so that the transfer function of the continuous PI controller for both d-axis and q-axis could be obtained by:

*Eqn.2.43*

To implement the controller in MCU, the continuous PI controller needs to be converted to discrete form. Applying the Bilinear Transformation, the transfer function of the discrete PI controller could be given by:

*Eqn.2.44*

*Eqn.2.45*

With the PI controller in discrete form, the next step is to implement it in the digital control system.

**2.6.3 Speed Controller**

The torque produced by a DC motor is proportional to the armature current and the strength of the magnetic field. It can be seen from the Chapter 2.7 that the FOC can model the q-axis of the PMSM motor as a DC motor. Assume the magnetic field is constant, then the torque is proportional to current by the torque constant . According to the Newton’s 2nd law, the torque could be given by ( is friction coefficient):

*Eqn.2.46*

Applying the Laplace Transform tothe above equation:

*Eqn.2.47*

Thus, plant’s transfer function of speed control could be given by:

*Eqn.2.48*

The natural frequency of current control is . The natural frequency of outer loop (speed control) should be at least three times of the natural frequency of inner loop (current control). Assume the speed control is three times faster than the current control, then the natural frequency of speed control is . According to *Eqn.2.41*, the transfer function of continuous PI speed controller is given by:

*Eqn.2.49*

Applying the Bilinear Transformation, the transfer function of the discrete PI controller could be given by:

*Eqn.2.50*

**2.6.4 DC-Link Voltage Balance Controller**

***2.7* DC-Link Capacitors**

The calculations of DC-link capacitance are complex and would not be discussed in this thesis. The procedures of

**Chapter 3: Hardware Design: Diode Clamped Inverter**

***3.1* Schematic**

The whole schematic of diode clamped inverter board is in the Appendix, which can be divided into the following parts:

**Inverter:**

The main topology of the inverter consists of 12 IGBTs (4 in each phase), 18 diodes (1 each IGBT plus 2 in each phase), and two DC-link capacitors, which is shown in **Figure 3.1**. Two 20k ohms SMD resistors are connected in parallel with the capacitors to ensure the voltage balance between them. IGBTs are chosen over MOSFETs for switching devices because IGBTs can handle higher voltages and currents, have lower switching losses, and have better thermal stability. The IGBT is chosen to have the maximum collector-emitter voltage of 600 V, and maximum continuous collector current of 30 A. The diode is also selected with the maximum reverse voltage of 600 V and maximum forward current of 30 A.

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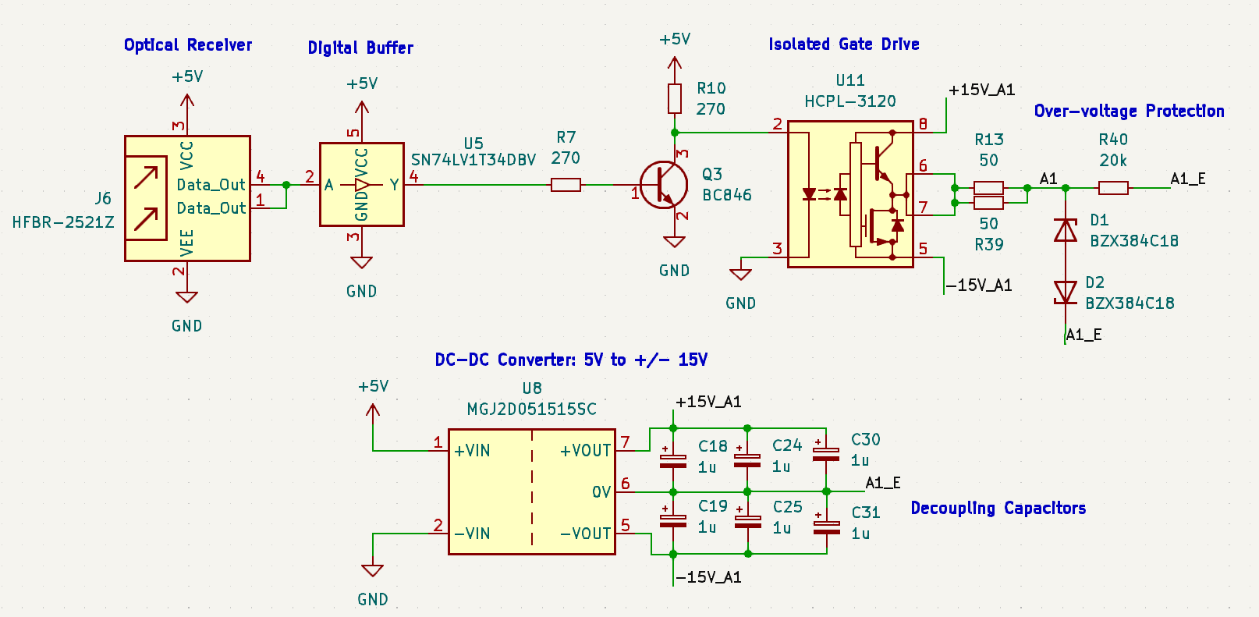
**Figure 3.1** Main Topology of Diode Clamped Inverter

**Gate Drive:**

The gate drive circuit of IGBT is presented in **Figure 3.2** below. Because there are several IGBTs needs to be driven in one phase, an optical isolated gate drive chip (HCPL-3120) is used to provide electrical isolation among them. Moreover, a 5 V to V DC-DC converter is also used to supply the isolated gate drive chip (+15 V to the , 15 V to the ). The positive 15 V is used to turn on the IGBT, and the negative 15 V is used to fully turn off it.

At the left-hand side of the isolated gate drive chip, an optical receiver (HFBR-2521Z) is used to receive the PWM signal from control board. Compared to copper cable, optical transmission offers higher bandwidth, longer transmission distance, and immunity to electromagnetic interference. Then, a digital buffer (SN74LV1T34DBV) is connected with the optical receiver to isolate the optical receiver from the rest part of the gate drive. Between the digital buffer and the isolated gate drive chip, a NPN transistor is used to regulate the input current of gate drive chip to 18 mA. When the control board transmitting logic “0” to the optical receiver, the output logic of the receiver would be “1” (5V), then the NP transistor would be turned on and the pin 2 of HCPL-3120 chip would be connected to GND. This equivalent to the control board’s transmitted logic “0” controls the pin 2 of HCPL-3120 to logic “0”, and logic “1” controls the pin 2 to logic “1”.

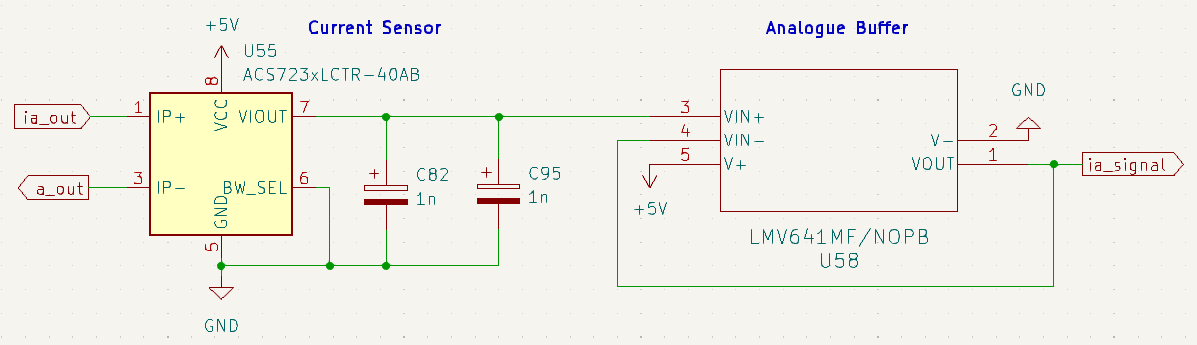
At the right-hand side of the isolated gate drive chip, two parallel resistors are used to limit the gate current of IGBT. A 20k ohms resistor is used to stabilize the gate-emitter voltage, and two 15V Zener diodes (tail-to-tail) are connected in parallel with the 20k ohm resistor to provide over-voltage protection in both directions (positive and negative).



**Figure 3.2** Schematic of Gate Drive (S1 in Phase A)

**Current Sensor Circuit:**

The current sensor chip (ACS723LLCTR-40AB-T) is able to measure A, which utilizes the Hall effect and is electrically isolated. Each phase has one sensor chip to measure the current and convert the signal to voltage (0 - 5 V), so that the signal can be sampled by ADC module in micro-controller. An analogue buffer (LMV641MF/NOPB) is connected to the current sensor chip to provide isolation between the inverter board and the control board.



**Figure 3.3** Schematic of Current Sensor (Phase A)

**Others:**

Decoupling capacitors are added between the 5V and GND. Moreover, there are seven terminals (connectors) in the board, except those optical receivers: One 2-pin terminal for the 5 V power supply, two 2-pin terminals for the 300 V power supply, one 6-pin terminal for the current signal feedback, and three 1-pin terminals for the inverter’s three-phase output voltage.

***3.2* Loss Calculations of IGBT**

The model of IGBT is selected to be RGCL60TK60. According to its datasheet, the ON-state resistance is about when the gate-to-emitter voltage is 15 V (under 25 ). In addition, when the collector current is 10 A, the collector-to-emitter voltage is approximately 1.1 V. Assume the duty cycle of PWM is , and switching frequency is 10 kHz. Then, the conduction loss and the switching loss of a single IGBT could be given by following equations:

*Eqn.3.1*

*Eqn.3.2*

where the rise time and fall time .

***3.3* PCB Layout**

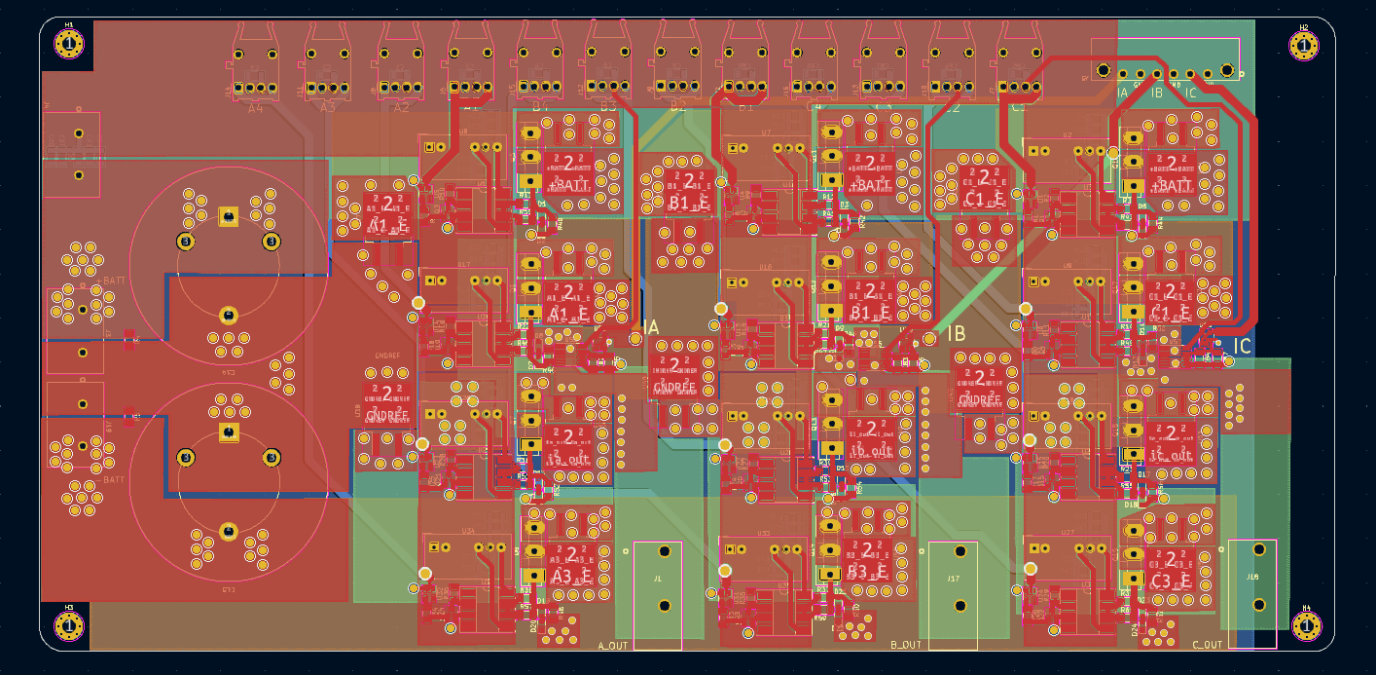
There are four layers in inverter’s PCB, the power connection within each layer is presented in **Table 3.1**.

**Table 3.1** Each Layer of the Inverter’s PCB

|  |  |  |
| --- | --- | --- |
| **Layer** | **Power Connection** | **Copper Thickness** |
| Top Layer | 5 V | 1 oz |
| Second Layer | + BATT | 2 oz |
| Third Layer | BATT | 2 oz |
| Bottom Layer | GND | 1 oz |

Because this PCB is designed for high voltage (300 V) and current (10 A), copper filled zones are used to replace wide traces to connect the power supplies in each layer. From a thermal perspective, in multi-layer PCB designs it is often recommended to use the outer two layers (top and bottom) for higher voltage and current connections, as they will generate more heats. However, most of the chips are surface-mount devices (more compact), so that their 5 V supplies are on the top layers. The distribution of the layers should be symmetrical, which means if the first layer is for 5 V connection, the bottom layer can only be GND, and the inner two layers can only be 300 V power connections. Otherwise, the PCB might be bent due to uneven heating within the layers. The copper thickness of the inner two layers is set to 2 oz to reduce the temperature rise.

Moreover, about 470 vias are used to make connections between two diffident layers in thus PCB. The size of vias is set to 2.5 mm pad diameter and 1.8 mm hole diameter. According to the Via Size Calculator in KiCad, the power loss would only be W when the applied current is 2 A, which is reasonably low. The PCB layout is presented in **Figure 3.4** below. The figures of each layer are presented in the Appendix.



**Figure 3.4** PCB Layout of Diode Clamped Inverter Board (4-Layer)

***3.4* Physical Product**

The manufacturing requirements are given in the **Table 3.2** below.

**Table 3.2** Manufacturing Requirements of Inverter Board

|  |  |
| --- | --- |
| Length (mm) | 294 mm |
| Width | 144 mm |
| Material | FR-4 |
| Layer | 4 |
| Thickness | 2 mm |
| Copper thickness of outer layer | 1 oz |
| Copper thickness of inner layer | 2 oz |
| Surface treatment | HASL LF |

The physical product of the diode clamped inverter board (4-layer) is presented in **Figure 3.5**.

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**Figure 3.5** Physical Product of Diode Clamped Inverter Board (4-Layer)

**Chapter 4: Hardware Design: Control Board and its Peripherals**

***4.1* Schematic**

The whole schematic of control board and its peripherals is in the Appendix, which can be divided into the following parts:

**ADC Sampling:**

Four operational amplifiers (op-amp) are used for ADC sampling, one used for the positive DC battery power sampling and the other three used for the phase currents sampling. The configurations of the non-inverting amplifiers are presented in **Figure 4.1**.



**Figure 4.1** Schematic of Non-inverting Amplifier (left: DC voltage; right: phase A current)

For positive DC battery power sampling, the positive pole is connected to “+BATT”, and the “GNDREF” of the inverter board is connected to GND of the control board. Assuming the voltages of two DC-link capacitors are equal (balanced), the voltage between “+BATT” and GND will be 150 V, which is half of the DC battery voltage. The potential divider consisting of R40 and R41 then divide the voltage by 101, and the voltage at amplifier’s pin 3 is 1.485 V. The output voltage of the non-inverting amplifier is given by:

*Eqn.4.1*

Thus, if the DC-link capacitors are balanced, the output voltage of non-inverting amplifier would be 1.5 V. If it is higher than 1.5V, then the high-side capacitor over-charged and the low-side capacitor under-charged, and vice versa. As the sum of two DC-link capacitors’ voltage equals to 300V, the voltage of low-side DC-link capacitor can be derived. Therefore, the relationship of non-inverting amplifier’s output voltage, high-side DC-link capacitor’s voltage , and low-side DC-link capacitor’s voltage can be given by:

*Eqn.4.2*

*Eqn.4.3*

For the phase current sampling, the output voltage of the op-amp could be given by:

*Eqn.4.4*

where the range of phase A signal voltage is from 0 V to 5 V, so that the output voltage of the amplifier would not exceed 3.3 V.

**Connectors to F28379D Launchpad:**

All the input of optical transmitters are connected to EPWM (Enhanced PWM) modules. ADC sampling of phase A current, phase B current, and DC voltage are connected to three different ADC channels. Moreover, there are two types of connectors are reserved for motor’s encoder: 3-pin and 5-pin. The 3-pin version receives UART to decode, and the 5-pin version receives quadrature AB square waves to decode.

图示

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**Figure 4.2** Schematic of Connectors to F28379D Launchpad

***4.2* PCB Layout**

There are two layers in this PCB, the top layer connects all 5 V, and the bottom layer connects all GND. PCB layout of the control board (2-layer) is presented in **Figure 4.3** below.

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**Figure 4.3** PCB Layout of Control Board (2-layer)

***4.3* Physical Product**

The physical product of the control board (2-layer) is presented in **Figure 4.4** below. The overall size is 193 mm 123 mm, the thickness of the board is 1.6 mm, and the thickness of copper is 1 oz.

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**Figure 4.4** Physical Product of Control Board (2-layer)

**Chapter 5: Software Design: Implementation on MCU**

***5.1* Files Structure and IDE Configurations**

**5.1.1 IDE Configurations**

**5.1.2 File Structure**

***5.2* Algorithm Implementation**

**5.2.1 ADC**

Single-end mode

**5.2.2 SPWM**

**5.2.3 PI Controller**

**5.2.4 Motor’s Encoder Decoding**

**5.2.5 Control Logic**

**Chapter 6: System Testing, Validation, and Analysis**

***6.1* Testing and Validation**

**6.1.1 Simulation: Current Control**

**6.1.2 Simulation: Speed Control**

**6.1.3 Simulation: DC-link Voltage Balance Contro**l

**6.1.4 Hardware: Gate Drive Validation in Inverter Board**

**6.1.5 Software: ADC Sampling**

**6.1.6 Software: SPWM Generation**

***6.2* Results Analysis**

**6.2.1 Simulation**

**6.2.2 Hardware**

**6.2.3 Software**

**Chapter 7: Conclusion and Reflection**

***7.1* Discussions**

**7.1.1 Simulations**

**7.1.2 Hardware**

**7.1.3 Software**

**7.1.4 Future Works**

Hardware in loop

GUI

***7.2* Reflection on Management**

**7.2.1 Budget Management**

**7.2.2 Time Management**

**References**

[1] B. Wu, “High Power Converters and AC Drives”, Wiley IEEE, 2nd Edition, 2016

[2] G. Abad, “Power Electronics and Electric Drives for Traction Applications”, Wiley, 2016

[3] A. Hughes “Electric Motors and Drives: Fundamentals, types, and applications”, 5th Edition, Elsevier, 2019

[4] S. N. Vukosavic, “Electrical Machines”, Springer, 2012

**Appendix**

Schematic of three-phase three-level diode clamped inverter in KiCad:

图示

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Top layer (5 V) of three-phase three-level diode clamped inverter in KiCad:

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Second layer (+BATT) of three-phase three-level diode clamped inverter in KiCad:

地图

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Third layer (-BATT) of three-phase three-level diode clamped inverter in KiCad:

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Bottom layer (GND) of three-phase three-level diode clamped inverter in KiCad:

地图

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Schematic of control board in KiCad:

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