3

DC-Link Capacitor Current and Sizing in NPC and CHB Inverters

3.1 Introduction

During the last decades, the presence of multilevel (ML) inverters has been steadily increasing in a variety of applications in the manufacturing, transport, energy, mining, and other industries [1, 2]. An essential part of ML inverter design is the selection of DC-link capacitors. The capacitors are a sensitive element of the inverter and a common source of failures. Capacitor lifetime is highly affected by thermal as well as overvoltage stresses, both of which can be estimated based on an analysis of the capacitor current [3, 4].

Thermal stress occurs due to losses on the DC-link capacitor's equivalent series resistance (ESR). The rms value of the current flowing through a DC-link capacitor can provide a first approximation for its losses. The literature contains rms expressions for the capacitor current of the two-level [5–7] and (single-phase) three-level cascaded H-bridge (CHB) inverters [8]. Use of these expressions for loss estimation assumes a fixed ESR value. However, the ESR is a function of the frequency of the capacitor current [3, 4]. Since the current of a DC-link capacitor comprises several harmonics located at different frequencies, it is necessary to determine the rms values of the capacitor current harmonics and use the appropriate value of ESR for each harmonic. For the two-level inverter, DC-link current harmonics have been derived in [9], while a general analytical method for calculating DC-link current harmonics in inverters has been proposed in [10].

Overvoltage stress may occur due to low-frequency (LF) capacitor voltage oscillations (ripple). In the two-level inverter, such oscillations do not appear under balanced load conditions. This is not the case, however, in three-level inverters. A plot of the amplitude of the capacitor voltage ripple in the three-level neutral point clamped (NPC) inverter [11] can be found in [12], for the case of sinusoidal pulse width modulation (SPWM). Moreover, capacitor-balancing techniques for the

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NPC inverter, which achieve smaller ripple amplitudes, are described in [13–16]. Regarding the CHB inverter topology, estimates for the capacitor voltage ripple can be found in [17], again for the case of SPWM.

This chapter presents a systematic analysis of the DC-link capacitor current in three-level NPC and CHB inverters, which provides the basis for DC-link capacitor sizing in these topologies. Methods for analyzing the two-level inverter DC-link capacitor current are extended to three-level inverters, to estimate the capacitor rms current and derive its harmonic spectrum. A new numerical approach for calculating the rms value and LF harmonics of the capacitor current is also proposed. Unlike existing methods, the proposed approach has the advantage of being easily adaptable to different modulation strategies and higher-level inverters. Results based on this approach are presented for a number of common modulation strategies.

The chapter is structured as follows: Section 3.2 gives a description of the parameters considered during DC-link capacitor sizing, explaining their relation to the capacitor current. Section 3.3 derives expressions for the rms value of the DC-link capacitor current in three-level NPC and CHB topologies [18], while Section 3.4 presents a harmonic analysis of this current [19]. Section 3.5 describes the proposed numerical method for deriving the current rms value and the amplitude of voltage ripple for the DC-link capacitors of the two topologies. Then, Section 3.6 validates the results of the previous sections using simulations in MATLAB®-Simulink. Finally, Section 3.7 compares the examined three-level topologies with respect to their capacitor requirements, discusses the accuracy and applicability of the presented methods, and describes the application of the proposed approach to higher-level inverters.

3.2 Inverter DC-Link Capacitor Sizing

The selection of inverter DC-link capacitors is determined by the required voltage, (ripple) current, and capacitance ratings, as explained below:

- The capacitor voltage rating is typically higher than the operating DC-link voltage, to account for voltage oscillations and other effects such as input (grid) voltage fluctuations or transitory regenerative operation of the inverter.
- The ripple (rms) current rating, $I_{\mathrm{C,max}}$, is a way of expressing the affordable limit for capacitor losses, $P_{\mathrm{C,max}}$. $I_{\mathrm{C,max}}$ is commonly given in capacitor datasheets [3, 4] for a certain value of ESR, R_C, as

$$P_{\mathrm{C,max}} = R_{\mathrm{C}} \cdot I_{\mathrm{C,max}}^2 \tag{3.1}$$

  According to the above, a calculation of the DC-link capacitor rms current in a certain inverter application can give a first estimate for the required ripple current rating. However, for electrolytic capacitors, the value of the ESR varies with the frequency of the capacitor current. A typical ESR–frequency characteristic is illustrated in Figure 3.1 [4].

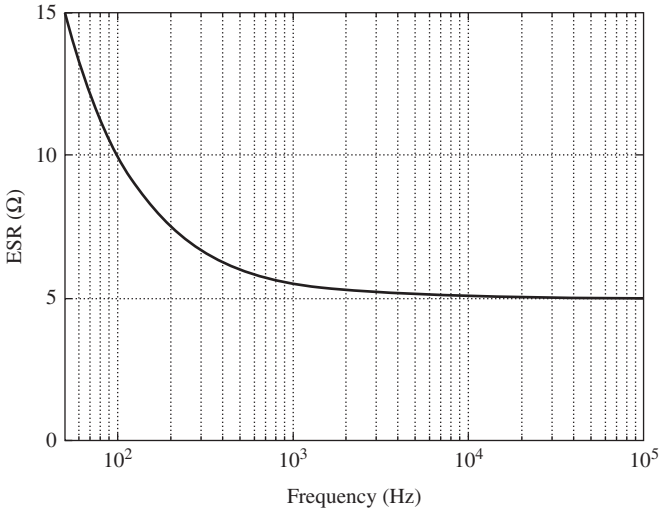

Figure 3.1 ESR–frequency characteristic of a 4.7 mF/450 V capacitor. (Reproduced from [4].)

Hence, if more than one current harmonic h, with amplitudes I_h (rms values $I_{h,\mathrm{rms}}$) and frequencies f_h flow through the capacitor, the losses should be calculated using

$$P_{\mathrm{C}} = \sum_h R_{\mathrm{C}}(f_h) \cdot I_{h,\mathrm{rms}}^2 \tag{3.2}$$

where $R_{\mathrm{C}}(f_h)$ stands for the value of ESR at frequency f_h. Then, the capacitor's ripple current rating can be selected so that P_{C} does not exceed $P_{\mathrm{C,max}}$.

- The required capacitance is determined by the affordable amplitude of the DC-link voltage oscillations ($\Delta V_{\mathrm{C,max}}/2$), which is also dependent on the capacitor current harmonics. Assuming that, in the worst case, all these harmonics (or equivalently all peaks of voltage harmonics) are in phase, the required capacitance is given by

$$C \geq \frac{1}{\Delta V_{\mathrm{C,max}}/2} \cdot \sum_h \frac{I_h}{2\pi f_h} \tag{3.3}$$

According to this equation, high-frequency (HF) capacitor current harmonics, which appear due to the switching (PWM, pulse width modulation) operation of the inverter, have a small effect on the capacitor voltage ripple. LF harmonics, on the other hand, located at multiples of the inverter fundamental frequency, can increase the required capacitance, since they give rise to LF capacitor voltage oscillations.

It is noted that this study focuses on the effect of the inverter on the rating of the DC-link capacitor. Increased capacitance can, therefore, be required for decreasing the DC-link capacitor voltage ripple caused by the inverter front end (e.g., a rectifier),

or for other purposes, such as for voltage support during a temporary loss of input power. Inversely, less capacitance may be required in cases where the power source (e.g., a battery) is capable of providing part of the LF capacitor current as this will decrease the capacitor voltage ripple.

3.3 Analytical Derivation of DC-Link Capacitor Current RMS Expressions

In this section the method used in [5] for the derivation of the two-level inverter capacitor current rms expression is summarized and extended to the three-level NPC and CHB topologies. The method considers each inverter IGBT-diode module as a switch that, while on, carries the current of the respective phase. If the sum of the currents through the upper switches of an inverter is i_{d}, then the DC component of i_{d} is (assumed to be) supplied by the inverter DC source, while the AC component is filtered, and hence carried by the DC-link capacitor. The rms value of the capacitor current, $I_{\mathrm{C,rms}}$, is calculated using the average (DC) and rms values of i_{d}, $I_{\mathrm{d,DC,}}$ and $I_{\mathrm{d,rms}}$, respectively as

$$I_{\mathrm{C,rms}} = \sqrt{I_{\mathrm{d,rms}}^2 - I_{\mathrm{d,DC}}^2} \tag{3.4}$$

The calculation of the average and rms values for current i_{d} is based on the analysis of its transitions within a single switching period. If i_{d} is equal to $i_{\mathrm{d,int1}}$, $i_{\mathrm{d,int2}}$, …, $i_{\mathrm{d,int}k}$, during k time intervals T_{int1}, T_{int2}, …, $T_{\mathrm{int}k}$, respectively, then its average and rms values during a switching period, T_{s}, centered at reference angle θ, are given by

$$i_{\mathrm{d,DC}}(\theta) = \frac{1}{T_{\mathrm{s}}}\left(\sum_k T_{\mathrm{int}k} \cdot i_{\mathrm{d,int}k}\right) = \sum_k \delta_{\mathrm{int}k} \cdot i_{\mathrm{d,int}k} \tag{3.5}$$

$$i_{\mathrm{d,rms}}^2(\theta) = \frac{1}{T_{\mathrm{s}}}\left(\sum_k T_{\mathrm{int}k} \cdot i_{\mathrm{d,int}k}^2\right) = \sum_k \delta_{\mathrm{int}k} \cdot i_{\mathrm{d,int}k}^2 \tag{3.6}$$

(where the interval duty cycles, $\delta_{\mathrm{int}k}$, and currents, $i_{\mathrm{d,int}k}$, are also functions of θ, but $\delta_{\mathrm{int}k}(\theta)$ and $i_{\mathrm{d,int}k}(\theta)$ are used in place of them, respectively, for reasons of conciseness). The interval duty cycles $\delta_{\mathrm{int}k}$ and respective currents $i_{\mathrm{d,int}k}$ are also functions of θ. The average and rms values of i_{d} over a fundamental period are obtained using the following expressions:

$$I_{\mathrm{d,DC}} = \frac{1}{2\pi}\int_0^{2p} i_{\mathrm{d,DC}}(\theta)\mathrm{d}\theta \tag{3.7}$$

$$I_{\mathrm{d,rms}} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_{\mathrm{d,rms}}^2(\theta)\ \mathrm{d}\theta} \tag{3.8}$$

If the expressions for $i_{\mathrm{d,DC}}(\theta)$ and $i_{\mathrm{d,rms}}(\theta)$ change during parts (sectors) of the fundamental cycle, the above expressions are written as sums of integrals for the different sectors.

3.3.1 NPC Inverter

For the three-level NPC inverter, the current i_{d} is shown in Figure 3.2a. The AC component of i_{d} is the current of the upper capacitor of the DC-link (C_2). Assuming SPWM, the (normalized w.r.t. $V_{\mathrm{DC}}/2$) phase reference voltages, $v_{x,\mathrm{ref}}$, shown in Figure 3.3, and the respective duty cycles, δ_x, are given by Equations 3.9 and 3.10 below,

$$v_{x,\mathrm{ref}} = M\sin(\theta + \theta_x) \tag{3.9}$$

$$\delta_x = v_{x,\mathrm{ref}} = M\sin(\theta + \theta_x) \tag{3.10}$$

where M is the inverter modulation index, while θ_x for phases *a, b*, and *c* is equal to θ_α, θ_b, and θ_c, respectively:

$$\theta_a = 0, \theta_b = \frac{2\pi}{3}, \theta_c = -\frac{2\pi}{3} \tag{3.11}$$

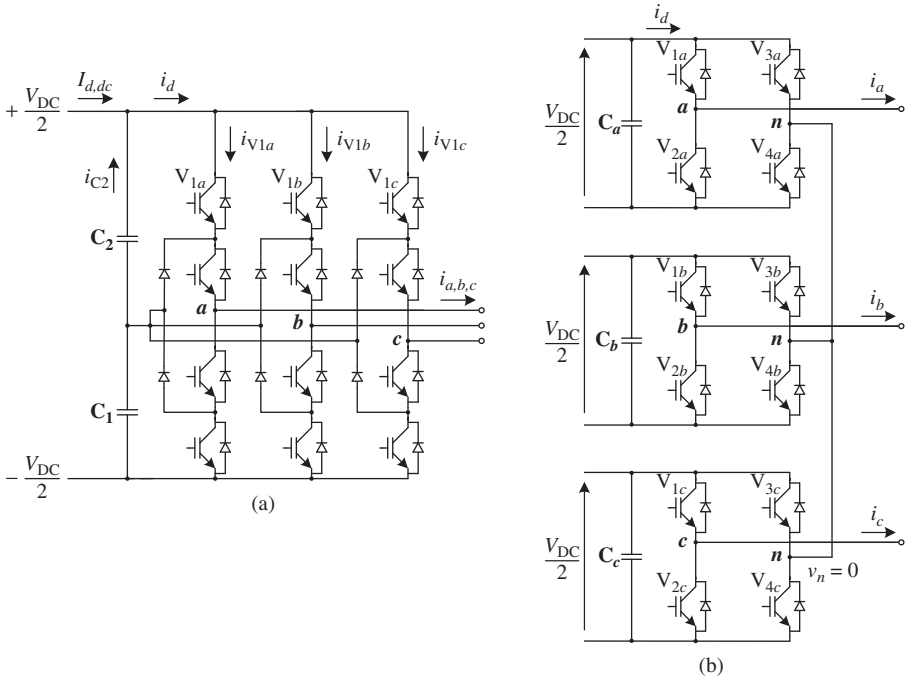

Figure 3.2 Three-phase three-level (a) neutral-point-clamped and (b) cascaded H-bridge inverter

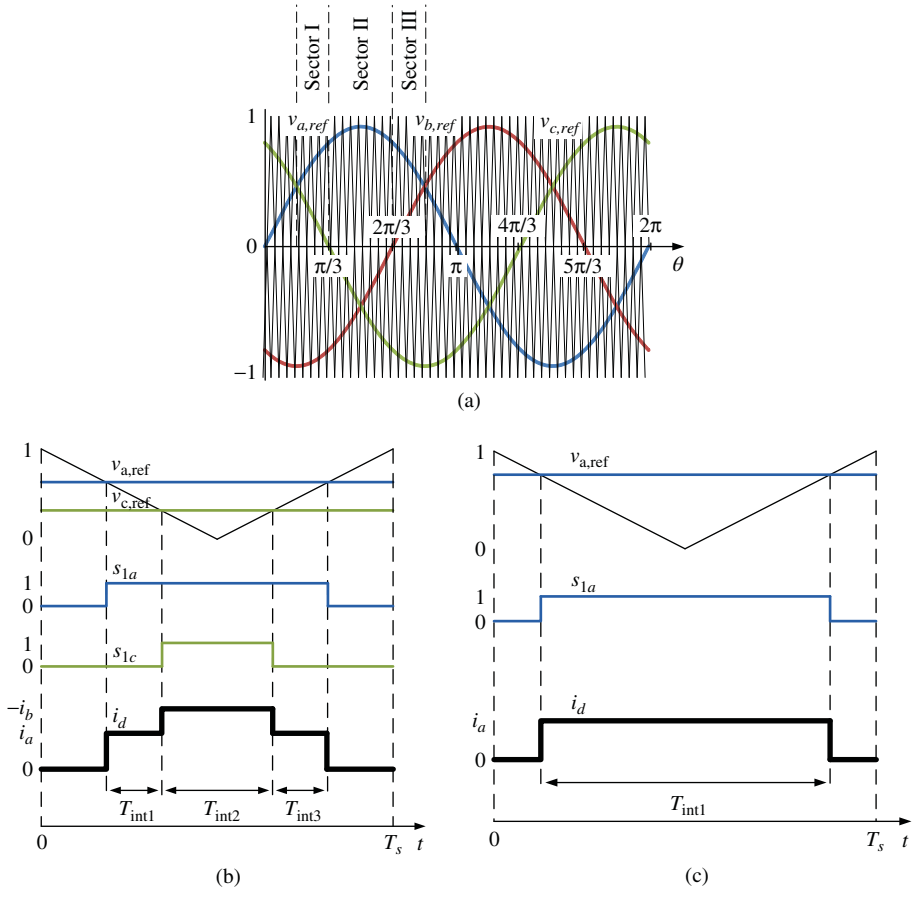

Figure 3.3 (a) Reference and upper carrier waveforms for the NPC inverter, and analysis of a switching cycle for (b) Sector I and (c) Sector II

Moreover, the sinusoidal phase currents i_x are assumed to be given by

$$i_x = I_{\text{pk}} \sin(\theta + \theta_x - \phi) \tag{3.12}$$

where I_{pk} is the current peak value (magnitude) and ϕ is the power angle of the inverter load.

The upper modules are modulated by the upper carrier waveform, as shown in Figure 3.3a. It can be shown that the waveform of i_{d} has a period of $T/3$, where T is the period of a reference waveform. Hence, for the derivation of $I_{\text{d,DC}}$ and $I_{\text{d,rms}}$, an angle interval of $2\pi/3$ needs to be analyzed. The selected interval covers the values of θ between $\pi/6$ and $5\pi/6$ and can be divided into three sectors (I, II, and III), as shown in Figure 3.3a. The duty cycles of the switching intervals ($\delta_{\text{int}k}$) and the respective i_{d} currents ($i_{\text{d,int}k}$) change between Sectors I and II, as shown in Figure 3.3b,c. In the figure, s_{1x} represents the state of module V_{1x} (0 for OFF and 1 for ON).

Tables 3.1 and 3.2 present the expressions of the above duty cycles in a concise form that can be used according to Equations 3.7 and 3.8 to derive the DC and rms values of i_{d} for each sector. The resulting expressions are shown in Table 3.3 (Sector III can be analyzed similarly to Sector I).

Since the expressions for $i_{\mathrm{d,DC}}(\theta)$ and $i_{\mathrm{d,rms}}(\theta)$ change during sectors of the fundamental cycle, Expressions 3.7 and 3.8 take the form of Equations 3.13 and 3.14, respectively,

$$I_{\mathrm{d,DC\text{-}NPC}} = \frac{3}{2\pi}\left(\int_{\pi/6}^{\pi/3} i_{\mathrm{d,DC,I\text{-}NPC}}(\theta)\,\mathrm{d}\theta + \int_{\pi/3}^{2\pi/3} i_{\mathrm{d,DC,II\text{-}NPC}}(\theta)\mathrm{d}\theta + \int_{2\pi/3}^{5\pi/6} i_{\mathrm{d,DC,III\text{-}NPC}}(\theta)\,\mathrm{d}\theta\right) \tag{3.13}$$

$$I_{\mathrm{d,rms\text{-}NPC}} = \sqrt{\frac{3}{2\pi}\left(\int_{\pi/6}^{\pi/3} i^2_{\mathrm{d,rms,I\text{-}NPC}}(\theta)\,\mathrm{d}\theta + \int_{\pi/3}^{2\pi/3} i^2_{\mathrm{d,rms,II\text{-}NPC}}(\theta)\mathrm{d}\theta + \int_{2\pi/3}^{5\pi/6} i^2_{\mathrm{d,rms,III\text{-}NPC}}(\theta)\mathrm{d}\theta\right)} \tag{3.14}$$

Table 3.1 Switching intervals for Sector I of the NPC inverter

Total duration	Total duty cycle	Current i_{d}
$T_{\mathrm{int1}} + T_{\mathrm{int3}}$	$\delta_a - \delta_c$	i_a
T_{int2}	δ_c	$-i_b$

Table 3.2 Switching intervals for Sector II of the NPC inverter

Total duration	Total duty cycle	Current i_{d}
T_{int1}	δ_a	i_a

Table 3.3 Expressions for $i_{\mathrm{d,DC}}(\theta)$ and $i_{\mathrm{d,rms}}(\theta)$ for the three sectors of the NPC inverter

Sector I	Sector II	Sector III
$i_{\mathrm{d,DC,I\text{-}NPC}}(\theta) = (\delta_a - \delta_c)i_a + \delta_c(-i_b)$	$i_{\mathrm{d,DC,II\text{-}NPC}}(\theta) = \delta_a i_a$	$i_{\mathrm{d,DC,III\text{-}NPC}}(\theta) = (\delta_a - \delta_b)i_a + \delta_b(-i_c)$
$i^2_{\mathrm{d,rms,I\text{-}NPC}}(\theta) = (\delta_a - \delta_c)i_a^2 + \delta_c(-i_b)^2$	$i^2_{\mathrm{d,rms,II\text{-}NPC}}(\theta) = \delta_a i_a^2$	$i^2_{\mathrm{d,rms,III\text{-}NPC}}(\theta) = (\delta_a - \delta_b)i_a^2 + \delta_b(-i_c)^2$

which results in:

$$I_{\text{d,DC-NPC}} = \frac{3}{4} M I_{\text{pk}} \cos\phi \tag{3.15}$$

$$I_{\text{d,rms-NPC}} = I_{\text{pk}} \sqrt{\frac{\sqrt{3}M}{4\pi}\left(\cos^2\phi + \frac{1}{4}\right)} \tag{3.16}$$

Finally, according to Equation 3.4, the rms current expression for the upper capacitor (C_2) of the three-level NPC inverter is shown below:

$$I_{\text{C,rms-NPC}} = I_{\text{pk}} \sqrt{\frac{M}{2}\left[\frac{\sqrt{3}}{2\pi} + \left(\frac{2\sqrt{3}}{\pi} - \frac{9}{8}M\right)\cos^2(\phi)\right]} \tag{3.17}$$

Due to symmetry (between the positive and negative half cycles) of the reference and carrier waveforms, the expression for the lower DC-link capacitor (C_1) is identical.

3.3.2 CHB Inverter

The derivation of the DC-link capacitor current rms for the three-phase CHB inverter is based on the analysis of a single H-bridge, that of phase *a*. Each phase of the H-bridge has its own capacitor whose ripple current, in contrast to the two-level and NPC topologies, is not affected by the switching operations of the other phases. Hence, the analysis of a single phase H-bridge inverter is enough to provide the three-phase inverter expressions. For the CHB inverter the sum of the currents through the two upper IGBT/diode modules is used for the derivation. The calculation of the capacitor rms current is based on the analysis of one out of two symmetrical sectors (Sector I) covering the interval of $\theta = [0, \pi]$.

According to Figure 3.4 and Table 3.4:

$$i_{\text{d,DC,I-CHB}}(\theta) = \delta_a \cdot i_a \tag{3.18}$$

$$i^2_{\text{d,rms,I-CHB}}(\theta) = \delta_a \cdot i_a^2 \tag{3.19}$$

The average (DC) and rms values of current i_{d} for the CHB inverter, are calculated using Equations 3.7 and 3.8, respectively, for $\theta = [0, \pi]$, as

$$I_{\text{d,DC-CHB}} = \frac{M I_{\text{pk}}}{2} \cos\phi \tag{3.20}$$

$$I_{\text{d,rms-CHB}} = I_{\text{pk}} \sqrt{\frac{M(3 + \cos(2\phi))}{3\pi}} \tag{3.21}$$

The rms current expression for each capacitor in this topology is then given by Equation 3.4, as

$$I_{\text{C,rms-CHB}} = I_{\text{pk}} \sqrt{\frac{M}{24\pi}[24 - 3M\pi + (8 - 3M\pi)\cos(2\phi)]} \tag{3.22}$$

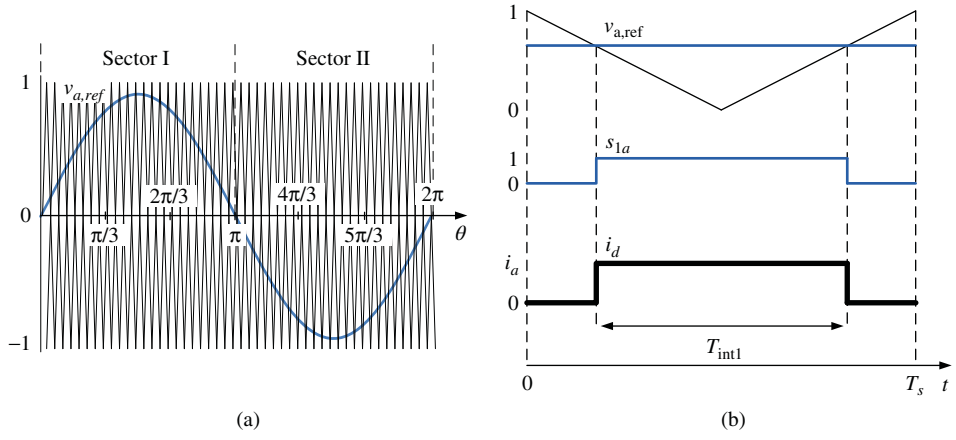

Figure 3.4 (a) Reference and upper carrier waveforms for the CHB inverter and (b) analysis of a switching cycle for Sector I

Table 3.4 Switching intervals for Sector I of the CHB inverter

Total duration	Total duty cycle	Current i_d
T_{int1}	δ_a	i_a

It is noted that the DC-link capacitor current of a single-phase H-bridge modulated by the SPWM strategy had been investigated in [8], deriving an expression for the rms value of HF capacitor current harmonics.

3.4 Analytical Derivation of DC-Link Capacitor Current Harmonics

In this section, the geometric wall model, a method introduced by Black in [20], is used to analytically derive the DC-link current spectra of three-level inverters. The geometric wall model provides an alternative way of representing the process of pulse generation in PWM converters. As shown in [21], the carrier and reference waveforms are redrawn in a transformed plane, so that the intersections between the new waveforms define the same train of pulses for a given PWM modulation strategy. The new plane can be divided into identical unit cells, which are characteristic for each strategy. The width of the generated pulses is periodic with respect to both dimensions of this plane, thus the function (F) that describes the pulse train can be written as a double Fourier series.

The Fourier analysis results in a spectrum that plots the function in the frequency domain. The (complex) Fourier coefficient for a harmonic, ${}^{mn}F$, located at frequency

$nf_o + mf_c$ (n, m are integers), where f_o and f_c are the fundamental and switching frequencies, respectively, are given by the following integral over the area of a unit cell:

$$^{mn}F = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} F(x,y)e^{j(mx+ny)}dxdy \tag{3.23}$$

The geometric wall model has been widely applied for analyzing the output (PWM) voltage harmonics of different inverter topologies and PWM strategies [21]. In this case, function F represents a phase voltage (commonly that of phase a). For the analysis of the DC-link capacitor current, on the other hand, F represents a module current, namely the current through the IGBT/diode module V_{1a}. The Fourier coefficients for the currents of the two other upper modules, V_{1b} and V_{1c}, are given by multiplying the coefficients for i_{V1a} by $e^{+2jn\pi/3}$ and $e^{-2jn\pi/3}$, respectively. Since current i_d is the complex sum of these three module currents, its Fourier coefficients can be calculated using the following equation:

$$^{mn}i_d = {}^{mn}i_{V1a} + {}^{mn}i_{V1b} + {}^{mn}i_{V1c} \tag{3.24}$$

The coefficients for the DC-link capacitor current are also given by Equation 3.24, excluding the DC component ($n = m = 0$). An analysis of the DC-link capacitor current harmonics for the two-level inverter can be found in [9].

3.4.1 NPC Inverter

As in the two-level inverter, the instantaneous current flowing through the DC-link capacitor of the NPC inverter is the complex sum of the currents through the inverter's three upper modules (V_{1a}, V_{1b}, and V_{1c}), shown in Figure 3.2a. Thus, harmonic analysis of i_{V1a} is sufficient to calculate the DC-link capacitor current harmonics.

The following solution is given for SPWM implemented as the three-level phase-disposition pulse width modulation (PD PWM) [21], which uses two in-phase triangular carriers (and a sinusoidal reference waveform). Application of the geometric wall model to the three-level PD PWM results in the unit cell illustrated in Figure 3.5.

The complex Fourier coefficients of i_{V1a} come from:

$$^{mn}i_{V1a\text{-NPC}} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} i_{V1a\text{-NPC}}(x,y)\, e^{j(mx+ny)}dxdy \tag{3.25}$$

According to [21], the output voltage for phase a is positive only in the closed region (III), at the center of the graph. Hence, this is the only region where module V_{1a} carries the current of phase a. In regions I and II, the current through V_{1a} is zero. The above integral therefore reduces to:

$$^{mn}i_{V1a\text{-NPC}} = \frac{I_{pk}}{2\pi^2}\int_{-\pi/2}^{\pi/2}\int_{-\pi M\cos y}^{\pi M\cos y} \cos(y-\phi)\cdot e^{j(mx+ny)}dxdy \tag{3.26}$$

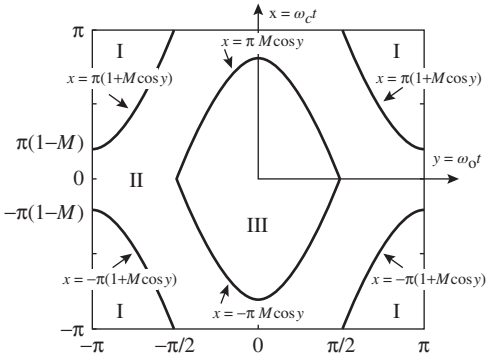

Figure 3.5 Unit cell for the three-level PD PWM method [21]

The solution of Equation 3.26 provides the complex Fourier coefficients for $i_{\mathrm{V1}a}$, while Equation 3.24 gives the respective coefficients for the upper DC-link capacitor of the three-level NPC inverter as follows:

Baseband harmonics, for ($m = 0$ and) $n = 3, 9, 15, \ldots$:

$$^{0n}i_{\text{C-NPC}} = (-1)^{\frac{n-1}{2}} \frac{6MI_{\text{pk}}}{\pi(n^2-4)} \left(\frac{2\cos\phi}{n} + \text{j}\sin\phi \right) \tag{3.27}$$

Carrier harmonics, for ($n = 0$ and) $m = 1, 2, 3, \ldots$:

$$^{m0}i_{\text{C-NPC}} = -\frac{3I_{\text{pk}}}{m\pi} J_1(Mm\pi)\cos\phi \tag{3.28}$$

Sideband harmonics, for n even and $m = 1, 2, 3, \ldots$:

$$^{mn}i_{\text{C-NPC}} = (-1)^{\frac{n}{2}} \frac{3I_{\text{pk}}}{2m\pi} \begin{bmatrix} \text{e}^{\text{j}\phi} J_{n-1}(Mm\pi) \\ -\text{e}^{-\text{j}\phi} J_{n+1}(Mm\pi) \end{bmatrix} \tag{3.29}$$

Sideband harmonics, for n odd and $m = 1, 2, 3, \ldots$:

$$^{mn}i_{\text{C-NPC}} = (-1)^{\frac{n-1}{2}} \frac{6I_{\text{pk}}}{m\pi^2} \sum_{k=1,3,5\ldots} J_k(Mm\pi)$$
$$\left[\frac{\cos\phi + \text{j}\,(n+k)\sin\phi}{1-(n+k)^2} - \frac{\cos\phi + \text{j}(n-k)\sin\phi}{1-(n-k)^2} \right] \tag{3.30}$$

3.4.2 CHB Inverter

As explained in Section 3.3.2, the current of each capacitor in this topology is only determined by the operation of the respective H-bridge. Hence, the derivation of a capacitor current is not given by an equation in the form of Equation 3.24.

Instead, similar to Section 3.3.2, the current that will be harmonically analyzed for this topology is i_{d}, shown in Figure 3.2b. The AC component of this current flows through the DC-link capacitor of phase *a*.

A modulation strategy for the CHB inverter that is equivalent to PD PWM for the NPC inverter is assumed. This strategy, that yields equal switching losses and the same output voltage spectra for the two topologies, is described in pages 504–506 of [21]. Pulse generation is again based on the unit cell of Figure 3.5, therefore

$$ {}^{mn}i_{\text{d-CHB}} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} i_{\text{d-CHB}}(x,y)\,\mathrm{e}^{\mathrm{j}(mx+ny)}\mathrm{d}x\mathrm{d}y \tag{3.31}$$

According to [21], the output voltage for phase *a* is positive in region III and negative in region(s) I, at the edges of the plot. The current i_{d} of the CHB inverter is therefore equal to the phase current i_a, or opposite to it ($-i_a$) in these regions, respectively. The above integral then reduces to:

$$ {}^{mn}i_{\text{d-CHB}} = \frac{I_{\text{pk}}}{2\pi^2}\left[\begin{array}{l}\displaystyle\int_{-\pi/2}^{\pi/2}\int_{-\pi M\cos y}^{\pi M\cos y}\cos(y-\phi)\cdot\mathrm{e}^{\mathrm{j}(mx+ny)}\mathrm{d}x\mathrm{d}y \\ \displaystyle -\int_{\pi/2}^{-\pi/2}\int_{\pi(1+M\cos y)}^{-\pi(1+M\cos y)}\cos(y-\phi)\cdot\mathrm{e}^{\mathrm{j}(mx+ny)}\mathrm{d}x\mathrm{d}y\end{array}\right] \tag{3.32}$$

which can be shown to be equal to:

$$ {}^{mn}i_{\text{d-CHB}} = \left\{\begin{array}{l}\frac{I_{\text{pk}}}{\pi^2}\displaystyle\int_{-\pi/2}^{\pi/2}\int_{-\pi M\cos y}^{\pi M\cos y}\cos(y-\phi)\,\mathrm{e}^{\mathrm{j}(mx+ny)}\mathrm{d}x\mathrm{d}y, \text{ for } n+m\rightarrow\text{even} \\ 0, \text{ for } n+m\rightarrow\text{odd}\end{array}\right\} \tag{3.33}$$

The solution of Equation 3.33 yields the Fourier coefficients of i_{d} which, apart from the DC component, are also the coefficients for the DC-link capacitor current of phase *a*:

Baseband harmonic, for ($m=0$ and) $n=2$, only:

$$ {}^{02}i_{\text{C-CHB}} = \frac{MI_{\text{pk}}}{2}\mathrm{e}^{\mathrm{j}\phi} \tag{3.34}$$

Carrier harmonics, for ($n=0$ and) m even:

$$ {}^{m0}i_{\text{C-CHB}} = -\frac{2I_{\text{pk}}}{m\pi}J_1(Mm\pi)\cos\phi \tag{3.35}$$

Sideband harmonics, for n even and m even:

$$ {}^{mn}i_{\text{C-CHB}} = (-1)^{1+\frac{n}{2}}\frac{I_{\text{pk}}}{m\pi}\left[\begin{array}{l}\mathrm{e}^{\mathrm{j}\phi}J_{n-1}(Mm\pi) \\ -\mathrm{e}^{-\mathrm{j}\phi}J_{n+1}(Mm\pi)\end{array}\right] \tag{3.36}$$

Sideband harmonics, for n odd and m odd:

$$
{}^{mn}i_{\text{C-CHB}} = (-1)^{\frac{n+1}{2}} \frac{4I_{\text{pk}}}{m\pi^2} \sum_{k=1,3,5\ldots} J_k(Mm\pi)
$$
$$
\left[\frac{\cos\phi + j\,(n+k)\sin\phi}{1-(n+k)^2} - \frac{\cos\phi + j(n-k)\sin\phi}{1-(n-k)^2} \right] \tag{3.37}
$$

3.5 Numerical Derivation of DC-Link Capacitor Current RMS Value and Voltage Ripple Amplitude

The analytical derivation of expressions for the rms value and the harmonics of the DC-link capacitor current in the previous sections assumed sinusoidal voltage reference waveforms (SPWM strategy). However, non-sinusoidal references are commonly used in practice in order to achieve higher output (line) voltages, corresponding to a maximum modulation index of $2/\sqrt{3}$ (≈ 1.1547). A numerical method for calculating the capacitor rms current in the case of such reference waveforms is proposed in this section.

The method is based on the analysis presented in Section 3.3 and operates according to the code included in Appendix B. The code divides the fundamental cycle into a number of intervals and calculates the values of Equations 3.5 and 3.6 for each of them. The cumulative sums of these values are then used to numerically evaluate Equations 3.7 and 3.8, and finally derive the rms capacitor current. Furthermore, in parallel to the rms current calculation, the proposed method calculates the amplitude of the capacitor voltage oscillations. The calculation can be performed for any modulation strategy, by accordingly changing the reference voltages (or, equivalently, the common-mode voltage) in the code. Results for the following strategies are presented in this study: (i) SPWM, (ii) SPWM with 1/6 third harmonic injection (SPWM + third harmonics), and (iii) space vector modulation (SVM) with equal distribution of duty cycles between the small vectors, implemented as a carrier-based strategy. The common-mode voltages for each strategy can be found in Appendix B.

Figure 3.6a,b plot the rms value of the capacitor current for the NPC and CHB topologies, normalized with respect to the phase rms current, I_{rms} (Norm. $I_{\text{C,rms}} = I_{\text{C,rms}}/I_{\text{rms}}$). For the NPC inverter the plot is the same for any modulation strategy (SPWM can reach up to $M = 1$), while for the CHB inverter it is shown for the SVM strategy.

The rms current rating of the DC-link capacitors is determined by the maximum value that $I_{\text{C,rms}}$ can take within the operating range of the inverter. Figure 3.6c illustrates this maximum (over the whole range of M) for each value of ϕ, for the examined modulation strategies. Given that the range of power factor (angle) is known for most inverter applications, this figure can be used to select the required capacitor rms current rating according to the applied strategy.

Similar graphs are derived below using the proposed method, for the amplitude ($\Delta V_{\text{C}}/2$) of the DC-link capacitor voltage ripple. Figure 3.7a,b plot this amplitude for

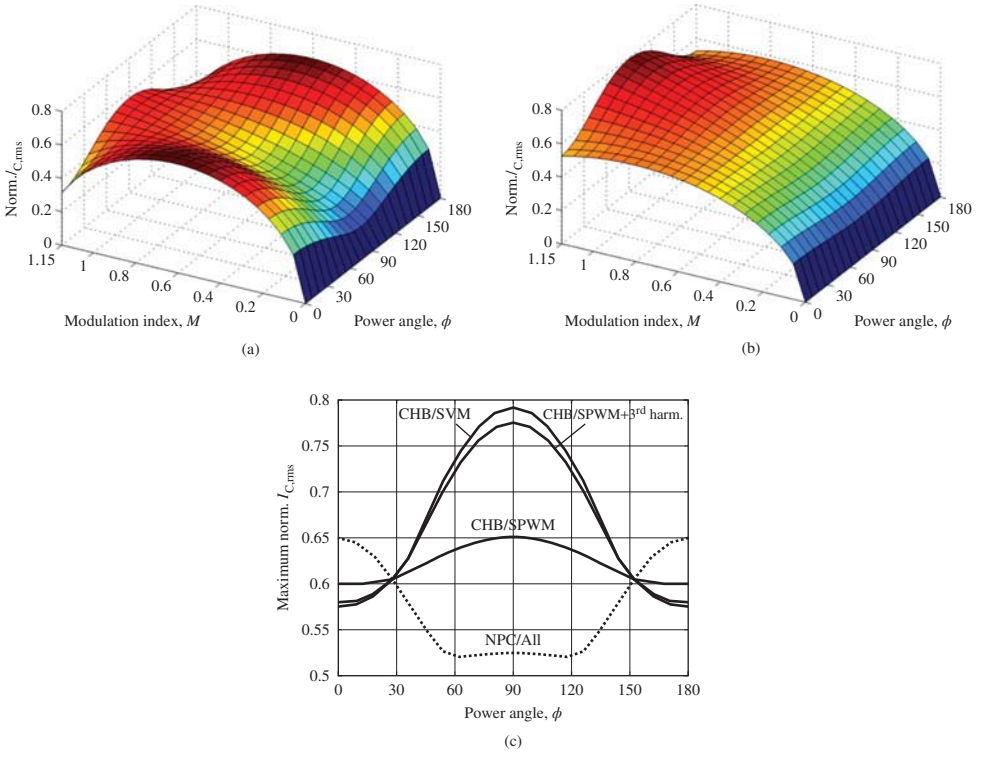

Figure 3.6 (a) Normalized rms capacitor current for the NPC inverter (same for all modulation strategies), (b) normalized rms capacitor current for the CHB inverter modulated by the SVM strategy, and (c) maximum normalized rms capacitor current for the NPC and CHB inverters, as a function of ϕ

the NPC and CHB topologies, respectively, for the case of the SVM strategy. Furthermore, Figure 3.7c,d illustrate the maximum amplitude of voltage ripple (which appears for maximum M) for the two topologies, for each modulation strategy. The presented values are normalized according to

$$\frac{\text{Norm.}\Delta V_{\text{C}}}{2} = \frac{f_{\text{C}}}{I_{\text{rms}}} \frac{\Delta V_{\text{C}}}{2} \tag{3.38}$$

and can be used to determine the capacitance required to limit the voltage ripple to a desired extent, $\Delta V_{\text{C,max}}$ (Section 3.3).

3.6 Simulation Results

In this section, the derived values of the DC-link capacitor rms current, voltage ripple, and current harmonics are validated using detailed circuit simulations in MATLAB®–Simulink (SimPowerSystems toolbox). An NPC and a CHB inverter

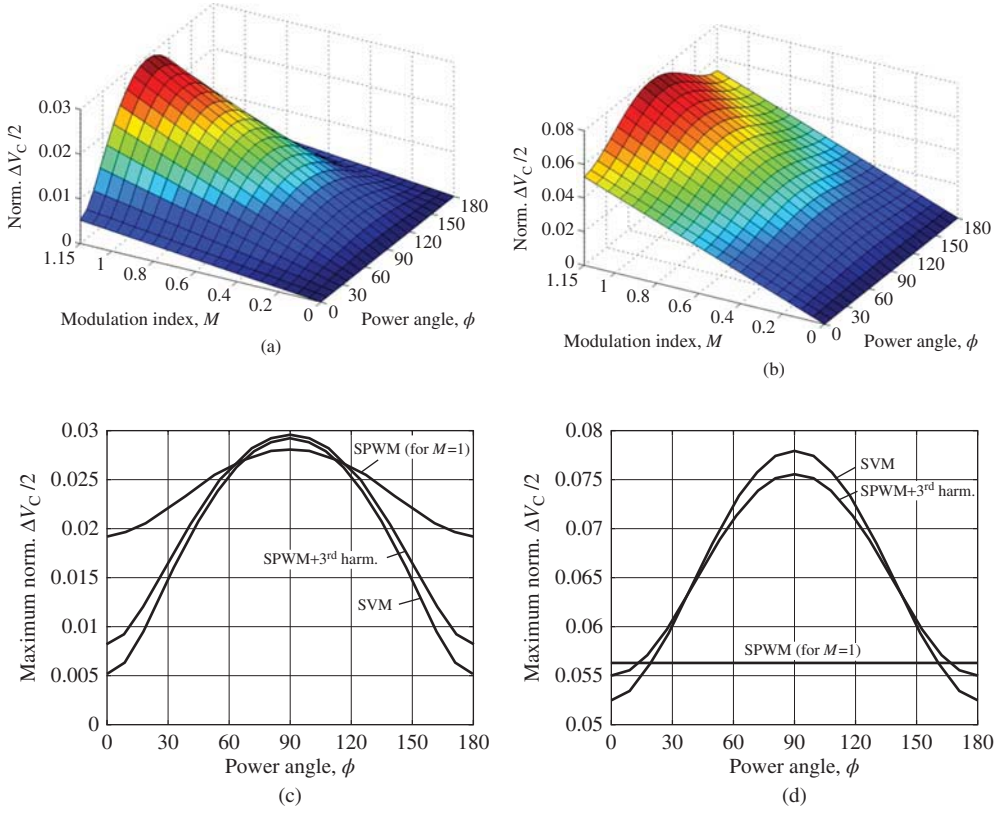

Figure 3.7 Normalized amplitude of capacitor voltage ripple for (a) the NPC and (b) the CHB inverter, modulated by the SVM strategy, and maximum normalized amplitude of capacitor voltage ripple for (c) the NPC and (d) the CHB inverter, as a function of ϕ

were simulated according to the operating parameters in Table 3.5. The capacitance value for the NPC inverter was set to 1 mF, as compared to 2.5 mF for the CHB inverter, on the basis of Equation 3.38 and Figure 3.7a,b. The estimated amplitude of voltage ripple for both topologies was then approximately 28 V, equal to a small percentage (7%) of the DC-link voltage, thus avoiding a significant distortion of the output voltages.

Figure 3.8 illustrates the line voltage v_{ab}, phase current i_a, and capacitor (C_2 for the NPC and C_a for the CHB) current i_C and voltage v_C for the two topologies. The simulated amplitude of capacitor voltage ripple agreed with the value of 28 V, calculated by the proposed method. Moreover, the rms values of the capacitor current measured during the simulations agreed with the values of 39.3 and 42.7 A given by the same method, as well as by Equations 3.17 and 3.22 for the NPC and CHB inverters, respectively.

Table 3.5 Simulation parameters

Parameter	Value
V_{DC}	400 V
I_{pk}	100 A
f_o	50 Hz
f_c	5 kHz
M	0.9
ϕ	30°
C_{NPC}	1 mF
C_{CHB}	2.5 mF

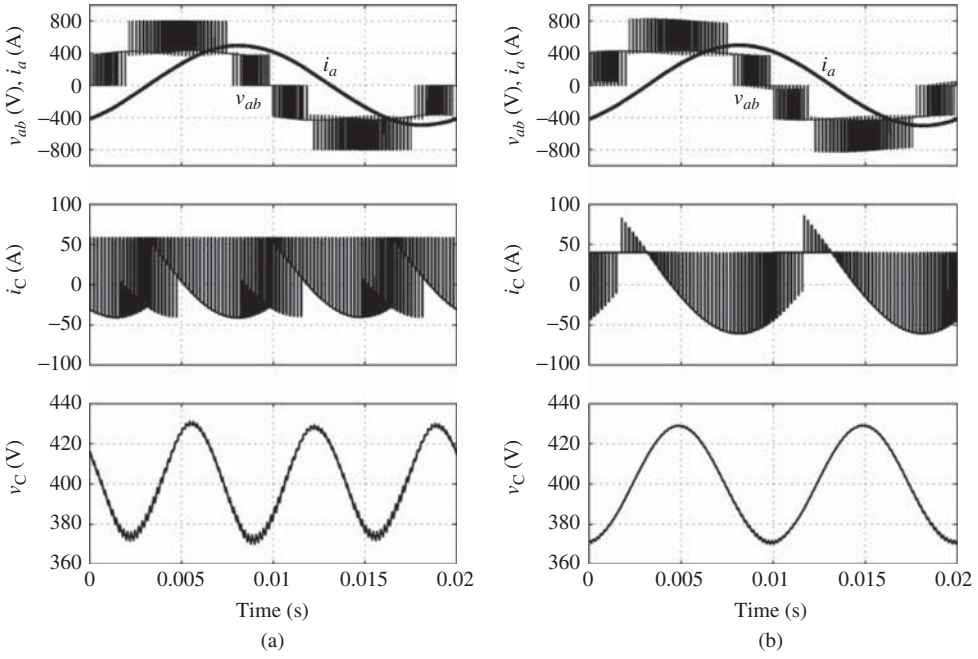

Figure 3.8 (a) DC-link capacitor rms current and (b) amplitude of voltage ripple for the NPC ($C = 1$ mF) and CHB ($C = 2.5$ mF) topologies as a function of M, for the parameters shown in Table 3.5

Figure 3.9 illustrates the capacitor current spectrum for the two topologies as derived from the above simulations, and uses it to validate the expressions presented in Section 3.4. Again, it can be seen that the frequencies and magnitudes of the current harmonics can be accurately reproduced by these expressions. Furthermore, the amplitude of the capacitor voltage ripple can be calculated by means of Equation 3.3. Considering only the baseband harmonics, this calculation gives a value of 28.6 V for both topologies, which is similar to that taken from the simulations.

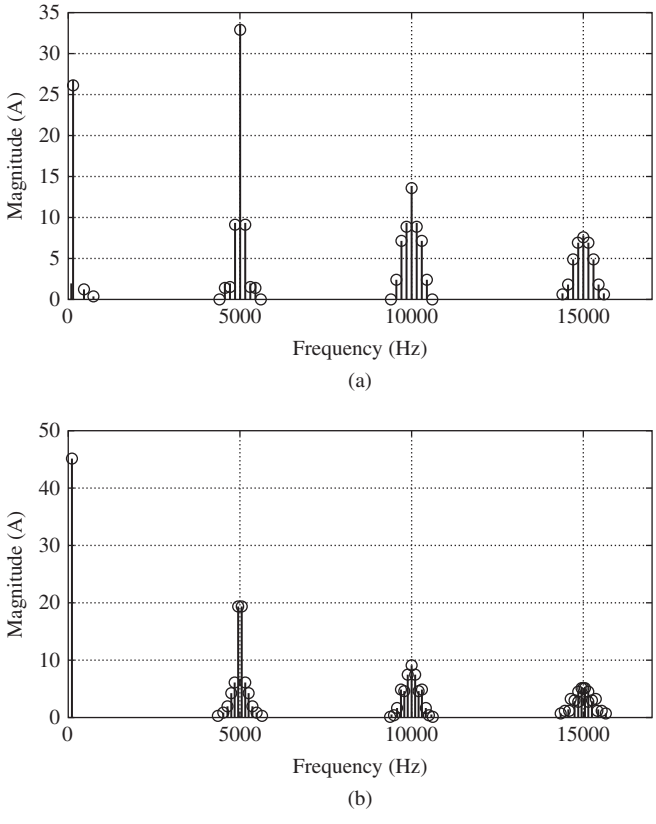

Figure 3.9 Spectrum of DC-link capacitor current for (a) the NPC and (b) the CHB inverter. Lines and circles represent the simulated and analytically derived magnitudes of the current harmonics, respectively

3.7 Discussion

3.7.1 Comparison of Capacitor Size for the NPC and CHB Inverters

The results presented in Section 3.5 were validated by simulations for a wide range of inverter operating parameters (modulation index, load power factor, fundamental, and carrier frequencies). Figure 3.10 illustrates representative results from the validation process, assuming the operating parameters in Table 3.5 and covering the whole range of M.

Figure 3.10 can also provide a comparative overview of the ripple current and capacitance requirements for the NPC and CHB topologies, at a condition ($\phi = 30°$) which is common for inverters operating as motor drives. Namely, it can be seen that the maximum ripple current is similar for both topologies, whereas the required capacitance is 2.5 times higher for the CHB inverter. Thus, each capacitor of the CHB inverter should have 2.5 times the size (equal voltage and ripple current rating, but 2.5 times more capacitance) of a capacitor for the NPC inverter.

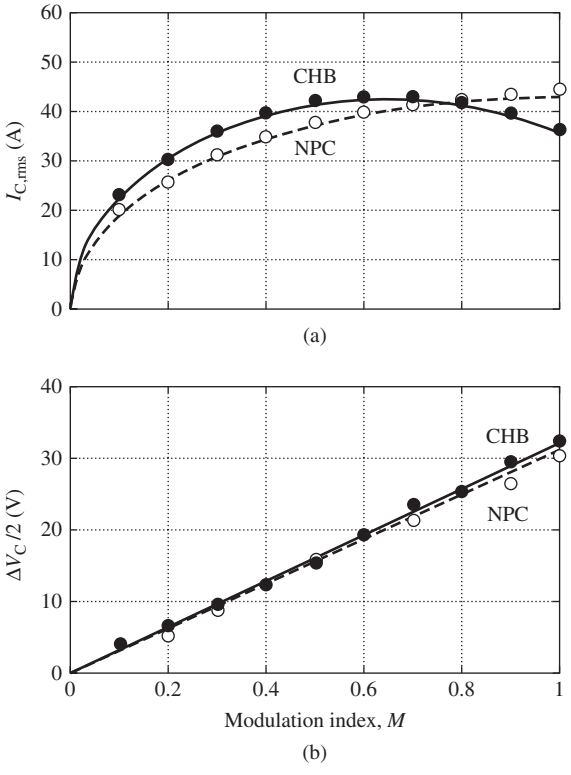

Figure 3.10 Simulation results for (a) the NPC ($C = 1$ mF) inverter and (b) the CHB inverter ($C = 2.5$ mF)

For a different value of ϕ, a similar comparison between the two topologies can be obtained by means of Figures 3.6c and 3.7c,d. As a general observation, however, we could note the following: according to Figure 3.7, for any value of ϕ, the capacitance required to obtain the same voltage ripple is at least twice that of the CHB inverter. For values of ϕ for which the ripple current is comparable for the two topologies ($\phi < 40°$, according to Figure 3.6c), each capacitor of the CHB inverter should therefore have double the size of that of the NPC inverter. Additionally, since the CHB inverter requires three (instead of two) capacitors for its DC-links, the total capacitor size will be at least three times greater for this topology. Even in cases where the ripple current is higher for the CHB inverter (ϕ approaching 90° in Figure 3.6c), a similar ratio of capacitor sizes can be expected. This is because increased capacitance (for the CHB inverter) is commonly achieved through the parallel connection of capacitors, which at the same time share the higher amounts of ripple current.

3.7.2 Comparison of Presented Methods for Analyzing DC-Link Capacitor Current

An examination of ESR characteristics of electrolytic capacitors indicates that their ESR decreases for harmonic frequencies between 50 Hz and 1 kHz, while it

remains approximately constant (to $R_C = R_{C,HF}$) for higher frequencies. Inverter switching (carrier) frequencies are commonly higher than 1 kHz. As a result, the majority of carrier and sideband harmonic groups, which appear around multiples of the switching frequency, belong to the constant-ESR frequency range. Baseband harmonics, however, have to be associated with higher ESR values (Figure 3.1). Loss estimation based on rms current expressions (Section 3.3) fails to treat these harmonics separately, which results in an underestimation of DC-link electrolytic capacitor losses for three-level inverters. It is noted that this is not the case for film capacitors, since their ESR remains approximately constant throughout the current frequency range [22].

Harmonic analysis, on the other hand, can be used according to Equation 3.2 to provide a more accurate estimate for electrolytic capacitor losses. Furthermore, given that the losses arising from the carrier and sideband capacitor current harmonics can be associated with $R_{C,HF}$ in Equation 3.2, the total capacitor losses can be taken from

$$P = \sum_{B} R_C(f_h) \cdot I_{h,rms}^2 + R_{C,HF} \cdot \sum_{C/S} I_{h,rms}^2 \tag{3.39}$$

The subscripts B and C/S under the sums in Equation 3.39 denote that they refer to baseband and carrier/sideband harmonics, respectively.

Equation 3.39 can also be written as

$$P = \sum_{B} R_C(f_h) \cdot I_{h,rms}^2 + R_{C,HF} \cdot \left[I_{C,rms}^2 - \sum_{B} I_{h,rms}^2 \right] \tag{3.40}$$

indicating that knowledge of the capacitor rms current and baseband harmonics is sufficient to obtain an accurate estimate for capacitor losses. The proposed numerical method can make use of Equation 3.40, based on its calculation of the capacitor current rms value and an approximation for the baseband harmonics. Namely, the baseband harmonics can be approximated by the dominant baseband harmonic, assuming that it alone generates the capacitor voltage ripple, ΔV_C (which is also calculated by the proposed strategy). Since this harmonic is located at a frequency of $3f_o$ and $2f_o$ for the NPC and CHB topologies, respectively, its amplitude is approximately given by

$$I_k = k \Delta V_C C \pi f_o \tag{3.41}$$

where k is equal to 3 and 2, accordingly. Thus, in addition to the calculation of ΔV_C, the proposed numerical method offers a more accurate estimate of capacitor losses than the analytical approach of Section 3.2. Moreover, in comparison to the harmonic analysis, it has the advantage of being easily adapted to different modulation strategies, as explained in Section 3.4. On the other hand, the harmonic analysis can provide closer estimates of capacitor power losses for inverters that operate at low switching frequencies. In these cases, certain carrier–sideband harmonic groups may belong to the LF ESR region and, therefore, the results of a complete harmonic analysis should be used according to Equation 3.2.

3.7.3 Extension to Higher-Level Inverters

This chapter focused on the DC-link capacitor current analysis of three-level NPC and CHB inverters. The presented methods can also be applied to higher-level inverters, provided that they are modulated by strategies whose reference and carrier waveforms can be defined analytically. However, such conventional modulation strategies are practically not applicable to NPC ML inverters, since they are unable to prevent voltage collapse of the intermediate DC-link capacitors. Furthermore, unconventional strategies which can retain the capacitor voltages, increase the switching frequency of the switching devices, induce higher output voltage steps (dv/dt), and distort the ML PWM waveform [2, 23].

As a consequence, ML converters with more than three-levels are predominantly based on the series connection of H-bridge cells, creating CHB ML topologies [24]. Extension to these topologies is possible for all presented methods for analyzing the DC-link capacitor current, but the complexity of the analytical derivations increases with the number of voltage levels. The proposed numerical approach, on the other hand, can be extended as shown in the relevant part of the code to cover the CHB ML topologies. As for the three-level inverter, the code simply calculates the duty cycle of each inverter cell and numerically integrates the current (and its square) through its DC-link capacitor. Results for CHB ML inverters have been validated with simulations by the authors.

3.8 Conclusion

This chapter presented a series of analytical and numerical tools for analyzing the DC-link capacitor current in three-level NPC and CHB inverters. The results can be practically useful for inverter designers performing the task of DC-link capacitor sizing. Analytical expressions were derived for the rms value and harmonics of the DC-link capacitor current, whose knowledge is essential for determining the required capacitance and ripple current rating of DC-link capacitors. Moreover, the proposed numerical method provided the possibility to estimate capacitor sizing parameters for different modulation strategies, offering a simpler alternative to repeating the analytical derivations. Results based on the proposed approach were illustrated for common modulation strategies and were validated using simulations in MATLAB®-Simulink. According to them, the CHB inverter has significantly (at least three times) higher capacitor size requirements as compared to the NPC inverter.

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