

Calculation of the DC-bus Capacitors of the Back-to-back NPC Converters

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Abstract—Nowadays the most used multilevel topology for variable-speed wind turbines (WTs) is the a back-to back three-level NPC (Neutral Point Clamped) VSCs (voltage source converter). One of the most critical elements in the design of this type of converters is the DC-bus capacitors. The calculus of these depends on the same factors that the same two-levels topology, and, moreover it is function of a low frequency ripple due to the current by NP point. In this work, the value of these capacitors is obtained from the analytical equations of the DC-bus voltage ripple due to the i_{DC} (DC-bus current) and the i_{NP} (NP current). These expressions are verified through simulation and practical results.

I. INTRODUCTION

Nowadays the most used topologies for variable-speed wind turbines (WTs) are: doubly-fed induction generator – wounded rotor; induction generator – squirrel cage rotor; and synchronous generator – permanent magnets. In the three cases, the most chosen converter structure as interface between the generator and the utility grid is a back-to-back VSC.

Besides, the evolution of this application is based on the gradually increase of the power of the wind-turbine installed in the park. The need of high currents, with low voltage ranges in high level power (3MW) energy generation, force to modify the design of the electrical current generators and the converters. The use of a multilevel converter allows the direct connection of the wind turbine to a grid of medium voltage without transformer, which is an advance not only due to the transformer removal but also because of the power limitations, that will be easily reached if generator of low level voltage ranges are maintained and energy demands are increasing like they are doing since many years.

Nowadays, the most used multilevel topology is the

NPC (Neutral Point Clamped), and Fig. 1 shows the structure of a back-to-back three-level NPC VSCs (voltage source converter). A critical part in these converters is the design of the DC-bus capacitors. The reduction of the DC-bus energy storage, which will then lead to the replacement of the electrolytic capacitors with film capacitors, which have lower energy density meaning that the volume is smaller, but will increase the converter lifetime. In these circumstances, operation under unbalanced and distorted supply voltage as well as high dynamic operation of the control makes the control task more challenging [1].

The calculation of the DC-bus capacitor for a back-to-back three-level NPC VSC depends on the same factors that the same two-levels topology [1], and, moreover it is function of a low frequency ripple due to the NP current, i_{NP} (Fig. 1). This current produces a voltage unbalance in the DC-bus capacitors, which if it is not delimited, it could produce the next effects:

- possible over-voltages in the power electronics devices, as well as in the DC-bus capacitors;
- worsening of the quality of the currents that circulate for the load, for example unbalance of these; and
- in the extreme case, an inappropriate operation of the converter.

There are technical works that studies the voltage unbalance in the DC-bus capacitors due to i_{NP} , such as [2], [3], [4] and [5]. The main contributions with respect to the previous works are the following: (1) these analyses are achieved on a back-to-back converter, (2) the ripples in u_{DC} due to i_{DC} and i_{NP} are related, and (3) the analytical equations for each ripple in u_{DC} of a back to back converter are obtained.

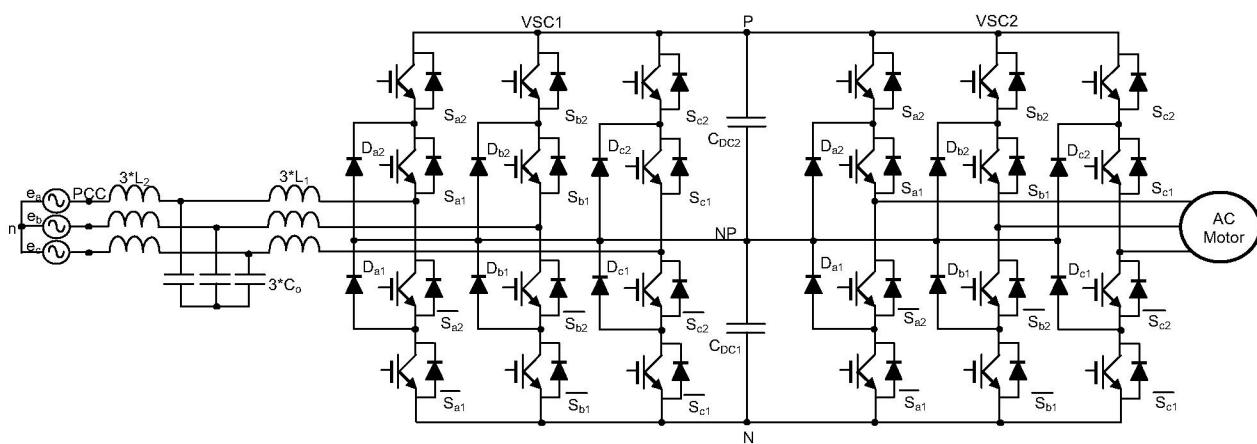


Fig. 1. Back-to-back three level NPC VSC.

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II. RELATION BETWEEN THE CALCULUS OF THE DC-BUS CAPACITORS IN CONVERTERS OF TWO-LEVELS AND THREE-LEVELS

The C_{DC} calculation for two-levels VSCs connected to the utility grid depends on the application kind. This way, if the VSC is working as:

- *PWM rectifier.* C_{DC} should take the value:

$$C_{DC} \geq \frac{i_{DC} T_{SW}}{2\Delta u_{DC}} = \frac{T_{SW} S_n}{2u_{DC} \Delta u_{DC}} \quad (1)$$

where Δu_{DC} is the maximum allowed ripple. If $S_n = 100kVA$, $T_{SW} = 400\mu s$, u_{DC} take the minimum value (610V), and Δu_{DC} is set to 10% of u_{DC} , then, $C_{DC} \geq 537.5\mu F$. This result is very conservative because it implies that the DC-bus capacitor is discharging to nominal power during half of the commutation period. In the practice, the discharge time, depends on the load, but, in general, it is considerably smaller.

- *Active filter.* The worst situation takes place when it is necessary to balance a load of negative sequence to nominal power. In these circumstances, the ripple is twice the utility grid frequency, and C_{DC} should take the value [1]:

$$C_{DC} \geq \frac{i_{DC} T_{SW}}{2\Delta u_{DC}} = \frac{S_n}{2\omega_{base} u_{DC} \Delta u_{DC}} \quad (2)$$

For the same values that in the previous example, $C_{DC} \geq 4277.2\mu F$.

These results are valid for VSCs connected to the grid with passive and active loads (back-to-back two-levels VSCs).

The C_{DC} calculation for a NPC VSC depends on the same factors that a two-level VSC, and, moreover it is function of a low frequency ripple due to the NP current, i_{NP} (Fig. 1). The frequency of this current is three times the modulation signal frequency, and it produces a unbalanced voltage between the two capacitor banks that conforms C_{DC} [2].

The equivalent dynamic circuit of the NP connection is shown in Fig. 2 [4]. In this model, the DC-bus voltage is assumed to be constant when the ripple due to i_{NP} is analyzed, which can be achieved by either a DC-power supply or by controlling this voltage through a proper control loop. The main assumptions for this analysis are that:

- each converter is independently controlled;
- $C_P = C_N = \frac{C_{DC}}{2}$; and
- only the fundamental harmonics for the input and output currents are considered.

From the point of view of the unbalance in NP, the capacitors are connected in parallel, and the equivalent value is $C_{NPequiv} = C_P + C_N = 2C_{DC}$. On the other hand, the capacitors are connected in series from the point of view of the DC-bus current, and therefore

$$C_{DCequiv} = \frac{C_P C_N}{C_P + C_N} = \frac{C_P}{2}, \text{ if } C_P = C_N. \text{ Differences in}$$

the values of the capacitors can cause effects very negative in the NP voltage balance.

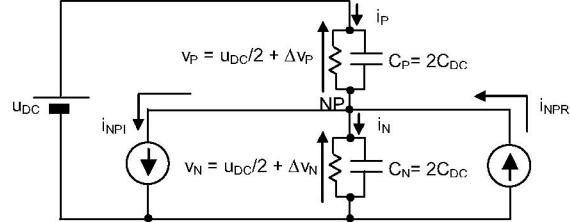


Fig. 2. Simplified diagram of a back-to-back converter based on two NPC's.

III. I_{NP} CALCULATION

A. For SVPWM (Space Vector Modulation).

In [5], a very detailed study is made to calculate i_{NP} in a three-level NPC VSC when the modulation technique is SVPWM. The conclusion is that i_{NP} is bigger as much as major is m_a (amplitude modulation index) and minor DPF (power factor displacement) in the load.

In the worst case, when $m_a=1$ and $DPF=0$, the instantaneous expression of i_{NP} for the third harmonic is:

$$i_{NP}(t)|_{3\omega_{base}} = \frac{8}{\pi^2} \hat{i}_{phase} \cos 3\omega_{base} t \quad (3)$$

where \hat{i}_{phase} is the peak value of the converter phase currents. This is this way, like it is shown in Fig 3, the i_{NP} waveforms are triangular for anyone of the four values of the current modulation indexes (m_{S0} and m_{S1}) indicated in Table I.

TABLE I.
SIMULATION DATA OF FIG. 3

	m_{S0}	m_{S1}	
i_{NP1}	1	1	m_a 1.0
i_{NP2}	1	-1	DPF of the load 0.0
i_{NP3}	Changing alternatively		Amplitude of the phase currents 100
i_{NP4}	0	0	

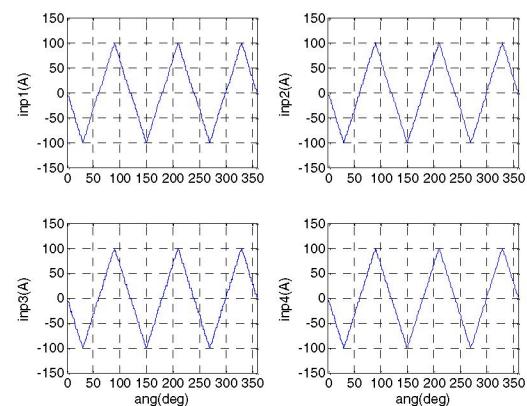


Fig. 3. Corriente i_{NP} para $PF=0$.

B. For SPWM (Sinusoidal Modulation)

To achieve a similar study with the modulation technique SPWM a model based on the comparison of the modulation signal of a phase with the two carrier signals is developed [6]. The waveform and the harmonics of i_{NP} are shown in Fig 4 for the same simulation data of Table I. In the worst case ($DPF = 0.0$), the peak value of the third order component is $\approx 0.74 \cdot \hat{i}_{phase}$.

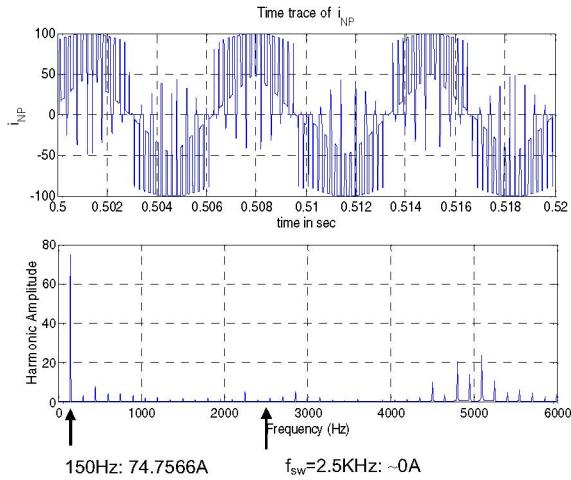


Fig. 4. i_{NP} representation with SPWM, and the Table I simulation data.

The i_{NP} study in function of the modulation technique THSPWM is exactly the same as the study for SPWM, it is only necessary to add the zero sequence to the modulation signals [6]. Under the same conditions, it can be checked that the harmonic amplitude located to three times the fundamental frequency for THSPWM is relatively smaller.

IV. CALCULATION OF THE DC-BUS CAPACITORS.

The ripple of the DC-bus capacitors of the three-level NPC VSCs has the next harmonic components:

1. Zero frequency, due to possible unbalances in the voltage of the two banks of capacitors.
2. Commutation frequency, called high frequency ripple.
3. Double of the fundamental frequency due to the unbalanced grid voltages, or other frequencies due to harmonic in the utility grid.
4. Three times the frequency of the modulation signals due to i_{NP} , called low frequency ripple. This current generates the voltage unbalance between the two banks of DC-bus capacitors.

The unbalanced continuous component (1) depends on the used modulation technique. But if any offset is not applied to the modulation signals, this unbalance is solved introducing equalization resistances like it is shown in Fig. 2 circuit. About the components (2) and (3), the eq. (1) and eq. (2), developed for a two levels VSC, are valid for a three-level NPC VSC. It is only to analyze in this section the calculation of the DC-bus capacitors in function of i_{NP} . The objective is to obtain an expression of the C_{DC} value to delimit the unbalance between the voltages of the two banks of DC-bus capacitors due to i_{NP} .

In the case of the components (2), (3) and (4), a C_{DC} expression is possible to obtain. Afterwards the most

restrictive value is chosen, and, this way, the ripple is delimited inside the established margin for each harmonic.

A. For a NPC VSC.

Fig. 5 shows the ripple waveforms in the two banks of capacitors due to i_{NP} if the Fig. 1 circuit is simplified eliminating one current generator (each current generator models the i_{NP} current of a VSC). This simplified model is valid for the two operation forms of the VSCs, as inverter (regenerative circuit) and as active rectifier, because in the simulations the next conclusions can be observed:

- In a NPC working as rectifier, u_{DC} has a ripple due to the commutation of the VSC (i_{DC} ripple), but the voltages in C_P or C_N due to this ripple are exactly same and they are compensated. Therefore, there is not unbalance between the two banks of capacitors due to the ripple produced by the commutations in i_{DC} .
- u_{DC} of the NPC working as rectifier has not ripple due to i_{NP} , it is absorbed by C_P and C_N .

From the previous summations, the circuits of Fig. 2 can be modelled with the following expressions:

$$u_{DC} = v_P + v_N = \frac{u_{DC}}{2} + \Delta v_P + \frac{u_{DC}}{2} + \Delta v_N \quad (4)$$

$$\nu_{NP} = \Delta v_P - \Delta v_N \quad (5)$$

$$i_N = i_P + i_{NP} \quad (6)$$

where v_{NP} is the unbalance between the two banks of capacitors, and i_{NP} is the difference between the currents of the two banks of the capacitors.

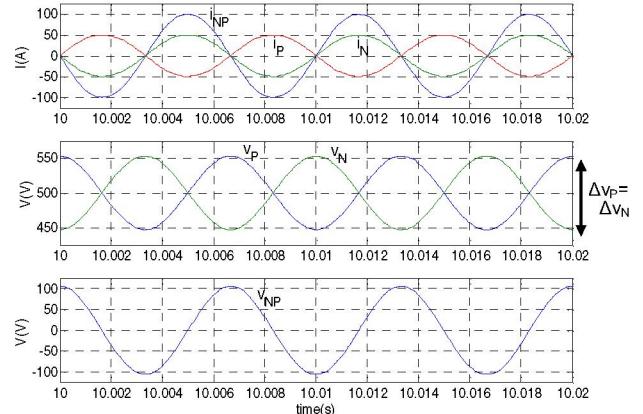


Fig. 5. Variation of the voltages in the two banks of capacitors of a NPC in function of i_{NP} .

If the i_P waveform is considered triangular, the charge increasing in C_P or C_N can be defined as:

$$\Delta Q = \frac{1}{24} \hat{i}_{NP} T_{base} \quad (7)$$

on the other hand, if it is considered sinusoidal:

$$\Delta Q = \frac{1}{6\pi} \hat{i}_{NP} T_{base} = \frac{\hat{i}_{NP}}{3\omega_{base}} \quad (8)$$

where \hat{i}_{NP} is the i_{NP} amplitude and T_{base} is the grid signal period. The calculus of the charge increasing is

more restrictive supposing i_{NP} sinusoidal, therefore, this assumption will be taken from this moment.

Δv_P due to i_{NP} , which is equal to Δv_N , $\frac{\Delta v_{NP}}{2}$ and \hat{v}_{NP} (peak value without the possible continuous component), for one VSC, for example the VSC connected to the grid, is defined as:

$$\begin{aligned} \Delta v_P|_{i_{NP}} &= \Delta v_N|_{i_{NP}} = \frac{\Delta v_{NP}}{2}|_{i_{NP}} = \hat{v}_{NP}|_{i_{NP}} = \\ &= \frac{1}{6\pi} \frac{\hat{i}_{NP} T_{base}}{C_P} = \frac{1}{12\pi} \frac{\hat{i}_{NP} T_{base}}{C_{DC}} \end{aligned} \quad (9)$$

supposing $C_P = C_N = 2C_{DC}$. In the worst case $\hat{i}_{NP}|_{3\omega_{base}} = \frac{8}{\pi^2} \hat{i}_{phase}$, therefore, C_P and C_N can be calculated as:

$$C_P = C_N \geq \frac{4}{3\pi^3} \frac{\hat{i}_{phase} T_{base}}{\Delta v_P} \quad (10)$$

The maximum possible value of \hat{i}_{phase} is $\hat{i}_{phase} = \hat{i}_n$, where \hat{i}_n is the peak value of the converter phase nominal current.

In a NPC converter, for example VSC 1 in Fig. 1, the ripple in v_P and v_N due to i_{DC} (when the converter connected to the grid is working as rectifier) can be calculated as:

$$\Delta v_P|_{i_{DC}} = \Delta v_N|_{i_{DC}} = \frac{\Delta u_{DC}|_{i_{DC}}}{2} = \frac{1}{2} \frac{i_{DC}}{C_{DC}} \frac{T_{SW}}{4} = \frac{S_n T_{SW}}{4u_{DC} C_{DC}} \quad (11)$$

where $\Delta u_{DC}|_{i_{DC}}$ is the u_{DC} ripple due to i_{DC} . If $S_n = 100\text{KW}$, $T_{SW} = 400\mu\text{s}$, u_{DC} changes between 610V and 1000V, and Δu_{DC} is fixed in a 10% of u_{DC} , then, $C_{DC} \geq 537.5\mu\text{F}$. This value coincides with the value obtained to two-levels VSCs applying the ec. (1). It is very conservative because it implies that the capacitor is discharging to nominal power during switching period half. In the practice, the capacitor discharge time depends on the load, but it is generally less.

The ripple due to i_{DC} is added to ripple due to i_{NP} , and the most cases, the first ripple is negligible front to the second ripple because the frequency is much bigger in the first. To calculate the DC-bus capacitors, the ripple due to i_{DC} can be negligible and, therefore the capacitors are calculated in function of i_{NP} , if next condition is verified:

$$\frac{1}{6\pi} \frac{\frac{8}{\pi^2} \hat{i}_n T_{base}}{2C_{DC}} \gg \frac{S_n T_{SW}}{4u_{DC} C_{DC}} \quad (12)$$

(eq. of the DC-bus middle) that simplifying can be written as:

$$u_{DC} \gg \frac{3\sqrt{3}\pi^3}{8\sqrt{2}} \frac{U_{base}}{m_f} \quad (13)$$

where m_f is the frequency modulation index. From the last equation, Fig. 6 represents $u_{DC} = f(m_f)$ for $U_{base} = 400V$. The line is the border area where the ripple in the C_P and C_N due to i_{DC} and i_{NP} is exactly equal.

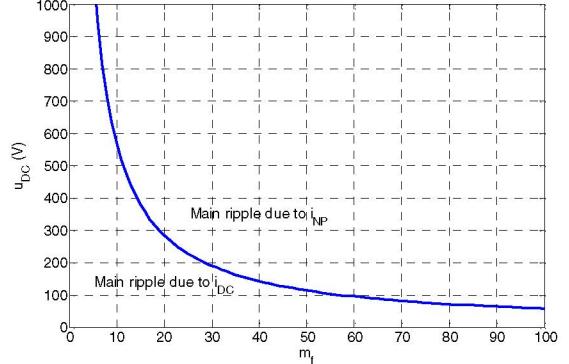


Fig. 6. Ripple places in function of u_{DC} and the DC-bus middle.

B. For a back-to-back NPC VSC.

Fig. 2 represents the equivalent dynamic circuit of the NP connection for a back-to-back three-level NPC VSC. The i_{NP} current circulates by C_P and C_N , and that produces the voltage unbalance, take the value:

$$i_{NP}(t) = i_{NPR}(t) - i_{NPI}(t) \quad (14)$$

where i_{NPR} is the i_{NP} current due to the converter that works as rectifier, whereas i_{NPI} is the i_{NP} current due to the converter that works as inverter.

If i_{NPR} and i_{NPI} have different frequencies, v_{NP} has two different frequency components, and the temporal wave is the sum of these two components. To calculate the capacitors, the eq. (10) is used for each frequency. So, the obtained capacitor values limit the \hat{v}_{NP} value for each harmonic component.

If for example, $i_{NPR} = 100 \sin(3(2\pi 50t))$ and $i_{NPI} = 100 \sin(3(2\pi 25t))$, then $\hat{v}_{NP75Hz} = 212V$ and $\hat{v}_{NP150Hz} = 106.1V$ if $C_{DC} = 2000\mu\text{F}$ (Fig. 7). It verifies the eq. (9) for each current harmonic.

A particular case happens when the i_{NPR} and the i_{NPI} have the same frequency. If $i_{NPR} = \hat{i}_{NPI}$, then $i_{NP} = 0$, and therefore $\Delta v_P|_{i_{NP}} = \Delta v_N|_{i_{NP}} = 0$. The worse situation is produces when $i_{NPR} = i_{NPI} \angle \pi$, then:

$$i_{NP} = 2i_{NPI} \quad (15)$$

so:

$$\Delta v_P|_{i_{NP}} = \Delta v_N|_{i_{NP}} = \frac{\Delta v_{NP}}{2}|_{i_{NP}} = \frac{2}{6\pi} \frac{\hat{i}_{NP} T_1}{C_P} = \frac{1}{6\pi} \frac{\hat{i}_{NP} T_{base}}{C_{DC}} \quad (16)$$

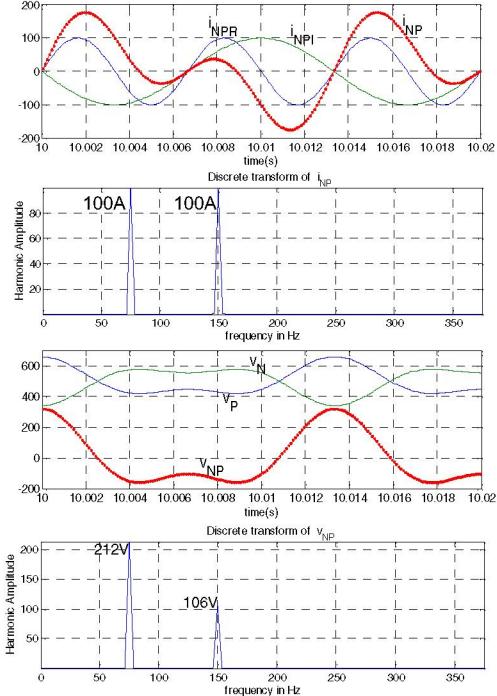


Fig. 7. Waveforms and harmonics of i_{NP} y v_{NP} in a back-to-back converter.

where $C_P = C_N = 2C_{DC}$. So, in the worst case, the obtained values of C_P and C_N are the double respect to the values calculated from the eq. (10), that is to say:

$$C_P = C_N \geq \frac{8}{3\pi^3} \frac{\hat{i}_{phase} T_{base}}{\Delta v_P} \quad (17)$$

With the preceding eq., $C_P = C_N \geq 14.3mF$. This value is enormous, and it is much bigger than the value obtained from eq. (10). It has been calculated in the worse case, that is to say with $DPF=0$, nominal power and $\Delta v_P \leq 30V$.

For cost reasons, in the practice C_{DC} should be considerably smaller. If the converter works under extreme conditions and v_{NP} takes high value for the chosen C_{DC} , then a v_{NP} control is essential to reduce this voltage.

V. SIMULATION RESULTS.

The objective of this section is to compare the results obtained in the previous sections from approximate models with results coming from the simulations of large signal models of the back-to-back three-level NPC VSCs. This way, the summations obtained in the previous sections are tested, and they can be applied in the analysis of real circuits.

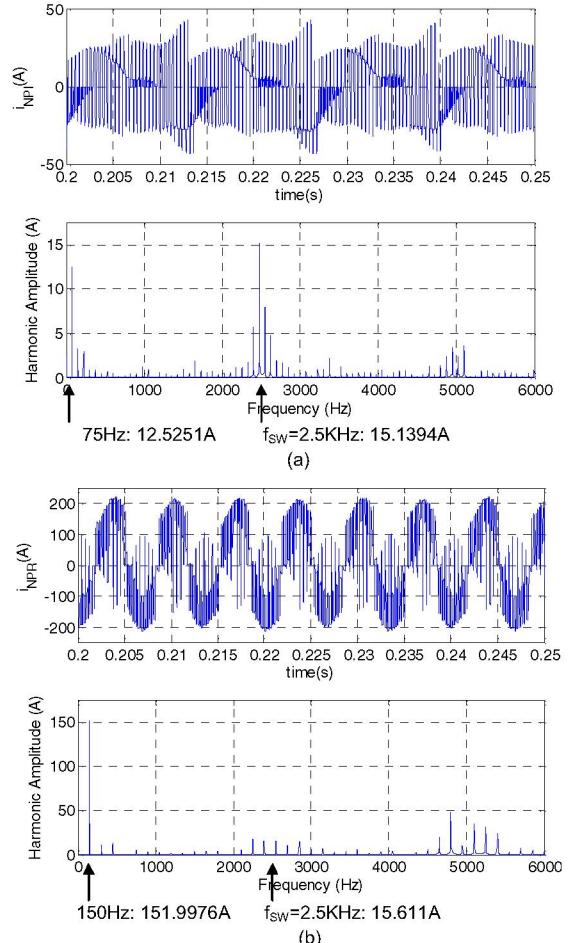
In the simulations, VSC1 (Fig. 1) is working as active rectifier and it is connected to a 50Hz utility grid, whereas VSC2 is working as inverter and it is connected to a 25Hz utility grid. Both VSCs are controlled through the phase displacement method [7]. The relative phase of the inverter modulator is +2.5 and for the rectifier is -2.5. The i_{NPI} first harmonic is placed in 75Hz (3·25 Hz), whereas the i_{NPR} first harmonic is placed in 150Hz (3·50 Hz). The modulation technique used for the two

converters is THSPWM, and $m_a \text{ THSPWM inversor} = m_a \text{ THSPWM rectificador} = \sqrt{3}/2$. The data used in the simulations are shown in the Table II.

TABLE II. SIMULATION DATA OF FIG. 8.

f_{SW}	2.5Khz
$C_P=C_N$	$1000\mu F$
Inverter	
R_I	0.075Ω
L_I	$0.75mH$
f_{base}	25Hz
U_{base}	400V
Rectifier	
R_I	0.075Ω
L_I	$0.75mH$
f_{base}	50Hz
U_{base}	400V

Fig. 8 shows the behaviour of the back-to-back converter. Fig. 8.d only represents the v_{NP} harmonics until 500Hz, because above this frequency the values are negligible. Whit these simulations are verified the equations obtained in the previous section. Besides it is tested that when the DC-bus capacitors are submitted to ripples of different frequencies, the voltage will have the components of those frequencies, and the temporary waveforms will be the sum of these components of frequency. To calculate the capacitors, overlapping techniques for each frequency can be used, limiting the ripple of each harmonic inside the security margins.



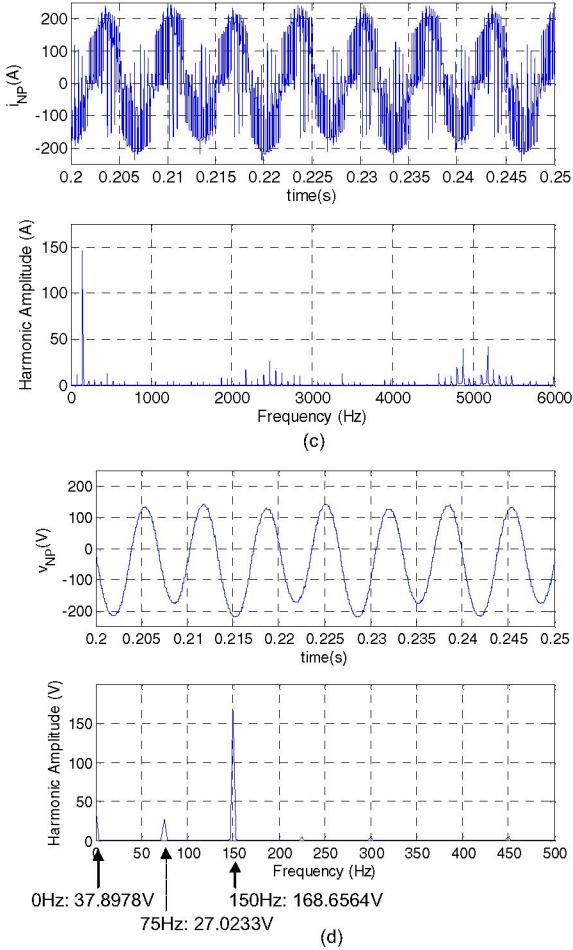


Fig. 8. Waveforms of the back-to-back three-level NPC VSC: a) i_{NP} , b) i_{NP} , c) i_{NP} , y d) v_{NP} .

VI. PRACTICAL RESULTS.

Fig. 9 represents some waveforms of the converter exposed in Fig. 1 when VSC1 is working as non-controlled rectifier and VSC2 is driving an induction motor of 11kW ($C_P = C_N = 1400\mu F / 750V$). The signals shown in Fig. 9.a are the phase current in the motor and one VSC2 line voltage; whereas the signals in Fig. 9.b show the two DC-bus voltages and the harmonics of u_{DCP} . In the last one, the two typical harmonics due to the three-level NPC VSC topology can be appreciated: one placed in 150Hz due to i_{NP} and another placed in 300Hz due to i_{DC} . From the signals shown in Fig. 9.b it can be asserted that the circuit presented in Fig 2 (where is modeled the NP connection) and the equations obtained in the previous section are correct to model the NP connection in a back-to-back three-level NPC VSC.

VII. CONCLUSIONS.

In this work, the analytical expressions to calculate the DC-bus capacitors of a back-to-back three-level NPC VSC due to the i_{DC} ripple and the i_{NP} ripple are obtained. These expressions and the obtained conclusions have been verified through simulation and practical results. If a controller of the NP voltage unbalance is added, it can decrease the DC-bus capacitors capacities considerably due to the i_{NP} ripple and, therefore, to reduce the cost of

the system. Anyway, the highest value in C_{DC} is obtained when this has to limit grid voltage unbalances, but in this case, the capacitor value can also decrease using controllers to compensate these unbalances.

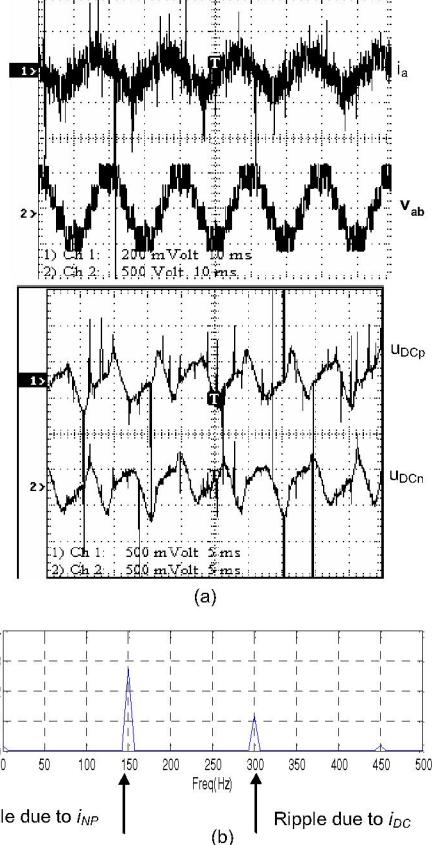


Fig. 9. a) Phase current and line voltage of the VSC2. b) DC-bus voltages and the harmonics of u_{DCP} .

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