Forward Converter Design Report

Design Solutions and Project Development

Report

Department of Electrical and Electronic Engineering
Faculty of Engineering

1. Introduction

This report focuses on the simulation and prototyping of an open-loop switch-mode power supply (SMPS) for the completion of a dual-switch forward converter whose main function is to convert an AC input voltage of 30V to a DC output voltage of 8V. Here PLECS was used and simulated for the ideal case and non-ideal case of a dual switched forward converter for DC and AC inputs respectively. A gate driver circuit that can control the MOSFETs in the converter was also simulated and its principle was discussed. The important parameter values for the simulated circuit were calculated in the second section and the parameter values for many components were also obtained from the respective datasheets. Simulation results for each circuit in various cases were presented in this report. The reasons for the presentation of the results and ways to improve them were also discussed to facilitate the construction of the circuit in a realistic situation.

2. Calculations for the Forward converter

2.1 Duty cycle and ideal transformer turns ratio

The duty cycle was first chosen to be 0.3. As the maximum duty cycle of the XFMR in continuous mode is 50% and the actual PWM output has a maximum duty cycle limit of 45%, the duty cycle here was chosen to be 0.3 as a reasonable value. In an ideal simulation, the forward converter is intended to have a DC input of 35 V, and an output designed for 8 V. Based on the relationship in Equation 1, the turns ratio of the transformer can be calculated:

$$\frac{V_o}{V_i} = d\frac{N_2}{N_1} \qquad \textbf{Eqn.1}$$

$$\frac{N_2}{N_1} = \frac{V_o}{V_i d} = \frac{8\,V}{35\,V\,\times 0.3} = \frac{16}{21} \approx \frac{4}{5}$$

2.2 Switching frequency

The switching frequency has been chosen to be 100kHz for the following reasons:

(1) A switching frequency of 100kHz can help to achieve high efficiency as it is high enough to reduce the size of the magnetic components (inductors and transformers) and capacitors in the converter, thus reducing costs. 100Hz is again low enough to maintain reasonable switching losses. Higher frequencies cause additional energy loss in the MOSFETs and reduce efficiency.

(2) The frequency is low enough to help reduce electromagnetic interference (EMI) emissions and electromagnetic compatibility (EMC) issues. Higher switching frequencies produce higher EMI emissions, as higher frequency harmonics may be radiated from the converter. On the other hand, lower switching frequencies generate more noise at the output, leading to more EMC problems.

(3) This frequency size can help to reduce output ripple. This is because the switching frequency determines the rate of change of the current and voltage in the converter and a lower frequency can result in a slower rate of change and therefore more output ripple.

2.3 Inductor of the output filter

Since the load resistance at the discontinuous output is 15% of P_{max}, the minimum output current I_o can be calculated as:

$$I_o = \frac{15\%P_{max}}{V_o} = \frac{15\%\times 50}{8} = 0.935\text{A} \qquad \textbf{Eqn.2}$$

The ripple of the inductor current ΔI_L is:

$$\Delta I_L = 2I_o = 2 \times 0.935 = 1.875A \qquad \textbf{Eqn.3}$$

Based on the known switching frequency (100 KHz), duty cycle (0.3) and current ripple (1.875 A), the value of the inductor can be calculated as:

$$L = \frac{VTA}{\Delta I_L} = \frac{V_o(1-d)T}{\Delta I_L} = \frac{8\,V\times 0.7\times \frac{1}{100\times 10^3 Hz}}{1.875\,A} = 29.87\,\mu H \qquad \textbf{Eqn.4}$$

2.4 Capacitor of the output filter

The maximum of the voltage ripple is 0.1V, so the minimum value of the capacitor is:

$$C = \frac{ITA}{\Delta V} = \frac{\frac{\Delta I_L}{2}\times\frac{T}{2}\times\frac{1}{2}}{\Delta V} = \frac{0.9375\,A\times\frac{1}{100\times 10^3 Hz}\times\frac{1}{2}\times\frac{1}{2}}{0.1} = 23.44\,\mu F \qquad \textbf{Eqn.5}$$

2.5 Maximum and minimum load

According to the datasheet, the maximum output power is 50 W, and the minimum load is 15%, so the maximum and minimum load resistance values can be calculated as follows:

$$R_{min} = \frac{{V_o}^2}{P_{max}} = \frac{64}{50} = 1.28\,\Omega \qquad \textbf{Eqn.6}$$

$$R_{max} = \frac{{V_o}^2}{15\%P_{max}} = \frac{64}{15\%\times 50} = 8.53\,\Omega \qquad \textbf{Eqn.7}$$

The main converter was built primarily based on the parameter values selected and calculated above, and its output results for maximum and minimum loads are discussed to investigate whether they meet the design expectation sated above.

3. Simulation results under ideal conditions

The main converter circuit has an input of 35V DC, two MOSFETs, and two diodes connected to this voltage source to alternate the DC current to AC for the input of the transformer. The switching frequency of the MOSFETs driven by the gate driver circuit can determine the AC voltage frequency on the primary side of transformer. At the secondary side of transformer, two diodes and one inductor were placed to rectify AC to DC and one decoupling capacitor was connected to narrow the output voltage ripple.

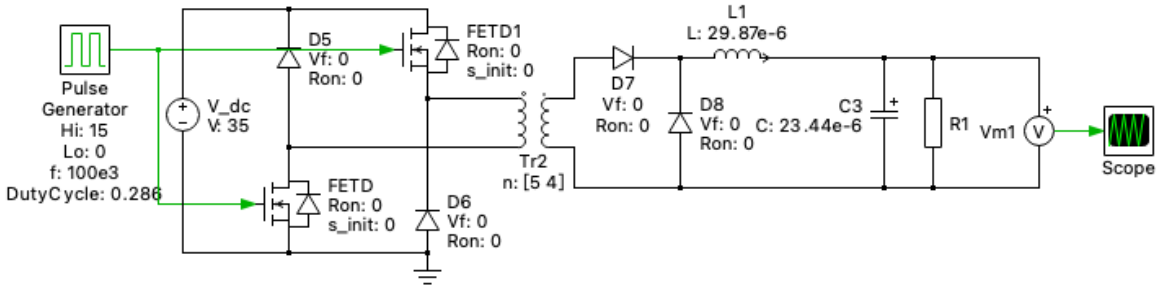

Figure 3.1: Main converter circuit for ideal simulation

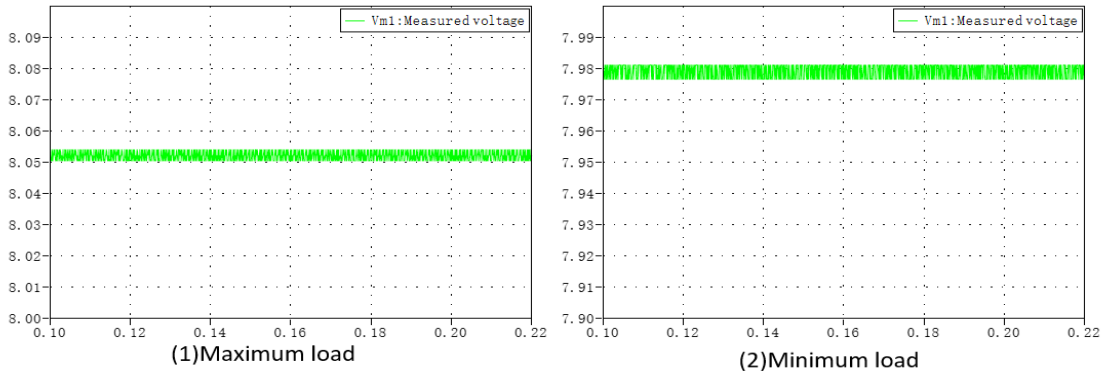

Figure 3.2: Main converter simulation results under ideal conditions

The number of turns must be an integer which had been chosen to be 5:4, the PWM duty cycle can be adjusted based on this integer ratio and Eqn1:

$$d = \frac{N_1}{N_2} \times \frac{V_o}{V_i} = \frac{5}{4} \times \frac{8}{35} = 0.286$$

Figure 3.1 shows the main converter circuit schematic under ideal conditions. Use a Pulse Generator in PLECS with a 0.286 duty cycle and 15 high state output voltage to power MOSFETs. The value of all other components was set based on previous calculations. Run the simulation under the maximum and minimum load, results are shown in Figure 3.2, their ripple is both less than 0.1V and the output voltage level is around 8V which fulfills the design requirement. As the simulation shows, a bigger load gives a slightly higher output voltage but a smaller ripple than a smaller load. This is because when the load resistance decreases, the current flow in the circuit increases under the constant output power, which results in a voltage drop on the output side.

4. Simulation results with non-ideal components

4.1 DC Input

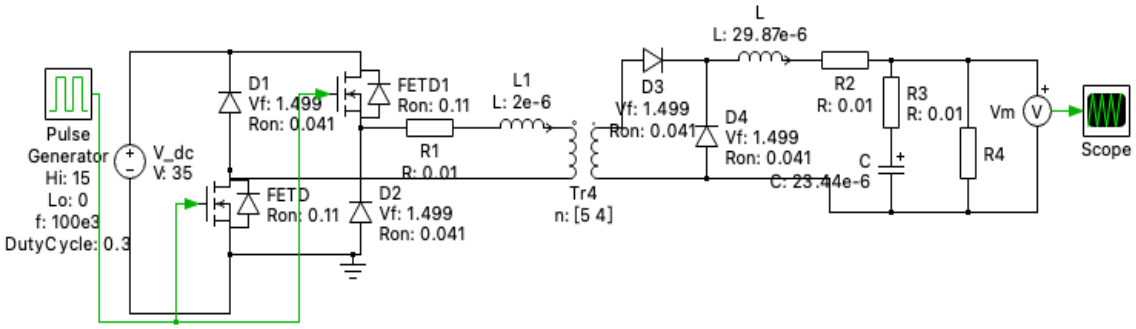

Figure 4.1: Main converter circuit for non-ideal simulation (DC Input)

Figure 4.1 illustrates the main converter circuit with 35 V DC at the input under non-ideal conditions. For the non-ideal components, the relative parameters were reset based on

their datasheets. Forward voltage and on-resistance of secondary side diodes were modified in PLECS and the on-resistance of MOSFETs as well. ESR of the capacitor, inductor resistance, and transformer winding resistance was represented by a series resistor.

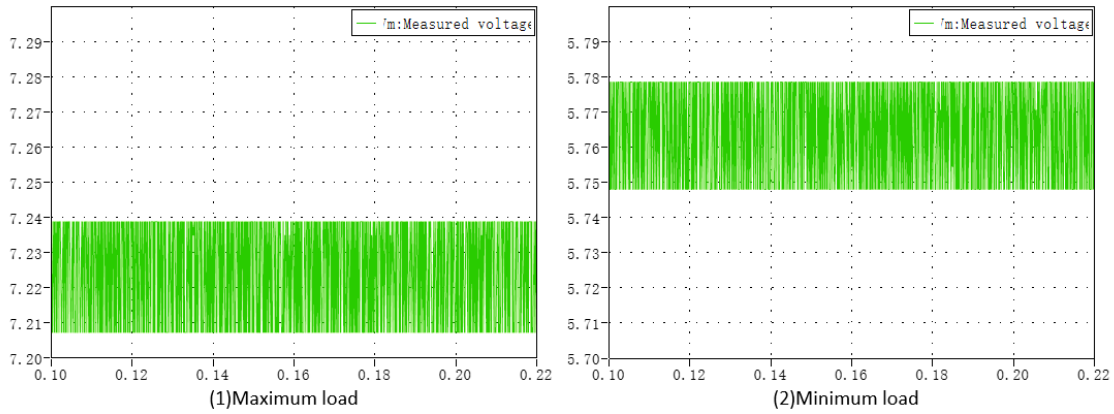

Figure 4.2: Main converter simulation results under non-ideal conditions (DC Input)

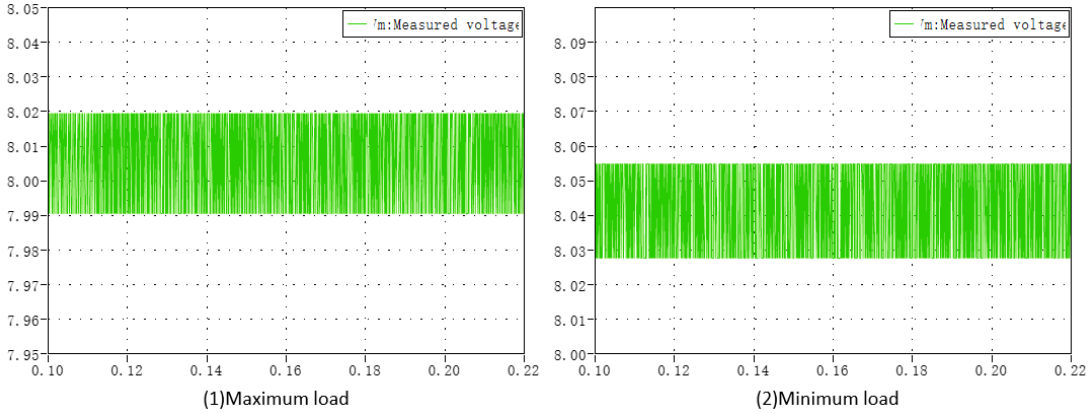

Figure 4.3: Adjusted main converter simulation results under non-ideal conditions (DC Input)

Figure 4.2 shows the simulation results for this circuit at maximum and minimum load, and it can be seen from the figure that the expected result of an output voltage of 8V is not met in either case. The voltage ripple for each result is less than 0.1 V as expected but is still greater than in the ideal state. There are several reasons for this phenomenon and ways of improving it has presented below:

(1) Power Loss: The output voltage drop mainly comes from power losses from non-ideal sources caused by inductors and resistors. Firstly, the diode has a voltage drop of approximately 1.499 which causes the voltage to vary to some extent. Second, a true transformer produces core losses brought on by flux changes in the core and coil losses brought on by the resistance of the copper wire. Thirdly, every real component has a resistance, which causes a loss of energy. All these points reduce the output voltage to some extent. Nevertheless, if the load resistance is low, the current flow through the circuit can be high which indicates more power losses on the equivalent resistors and a lower output voltage. To solve the problems caused by energy losses, the duty cycle of the circuit should be increased, which largely improves the magnitude of the voltage to match expectations.

(2) Ripple: The ripple of the DC powered circuit output voltage is bigger than the ideal condition, the reason is that the value of decoupling capacitor C was designed under ideal conditions when taking the ESR and ESL into consideration, the capacitance is

too small to decouple this ripple. The main way to improve this phenomenon is to increase the capacitance of this capacitor. Or increase the MOSFETs switching frequency and recalculate the inductor, capacitor value for this new design.

To erase the mismatch between ideal and non-ideal output voltage researchers need to adjust the parameters on real components that make it differ from ideal one. The capacitance of decoupling capacitors and the duty cycle of the PWM signal are chosen to set up circuit to match requirements because they have a significant influence on output results and are operatable. When the input voltage source is DC, ripple on output side still matches the requirement which means the value of decoupling capacitor needs no adjustment. But output voltage amplitude has significantly dropped especially under minimum load condition, so operation on duty cycle is indeed to gain proper output. The duty cycle was set at 0.325 for maximum load and 0.365 for minimum load, simulation results have shown in Figure 4.3.

4.2 AC Input

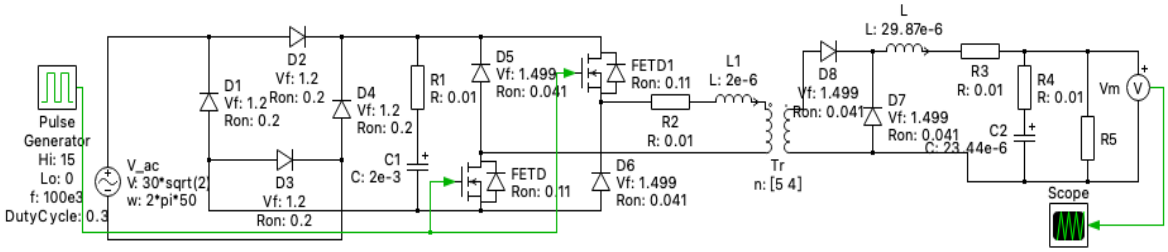

Figure 4.4: Main converter circuit for non-ideal simulation (AC Input)

Figure 4.4 illustrates the main converter circuit being powered by a $30\sqrt{2}$ V AC source at a frequency of 50Hz under non-ideal conditions. In addition to changing the parameters of some of the non-ideal components as in Figure 4.1, a rectifier diode, and a filter capacitor for it was added. The rectifier diode forward voltage and on-resistance were set to 1.2 V and 0.2 Ω according to the datasheet, and the series resistance (ESR) of the filtering capacitor was also added to the circuit.

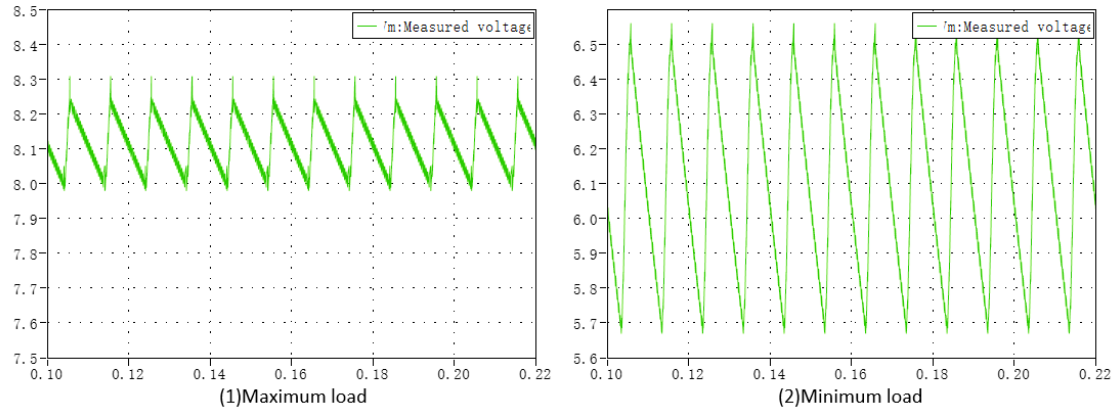

Figure 4.5: Main converter simulation results under non-ideal conditions (AC Input)

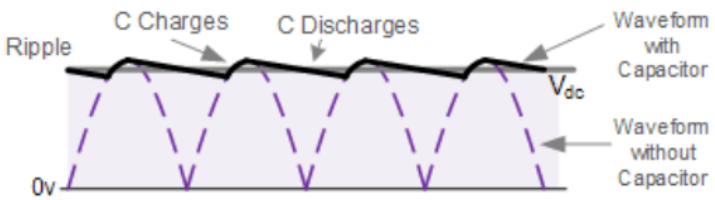

Figure 4.6: Voltage signal on rectify circuit [1]

Figure 4.5 shows the simulation results for this AC input circuit at maximum and minimum load. It can be observed that the output voltages achieve the desired result of being 8 V at maximum load, but not at minimum load. They both have a voltage ripple greater than 0.1 V, which is not at all consistent with the intended design. The followings are the analysis of the simulation results and ways to improve them:

(1) Power loss: The voltage drop of output was mainly caused by the forward voltage drop of diodes and the equivalent resistance of real components as presented in DC input analysis. However, when the input voltage source changed from DC to AC, the output voltage under either max or min load was slightly higher. This was caused by the increase of input voltage level, $30\sqrt{2}$ V AC is approximately 42.45V which is clearly bigger than 35V DC value. Increasing the duty cycle can neutralize the voltage drop caused by real component power loss which basically were increase the power inputted but can't promote efficiency. If the resistance and forward voltage drop of them could be significantly reduced, a slight change of duty cycle would make the system work properly with higher efficiency.

(2) Ripple: The ripple of both AC and DC powered circuit output voltage was bigger than the ideal condition (Figure 3.2), the reason is that the value of decoupling capacitor C (In Figure 4.1), and C2 (In Figure 4.3) were both designed under ideal conditions. When the circuit was powered by an AC source, the ripple was even ten times bigger than the requirement (0.1V). This ripple was caused by the ripple on the input DC voltage which is significantly bigger than the ripple caused by switching time of the switches as the transformer switching frequency (100 kHz) is much bigger than the rectified DC ripple frequency (100Hz). Figure 4.6 have demonstrated how the voltage ripple formed over a smoothing capacitor in rectifying circuit. To erase this phenomime, increasing the capacitance of decoupling capacitors is a good solution, either primary side (C1) or secondary side (C2) as capacitors can reduce voltage sudden change. Decreasing the DC voltage ripple on the primary side can also reduce the output ripple, to achieve that, the diodes on rectify circuit need a lower on-resistance or a lower forward voltage drop.

To erase the mismatch between ideal and non-ideal output voltage under an AC input voltage source, researchers need to consider both decoupling capacitor and duty cycle as output ripple is out of the required range. If the adjustment on the two parameters doesn't change and is inadequate to erase this mismatch, replacing some components such as diodes, inductors, etc. could be taken into consideration as a component closer to ideal condition would help a lot when building a real electrical device.

5. Gate drive circuit design

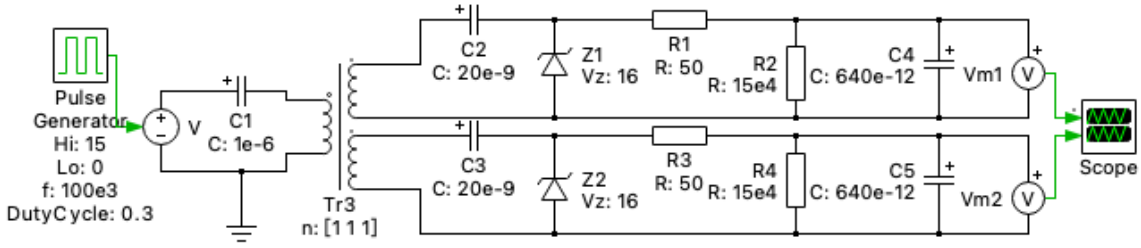

Figure 5.1: Schematic of the gate driver circuit

Figure 5.1 shows the schematic of the gate driver circuit. This circuit can use a PWM signal source to control two MOSFETs simultaneously via a 1:1:1 transformer. The basic

principle of the gate driver circuit is to supply a large enough signal to the gate of the MOSFET to quickly switch the MOSFET between its on and off states, but not so large as to cause damage to the MOSFET. Several resistors and capacitors were used in this circuit. They were used to control the charge/discharge rate of the gate to provide a stable supply voltage, filter out noise and interference, and allow the MOSFET to turn fully on. (C_4 and C_5 are just the input capacitance of the MOSFET, these values depend on the datasheet) The roles of these components are described below, and the output simulation results for different component value selections are also shown below to better illustrate the role of the components in the circuit. When an element is explored, all other element values remain the same.

Gate Resistor (R_1/R_3): The main function of the gate resistor is to be able to limit the charge /discharge rate to ensure the safe and reliable operation of the MOSFET. It forms an RC circuit with the gate capacitor of the MOSFET. The time constant of this RC circuit is determined by the product of the resistor and the capacitor. The higher the value of the resistance, the longer the time constant and the slower the charging/discharging of the gate capacitor. When the MOSFET is turned on or turned off, the gate resistor limits the current flow or voltage drop across the gate and prevents sudden voltage change which could lead to excessive power dissipation or even damage the device. A smaller gate resistance can result in faster charging/discharging of the gate and significant current flow while a larger one can slower the switching times and higher power loss. (Figure 5.2 shows this point) Therefore, in a comparison of the results of several simulations, this value was chosen to be 50 Ω.

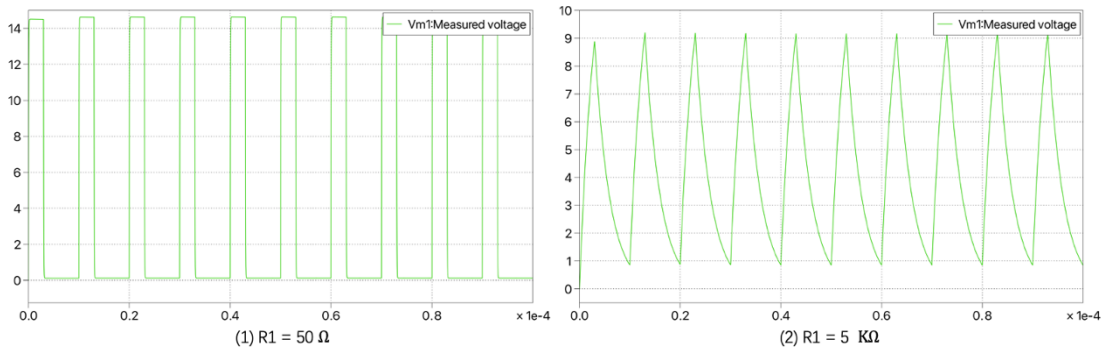

Figure 5.2: Simulation results of the gate driver circuit with different gate resistor values

Pull-down resistor (R_2/R_4): The main purpose of it is to prevent the gate of the MOSFET from floating when the gate driver output is in a high impedance state. When the gate driver output is not actively driving the gate, the gate may be charged due to parasitic capacitance or leakage current in the system. If the gate voltage is not properly discharged to a known state before the next switch, the MOSFET may be damaged. A suitable pull-down resistor provides a low impedance path for the gate to discharge to a known state while minimizing power dissipation from the resistor. The pull-down resistor value is usually chosen to be significantly greater than the gate resistance value. Figure 5.3 shows a simulation with the choice of 15 KΩ and 150 KΩ pull-down resistors, and it can be observed that 15 KΩ causes more energy loss. So, this value is chosen to be 150 KΩ.

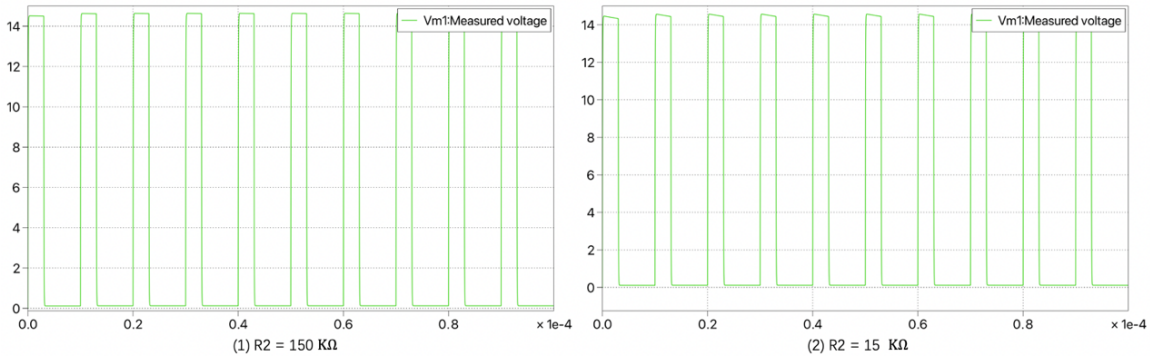

Figure 5.3: Simulation results of the gate driver circuit with different pull-down resistor values

Zener diode (Z_1/Z_2): The role of it in this circuit is to act as a voltage clamp. Zener voltage is selected to be slightly higher than the maximum voltage that the gate of the MOSFET can safely withstand. This configuration ensures that the voltage across the gate is limited to a safe level, even if the input voltage exceeds the safe operating range. Figure 5.4 shows the output voltage results of the circuit when the Zener voltage is equal to 16 V and 10 V respectively and the input is always 15 V at the maximum. It can be seen that the Zener diode does protect the circuit and limits the voltage. As the voltage that ensures normal switching operation of the MOSFET is 12-15 V, the Zener voltage is chosen to be 16 V.

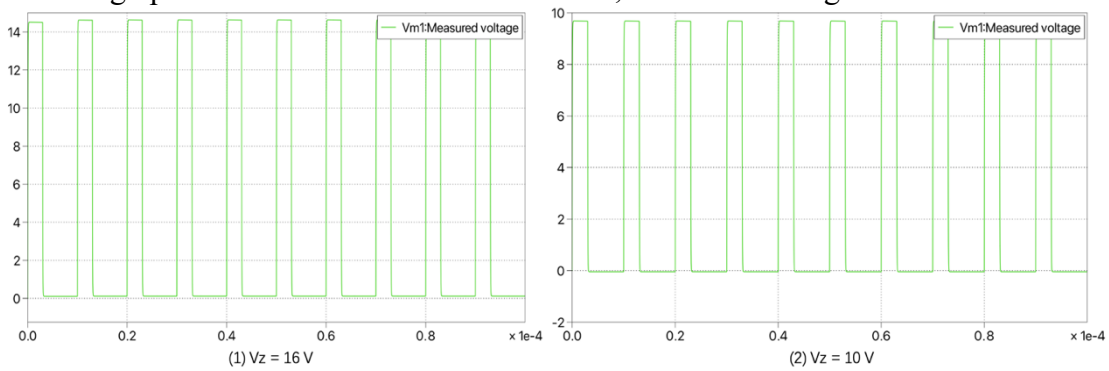

Figure 5.4: Simulation results of the gate driver circuit with different Zener voltage

Decoupling capacitor (C_1): It is typically used in gate drive circuits to reduce noise and stabilise the supply voltage. It provides a low impedance path to the ground for high frequency noise generated by the gate driver circuit or other components in the system. This helps to prevent noise from interfering with the operation of the gate driver. It also helps to stabilise the supply voltage to the gate driver circuit. Its value here is chosen to be 1μF to prevent it from being too small and failing to affect the circuit or too large which affects the saturation of the transformer. Figure 5.5 illustrates the difficulty of stabilising the voltage when the value is too small.

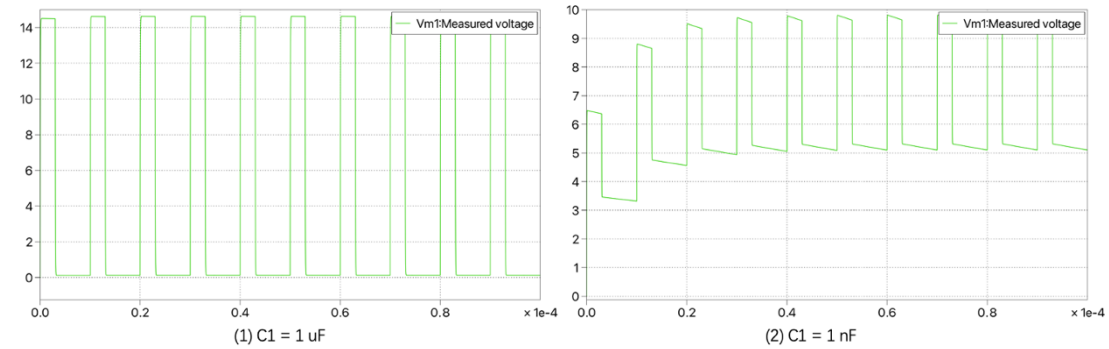

Figure 5.5: Simulation results of the gate driver circuit with different gate resistor values

Other capacitors (C_2/C_3): It is used to generate a higher voltage than the input voltage to fully turn on the MOSFET, which is charged to a high voltage level when the MOSFET is turned off. This voltage is used to drive the MOSFET gate when it needs to be switched on, thus increasing the efficiency of the circuit. This value was chosen as 20 nF.

Figure 5.6 shows the output of the two circuits when all the components are taken to the appropriate values, and both circuits have the same output, and the maximum output is approximately 15 V. This is in line with the original design of the gate driver circuit, which controls both circuits at the same time and. The output signal is also in the range where the MOSFETs can be controlled to operate reasonably well on and off. The reason that the maximum output voltage is slightly less than 15 V is that there is power loss in the Zener diodes and resistors, but this does not affect the overall result too much.

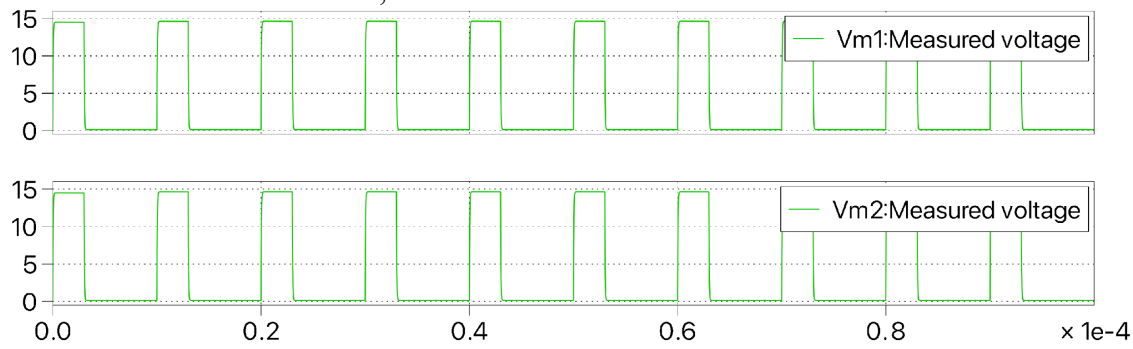

Figure 5.6: Simulation results of the gate driver circuit

6. Conclusion

This report has discussed how to design an open loop control Two Switch Forward DC/DC converter circuit in PLECS. Four parts of simulations had been carried on, which are: DC input main converter under ideal condition, DC input converter under non-ideal condition, AC input converter under non-ideal condition, and Gate driver circuit. Simulations show the circuit can work properly under ideal condition. However, in the non-ideal state, the results did not match the requirements and it was observed that the unaccepted resistance and forward voltage drop of the actual components influenced the output voltage of the circuit, and the output voltage ripple was also affected by the size of the decoupling capacitor. Using this data in conjunction with methods from the power electronics lecture, the researchers adjusted the duty cycle and decoupling capacitance values of the circuit to be as close as possible to the ideal values, thus reducing the possible risks when building the actual converter. To build up a real Two Switch Forward DC/DC converter in the lab, future studies on close loop control, ESR, and ESL measurement is indeed.

7. Reference

[1] W. Storr, “Full wave rectifier and bridge rectifier theory,” Basic Electronics Tutorials, 06-Aug2022.
[Online].Available:https://www.electronicstutorials.ws/diode/diode_6.html. [Accessed: 22-Feb-2023].