ESE5730 Warm-up Project

Cascode Amplifier Design and Tape-out

Team 8

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Directory in Cadence: (**Library: Cascode_Amp2**)

Amplifier Schematic/Layout in **Cell**: **cascode_amp_cell_1_symbol**

Top Cell Schematic/Layout in **Cell**: **cascode_amp_cell_1_pad**

Test Bench in **Cell: cascode_amp_cell_1_pad_test** | ADE State Name: **final_test_PELASE_CHECK_THIS**

1. Specifications

No.	Parameter	Value	Pre-Layout	Post-Layout
1	Voltage gain	6 V/V	9.4 V/V	7.7 V/V
2	Bandwidth (3dB high cut-off)	400MHz	695MHz	650MHz
3	Maximum chip power consumption	10mW	8.5mW	7.8mW
4	Pad pitch	100um	>100um	>100um

2. Statement of Contribution

Shun Yao (~35 Hours): First Version Schematic/Layout/DRC/PEX; Final Version PEX/Correction/Verification

Yue Zhang (~35 Hours): Second Version Schematic/Layout/DRC/LVS; Final Version Schematic/Layout/DRC/LVS

3. Schematics

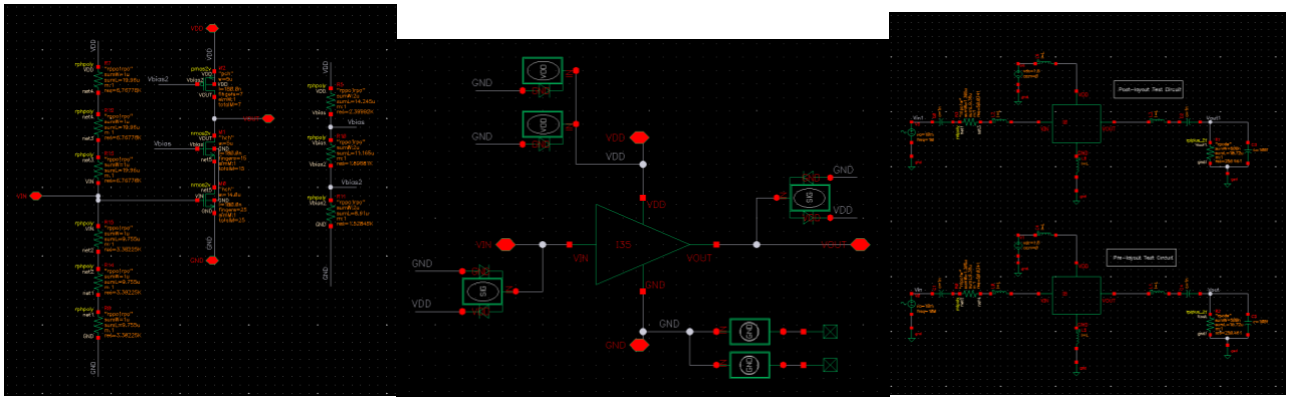

Figure 1. Schematics for Cascode Amplifier (left), Cascode Amplifier with Pads (middle), Full Test (right)

4. Pre-Layout Simulations

DC Operating Points:

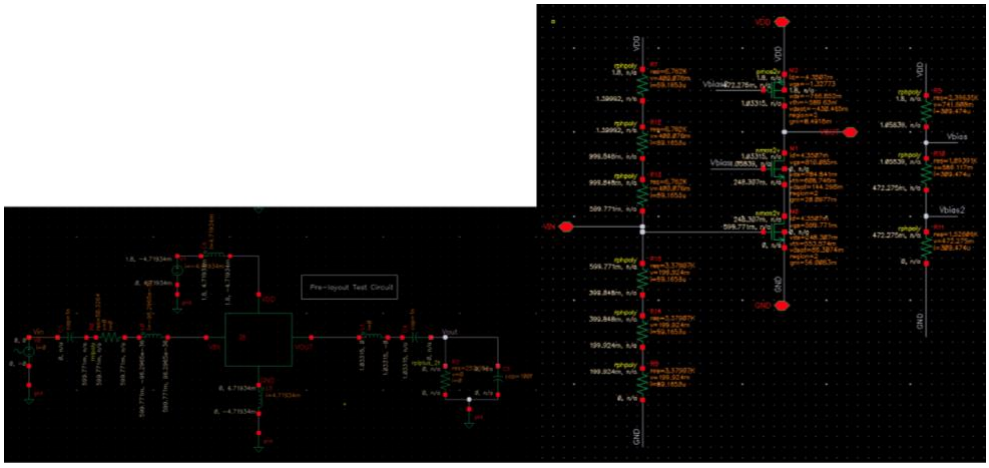

Figure 2. DC Simulation Result for 0.5nH

The DC simulation results are all the same for bondwires between 0.5nH and 2nH.

AC Simulation:

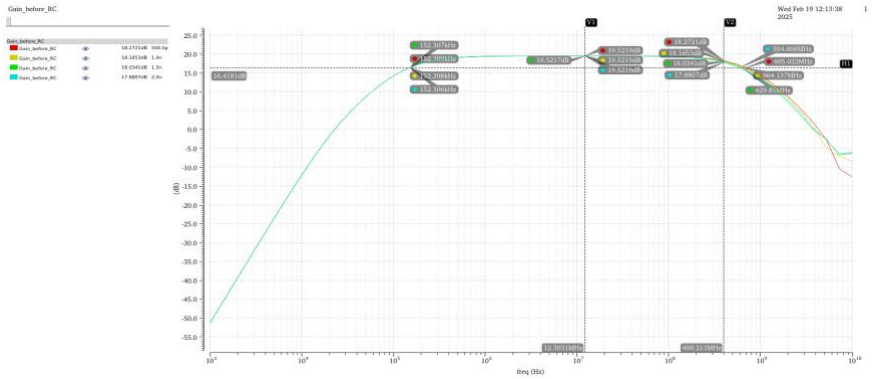

Figure 3. AC Simulation Result from 0.5nH to 2nH

Transient Simulation:

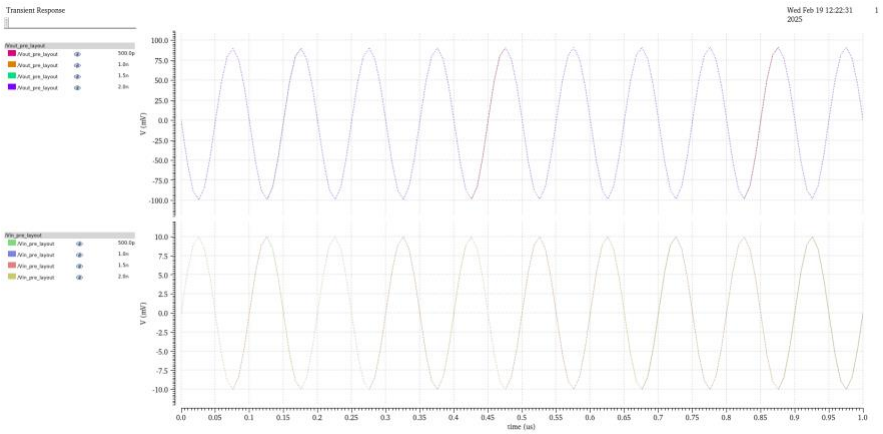

Figure 4. Transient Simulation Result from 0.5nH to 2nH

Transient Pulse Simulation:

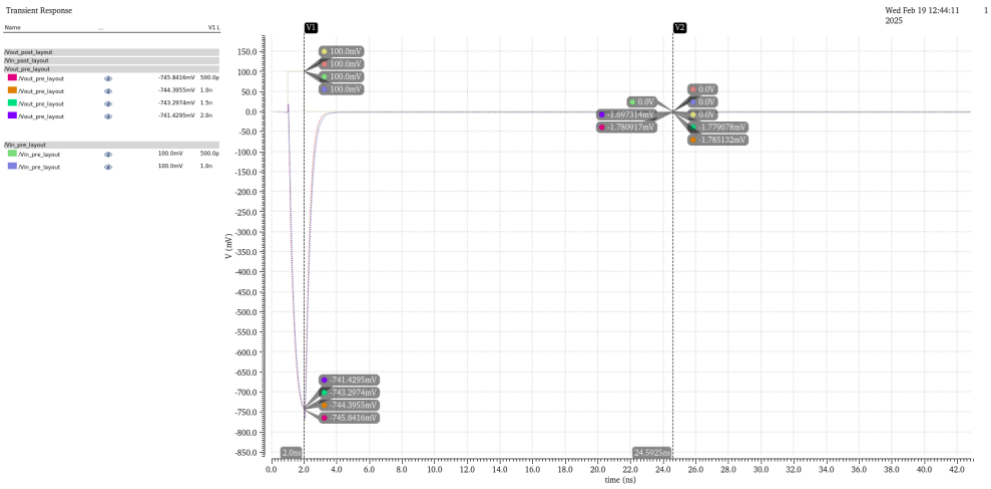

Figure 5. Transient Pulse Simulation Result from 0.5nH to 2nH

5. Layout

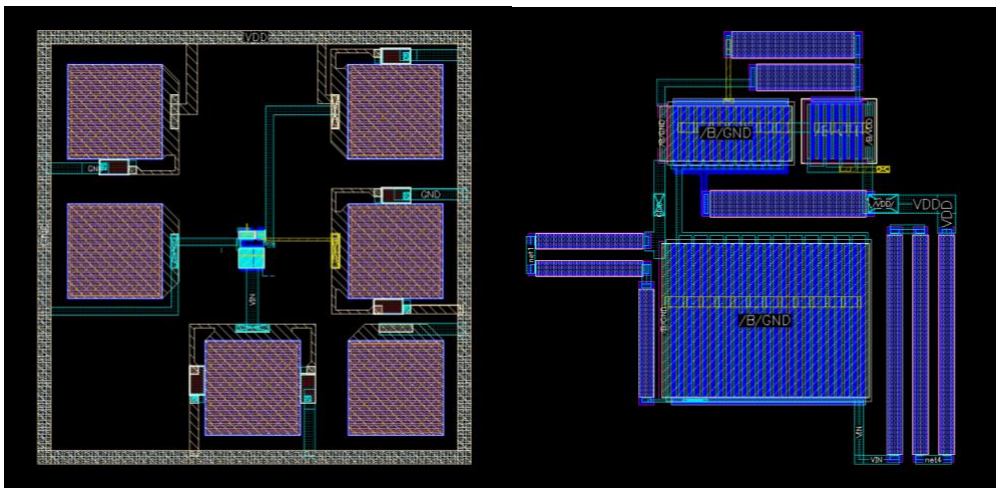

Figure 6. Full Layout (left) & Cascode Amplifier (right)

6. DRC LVS Result

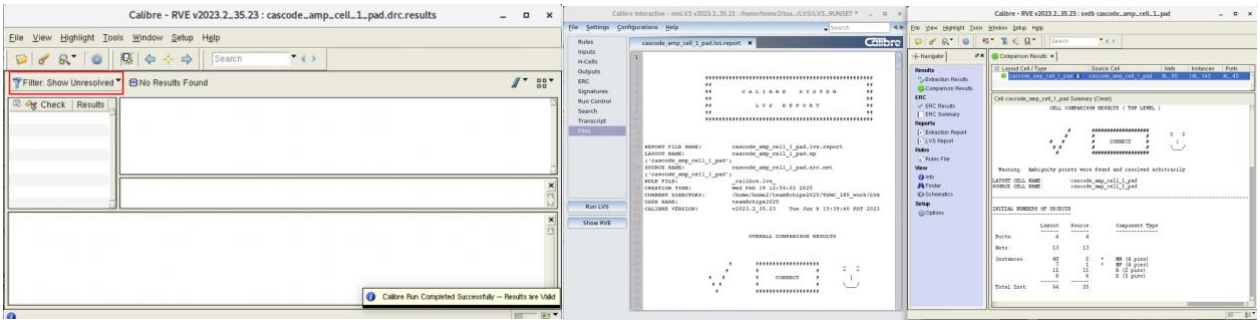

Figure 7. DRC Result (left) & LVS Result (right)

7. Post-Layout Simulations

DC Operating Points (The DC simulation results are all the same for bondwires between 0.5nH and 2nH):

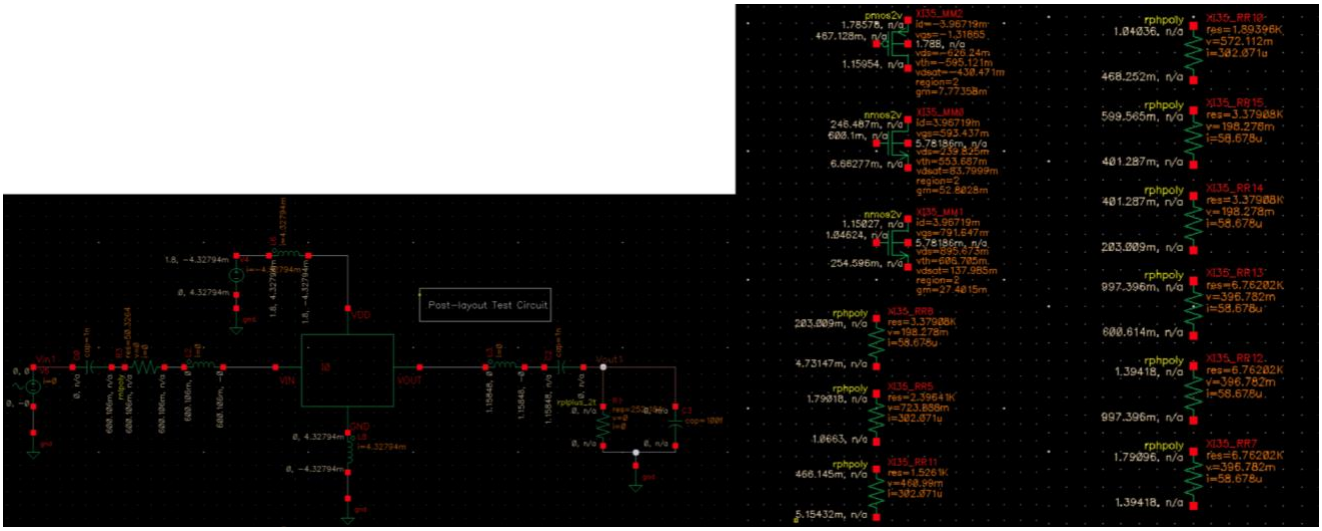

Figure 8. DC Simulation Result for 0.5nH

AC Simulation:

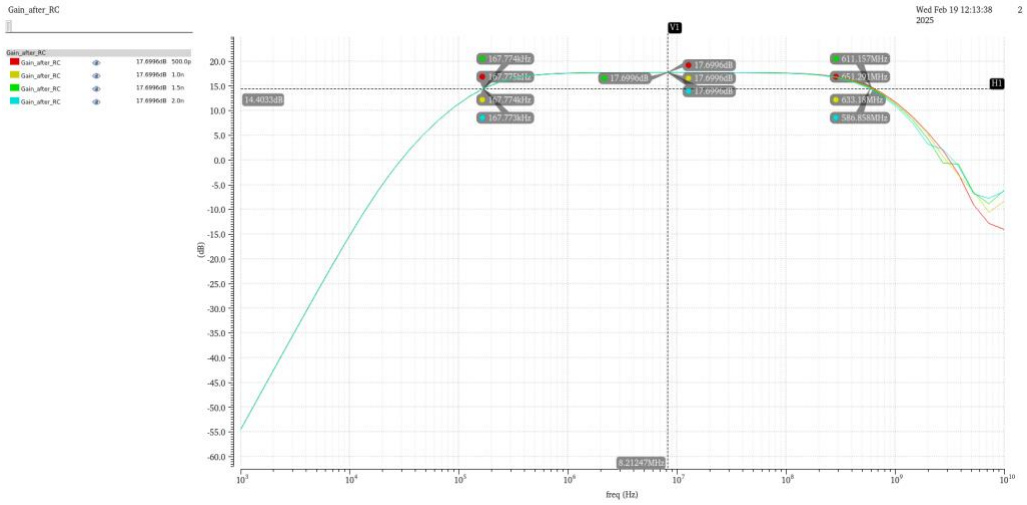

Figure 9. AC Simulation Result from 0.5nH to 2nH

Transient Simulation:

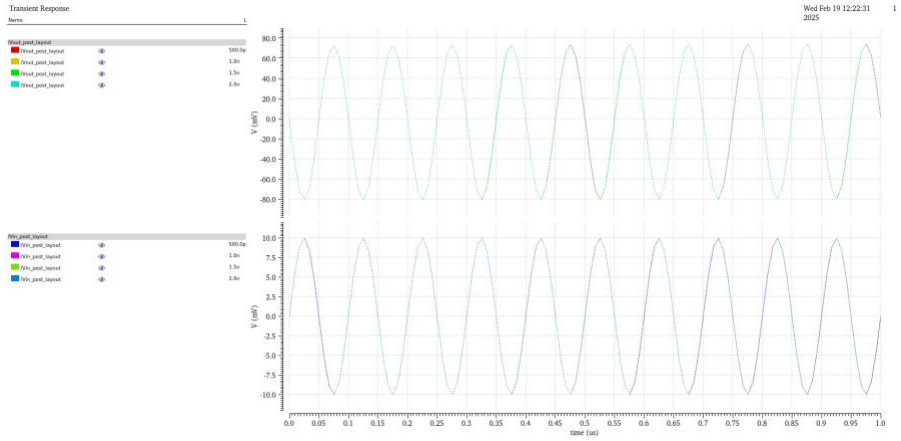

Figure 10. Transient Simulation Result from 0.5nH to 2nH

Transient Pulse Simulation:

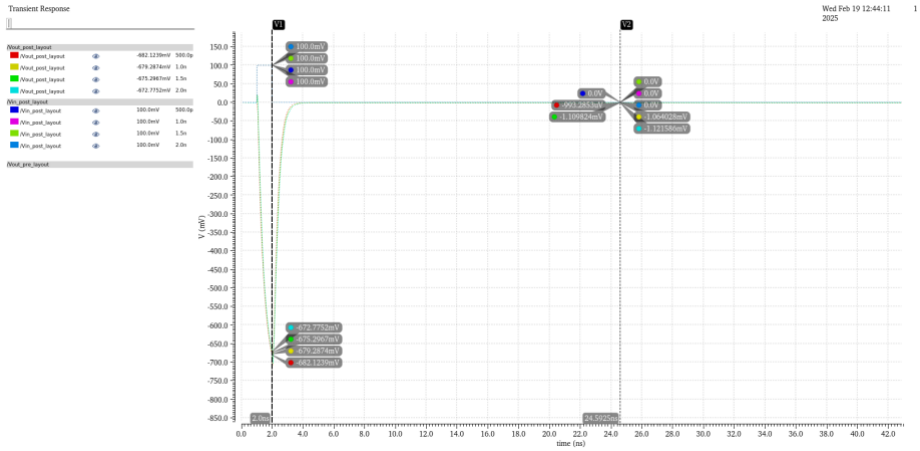

Figure 11. Transient Pulse Simulation Result from 0.5nH to 2nH

8. Current Verification

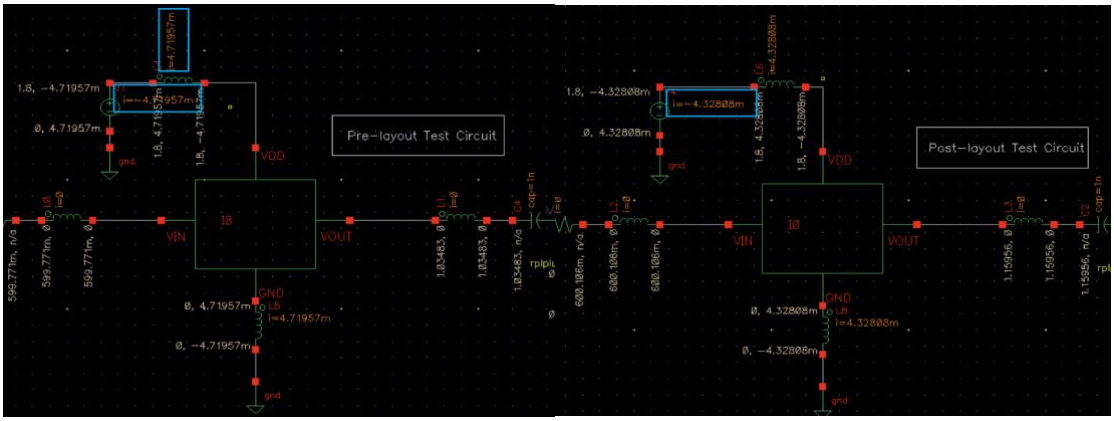

Figure 12. Current Verification for pre-layout (left) and post-layout (right)

In the layout, the Minimum trace width is 0.23um. According to the TSMC handout, the metal current density is no more than 250mA/um, the Maximum current in our design is 4.7mA, therefore, all traces could handle the intended current.

Metal TLP CD	TLP (Tr=10ns; Td=100ns)	Specification I_{ESD}>1.3A (ESD.CD. 1g^{U})	Specification I_{ESD}>12mA (ESD.CD. 2g^{U})
	I_{ESD} (Normalized by width)	The suggested metal width	The suggested metal width
M1 (4000Å)	250 mA/um	5.2 um	0.048 um
Mx (4000Å)	243.5 mA/um	5.34 um	0.049 um
Mn (8000Å)	342.5 mA/um	3.8 um	0.035 um

Figure 13. TSMC Metal Current Density Table