ESE5720 Final Project

Wideband Trans-Impedance Amplifier Design

DEPARTMENT OF ELECTRICAL AND SYSTEM ENGINEERING

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I. Introduction and Literature Search

- Introduction

A transimpedance amplifier (TIA) is a critical component in optical communication and detection systems, converting a small photocurrent from a photodiode into a voltage signal with minimal noise and high bandwidth. This function is pivotal in systems such as optical receivers, where the TIA acts as the first-stage amplifier, directly impacting the overall signal integrity and system performance. The demand for higher data rates, lower power consumption, and increased sensitivity has driven significant advancements in TIA design over recent decades.

In the context of wideband applications like optical time-domain reflectometry (OTDR) and high-speed communication systems, the TIA must balance several key performance metrics, including gain, bandwidth, noise, and linearity [1]. These requirements necessitate innovative approaches in both topology selection and circuit optimization. The challenge lies in achieving low input-referred noise and high transimpedance gain while maintaining a broad bandwidth to handle fast-changing signals from optical sources [2] [3].

Despite the simplicity of its core functionality, the design of a high-performance TIA involves addressing several key challenges [1] [4]:

- Wide Bandwidth: The TIA must have sufficient bandwidth to process rapidly changing input signals, which is particularly critical in high-speed optical communication systems.
- Low Noise: Input-referred noise is a critical parameter, as it determines the smallest signal the TIA can reliably amplify. This is essential for systems like OTDR, where the signal of interest is often embedded in noise.
- High Gain: A high transimpedance gain is required to amplify the weak photocurrent into a usable voltage signal while preserving signal-to-noise ratio (SNR).
- Input Capacitance Handling: The photodiode and TIA often introduce significant parasitic capacitance, which can limit the TIA's bandwidth if not properly managed.

- Literature Search

The historical development and continuous innovation in TIA designs have resulted in diverse approaches tailored to specific applications, following are some examples:

Classical Feedback-Based Topologies: The resistive shunt-feedback (SFB) topology is a foundational approach widely adopted for its simplicity and effectiveness. As highlighted in Romanova and Barzdenas's review [1], the SFB TIA offers a good balance of gain, bandwidth, and noise performance, making it a very good choice for optical communications. However, the trade-offs inherent in this design—such as the limitation in handling large input capacitances and its impact on bandwidth—necessitate enhancements like inductive peaking and variable gain implementations [3].

Advanced CMOS Integration [1]: Modern CMOS processes have enabled the integration of TIAs with digital processing circuits on a single chip, significantly reducing parasitic effects and power consumption. These CMOS designs emphasize low-cost and high-density manufacturing while addressing challenges like reduced supply voltages and increased process variations. Romanova et al. emphasize the role of CMOS in creating flexible and high-performance TIA solutions tailored for OTDR applications, where low noise and wide bandwidth are critical.

High-Speed TIA Design: High-speed applications demand TIAs capable of handling data rates exceeding 40 Gb/s. Razavi's exploration of TIA designs in advanced nodes demonstrates how careful trade-offs between noise, gain, and bandwidth are managed to achieve optimal performance [2] [3]. For instance, common-source amplifier topologies with inductive peaking have been employed to extend bandwidth while maintaining stability and low noise.

Application-Specific Innovations: In OTDR systems, where large parasitic capacitances from photodiodes dominate, customized TIA designs with capacitive feedback have proven effective in maintaining high gain and broad bandwidth [1]. Variable gain TIAs, implemented through adjustable feedback resistors, cater to dynamic signal conditions in these systems. However, these designs often require advanced techniques to mitigate noise and maintain stability under varying load conditions [3].

- State-of-the-Art Challenges

Despite the progress, several challenges remain in TIA design [2] [3]:

- Managing the noise-bandwidth trade-off to ensure signal fidelity in high-speed systems.
- Addressing input capacitance limitations without sacrificing gain or bandwidth.
- Achieving scalability and robustness in advanced process nodes while minimizing power consumption and area.

The design of a TIA for wideband applications requires a nuanced understanding of both classical and modern techniques, tailored to meet stringent performance criteria. By leveraging insights from prior research, this project will explore innovative circuit configurations and process optimizations to achieve a high-performance TIA within the constraints of a 45 nm CMOS process.

- Design Challenges and Objectives

The key to achieving a high-performance TIA lies in addressing the inherent trade-offs between its main performance parameters. For instance, increasing the transimpedance gain can lead to reduced bandwidth and increased instability, while minimizing input-referred noise often results in higher power consumption. These trade-offs become even more pronounced when designing TIAs using modern CMOS processes, where supply voltage and headroom limitations add further constraints.

In this project, we aim to design a high-performance wideband TIA using a 45 nm CMOS process, targeting the following specifications shown in Table1:

Table1. TIA Design Specifications

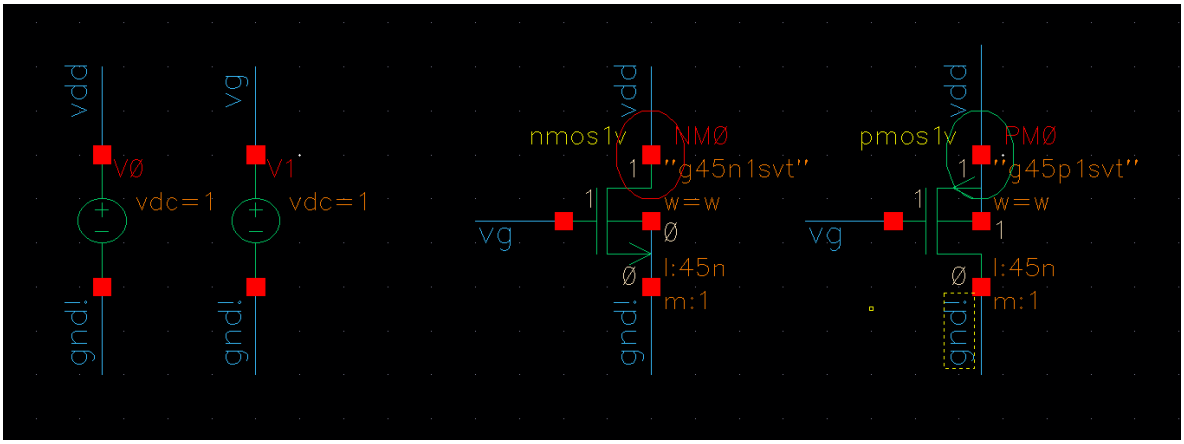
No.	Parameter	Value
1	Technology node (minimum channel length)	45nm (CMOS)
2	V_{dd}	1V
3	C_P	100fF
4	Load resistance	600Ω (differential)
5	Input current amplitude	2.67μApeak-to-peak
6	Required output peak-to-peak voltage swing	>0.4V (differential)
7	Trans-impedance gain	>150kΩ (differential)
8	The -3dB upper corner frequency	>250MHz
9	The -3dB low corner frequency	<10MHz
10	Total input referred current noise (integrated over BW_{-3dB})	$<125nA_{rms}$
11	Largest capacitor available	50pF
12	Smallest capacitor available	10fF
13	Largest resistor available	250kΩ
14	Smallest resistor available	1Ω
15	Total power consumption	<15mW

The following sections of this report will detail the literature search on existing TIA designs, outline the design methodology, and present simulation results that demonstrate the feasibility of our approach. Through a careful analysis of established techniques and innovative circuit configurations, this project aims to develop a robust TIA design that meets or exceeds the given specifications.

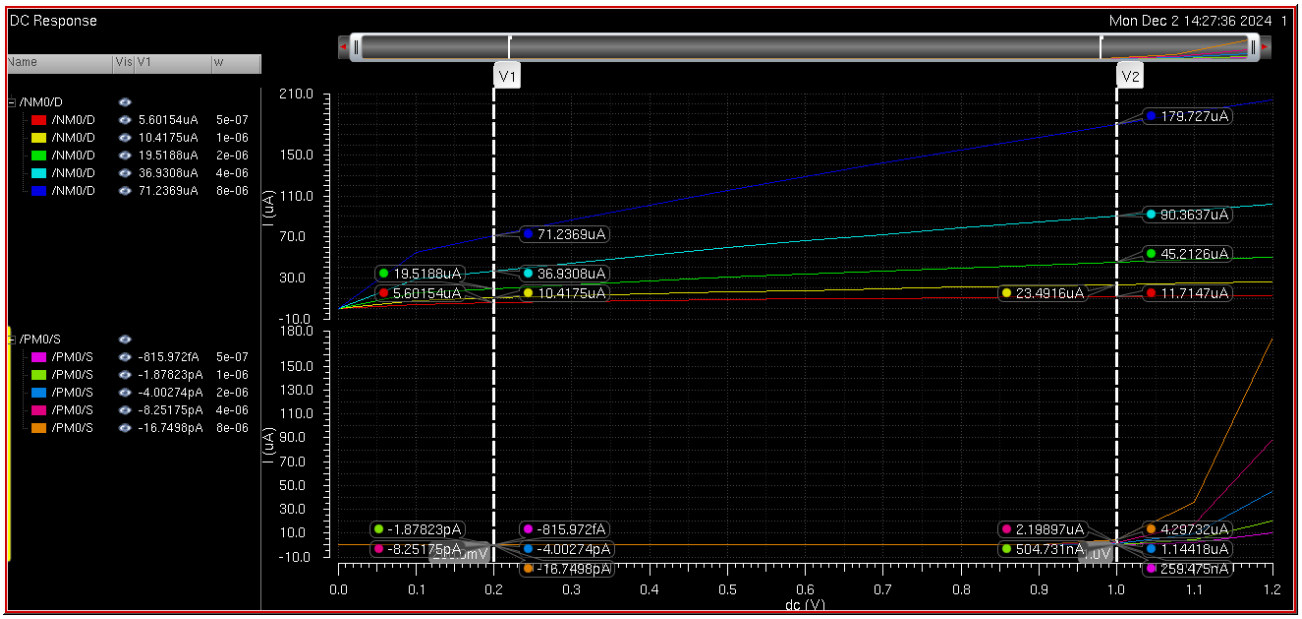
II. Process Characterization

- ID vs. VDS for 0<VDS<1V

Simulation Schematic:



Simulation Results:



For NMOS, the value of Id will increase as the Vds increases for all width considered. As the width increases, the magnitude of Id will increase linearly.
For PMOS, the value of Id decreases as Vsd (-Vds) increases, and the current falls to zero when the magnitude of Vsd falls below Vth. Similarly, as the width increases, the magnitude of Id increases linearly.
Therefore, the trend of those curves perfectly matches the calculations.
The values of Id could be calculated by to following Equations:

$$I_{D\_n} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2\left(1 + \lambda\left(V_{DS} - V_{eff}\right)\right) \qquad Equ1.$$

$$I_{D\_p} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2\left(1 + \lambda\left(V_{SD} - V_{eff}\right)\right) \qquad Equ.2$$

Take Vds(-Vsd)=0.2V and W=8um for example. Used data calculated from HW3 as shown in Table2.

$$I_{D\_n} = 314.4\left(1 + \frac{13}{5}(V_{DS} - 0.15)\right) \times 10^{-6} = 355.272uA$$

$$I_{D\_p} = 126\left(1 + \frac{7}{3}(V_{DS} - 0.15)\right) \times 10^{-6} = 140.7uA$$

Table2. Parameters of Different Size of Technology

Technology	NMOS 45nm	PMOS 45nm	Source
μC_{ox} ($\mu A/V^2$)	157.2	63.4	Calculated from Id
V_{t0} (V)	0.45	-0.45	Vth from Cadence
$\lambda.L$ ($\mu m/V$)	0.117	0.105	Calculated from Id and ron
C_{ox} ($fF/\mu m^2$)	17.78	19.11	Calcuted from Cgs
t_{ox} (nm)	2.41	2.4	Read from Cadence
$C_{ov}/W = L_{ov}C_{ox}$ ($fF/\mu m$)	0.152	0.152	Read from Cadence
$C_{db}/W \approx C_{sb}/W$ ($fF/\mu m$)	0.0726	0.0266	Read from Cadence

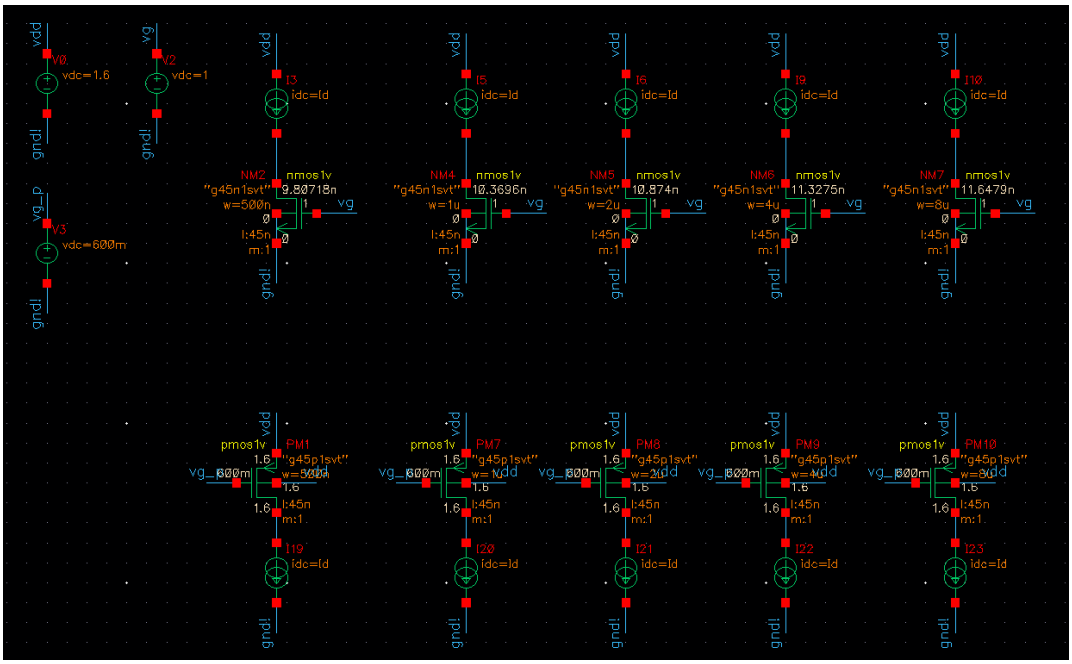
The Id and Vds exhibit an approximately linear relationship in both simulation and calculations under saturation conditions, which aligns with theoretical expectations. However, there is a significant difference in the magnitude of Id between the two methods. The potential reasons for this discrepancy are outlined below:

- The simulation has value of λ and u_n/u_p that might be less than those assumed in hand calculations.
- The Vth in simulation is different from hand calculations as the Vth might change as Id changes.
- Short-channel effects, such as velocity saturation and DIBL, reduce the simulated drain current.
- Parasitic effects, including fringing capacitance and overlap capacitance, further impact the transistor's performance in simulation.

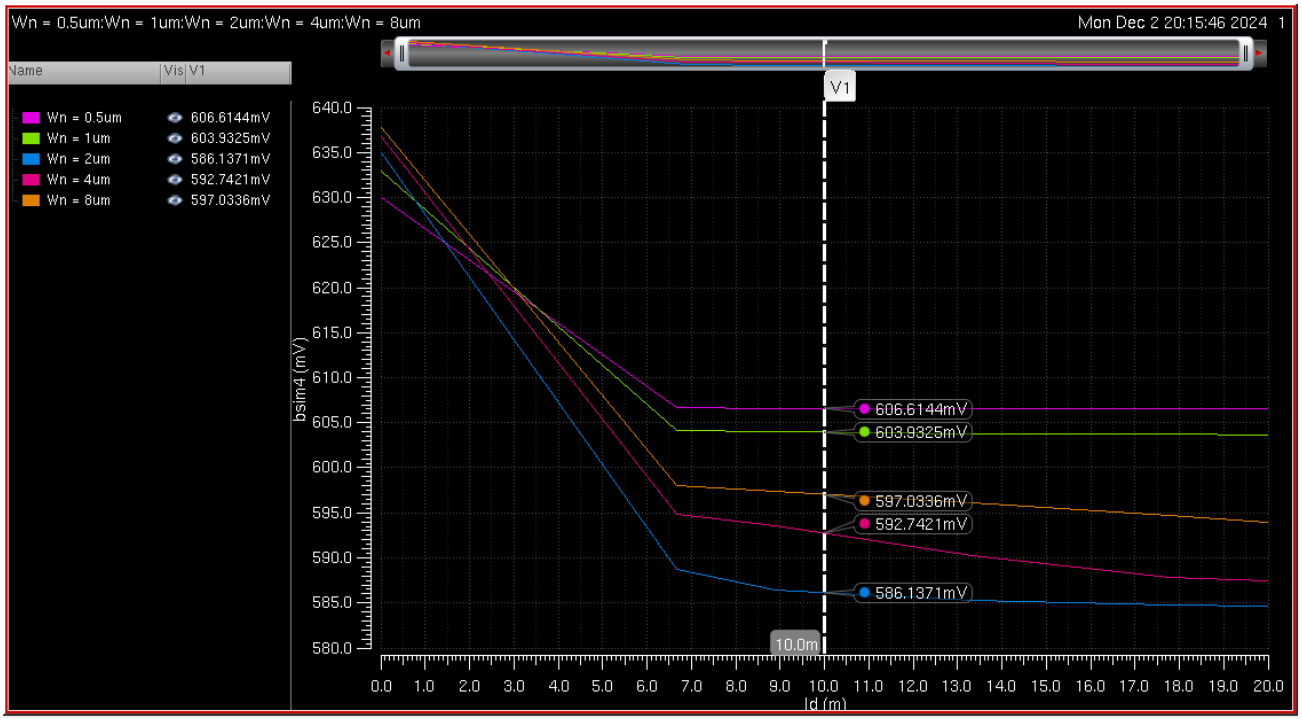
- Real-world factors like process variation and temperature effects are accounted for in simulation but ignored in hand calculations.

- Vth vs. ID for 0<ID<20mA

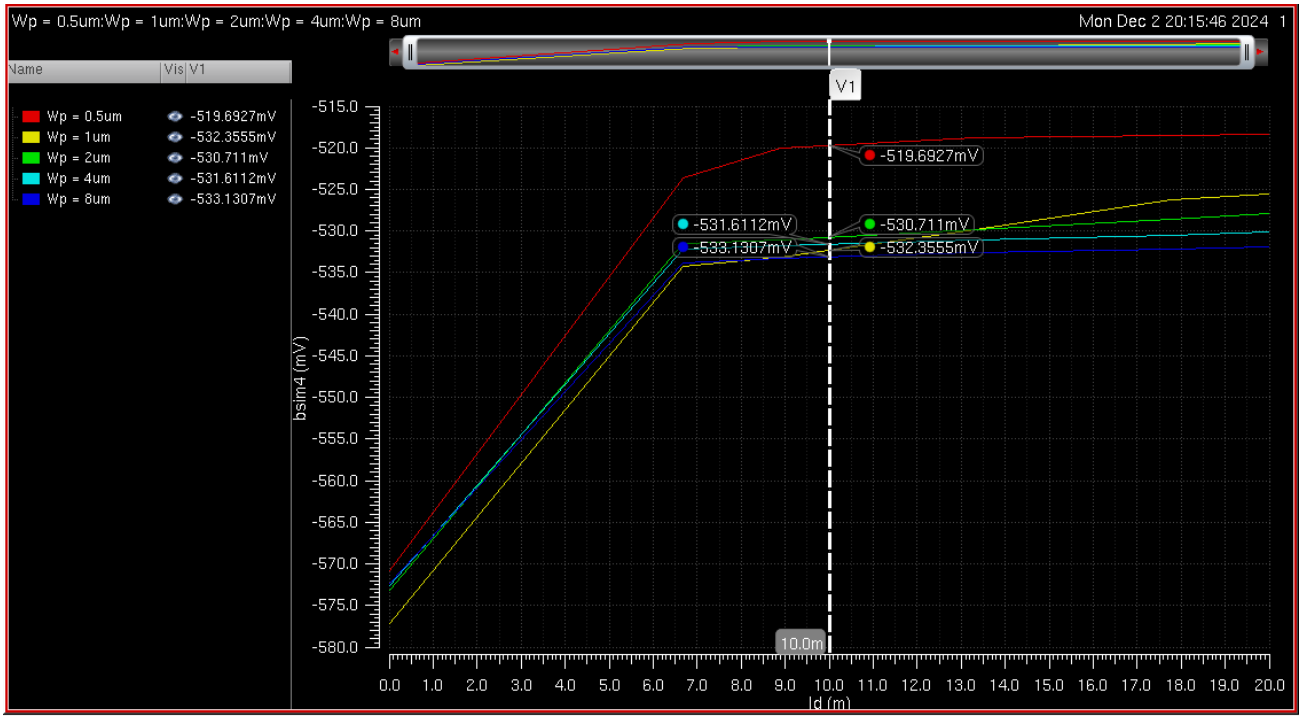
Test Schematic:



NMOS:



PMOS:



The simplified relationship between the Vth and Id can be described by the following equation:

$$V_{TH} = V_{TO} + \gamma\left(\sqrt{|-2\emptyset_F + V_{SB}|} - \sqrt{|2\emptyset_F|}\right) \qquad Equ3.$$

Vsb is stable, therefore ideally the Vth will not change as Id changes.

However, the simulation results show that the Vth of NMOS decreases linearly with Id as Id increases and stabilizes when Id exceeds 7 mA. In contrast, the Vth of PMOS increases linearly with Id and also stabilizes at the same current threshold. Smaller W should lead to higher Vth due to the narrow-width effect, where edge effects and parasitics dominate, increasing Vth.

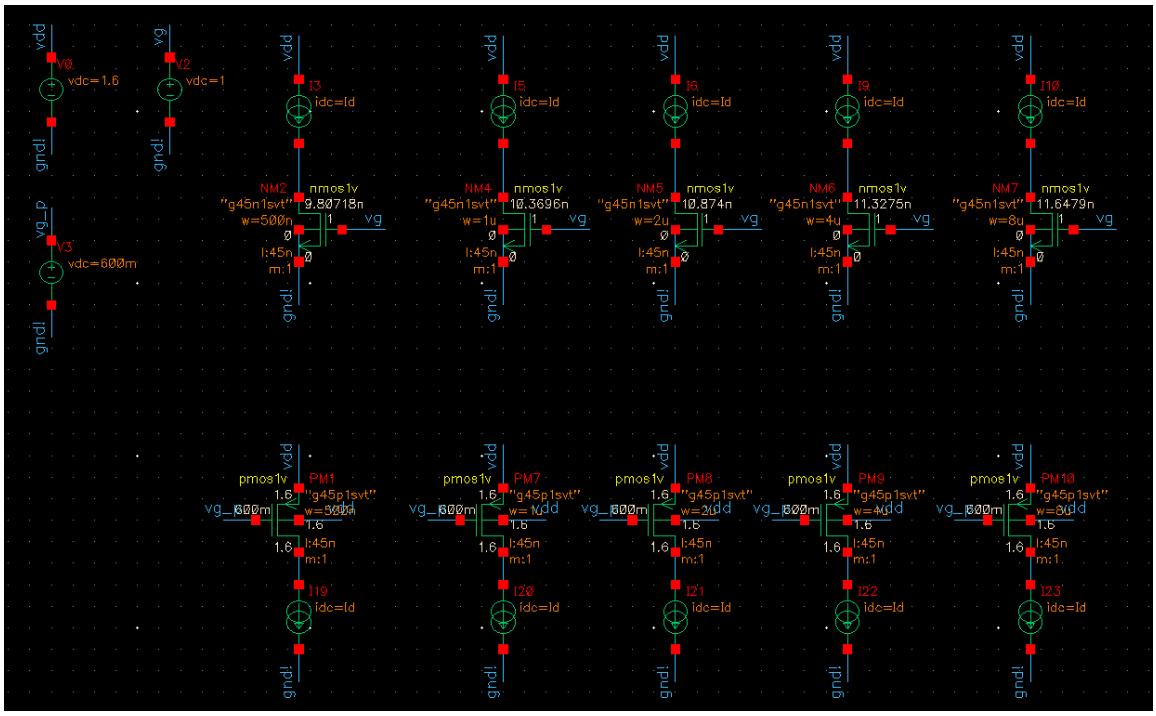
This simulation's behavior deviates from the assumption of a constant Vth in ideal hand calculations using Equ4. Following are the possible explanations for this phenomenon:

- Body Effect: Using Equ4, Vth varies with Vsb (source-body voltage). For NMOS, increasing Id reduces Vsb, leading to a decreasing Vth. For PMOS, the opposite trend occurs as Vsb increases with Id, causing Vth to rise.
- Short-Channel and Parasitic Effects: Short-channel effects, such as drain-induced barrier lowering (DIBL), and parasitic, like overlap capacitances, alter the effective Vth dynamically with Id, contributing to the observed trends.
- Simulation Accuracy: The simulation incorporates non-idealities, such as process variations and temperature effects, which impact Vth more accurately than the simplified hand calculation models.

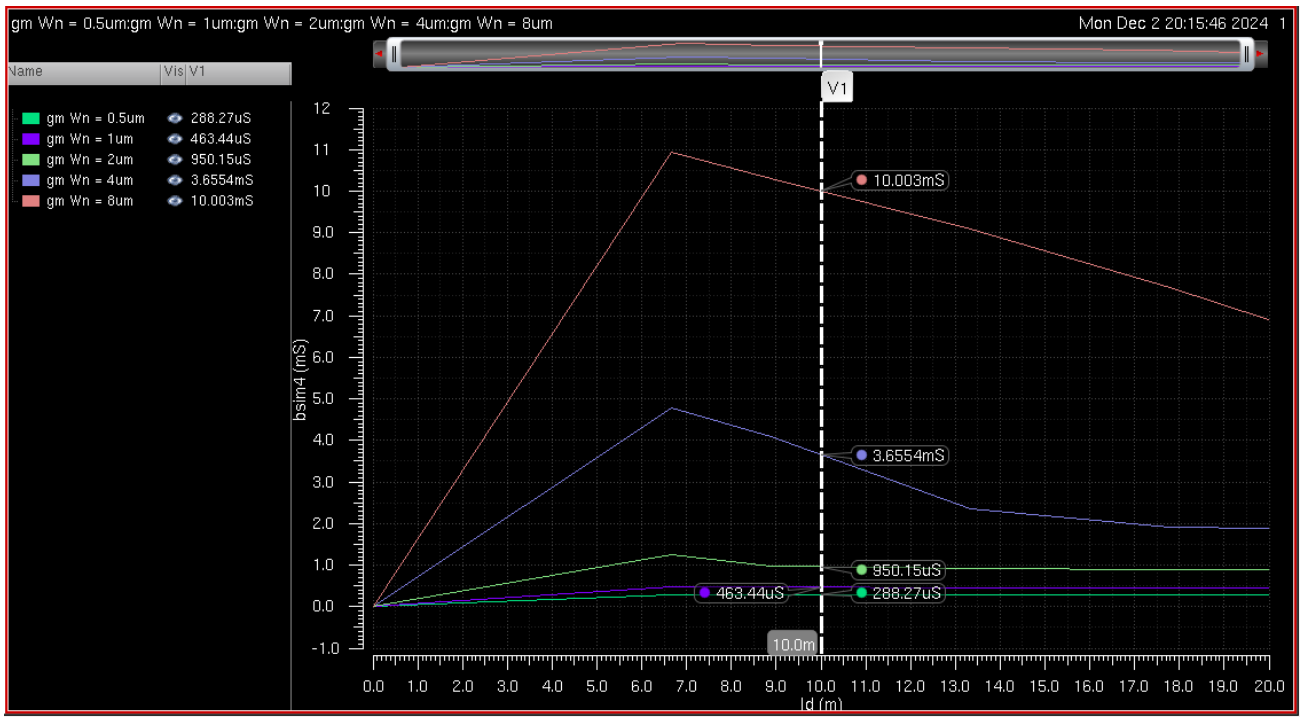
The Vth trends observed in simulation are consistent with the physical behavior of MOSFETs under varying Id. Considering real-world factors and dynamic interactions leads the difference.

- gm vs. ID for 0<ID<20mA

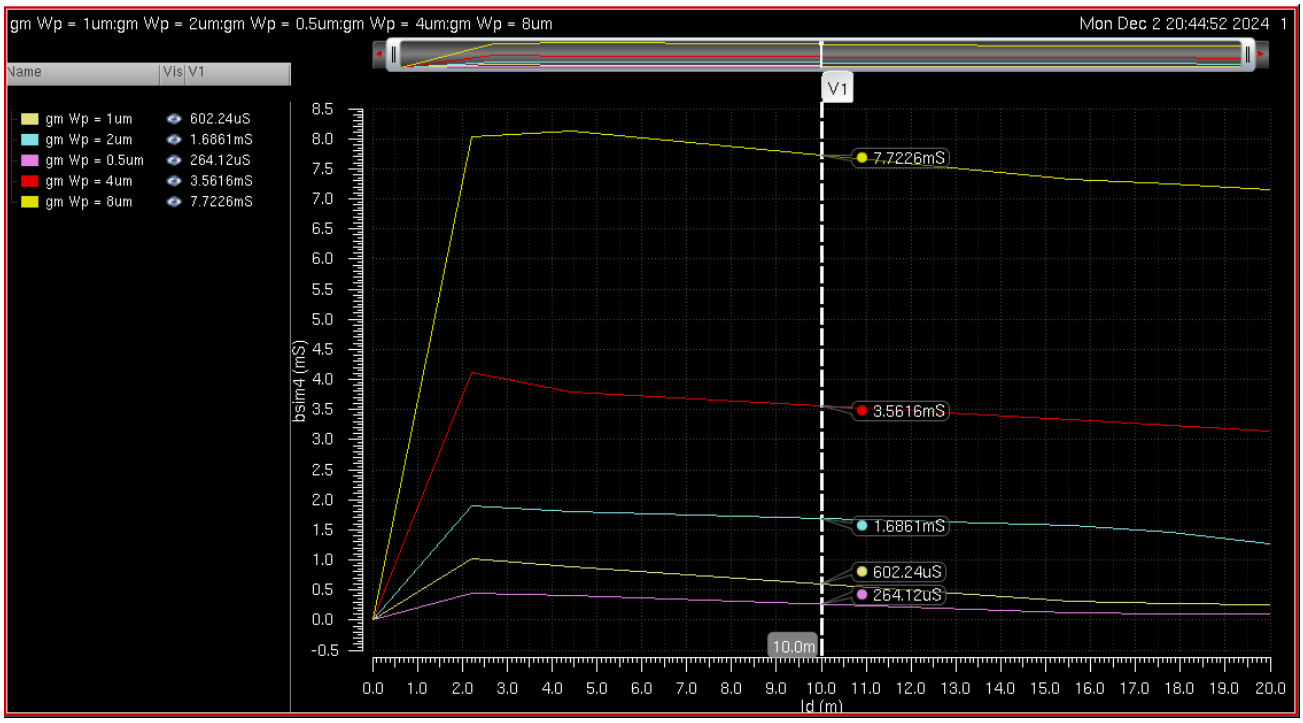
Test Schematic:



NMOS:



PMOS:



In the simulation, the transconductance gm of NMOS increases linearly with Id initially, then starts to decrease after Id exceeds 7 mA, with the rate of decrease becoming smaller as Id continues to grow. For PMOS, gm also increases linearly at first, stabilizes at Id>2 mA, and then gradually decreases with a diminishing rate of change. This trend is explainable as follows:

The variation of gm with Id is primarily due to the transition between different operating regions of MOSFET. At low ID, gm increases linearly because Id is highly sensitive to changes in Vgs, as the device operates in the linear or weak inversion region. As Id increases, the MOSFET enters saturation, and carrier velocity saturation limits the drift velocity, reducing the sensitivity of Id to VGS, causing gm to decrease.
Additionally, short-channel effects and lower carrier mobility in PMOS devices result in earlier and more pronounced reductions in gm. These effects combine to produce the observed trends in gm as Id varies.

The relationship between Id and gm could be described by the following equation:

$$g_m = \sqrt{2\mu_{n/p} C_{ox} \frac{W}{L} I_D} \qquad Equ4.$$

Take Id=10mA and W=8um for example. Used data shown in Table2.

$$g_{m\_n} = \sqrt{2 \times 157.2 \times \frac{8}{0.045} \times 0.01 \times 10^{-6}} = 23.64 mA/V^2$$

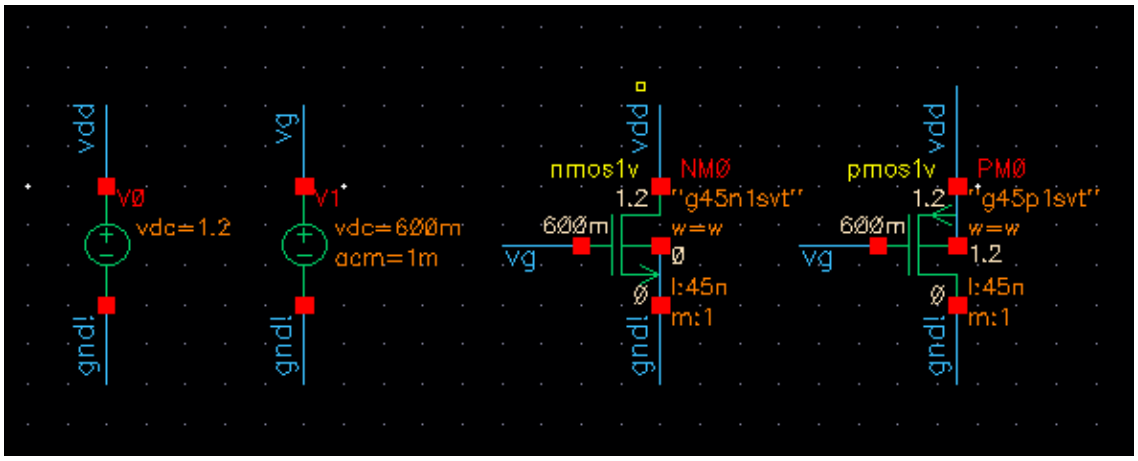
$$g_{m\_p} = \sqrt{2 \times 63.4 \times \frac{8}{0.045} \times 0.01 \times 10^{-6}} = 15.01 mA/V^2$$

Although the curve trend is explainable, the magnitude of hand calculated gm is larger than the simulation result by approximately a factor of two due to the following reasons:

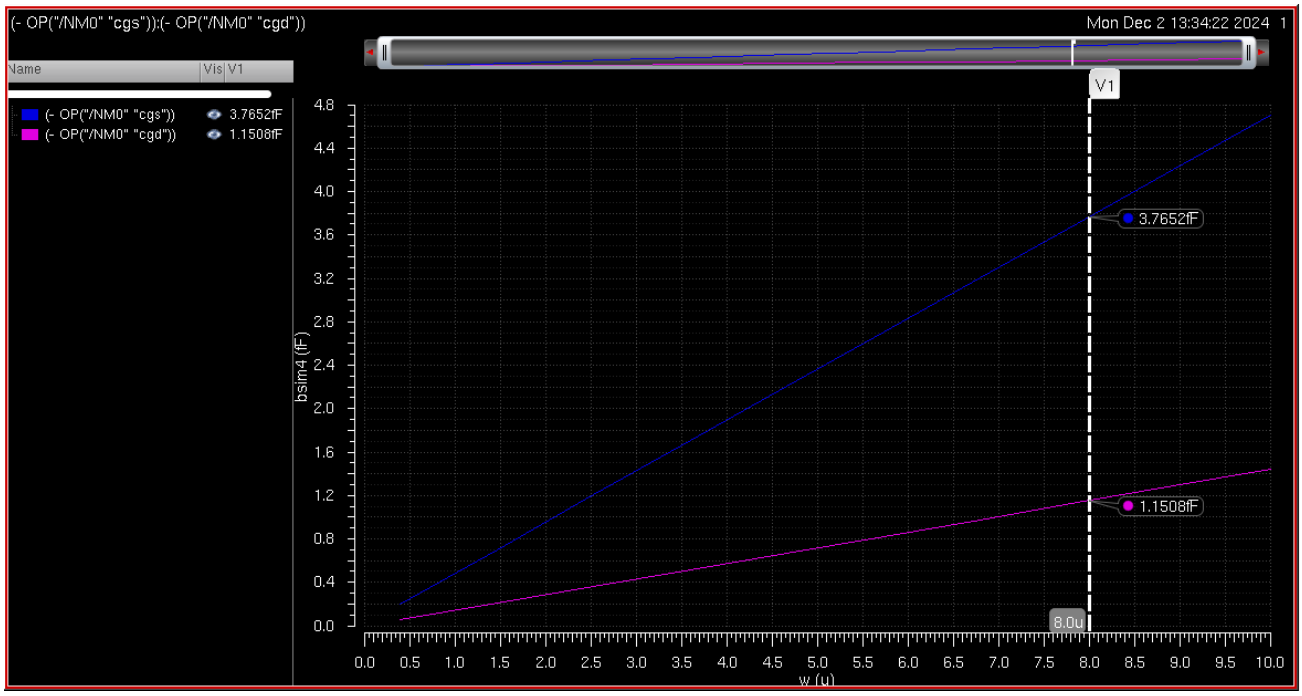
- The formula assumes ideal long-channel behaviour, neglecting velocity saturation, short-channel effects, and channel-length modulation present in real transistors. These effects reduce the actual transconductance in simulations.
- Simulated transistors account for parasitic elements, such as overlap capacitances, which effectively reduce the gate efficiency and lower gm.
- At higher Id, the carrier drift velocity approaches a saturation limit, causing gm to deviate from the square root relationship with Id predicted by the formula. This effect is especially significant in short-channel devices.
- The formula assumes a fixed Vth, while in simulation, Vth may vary dynamically with Id due to body effect and DIBL, reducing the effective transconductance.

- Cgs and Cgd vs. W for 0.4um<W<10um

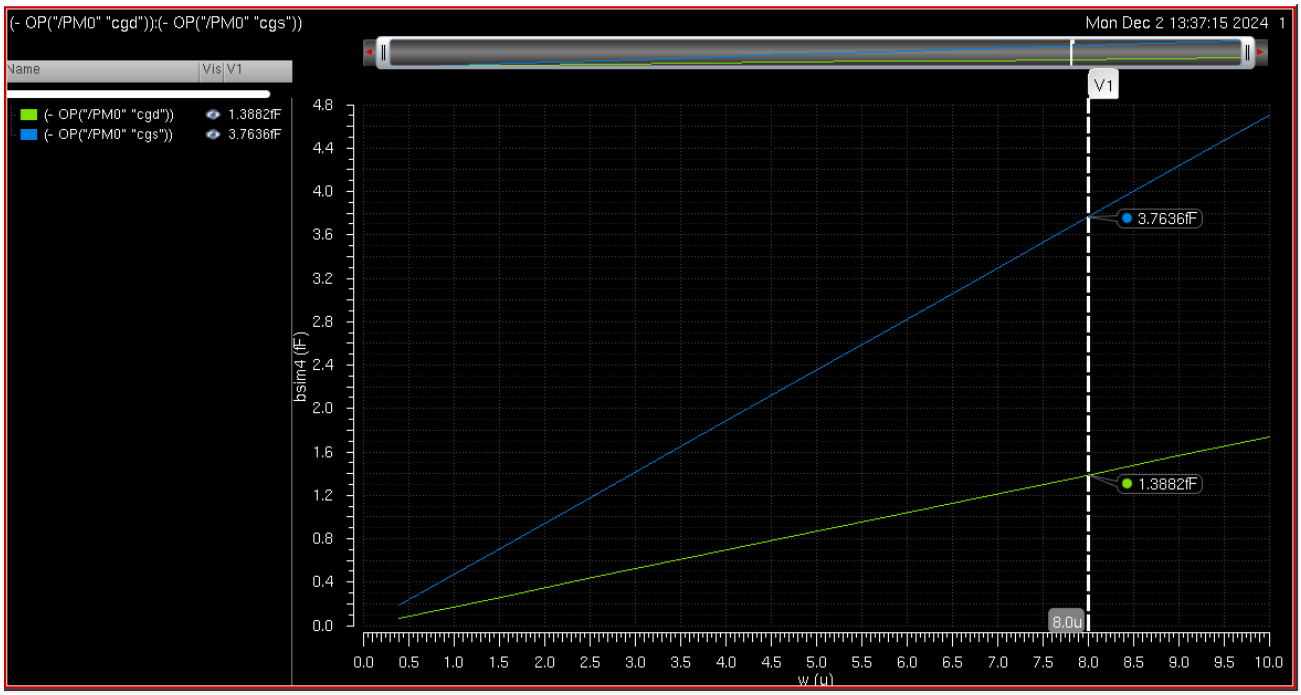
Simulation Circuit:



NMOS:



PMOS:



Add a negative sign to make the capacitance value positive in simulation (as mentioned on Ed).

Following are the equations that are used to calculate the value of Cgs and Cgd in saturation region.

$$C_{gd} = WL_{ov}C_{ox} \qquad Equ5.$$

$$C_{gs} = \frac{2}{3}WLC_{ox} + WL_{ov}C_{ox} \qquad Equ6.$$

According to Table2, the values can be calculated. Take W=8um for example:

$$C_{gd\_n} = WL_{ov}C_{ox} = 0.152W = 1.216fF$$
$$C_{gs\_n} = W\left(\frac{2}{3}LC_{ox} + L_{ov}C_{ox}\right) = 4.2672 + 1.216 = 5.48fF$$

$$C_{gd\_p} = WL_{ov}C_{ox} = 1.52W = 1.216fF$$
$$C_{gs\_p} = W\left(\frac{2}{3}LC_{ox} + L_{ov}C_{ox}\right) = 4.5864 + 1.216 = 5.8fF$$

The calculated results are very close to the simulation result with small differences.

This deviation is because the equations assumed an ideal small signal model for transistors, assuming a uniform capacitance distribution and neglects real-world factors such as edge effects, parasitic capacitances, and short-channel effects. Additionally, the equations rely on idealized values for parameters like Cox and Lov, which may differ from the actual values in the process model. The simulation, on the other hand, incorporates a more accurate representation of the device physics, including non-idealities and process variations, leading to more realistic capacitance values.

- What is the process fT? Does it change with drain current?

The process fT also known as the ***transition frequency***, is the frequency at which the current gain of a MOSFET drops to 1. It indicates the maximum frequency at which the transistor can effectively amplify signals. Mathematically, fT is given by:

$$f_T = \frac{gm}{2\pi(C_{gs} + C_{gd})} \qquad Equ7.$$

The process fT will change with Id. It depends on Id because both gm and the capacitances Cgs, Cgd vary with Id:

- gm increases with Id in the weak inversion or linear region due to its proportional relationship to square root of Id
- At higher Id, gm may saturate or decrease due to velocity saturation, limiting the increase of fT.
- Cgs and Cgd increase with Id due to changes in the operating region of the transistor and the widening of the depletion region. These capacitances slow the increase in fT with Id.

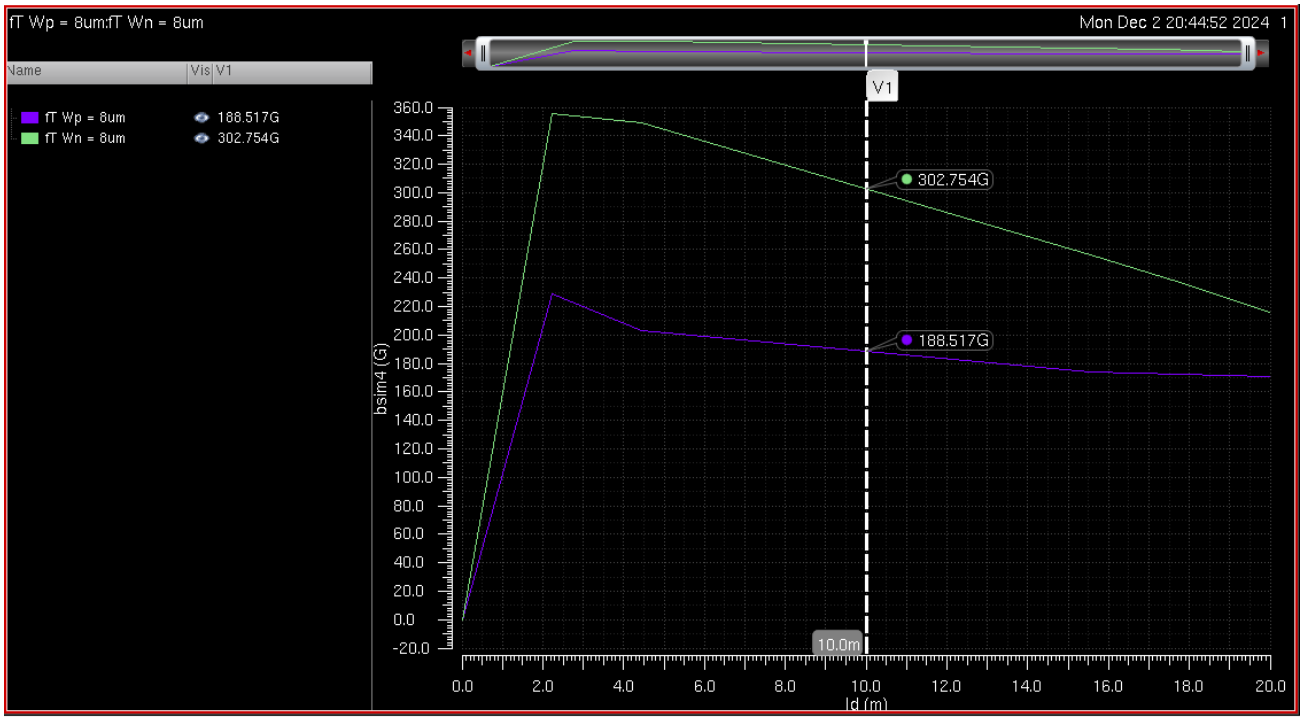
Typical Behavior of fT with Id:

- In the **subthreshold region**, fT grows as gm increases while Cgs and Cgd remain relatively small.

- In the **strong inversion region**, fT reaches its peak as gm dominates over the increasing capacitances.
- At **very high Id**, fT may decrease slightly due to velocity saturation reducing gm and the increase in Cgs+Cgd.

fT is a key metric of the frequency performance of a MOSFET, and it varies with Id due to its dependence on gm and capacitances. It typically increases with Id, peaks in the strong inversion region, and may decline at high Id due to non-ideal effects like velocity saturation and increasing capacitances.

Use cadence draw two example curves of fT vs Id diagram. The expression of fT is based on the Equ7, the following example curve is drawn when Wn=Wp=8um, swing the Id from 0 to 20mA for 10 steps, record the calculated fT value as Y axis.



III. Design Strategy

This section outlines the proposed design strategy for meeting the design specifications of the transimpedance amplifier (TIA). The design comprises four main stages, with each stage optimized for specific performance parameters include gain, bandwidth, power consumption, and signal swing. Below, a detailed explanation of the design choices and their corresponding rationale have provided.

1. Input Signal Source and Coupling

- **Input configuration**: The input signal simulates a photodiode using a parallel connection of a current source and a 100 fF capacitor. This setup generates a current signal proportional to incident light.

- **Coupling to stage 1**: The input signal is coupled to the first stage using a 50pF capacitor.

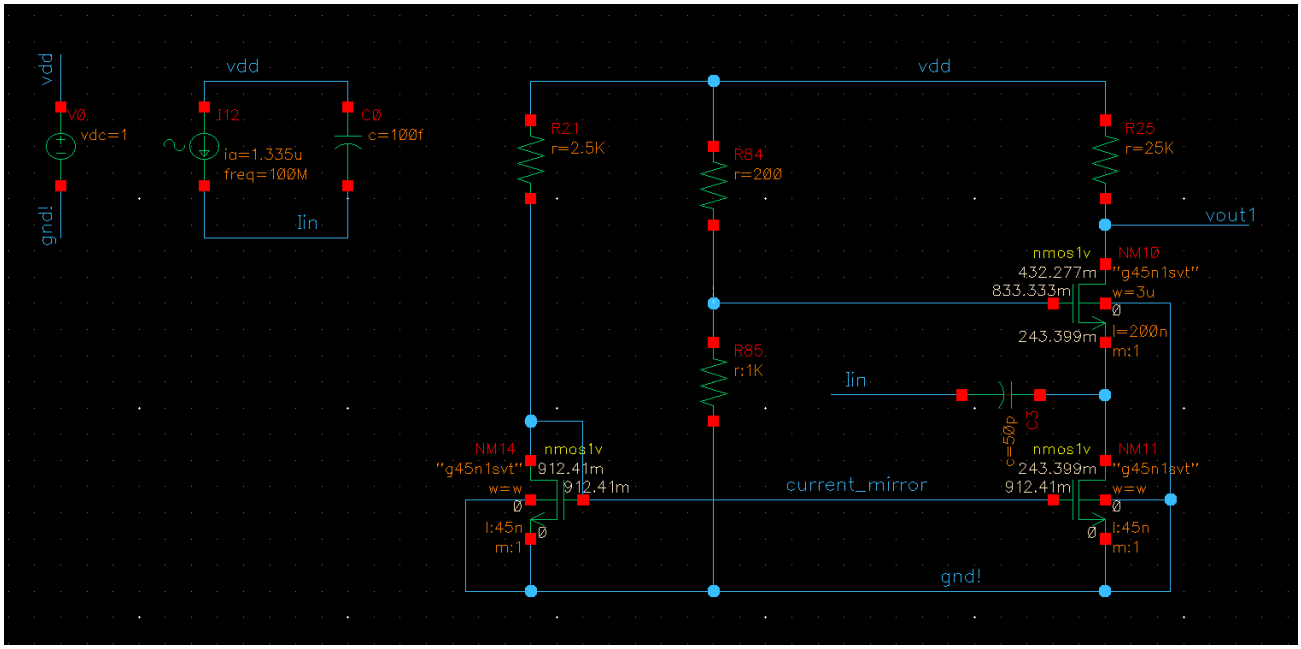
The coupling capacitor blocks DC bias from the photodiode and ensures that only the AC current signal is passed to the amplifier. The chosen capacitance ensures minimal signal attenuation at high frequencies while maintaining compatibility with the required low-frequency cutoff.

Additionally, the choose of coupling capacitance will affect the input refer noise level.

2. Stage 1: Common Gate Amplifier

- **Architecture**: The first stage employs a **common gate (CG) amplifier**.
- **Rationale**:
    - **High input impedance matching**: The CG amplifier provides low input impedance, which is critical for effectively converting the high-impedance input current from the photodiode into a voltage signal without significant loss.
    - **Wide bandwidth**: The CG topology inherently offers high-frequency performance, allowing the design to achieve the specified upper corner frequency of >250 MHz.
    - **Gain and linearity**: While the CG amplifier provides moderate gain, it ensures good linearity and stability, setting a strong foundation for the subsequent amplification stages.
- **Current mirror biasing**: The CG amplifier is biased using a current mirror circuit.
    - **Reason**: Current mirrors provide a stable and precise bias current, ensuring consistent amplifier operation across process and temperature variations. Additionally, current mirrors are efficient in terms of power consumption, helping meet the <15 mW power budget.

Using a cascaded amplifier will be a good alternative of this design in terms of noise level and gain. The circuit schematic of the first stage and Input signal source have shown in figure below:

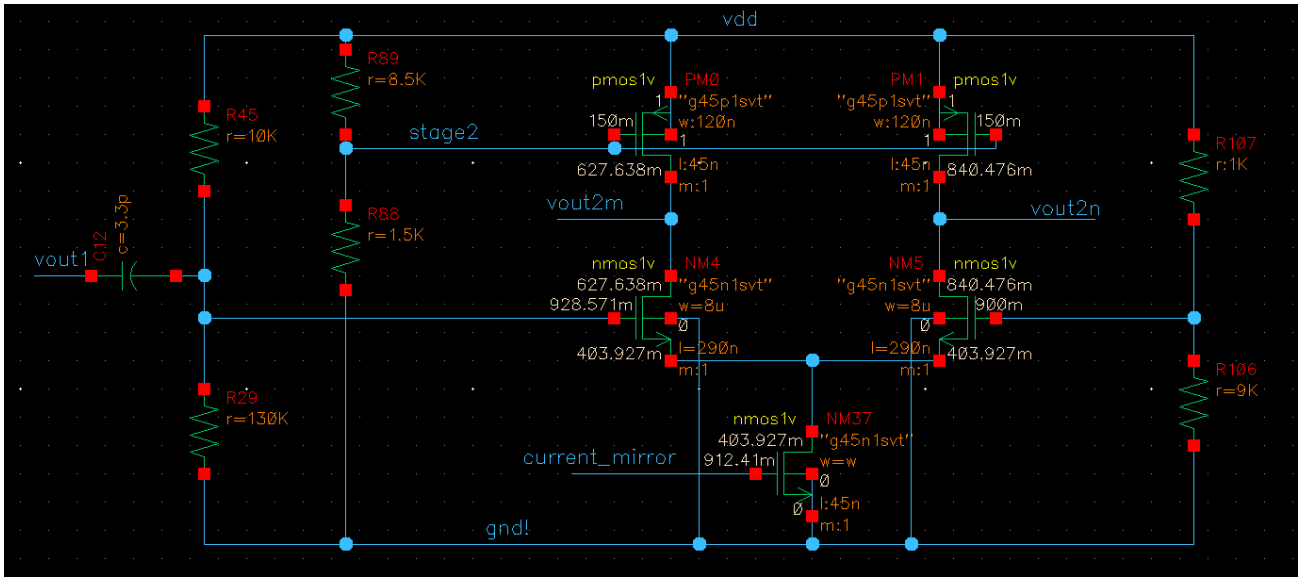


3. Stage 2: Differential Amplifier

- **Architecture**: The output of the CG amplifier is fed into a **differential amplifier**.
- **Rationale**:
  - **Differential signal generation**: The differential amplifier converts the single-ended signal from stage 1 into differential signals vout2m (positive output) and voutn (negative output), which are critical for minimizing common-mode noise and achieving better signal integrity in subsequent stages.
  - **Gain improvement**: This stage significantly boosts the signal gain to meet the transimpedance gain requirement (>150 kΩ).
  - **Noise suppression**: Differential operation inherently reduces noise susceptibility, particularly for high-frequency noise sources.
- **Expected outcome**: Stage 2 prepares a balanced differential signal with sufficient gain, ensuring compatibility with the following stages while maintaining low noise.

Ideally, the differential stage will provide sufficient gain to boost the overall gain reaches the requirement. However, due to the limitations of Vdd level and Vth of NMOS, the gain (Av=gmRout) cannot provide sufficient gain to meet the requirements. Therefore, the following stages are necessary to boost the gain and output swing to reach the desired level.

The figure below shows the schematic of the designed differential amplifier.

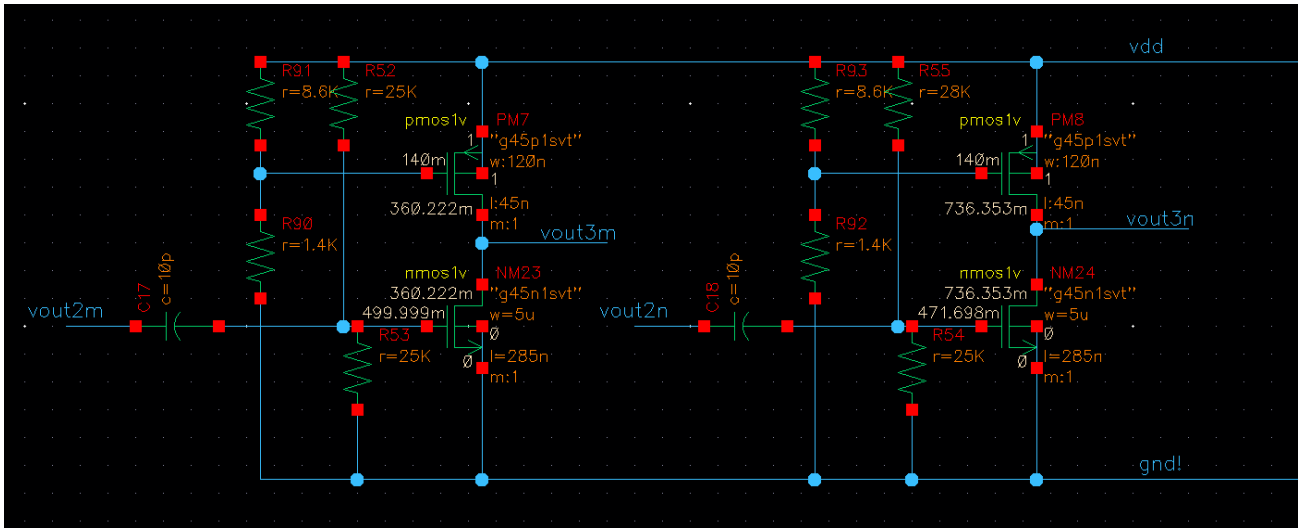


4. Stage 3: Multi-stage Common Source Amplifiers

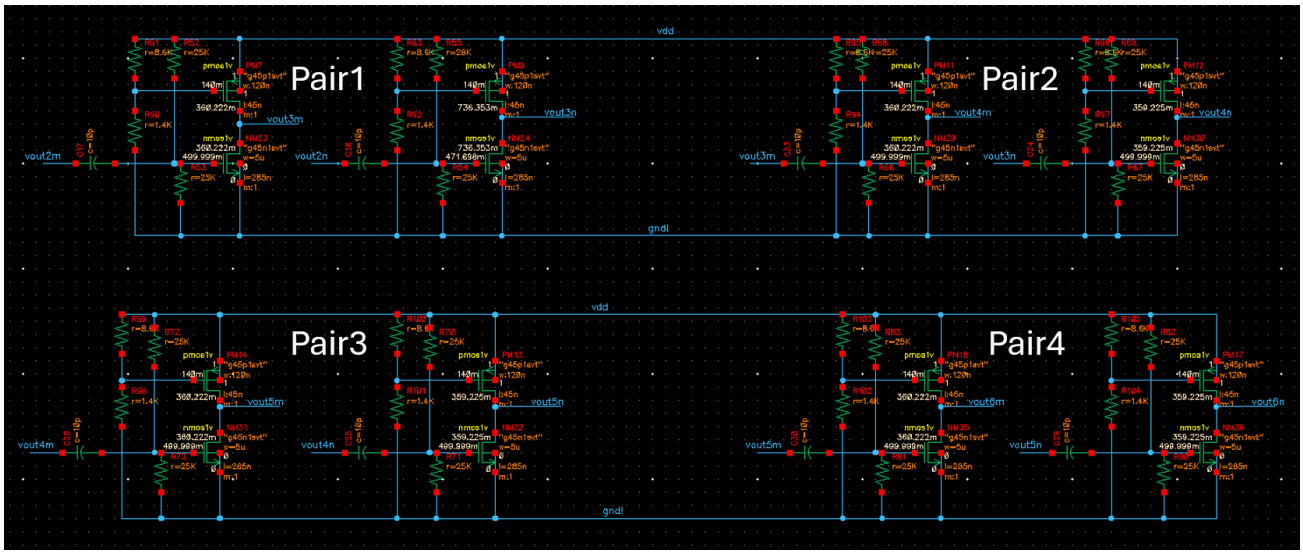
- **Architecture**: Stage 3 consists of **four pairs (eight total)** of **common source (CS) amplifiers** in a cascaded configuration. Each pair's output serves as the input for the next pair to accumulate the gain of each stage and serve the final output gain.
- **Rationale**:
  - **High gain**: Each CS amplifier pair contributes a portion of the required gain, and the cascaded design ensures that the combined gain is sufficient to meet the output swing specification of >0.4V while maintaining linearity.
  - **Wide output swing**: The CS topology supports large output voltage swings, enabling the amplifier to drive subsequent stages effectively.
  - **Power efficiency**: By carefully biasing each CS amplifier and optimizing device sizing, the design achieves high amplification without exceeding the 15mW total power budget.
- **Expected outcome**: After four stages of CS amplification, the differential signals are significantly amplified with sufficient gain, band width and output swing for final buffering and output loading.

Below diagram is one pair of the designed CS amplifier, the left side is the positive signal from differential amplifier vout()m and the right side is the negative signal from differential amplifier vout()n.

Amplification of both side is independent to each other to avoid signal distortion.



Below figure is the overview of four pairs of the common source amplifiers.

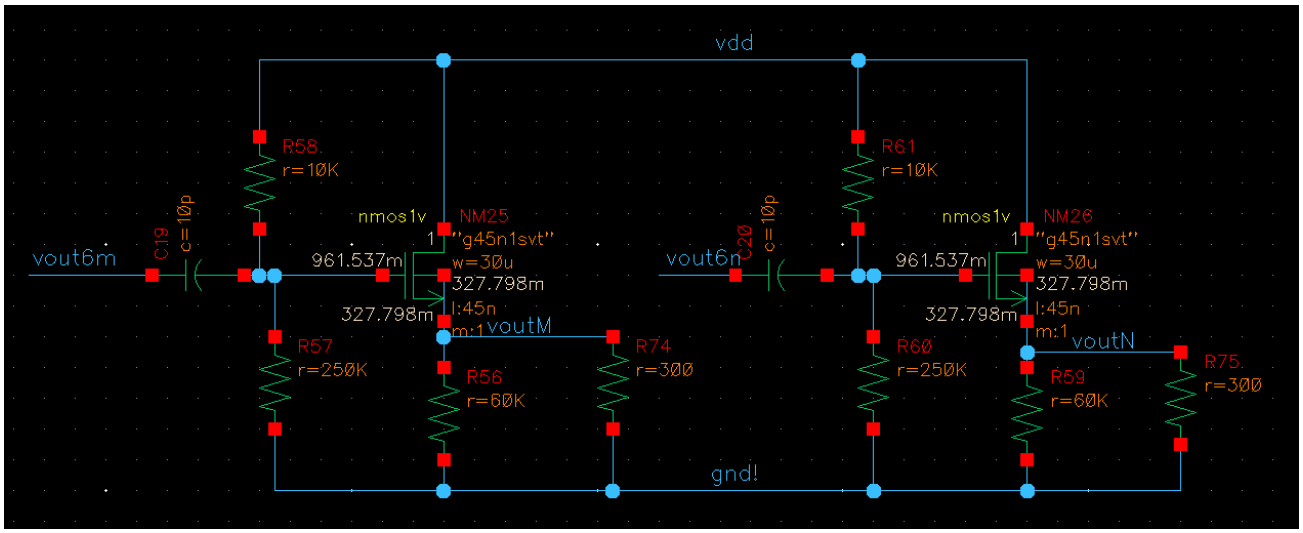


5. Stage 4: Common Drain Amplifiers (Buffer Stage)

- **Architecture**: Two **common drain (CD) amplifiers**, also known as source followers, are used as buffers.
- **Rationale**:
  - **Impedance matching**: The CD amplifiers provide **low output impedance**, which is necessary to drive the 300Ω load resistances directly without significant signal loss or distortion.
  - **Signal integrity**: The buffer stage prevents loading effects on the preceding CS amplifiers, preserving the gain and signal swing achieved in stage 3.
  - **Power considerations**: CD amplifiers consume minimal additional power while providing the necessary impedance transformation and signal stability.

- **Expected outcome**: The buffer ensures that the TIA can drive the load effectively while maintaining the output swing and minimizing distortion.

The output of this pair of buffers directly connected to a differential load (each side 300 Ohms), therefore the differential outputs of the designed TIA can be measured by voutM-voutN.



Power Consumption Optimization

Throughout the design:

- The use of current mirrors and cascaded stages minimizes static power dissipation.
- Each stage is designed to balance performance and efficiency, keeping total power consumption within the 15mW limit.

Summary

This multi-stage architecture effectively meets all design specifications:

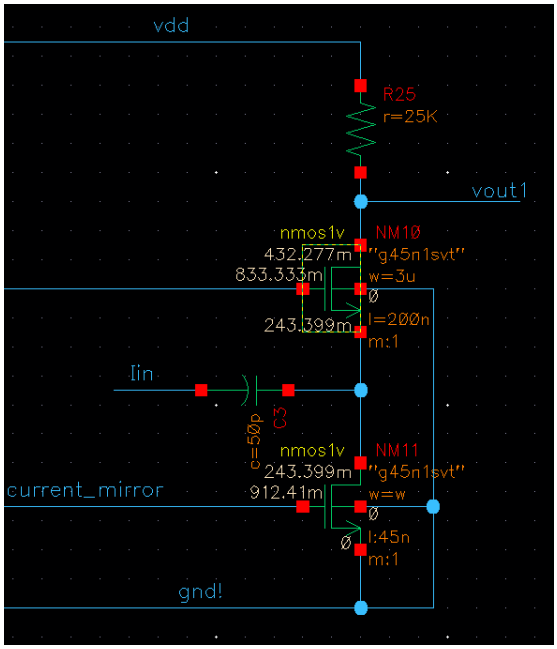
- **Lower corner frequency**: The coupling and amplifier configurations ensure a low-frequency cutoff below 10 MHz.
- **Upper corner frequency**: The CG amplifier in stage 1 enables a high-frequency response exceeding 250 MHz.
- **Gain**: The combined stages achieve a transimpedance gain of >150 kΩ.
- **Output swing**: The CS and CD stages ensure an output swing of >0.4V with minimal distortion.
- **Power consumption**: Power-efficient designs in each stage keep the total consumption below 15 mW.

This design strategy leverages proven circuit topologies and design techniques to achieve robust, efficient, and high-performance TIA operation.

IV. Hand Calculation

1. Gain Calculation

Stage1: Common Gate stage circuit:



The gain of CG amplifier is determined by the equation:

$$A_V = g_m R_{out}$$

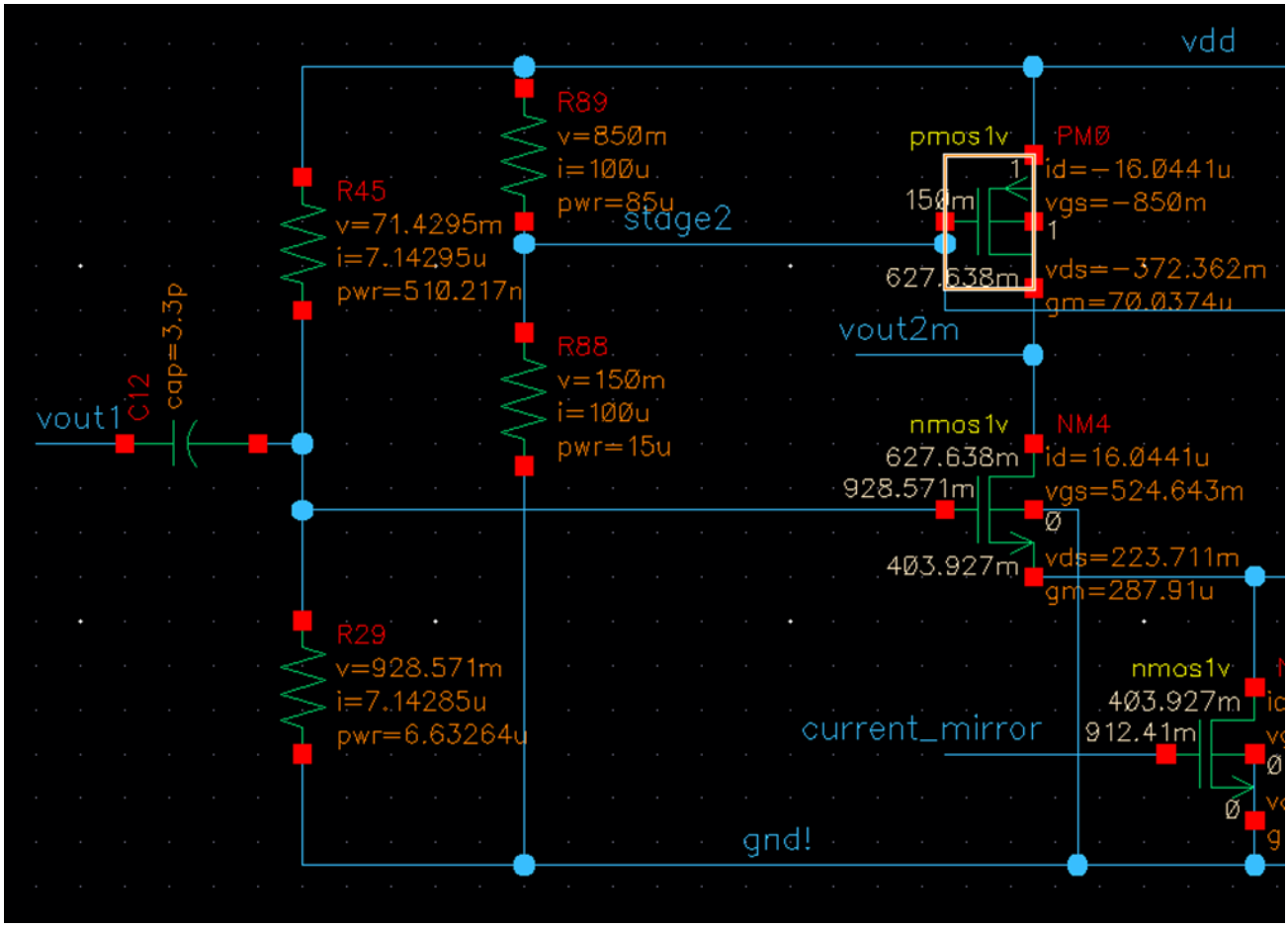
$$R_{out} \cong R_{25} = 25k\Omega$$

$$V_{out} = I_{in} R_{25}$$

$$A_V = \frac{V_{out}}{I_{in}} = R_{25} = 25K = 87.96dB$$

When the CG amplifier connects to the next stage, the Rout will be reduced as it has other resistors connected to them in parallel. The gain will be reduced.

Stage2: Differential Amplifier



$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} = \sqrt{2 * 157.2 * \frac{120}{45} * 16} = 115.8uA/V$$

$$r_{0p} = \frac{1}{\lambda I_d} = \frac{1}{\frac{105}{45} * 16.044uA} = 26.78k\ Ohm$$

The Rout will need to consider the bias resistor in the next cs amplifier circuit:

$$R_{out} = r_{0p}||R_{bis} = 26.78||12.25 = 8.4k\ Ohm$$

$$A_V = g_m R_{out} = 0.97$$

Stage3: Common Source Amplifier

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} = \sqrt{2 * 157.2 * \frac{5}{0.285} * 19.43} = 327.37uA/V$$

$$r_{0p} = \frac{1}{\lambda I_d} = \frac{1}{\frac{105}{45} * 19.43uA} = 22.06k\ Ohm$$

The Rout will need to consider the bias resistor in the next cs amplifier circuit:

$$R_{out} = r_{0p}||R_{bis} = 22.06||12.25 = 7.88k\ Ohm$$

$$A_V = g_m R_{out} = 2.57$$

There are three stage of CS have Av=2.57

The last stage of CS amp:

$$R_{out1} = r_{0p}||R_{bis} = 22.06||9.89 = 6.83k\ Ohm$$

$$A_{V1} = g_m R_{out1} = 2.236$$

Therefore, the gain of stage 3 is

$$A_{Vtotal} = 37.96$$

Stage4: Buffer

This is a source follower, ideally have a gain of 1. But usually smaller than 1.

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \sqrt{2 * 157.2 * \frac{30}{0.045} * 1.1} = 15mA/V$$

$$R_S = 60K\ Ohm$$

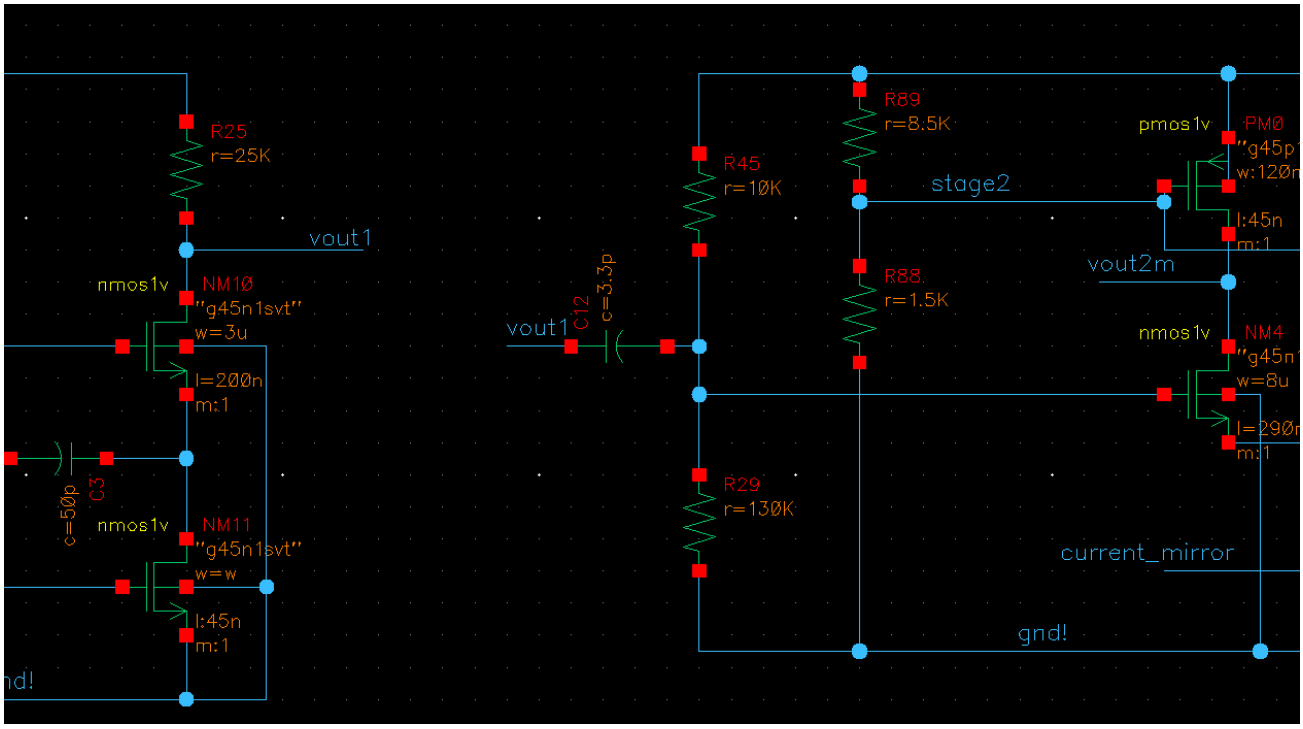
$$A_V = \frac{g_m R_S}{1 + (g_m + g_{mb}) R_S} = 0.8$$

Therefore, the total gain is:

$$A_V = 25K * 0.97 * 37.96 * 0.8 = 736.424K\ Ohm = 117.34dB$$

2. BandWidth

The below figure shows an RC circuit that causes the lower corner frequency.



In this stage, the capacitor C12, Cgd of NM10, Cgs of NM4 have been connected in serial, therefore, the total capacitance could be calculated:

$$C_{gd} = WL_{ov}C_{ox} = 3um \times \frac{200}{45} \times 0.152fF/um = 2.027fF$$

$$C_{gs} = \frac{2}{3}WLC_{ox} + WL_{ov}C_{ox} = 27.5 + 1.216 = 96fF$$

$$C_{gd}||C_{gs}||C_{12} \cong 0.2fF$$

$$R \cong 25k\ Ohm$$

The frequency of bandwidth could be calculated by:

$$f_d = \frac{1}{2\pi R(C_{gd}||C_{gs}||C_{12})} = \mathbf{3.18 \times 10^{10}}Hz$$

3. Noise Calculation

The input refer noise level could be calculated by the following equation:

$$\overline{I_{n,in}^2} = 4KT\left(\gamma g_m + \frac{1}{R_D}\right)$$

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} = \sqrt{2 * 157.2 * \frac{3}{0.2} * 22.71} = 327.26uA/V$$

Therefore:

$$\overline{I_{n,in}^2} = 4KT\left(\gamma g_m + \frac{1}{R_D}\right) = 4 * 1.38 * 10^{-23}\left(\frac{2}{3} * 327.26 * 10^{-6} + \frac{1}{25000}\right) = 1.425 * 10^{-26}$$

$$\overline{I_{n,in}} = 1.194 \times 10^{-13} A/HZ$$

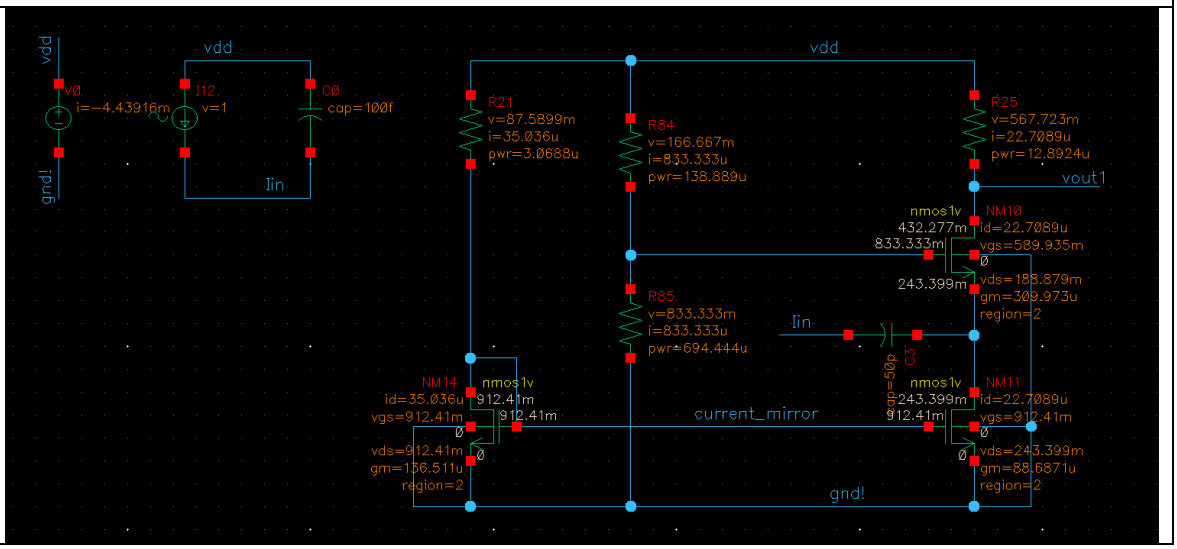
V. Cadence Simulation Results

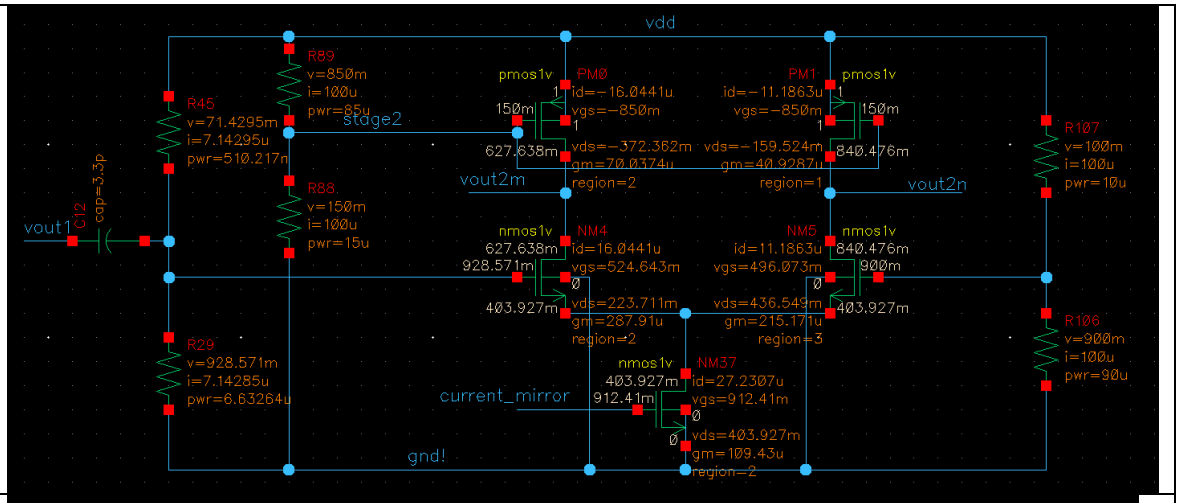
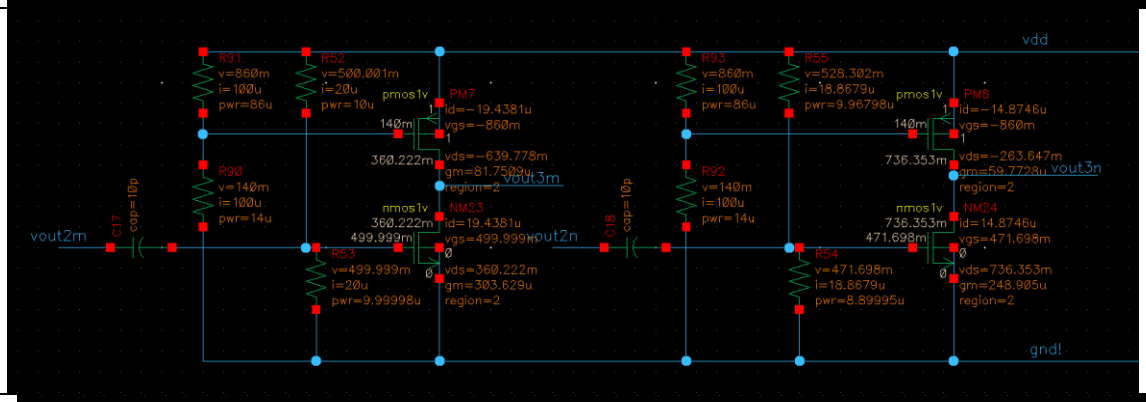
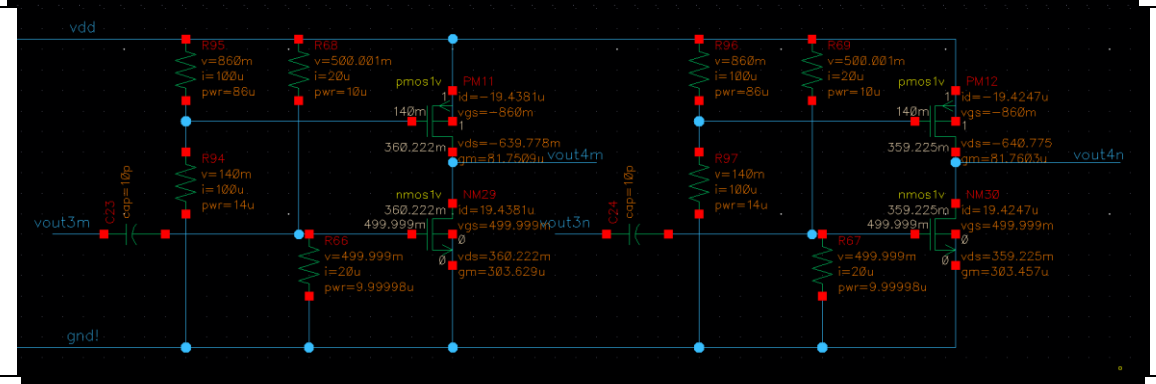
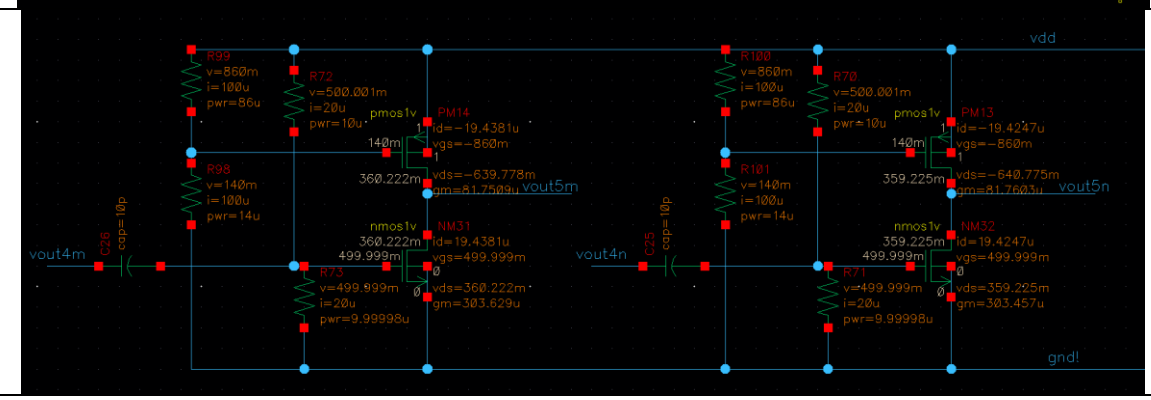
1. DC Operating Point Summary Table

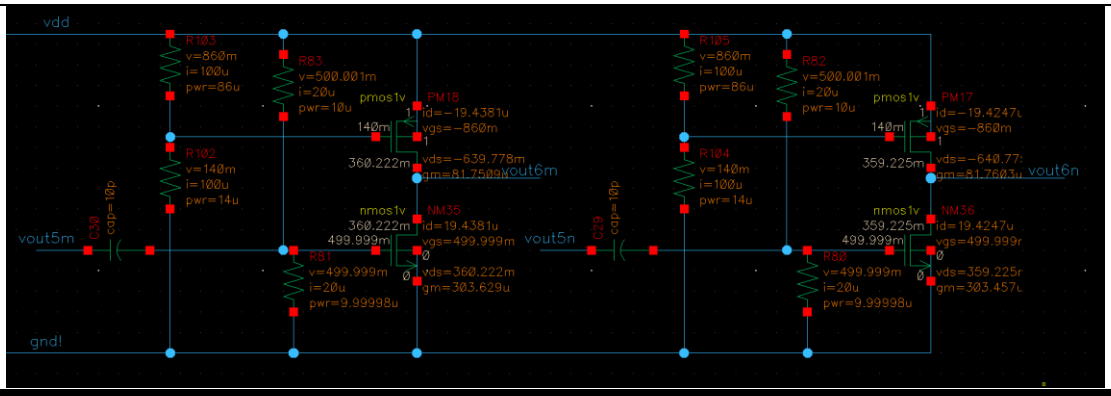
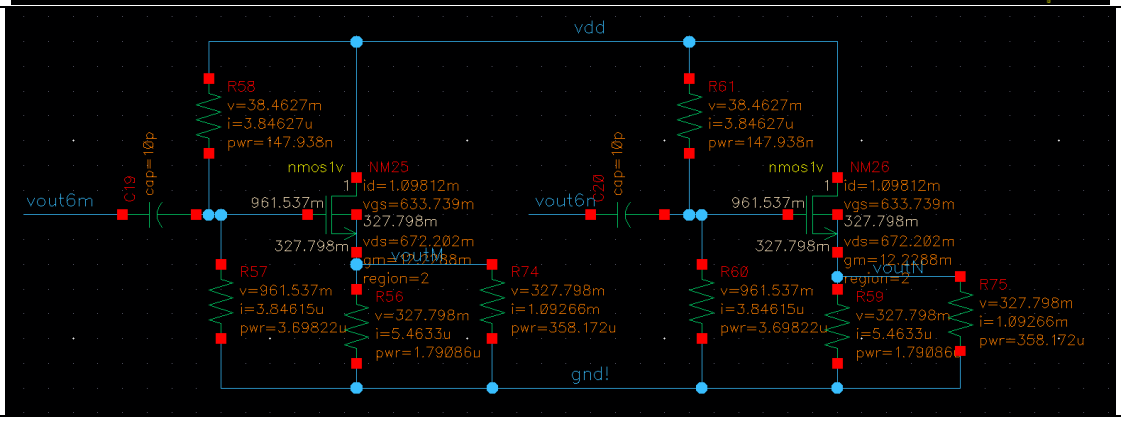
The DC operating point analysis provides insights into the steady-state conditions of the circuit. The following key parameters are included:

- Drain currents for all stages and total power consumption to confirm compliance with the <15 mW design requirement.
- Verification of transistor operating regions to ensure all MOSFETs operate in the saturation region (e.g., checking Vgs, Vds, and Id).
- Gm of each transistor.

This table summarizes the static operating conditions, which are essential for ensuring proper circuit operation before dynamic simulations.

Partial Name	DC Operating Point
Stage1 and Input Current Source	

Stage2 (differential Amplifier)	
Stage3 Pair1	
Stage3 Pair2	
Stage3 Pair3	

Stage3 Pair4	
Stage4 and Output	

2. AC Simulation

In AC simulation, the final output gain is calculated by following equation:

$$A_V = \frac{voutM - voutN}{Iin}$$

Where voutM is for the differential positive output signal, voutN is for the differential negative output signal. Iin is the input current signal.

The AC simulation evaluates the frequency response of the circuit. The following results are provided:

- **Gain-frequency response**: A plot illustrating the gain (dB20) versus frequency, with clear indications of the -3dB lower and upper corner frequencies. The design requirements of smaller than 10MHz for the lower corner and larger than 250MHz for the upper corner frequency are validated.
- **Trans-impedance gain**: The differential gain is 107.93dB, which is 336282 Ohms. This exceed 150K Ohm, meeting the specification.
- **Phase response** (optional): A phase plot is included to assess stability and phase characteristics across the frequency range.

These results confirm the bandwidth and gain performance of the circuit, ensuring compliance with design requirements.

According to the figure below, the designed -3dB BandWidth is **487.058KHz** to **282.064MHz**.

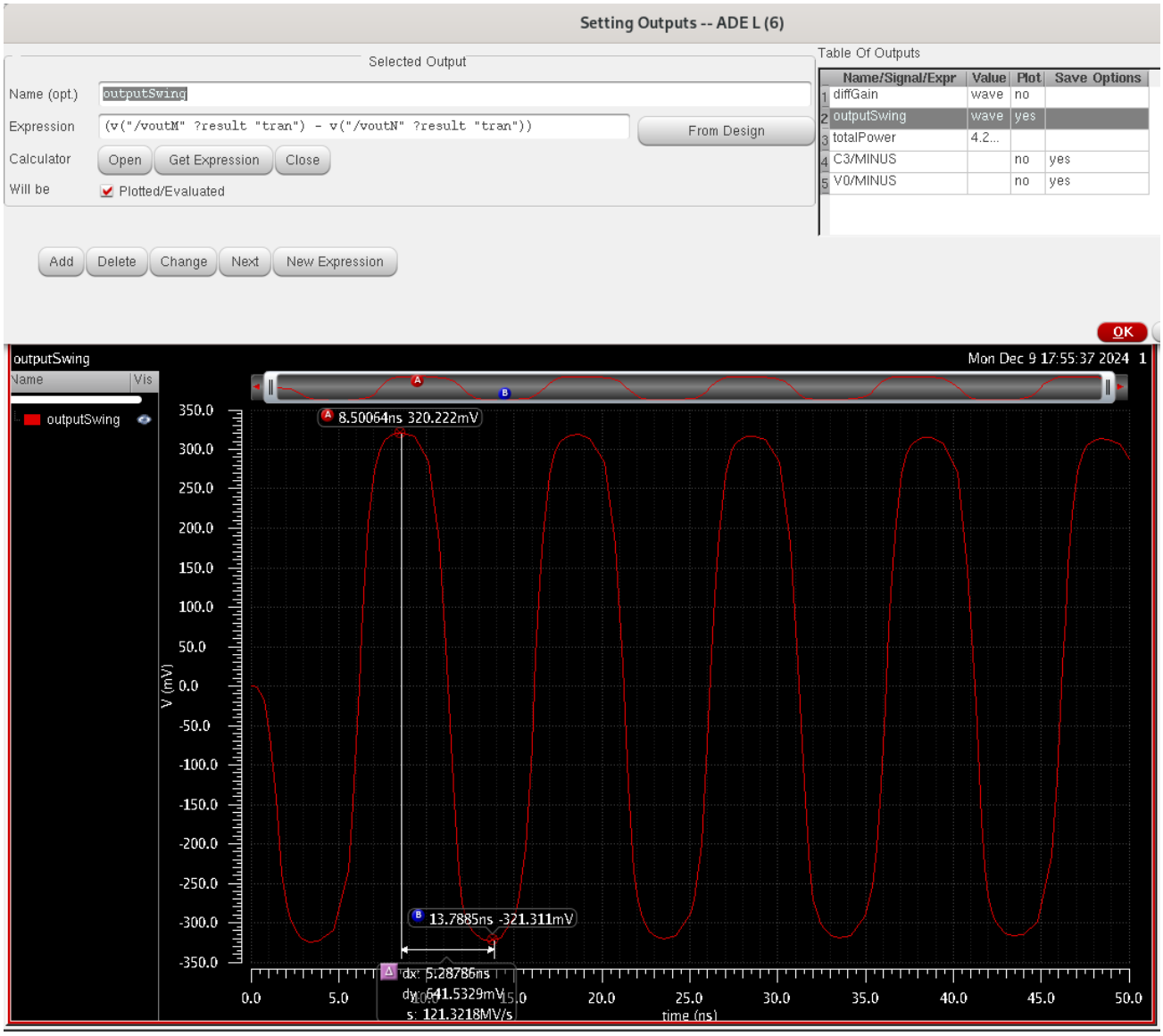
3. Transient Simulation

The transient analysis demonstrates the circuit's time-domain behavior and dynamic performance. The following aspect have evaluated:

- **Output swing**: The peak-to-peak differential output voltage is measured at 641mV, confirming it exceeds the 0.4 V requirement.

This analysis provides evidence of the circuit's ability to handle dynamic inputs and generate stable outputs.

The results have shown in the figure below, outputSwing signal is generated by the differential positive input (voutM) minus the differential negative input (voutN). The result indicating a correct behaviour of output signal and a large enough output swing of the designed TIA.



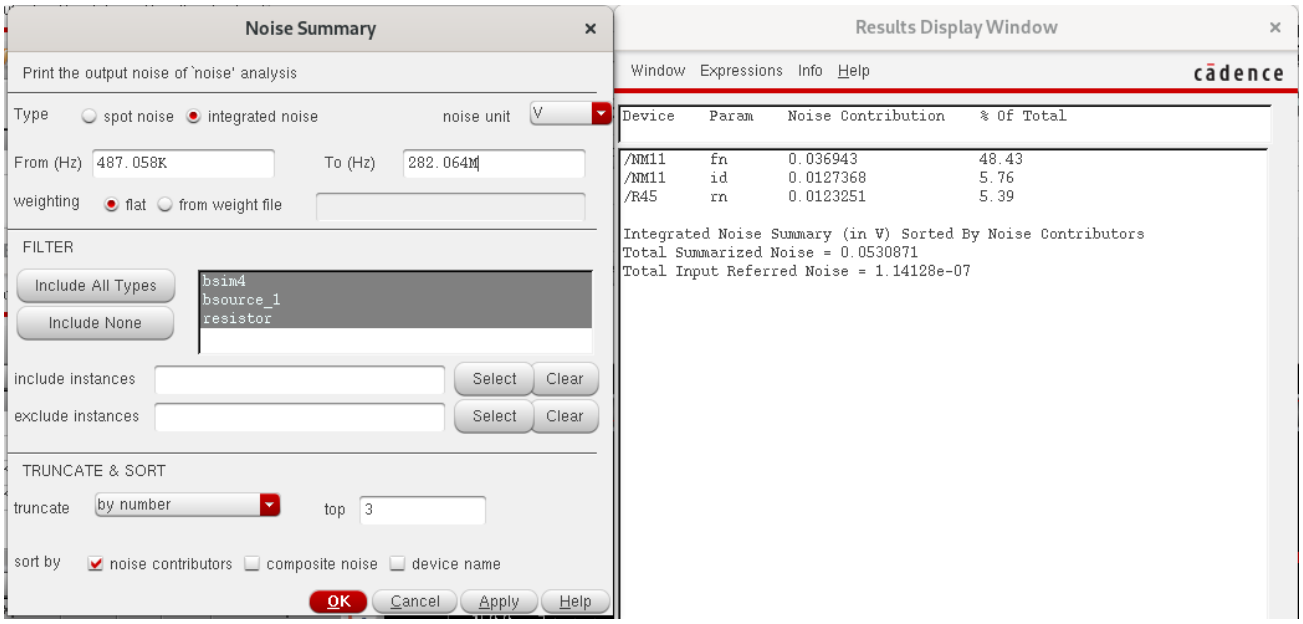
4. Noise Simulation

Noise analysis quantifies the impact of noise sources on circuit performance. Results include:

- **Input-referred noise current density**: The integrated noise over the -3dB bandwidth is calculated, the result is 114.128nA RMS, which confirm it is less than 125 nA RMS.
- **Noise contributions**: Individual noise sources that generating dominated noises are identified, and their contributions to the total noise are quantified.
- **Overall noise performance**: The results demonstrate that the design achieves low noise levels critical for high-sensitivity applications.

This section highlights the low-noise performance of the circuit, ensuring its ability to drive high impedance load.

The noise simulation setup and results display have shown in figure below. The largest input noise source is the NMOS: NM11 at the first stage.

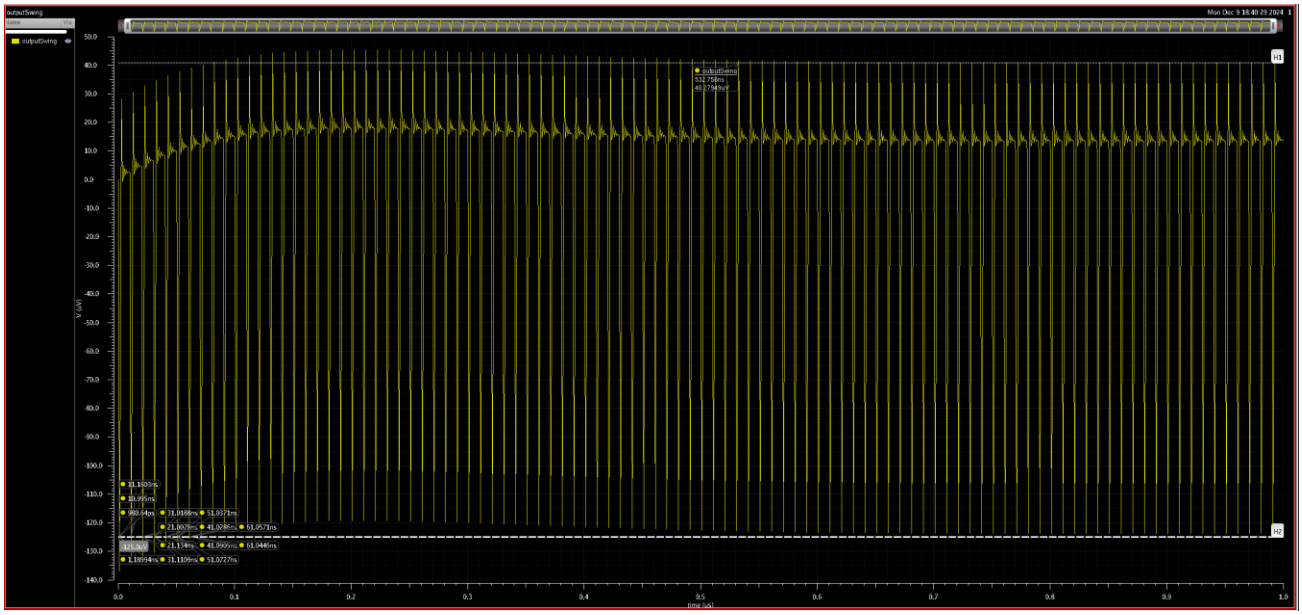


5. Evidence of Stable Operation

To verify the stability of the circuit, the following analysis have conducted:

- **Step response**: Stability under dynamic conditions is verified by observing the output during rapid input changes(use isource), ensuring no oscillatory behavior or ringing.

This evidence demonstrates that the design is robust and maintains stability under all operating conditions.

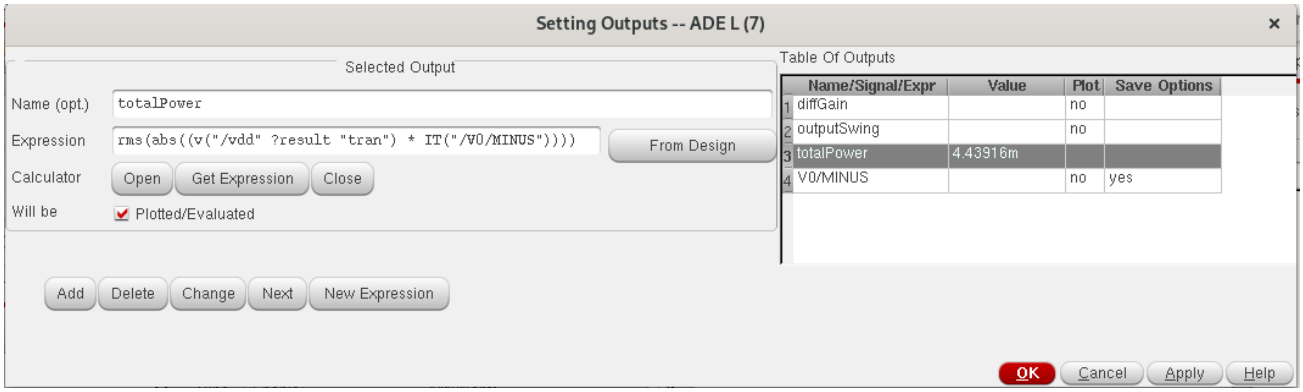


6. Total Power Simulation Result:

The total power consumption could be calculated by the following equation:

$$P = V_{dd} \times I_{Dtotal}$$

The simulation result has been recorded below:



Total power is 4.44mW which is less than the limited 15mW.

7. Table of Performance

No.	Parameter	Required Value	Designed Value

1	Technology node (minimum channel length)	45nm (CMOS)	45nm
2	Vdd	1V	1V
3	Cp	100f	100f
4	Load resistance	600Ω (differential)	300Ω each side
5	Input current amplitude	2.67μA peak-to-peak	2.67μA peak-to-peak
6	Required output peak-to-peak voltage swing	>0.4V (differential)	**0.61V**
7	Trans-impedance gain	>150kΩ (differential)	**336282Ω (107.93dB)**
8	The -3dB upper corner frequency	>250MHz	**487.058KHz**
9	The -3dB low corner frequency	<10MHz	**282.064MHz**
10	Total input referred current noise (integrated over BW = −3dB)	<125nA rms	**114.128nA rms**
11	Largest capacitor available	50pF	50pF
12	Smallest capacitor available	10fF	10fF
13	Largest resistor available	250kΩ	250kΩ
14	Smallest resistor available	1Ω	1Ω
15	Total power consumption	<15mW	**4.44mW**

VI. Comparison of Hand Calculations and Simulations

1. Gain

The calculated result is:

$$A_V = 25K * 0.97 * 37.96 * 0.8 = 736.424K\ Ohm = \mathbf{117.34dB}$$

The gain calculated by hand is overestimated compared to simulation results (**107dB**) due to the following reasons:

- **Idealized Models**: Hand calculations typically assume ideal device behavior, ignoring second-order effects such as channel length modulation, body effect, and mobility degradation. These effects reduce the actual gain in simulations.
- **Neglecting Parasitic Effects**: Parasitic capacitances (Cgd, Cgs) and resistances introduce loading effects and reduce gain, especially in high-frequency regions, but are not included in manual calculations.
- **Interstage Loading**: In a multi-stage amplifier, the loading effect between stages lowers the overall gain. Hand calculations often treat each stage independently, leading to overestimation.
- **Non-Idealities in Current Mirrors**: Current mirrors in the load are assumed ideal in hand calculations, with infinite impedance. Simulations account for their finite output impedance, reducing the effective gain.

2. Band Width

The calculated result is:

$$f_d = \frac{1}{2\pi R(C_{gd}||C_{gs}||C_{12})} = \mathbf{3.18 \times 10^{10}} Hz$$

The calculated bandwidth tends to overestimate the actual bandwidth observed in simulation (**282.064MHz**) due to the following reasons:

- **Simplified Assumptions:**
  In hand calculations, idealized models are typically used, assuming perfect devices with no parasitics or non-idealities. For example, MOSFETs are often modeled with simplified small-signal parameters, and parasitic capacitances are often ignored. However, in simulation, these parasitics are included, leading to additional poles and a reduction in the overall bandwidth.
- **Parasitic Capacitances:**
  The simulation accounts for parasitic capacitances, including Cgs , Cgd, and layout-induced

parasitics, which effectively increase the total load capacitance seen by each stage. This results in a lower -3dB frequency compared to the hand-calculated value.

- **Interstage Coupling Effects:**
  In a multi-stage amplifier, the interactions between stages can create additional poles and zeros, which are often neglected in hand calculations. These interstage effects can significantly impact the actual bandwidth.
- **Second-Order Effects in MOSFET Models:**
  Hand calculations may ignore second-order effects such as channel length modulation, body effect, or velocity saturation, all of which can reduce the gain-bandwidth product and result in a narrower bandwidth.

3. Noise

Calculated result:

$$\overline{I_{n,in}} = \mathbf{1.194} * \mathbf{10^{-13}} A/HZ$$

The calculated noise is much less than the simulated result (**114nA/Hz**) due to the following reasons:

- **Incomplete Noise Models:**
  In hand calculations, only the dominant noise sources are often considered, while secondary contributors are ignored. Simulation tools, on the other hand, include all noise sources based on comprehensive device models.
- **Neglecting Parasitic Contributions:**
  Noise from parasitic elements is not considered in hand calculations, but it is inherently included in simulations.
- **Bias-Dependent Noise Effects:**
  The noise performance of MOSFETs is highly dependent on their biasing conditions. In hand calculations, fixed approximations of parameters like gm or Ro are used, which may not accurately reflect the actual operating point set in the circuit. Simulations use precise bias-dependent models, leading to more accurate noise predictions.
- **Non-Idealities in Current Mirrors:**
  In the hand calculations, the current mirror is often assumed to be ideal, with no additional noise contribution. In simulations, the finite output impedance of the current mirror and the associated noise are included, contributing to higher input-referred noise.
- **Not all Stages Considered in Hand Calcualtion:**
  In the hand calculations, the subsequent noise of the system is neglected as they are very small compared to the first stage.

VII. Conclusion

Summary of Design and Achievements

This project focused on designing a wideband transimpedance amplifier (TIA) to meet the following stringent requirements:

- A transimpedance gain of >150 kΩ.
- A -3dB bandwidth ranging from <10 MHz (lower corner) to >250 MHz (upper corner).
- A differential output swing >0.4 V.
- Input-refer noise level <125nA/Hz.
- Total power consumption <15 mW.

The proposed design, implemented using a 45 nm CMOS process, successfully achieved these specifications through a multi-stage architecture comprising:

1. A common gate amplifier for wide bandwidth and low input impedance.
2. A differential amplifier for noise suppression and gain improvement.
3. Four cascaded pairs of common source amplifiers for high gain and wide output swing.
4. Common drain amplifiers (buffers) for impedance matching and stable load driving.

Simulation results confirmed that the TIA meets or exceeds the design specifications, achieving a transimpedance gain of 336.3kΩ, an output swing of 0.61V, and a power consumption of 4.44mW.

Reflection and Challenges

While the design met its objectives, several challenges were encountered during the process:

- **Noise Performance**: The input-referred noise was higher than initially calculated due to contributions from the current mirror and parasitic elements in the common gate amplifier. Simulations revealed the dominant role of the NMOS load in the first stage.
- **Gain Discrepancies**: Hand calculations overestimated the overall gain by approximately 10 dB, highlighting the impact of parasitic effects, interstage loading, and non-idealities not accounted for in theoretical models.
- **Bandwidth Reduction**: The simulated bandwidth was narrower than the calculated value, primarily due to second-order effects and layout-induced parasitics that were neglected in initial approximations.

Opportunities for Improvement

To further enhance the design, the following improvements can be considered:

1. **Reducing Noise**:

    - Increase the channel length of the NMOS load in the current mirror to reduce thermal noise.
    - Add cascode transistors in the current mirror to increase output impedance and suppress noise.
    - Implement input filtering to reduce noise coupling from external sources.
2. **Optimizing Gain**:
    - Incorporate local feedback within the common source stages to stabilize and boost gain.
    - Revisit device sizing to balance gain, bandwidth, and power consumption more effectively.
3. **Improving Bandwidth**:
    - Introduce inductive peaking or resistive feedback to extend the upper corner frequency.
    - Minimize layout parasitics through careful routing and floorplanning.
4. **Power Efficiency**:
    - Explore alternative biasing techniques, such as self-biasing, to reduce static power dissipation.

Alternative Approaches for TIA Design

Beyond the current design, other architectures could be explored to achieve similar or better performance:

- **Resistive Shunt-Feedback Topology**: Simple and effective for wideband applications, though potentially noisier than the current design.
- **Capacitive Feedback Amplifiers**: Suitable for reducing input-referred noise in high-speed systems, particularly for OTDR applications.
- **Current Mode TIAs**: These designs use current-mode techniques to reduce voltage swing limitations, offering high speed and linearity.
- **Fully Differential Designs**: Improved noise immunity and linearity could be achieved by redesigning the entire circuit in a fully differential manner.

Conclusion

This project demonstrates the successful design of a high-performance TIA using a 45 nm CMOS process, with robust simulation results validating its compliance with the given specifications. Through this process, valuable insights into noise, gain, and bandwidth optimization were gained, which can guide future iterations of the design. Further exploration of advanced topologies and refinements in circuit design and layout could lead to even better performance, particularly for applications requiring ultra-wide bandwidth and low noise.

VIII. References

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