EE 443
Computer Engineering Analysis and Design Laboratory

Lab 0
1/20/2015

Prepared by: Shane Tachick

Lab Participation

Provide the percent participation in lab by each lab partner (if you feel each partner did equal work, enter 50% for each partner):

Lab member name	Percent participation
Shane Tachick	

Does your solution work the way it's supposed to work? YES

[1] If your answer is NO, please explain in your report.

Instructor/TA comments and grading

Objective and Background

In this lab we designed a quartus project that took a 4 bit binary input and used a 7 segment display to output its corresponding hex symbol (0 through F). The purpose of this lab was to refamiliarise ourselves with quartus. This lab is addressing the prerequisite portion of the class and making sure we remember how to code in VHDL and use quartus to program a board.

Equipment

Hardware: Computer, Altera Cyclone II FPGA board.
Software: Quartus II 9.1 service pack 2

Procedure

This lab began by programming an entity to convert a 4 bit binary number into the corresponding Hex symbol on a 7 segment display. Once properly coded it was converted in a symbol and the project was continued using the block diagram. Once the block diagram had the desired functionality the pins were mapped to the FPGA board and the final product was tested.

Results

The VHDL code was written properly and the block diagram was assembled properly, however I accidently saved the files in 2 different locations so Quartus threw a few errors when I tried the final compilation. Once this problem was sorted out the final project worked as expected.

Discussion and Questions

There were no discussion questions for this lab..

Conclusion

The point of this lab was to create a project using quartus that would be fit for an end of the semester EE 341 assignment in order to remind us how to use quartus and provide an assignment so that we can receive grading feedback.

Attachments

See attached.