IS2202 - Computer Systems Architecture
Caches and Software Optimization
Bonus assignment 1

April 2, 2014

Instructions

- The assignment should be solved *individually*.
- Solutions should be properly *motivated*, a few short sentences is usually enough.
- Answer the question in your own words. Copying answers from other sourses such as text books is not acceptable. You may qote other sources. In thtat case, make sure to include the source and say how you interpret the quoted text.
- Solutions should be given in English (as we have non-Swedish speaking TA:s).
- Solutions need to be handed in as PDF document *before the deadline* at the appropriate place on the course web (https://www.kth.se/social/course/IS2202).
- You need to core at least 20 points to qualify for a bonus point at the exam.

1 Cache design

You have all a Swedish national civic registration number (personnummer) of the form *YyMmDd-XXXX*. Use the following formulas to calculate the parameters of a cache in the next problems:

$$S = 32 \times 2^{d} \quad \text{(kilo bytes)} \tag{1}$$

$$L = 32 \times 2^{D} \quad \text{(bytes)} \tag{2}$$

$$A = 2 \times 2^{m \bmod 4} \quad \text{(number of ways)} \tag{3}$$

$$W = 16 \times 2^{y \bmod 4} \quad \text{(bits)} \tag{4}$$

1.1 Cache parameters, 5 points

1. Assume that you have a direct mapped cache of size S (Eq. 1) with the line size L (Eq. 2). The cache is physically indexed and tagged. The physical address is 50 bits, numbered from 0 to 49 (with 0 being the least significant bit). The machine has a word size of W bits (Eq. 4) and the memory is byte-addressable.

   (a) Write your personal values of the parameters S, L, A, and W (along with the parameters y, d, D, and m).

   (b) Make a schematic drawing of the cache.

   (c) Describe which bits are used to index the cache, i.e., used to select the row in the cache.

   (d) Which bits are compared with the address tag?

   (e) Which bits are used to select a word from the selected cache line?

1.2 Associative cache, 5 points

2. Now, assume that you have an A-way (Eq. 3) set associative cache of size S (Eq. 1) and cache line size L (Eq. 2).

   (a) Make a schematic drawing of the cache.

   (b) Describe which bits are used to index the cache, i.e., used to select the row in the cache.

   (c) Which bits are compared with the address tag?

   (d) Which bits are used to select the word to read from the selected cache line?

1.3 Replacement algorithms and other cache issues, 7 points

3. Describe how the *LRU* and *RANDOM* replacement policies work.

4. Why would a computer architect choose to implement:

   (a) *LRU* instead of *RANDOM*?

   (b) *RANDOM* instead of *LRU*?

5. Explain when the following miss ttypes occur and how they can be avoided:

   (a) *Compulsory* misses

   (b) *Capacity* misses

   (c) *Conflict* misses

2 Virtual memory, 8 points

6. Describe two reasons for implementing virtual memory.

7. Give at least one reason why a computer system with virtual memory should have a TLB.

8. What is the reach of a TLB with the page size 4 kB and 512 entries?

9. What is the benefit of using a *virtual indexed* and *physically tagged* cache? Are there any problems?

10. What is the benefit of using a *virtually indexed* and *virtually tagged* cache? Are there any problems?