Multi Core Architecture

Lab Assignment 1

SystemC Intro and L1 Cache

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Due date: 10 Nov 2014, Monday

Cache design:

Cache size: 32 x 1024 B
Block size: 32 B
Number of ways: 8

Number of sets = (cache size) / (Block size * No.of ways) = 128

Calculations from Address:

Parameter	Variable	Bits	Calculation	Comments
Given address	address	m31-m0		
Set Number	set_no	m11-m5	(address & 4064) >> 5	7 bits after the block offset
Tag Number	tag_no	m31-m12	(address & 4294963200U)>>12	20 bits after block offset and set number
Word	word_in_line	m4-m2	(address &28) >> 2	Most significant three bits in the block offset

Address

m31... m12	m11... m5	m4... m2	m1 m0
Tag	Set Number	Word	

pseudo LRU algorithm:

Present state							Replace	Next State						
b6	b5	b4	b3	b2	b1	b0		b6	b5	b4	b3	b2	b1	b0
x	x	x	0	x	0	0	Line_0	-	-	-	1	-	1	1
x	x	x	1	x	0	0	Line_1	-	-	-	0	-	1	1
x	x	0	x	x	1	0	Line_2	-	-	1	-	-	0	1
x	x	1	x	x	1	0	Line_3	-	-	0	-	-	0	1
x	0	x	x	0	x	1	Line_4	-	1	-	-	1	-	0
x	1	x	x	0	x	1	Line_5	-	0	-	-	1	-	0
0	x	x	x	1	x	1	Line_6	1	-	-	-	0	-	0
1	x	x	x	1	x	1	Line_7	0	-	-	-	0	-	0

Read operation:

Cache controller determines the line number of the given address. Then checks for the tag bit and subsequently the status bit. Read hit occurs when the tag number is matching and the data is valid. Otherwise its reported as read miss. The data has to be brought from memory.

Write operation:

Its almost the same way as reading from cache. Whenever the tag is not matching, it is

reported as write miss. Otherwise write hit counter increases its value by 1.

Results:

fft single processor

CPU	Reads	RHit	RMiss	Writes	WHit	WMiss	Hitrate
0	86298	7549	78749	43195	10882	32313	14.233202

dbg single processor

CPU	Reads	RHit	RMiss	Writes	WHit	Wmiss	Hitrate
0	40	19 21	60	26	34		45.000000

rnd single processor

CPU	Reads	RHit	RMiss	Writes	WHit	WMiss	Hitrate
0	33031	18659	14372	32505	18306	14199	56.404114