Reduction of Radar Processing Latency

01-June-2015 to 16-Dec-2015

Date: 21-Apr-2016

Master thesis presentation by
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Matrik #: 367975

Agenda

- Background
- Existing analysis by Airbus DS
- Testbed
- Implementation
- Summary & Conclusion

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Background

- Minimize SWaP, Cost – ARM Cortex A9

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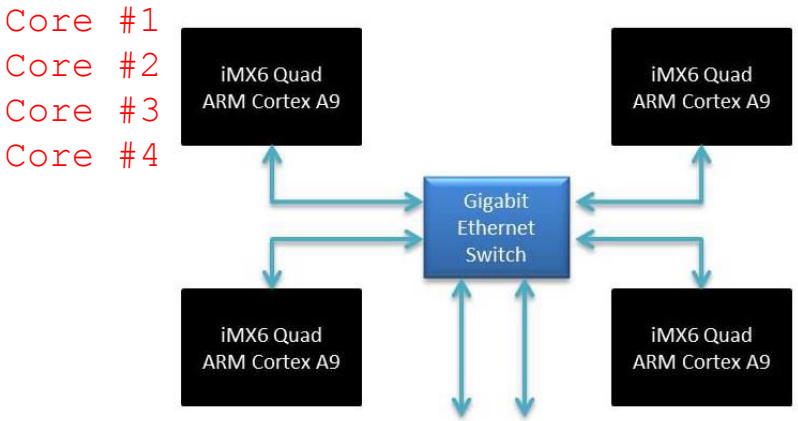
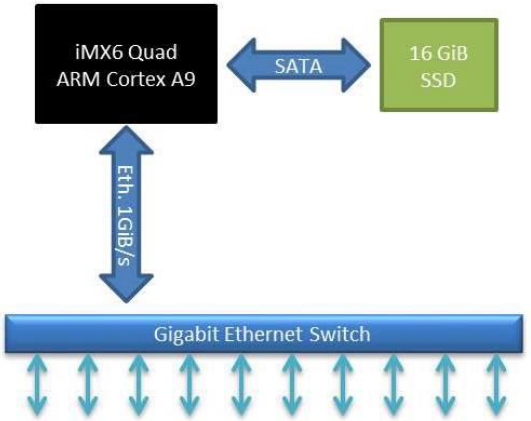
- Integrated Modular Avionics(IMA)



Data Graphics Processing Module (DGPM)



Platform Support Module (PSM)

Terminologies

- Pulse

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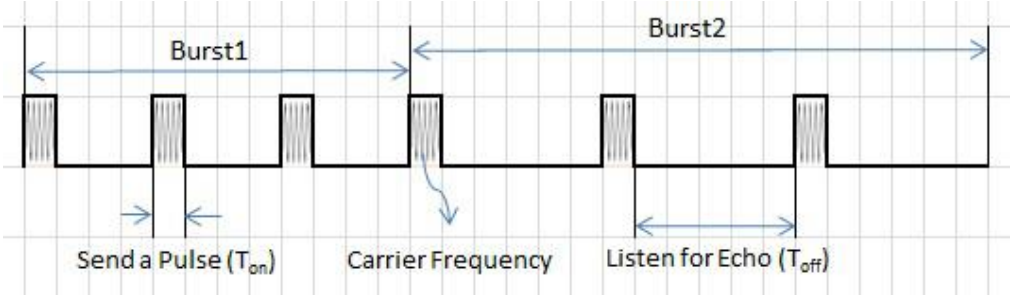
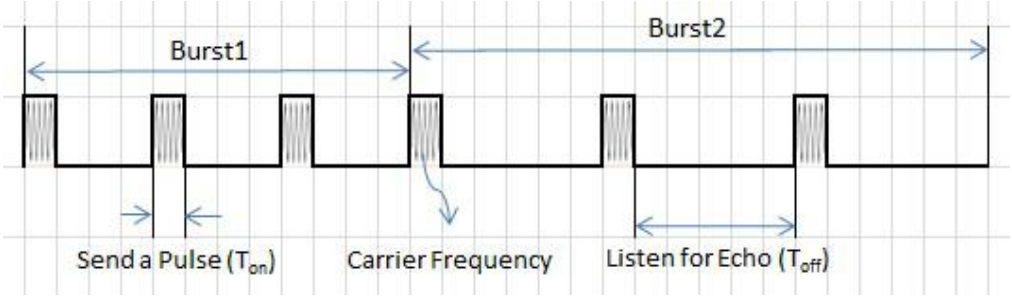
- Pulse
- Burst



Terminologies

- Pulse
- Burst



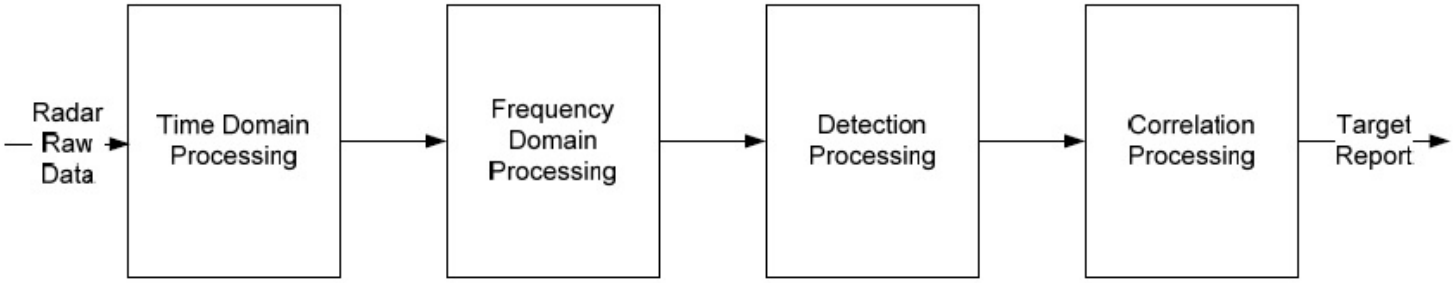
- Dwell

Requirements

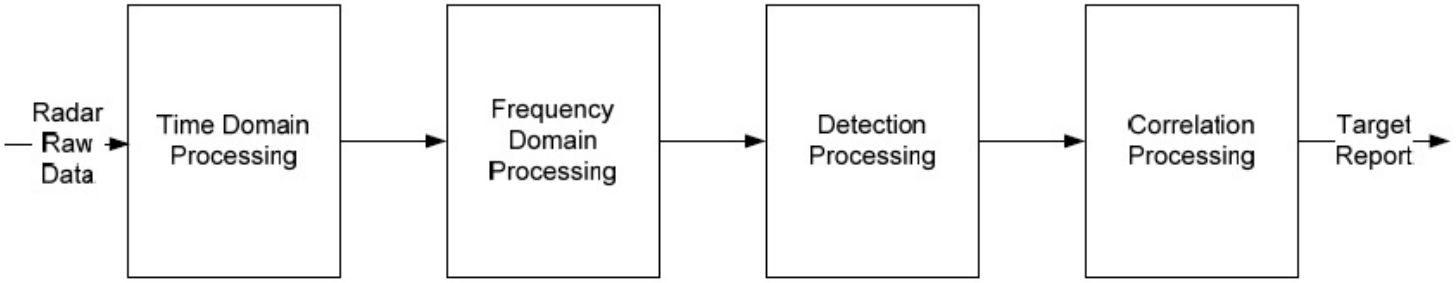
- 2x Dwell time latency

- 50% Utilization
  - CPU
  - Memory
  - Memory transfer band-width

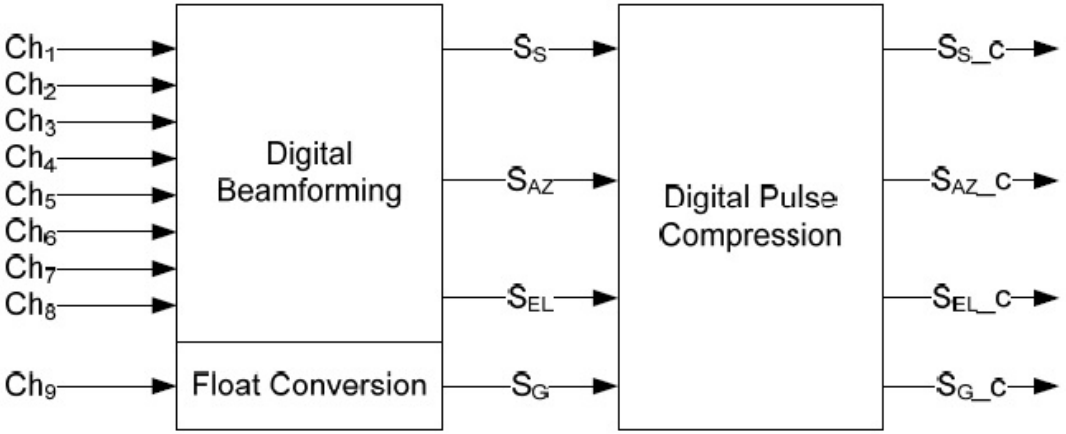
A/A Mode Processing Chain



A/A Mode Processing Chain

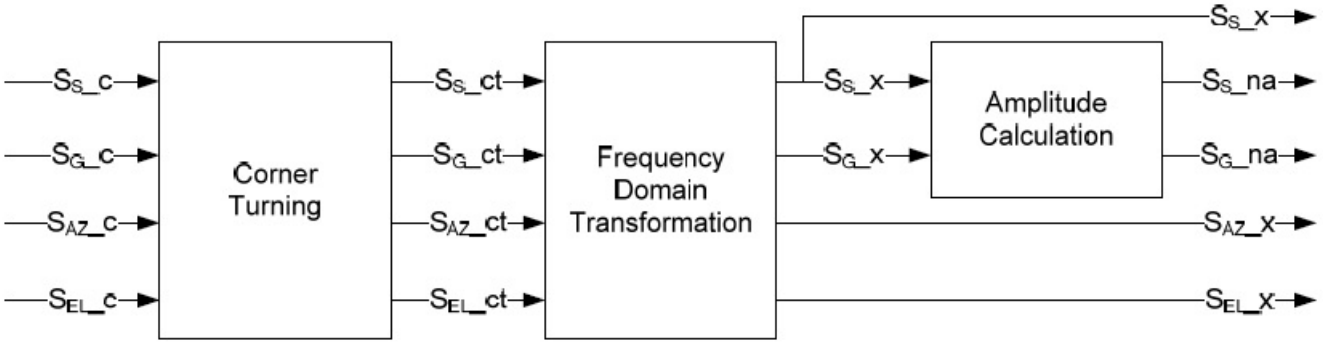


Time Domain Processing



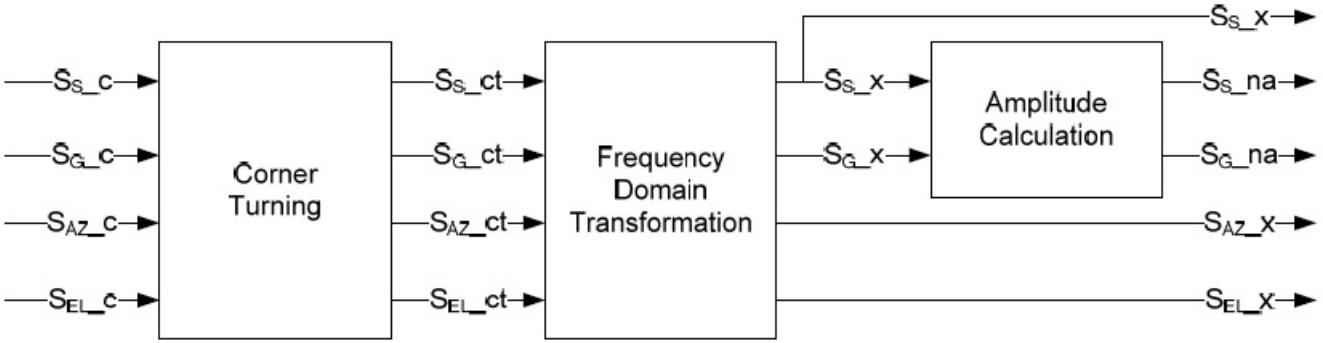
A/A Mode Processing Chain

Frequency Domain Processing

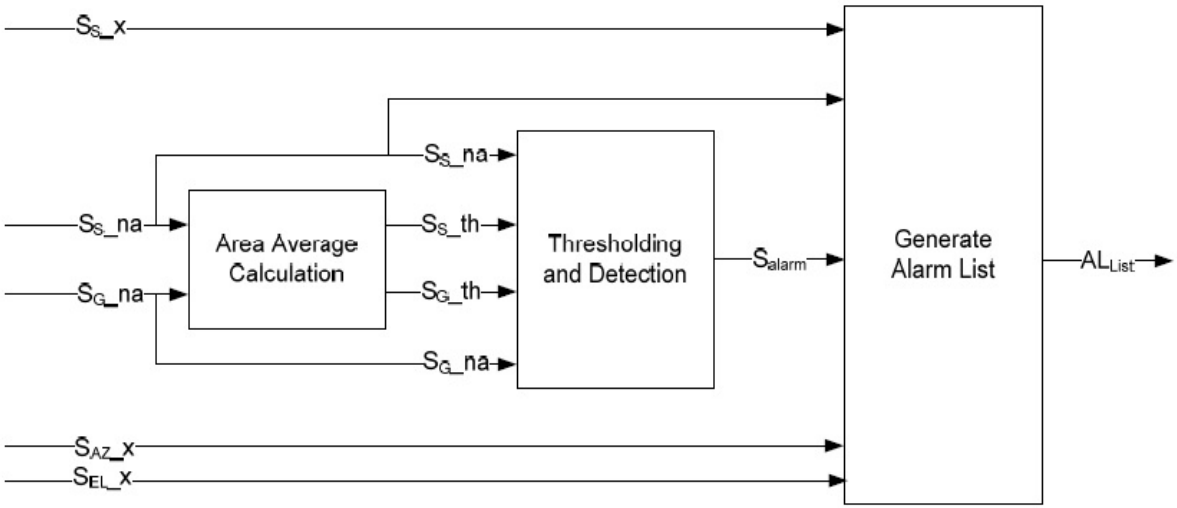


A/A Mode Processing Chain

Frequency Domain Processing

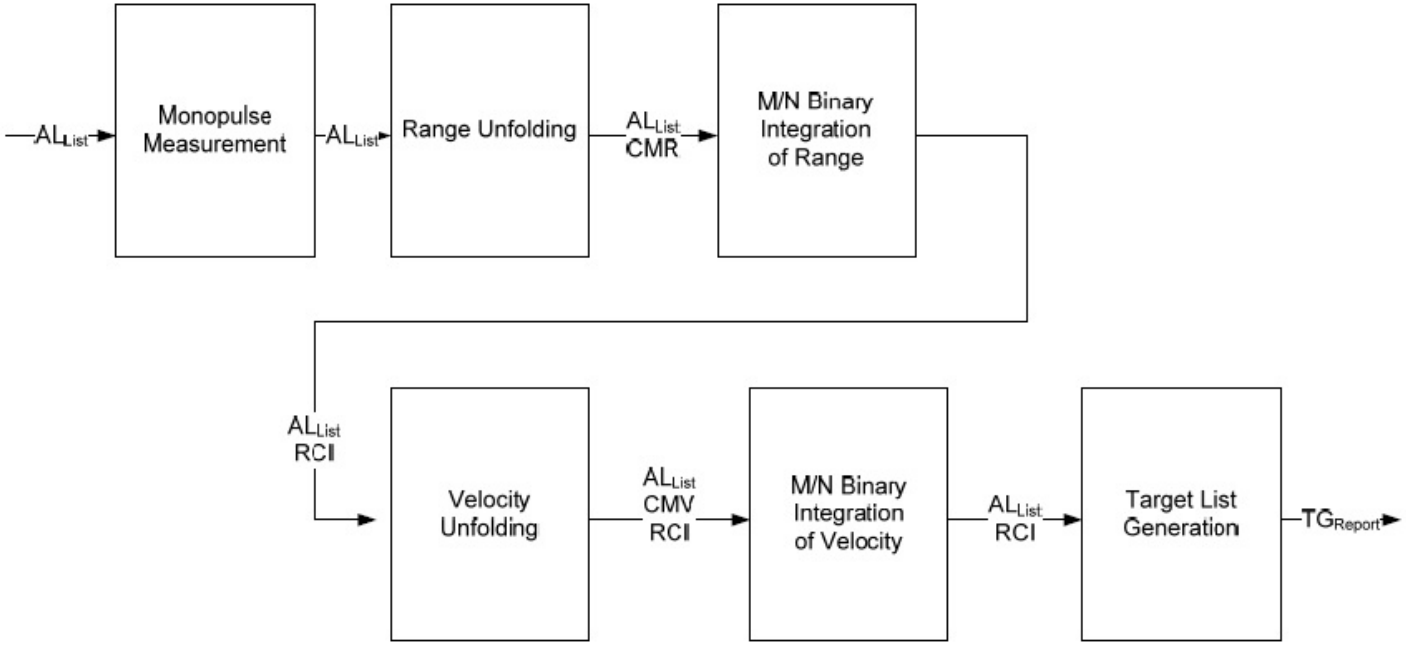


Detection Processing



A/A Mode Processing Chain

Correlation Processing



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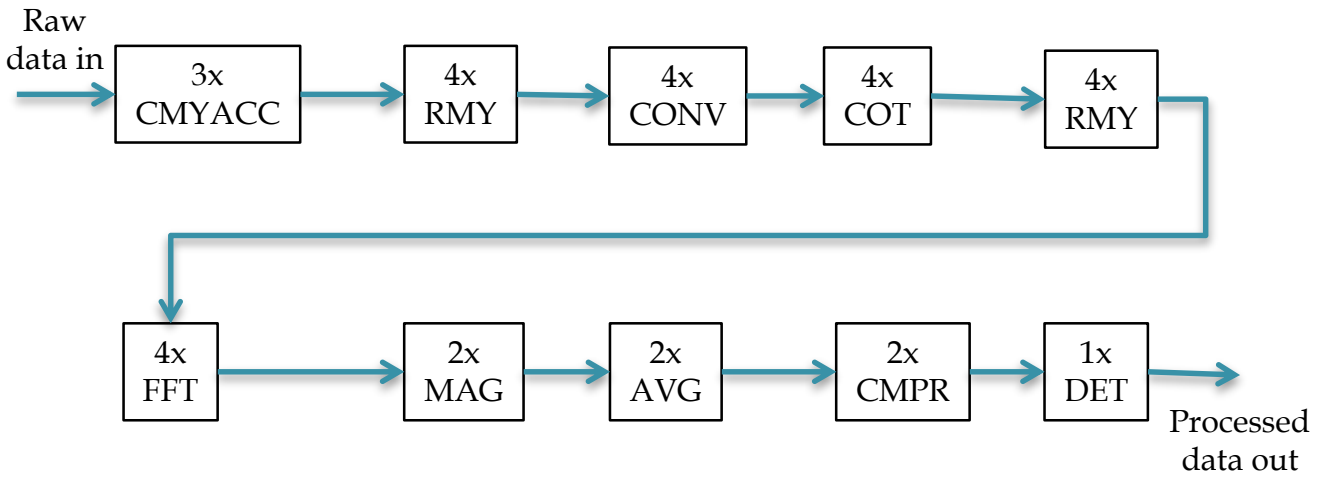
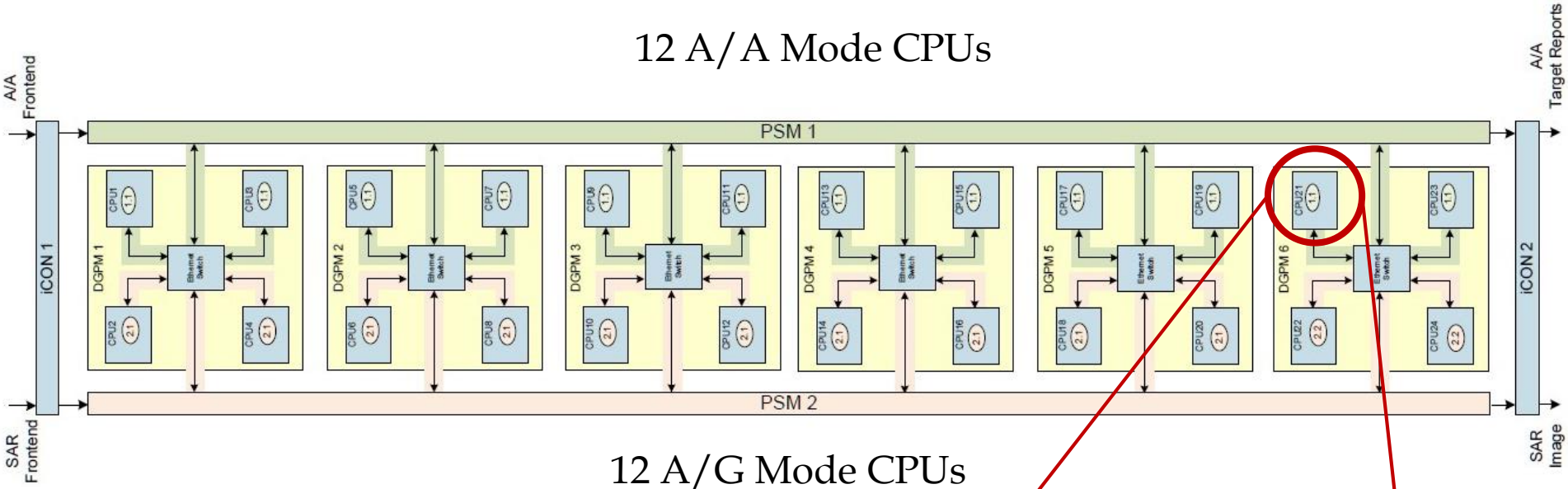
Functional Blocks



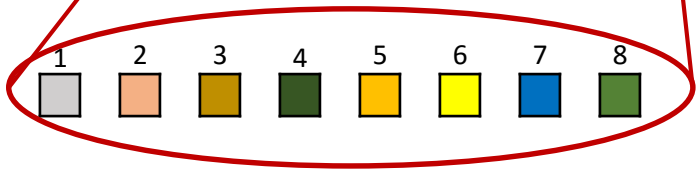
Scheme-1, Space Partitioning

12 A/A Mode CPUs



12 A/G Mode CPUs

1 Dwell(8-bursts) per CPU



Scheme-1, Data Distribution

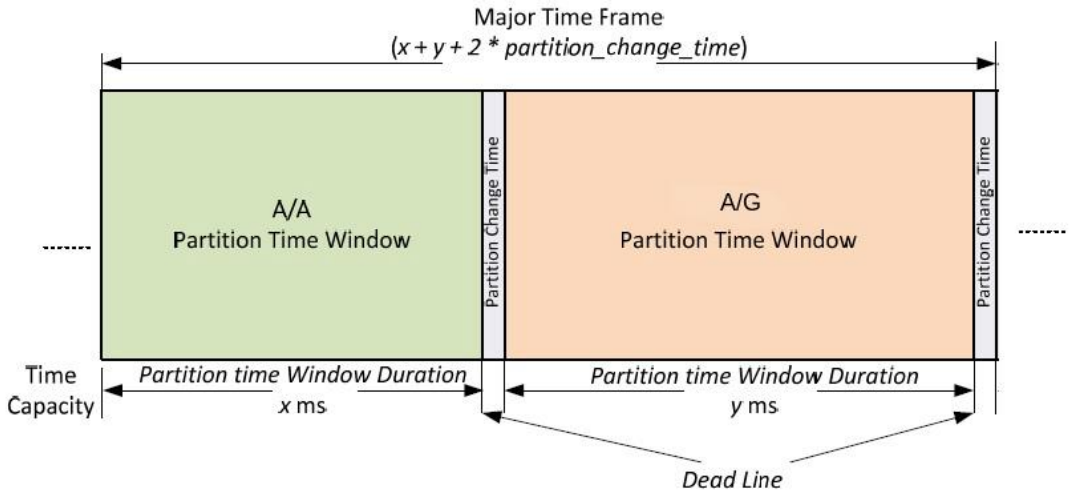
Scheme-1, Processing Latency

- Data fetch
  - SDRAM Buffer to SDRAM
  - SDRAM to L2 cache
- Execute
- Store back
  - L2 Cache to SDRAM
  - SDRAM to SDRAM Buffer

Scheme-1, Results

- CPU Util: 75.58%
- Memory Util: 7% of 1GB
- Interface Util: 72% of 100MB/s
- Processing Latency: 333.67ms (12x dwell time)

Scheme-2, Time Partitioning



24 CPUs for A/A Mode and A/G Mode

	Major Time Frame capacity [ms]	X A/A Appl. Partition Time capacity [ms]	A/A L2-cache Partition [Byte]	Partition Change Time [ms] A/A -> A/G	Y A/G Appl. Partition Time capacity [ms]	Partition Change Time [ms] A/G -> A/A	A/G L2-cache Partition [Byte]
Core1	40	19,50	65.536	0,50	19,50	0,50	65.536
Core2	20	5,50	65.536	0,50	13,50	0,50	65.536
Core3	40	25,50	65.536	0,50	13,50	0,50	65.536
Core4	20	14,50	524.288	0,50	4,50	0,50	131.072

Scheme-2, Results

- CPU Util: 71%
- Memory Util: 9% of 1GB
- Interface Util: 72% of 100MB/s
- Processing Latency: 640ms (23x dwell time)

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Testbed

- Memory Transfer Bandwidth
  - STREAM Benchmark, 4threads – 1048MiB/s
- Memory Utilization
  - Monitor '**top**' output
- Processing Latency
  - 4 threads to 4 cores, 1000 runs
- CPU Load

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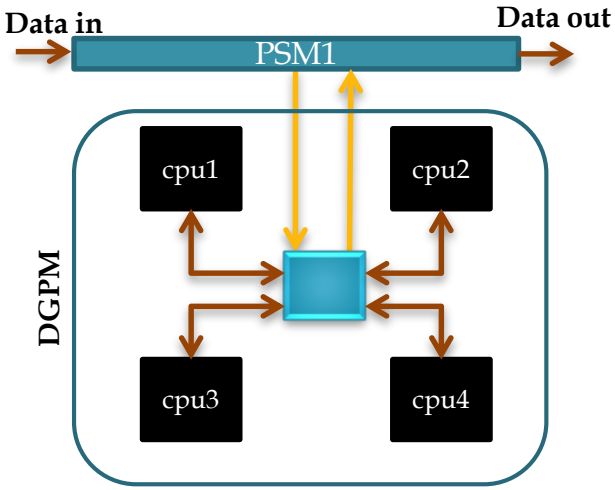
Design Decisions

Design Decisions

Space Partition

Design Decisions

Space Partition

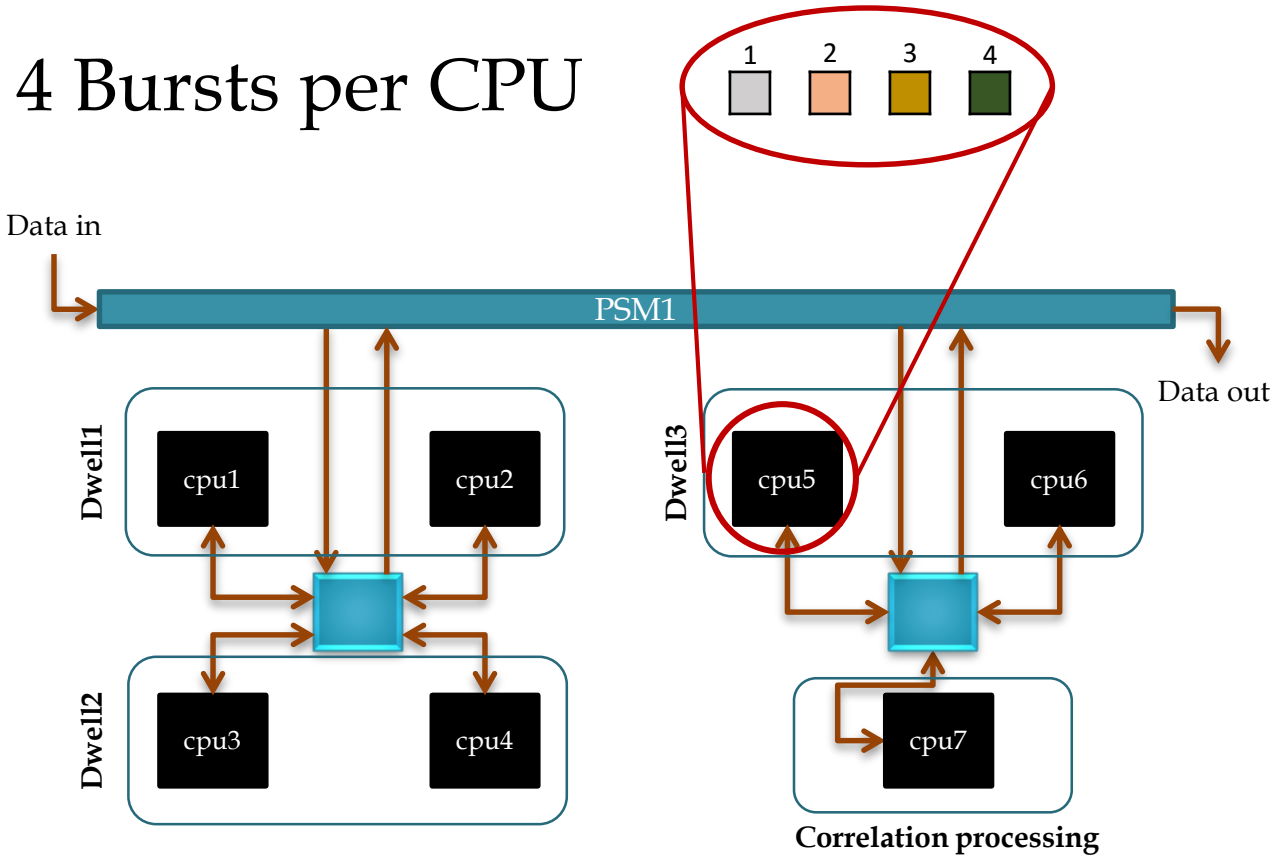


Scheme-3

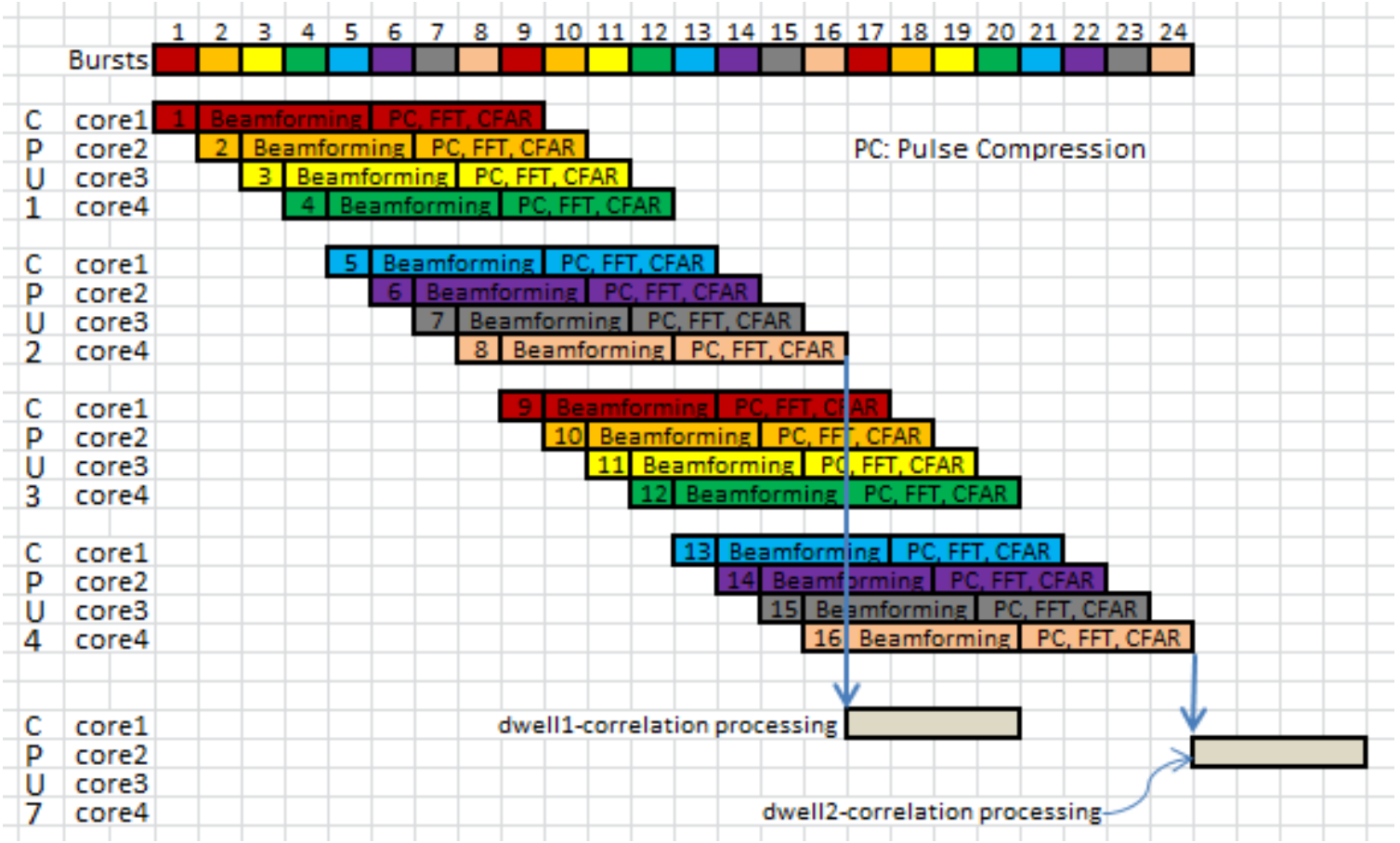
- Correlation Processing – Data Dependent

Scheme-3

- Correlation Processing – Data Dependent
- 4 Bursts per CPU

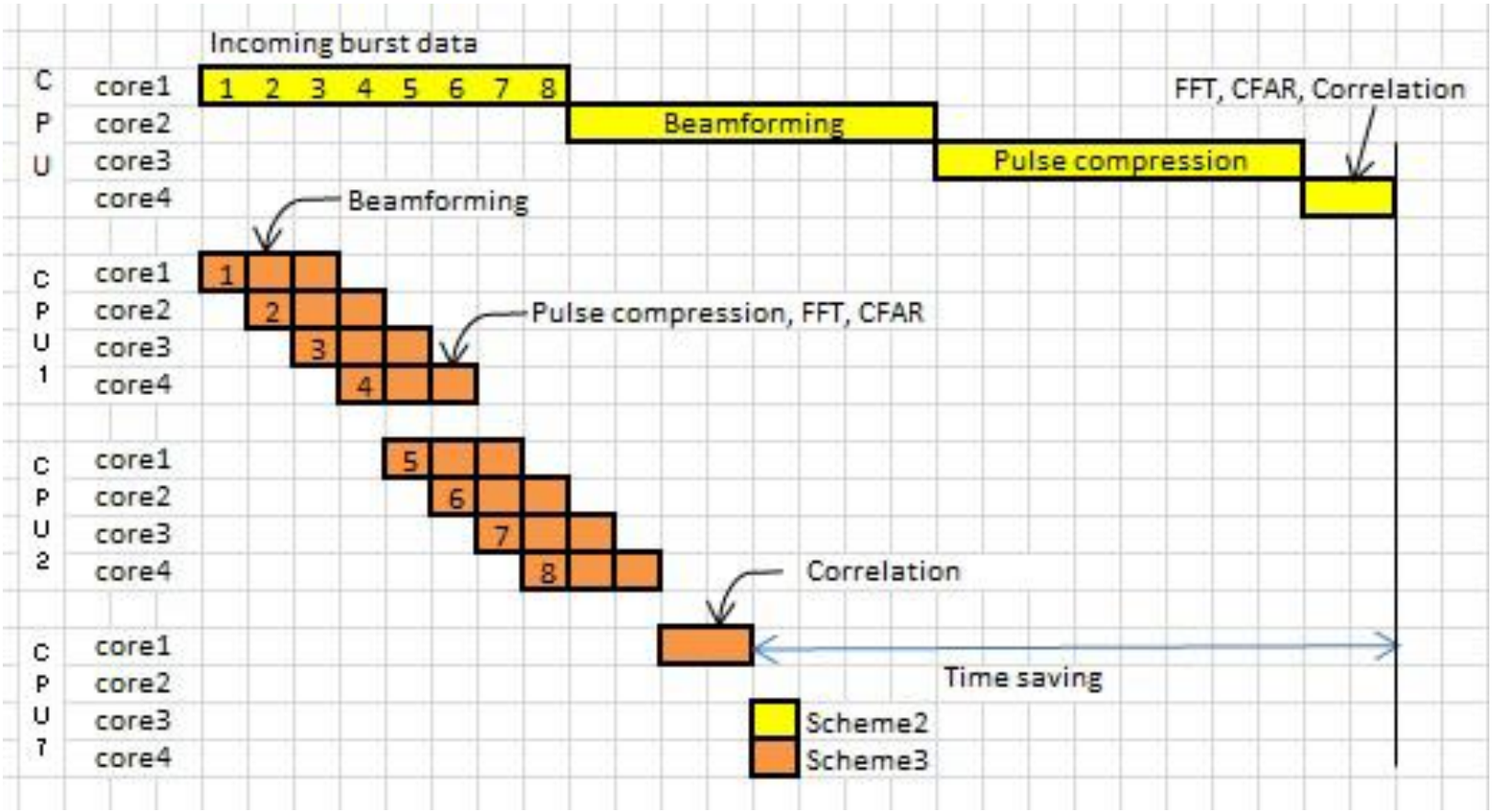


Scheme-3, Data Distribution



CPU7 – 1 dwell per core

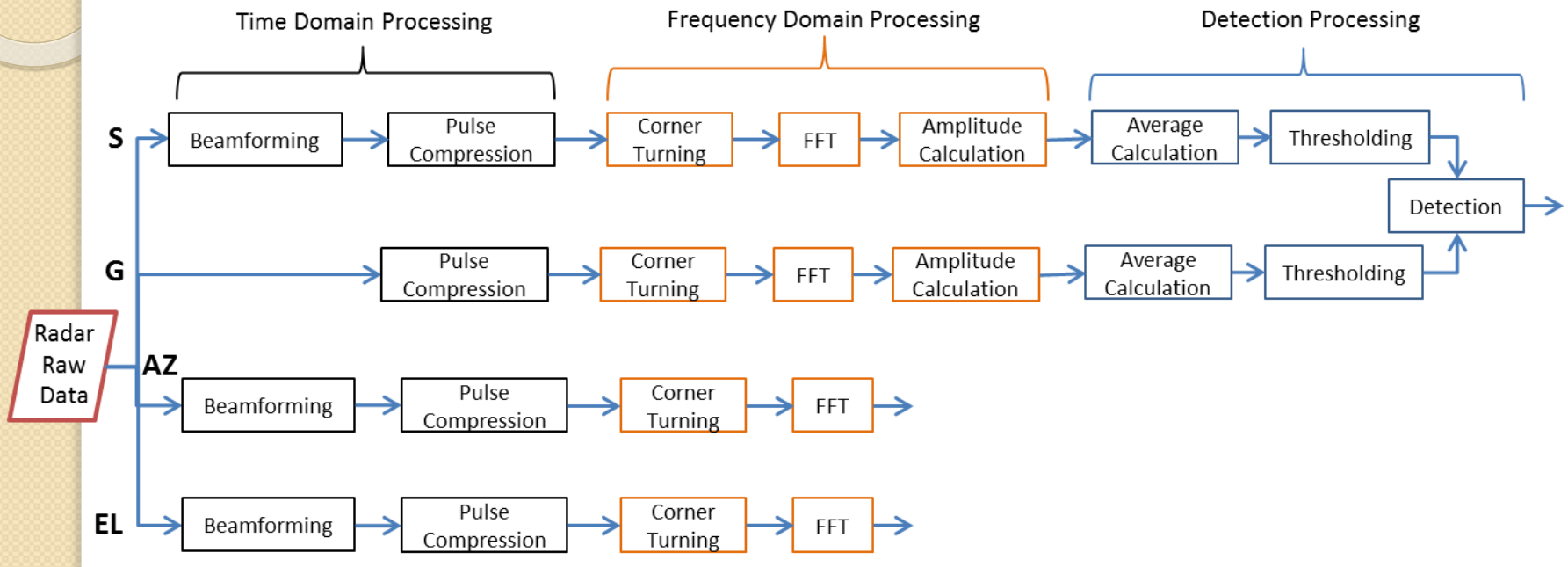
Scheme-3, Time Saving



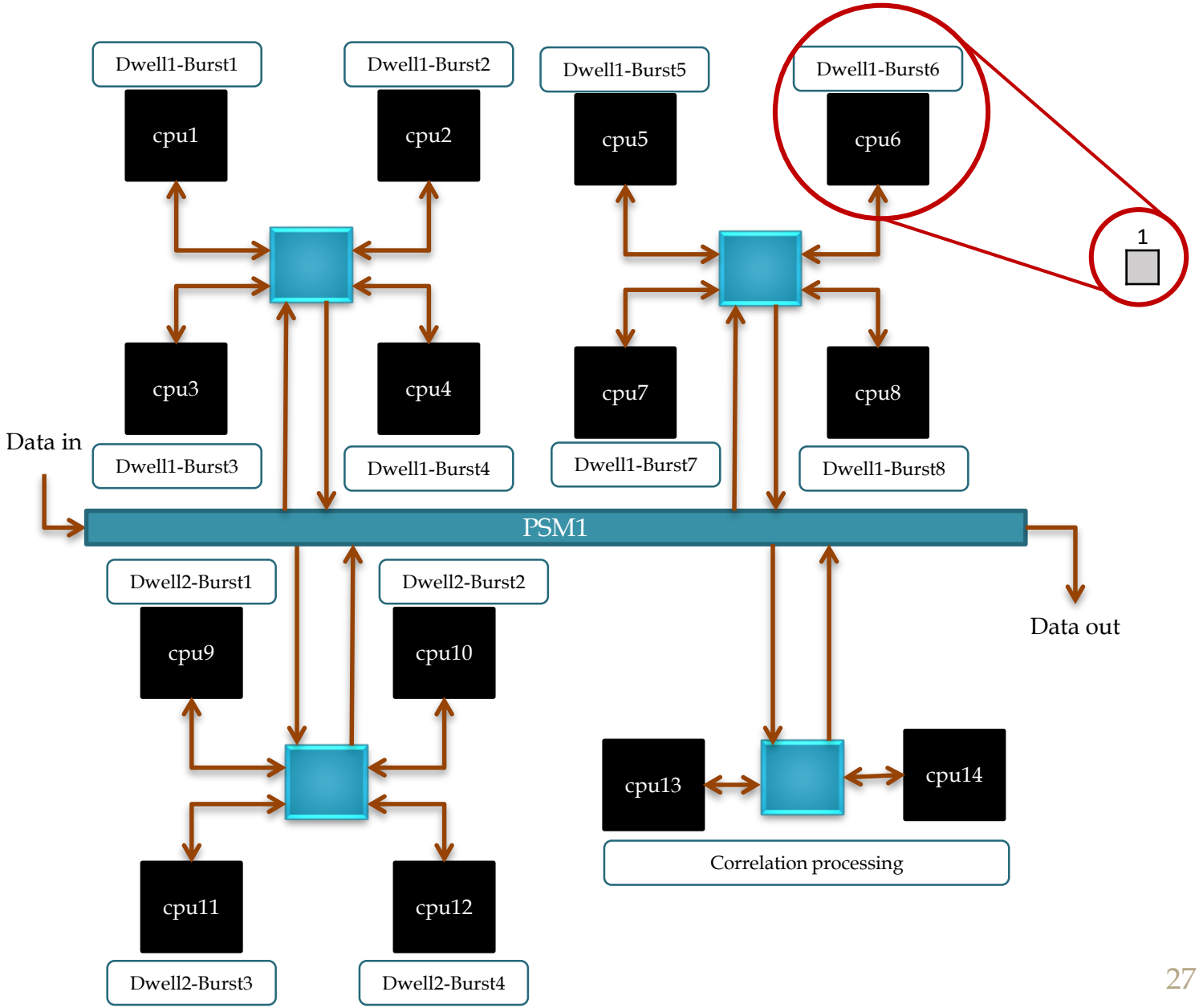
Scheme-3, Results

- CPU Util: 66%
- Memory Transfer BW: 39.4% of 1048MiB/s
- Memory Util: 0.9% of 879MiB
- Processing Latency: 167ms (4x dwell time)

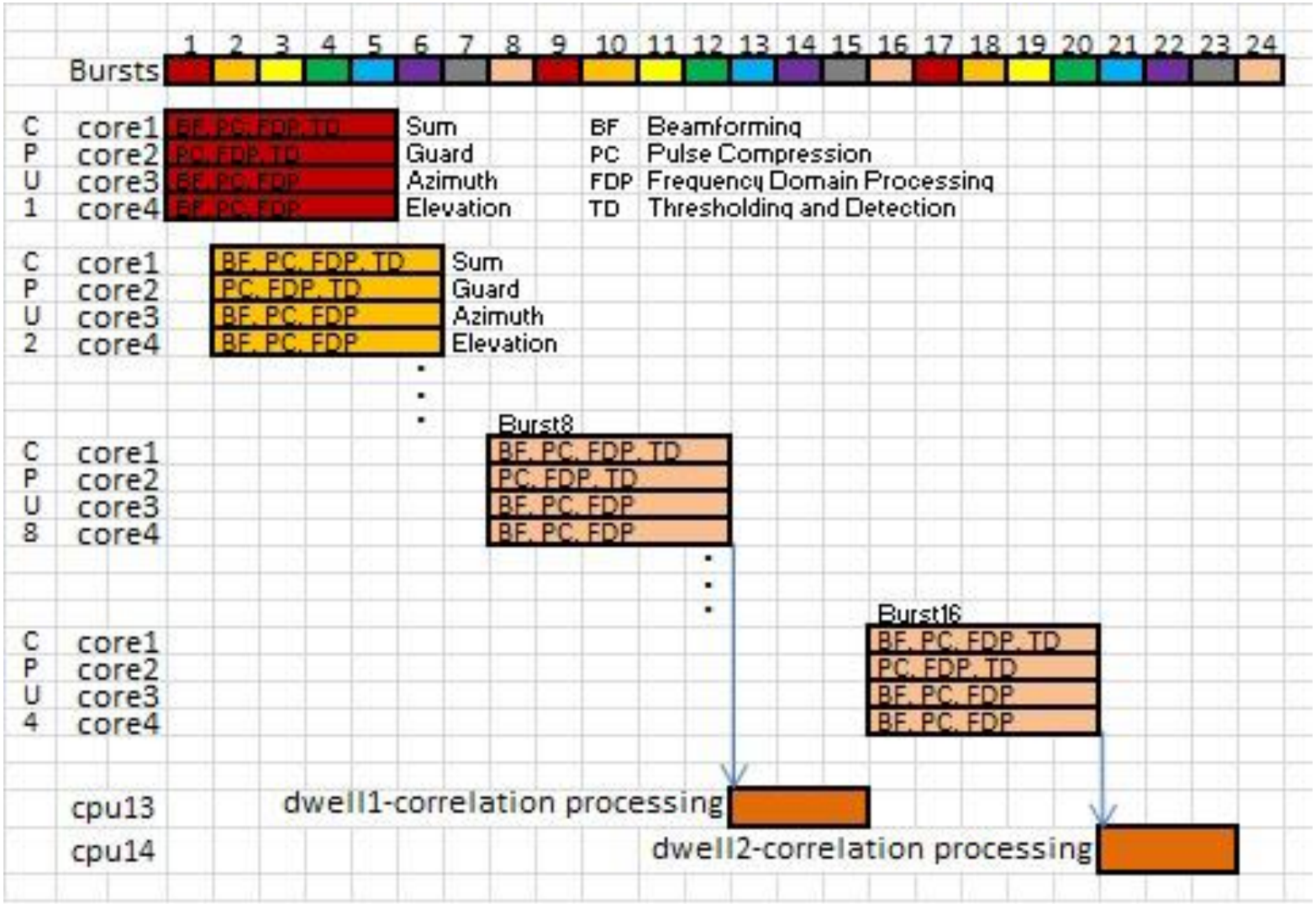
Scheme-4


Time Domain Processing
Frequency Domain Processing
Detection Processing
Radar Raw Data
S
G
AZ
EL
Beamforming
Pulse Compression
Corner Turning
FFT
Amplitude Calculation
Average Calculation
Thresholding
Detection

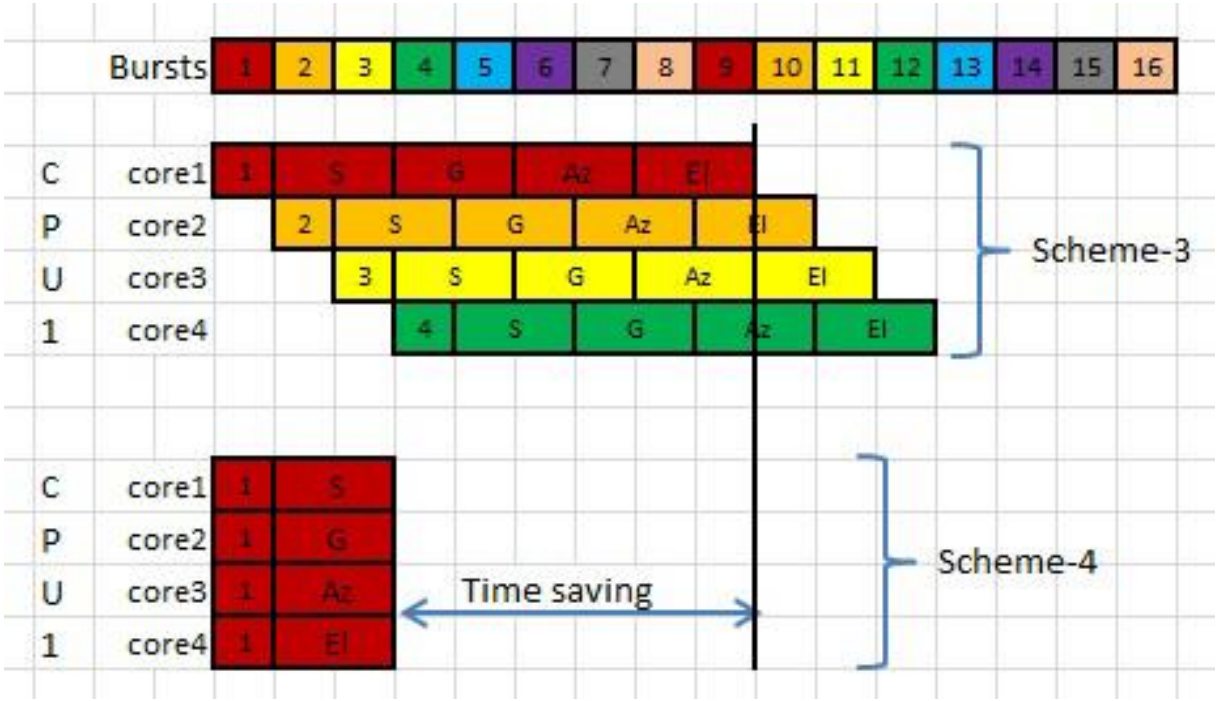
Scheme-4


Dwell1-Burst1
cpu1
Dwell1-Burst2
cpu2
Dwell1-Burst5
cpu5
Dwell1-Burst6
cpu6
1
cpu3
cpu4
cpu7
cpu8
Data in
Dwell1-Burst3
Dwell1-Burst4
Dwell1-Burst7
Dwell1-Burst8
PSM1
Dwell2-Burst1
Dwell2-Burst2
Data out
cpu9
cpu10
cpu13
cpu14
Correlation processing
cpu11
cpu12
Dwell2-Burst3
Dwell2-Burst4

Scheme-4, Data Distribution



Scheme-4, Time Saving



Correlation Processing

- Execution time = 43.34ms = 1.5x dwell time

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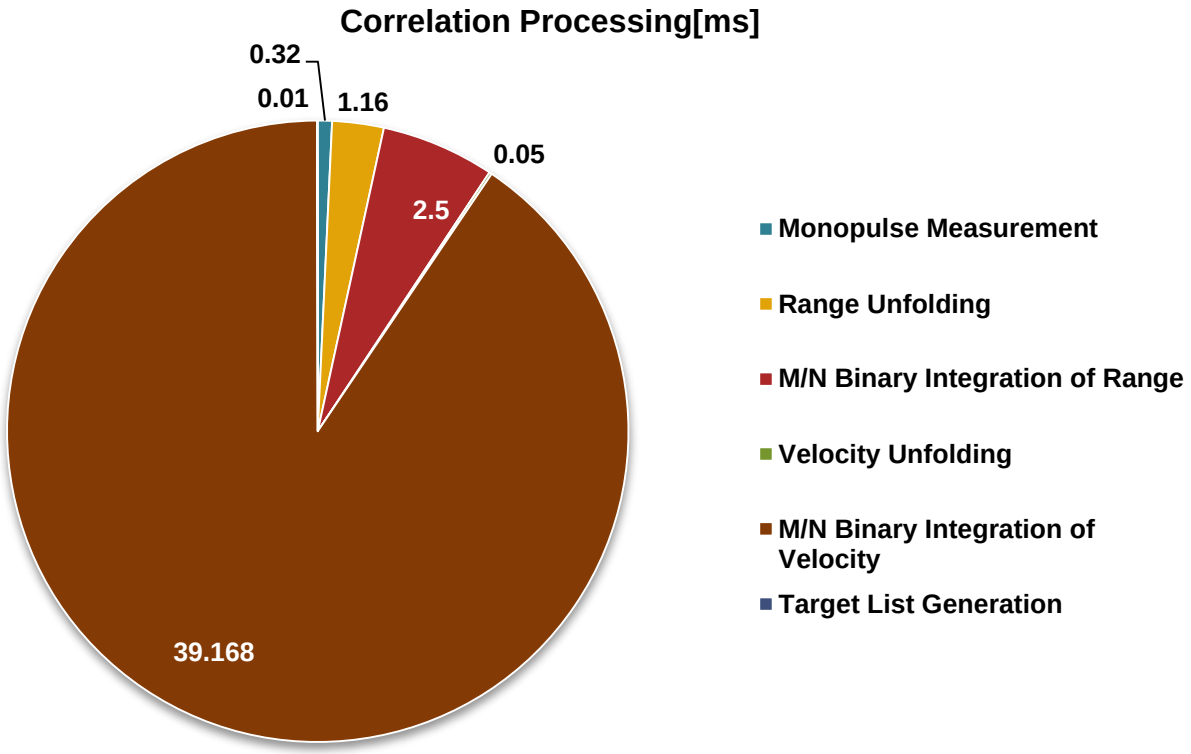
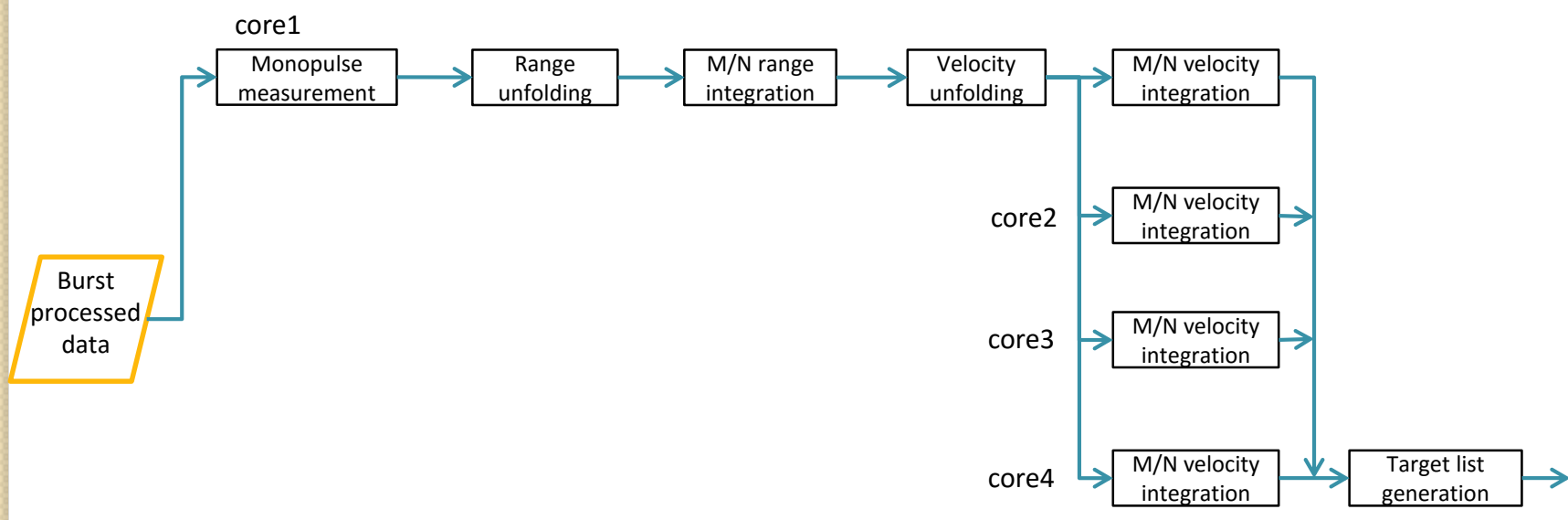


Scheme-4, Correlation Processing



Scheme-4, Results

- CPU Util: **50.8%**
- Memory Transfer BW: **30.3%** of 1048MiB/s
- Memory Util: **0.5%** of 879MiB
- Processing Latency: 54.7ms (**1.9x** dwell time)

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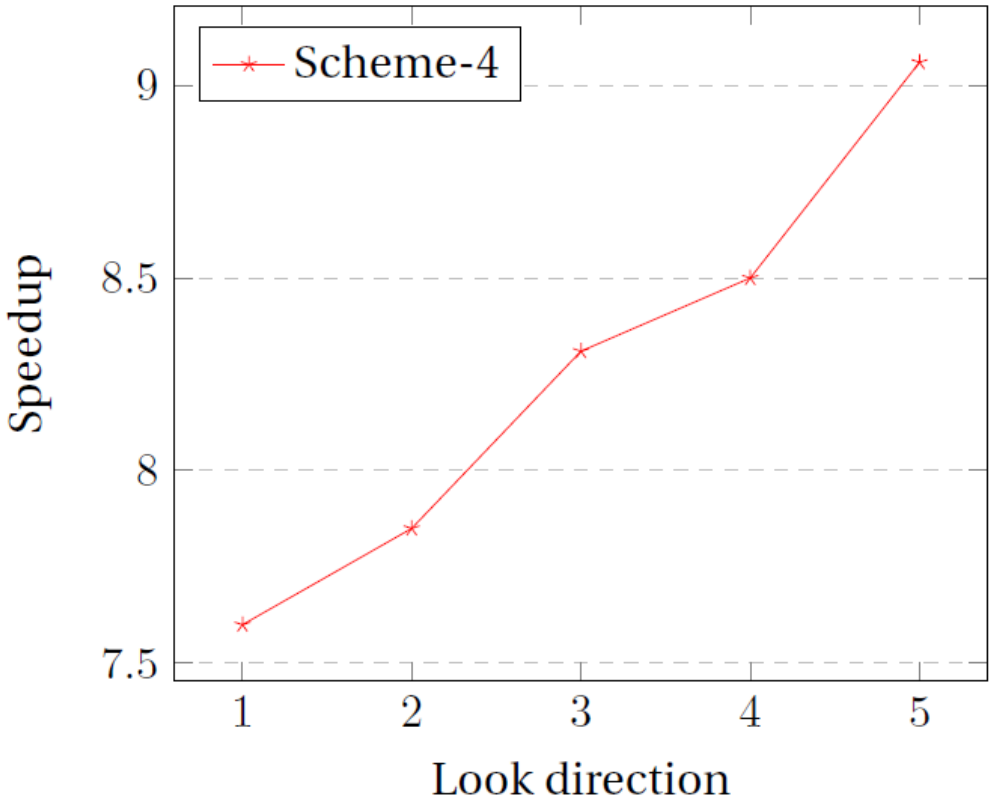
Summary

- Objective
  - Real-time processing
  - Less SWaP and Cost
- Contributions
  - Single core to Multicore
  - Optimized Scheduling

Conclusion




Thank you!