TP6311QG

1/8 - 1/16 Duty VFD Controller/ Driver

DataSheet

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General Specification

The TP6311QG is a FIP (Fluorescent indicator Panel or Vacuum Fluorescent Display) controller/driver that is driven on a 1/8 – to 1/16 duty factor. It consists of 12 segment output lines, 8 grid output lines, 8 segment/grid output drive lines, a display memory, a control circuit, and a key scan circuit. Serial data is input to the TP6311QG through a three-line serial interface. This FIP controller/driver is ideal as a peripheral device of a single-chip microcomputer.

FEATURE

- Many display modes (12-segment & 16-digit to 20-segment & 8-digit)
- Key scanning (12 × 4 matrices)
- Dimming circuit (eight steps)
- High-voltage output (V_{DD} – 35V max)
- LED ports (5 chs, 20 mA max)
- General-purpose input port (4 bits)
- No external resistor necessary for driver outputs (P-ch open-drain + pull-down resistor output)
- Serial interface (CLK, STB, D_{IN}, D_{OUT})

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Topro Technology Inc.

TP6311QG

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Contents：

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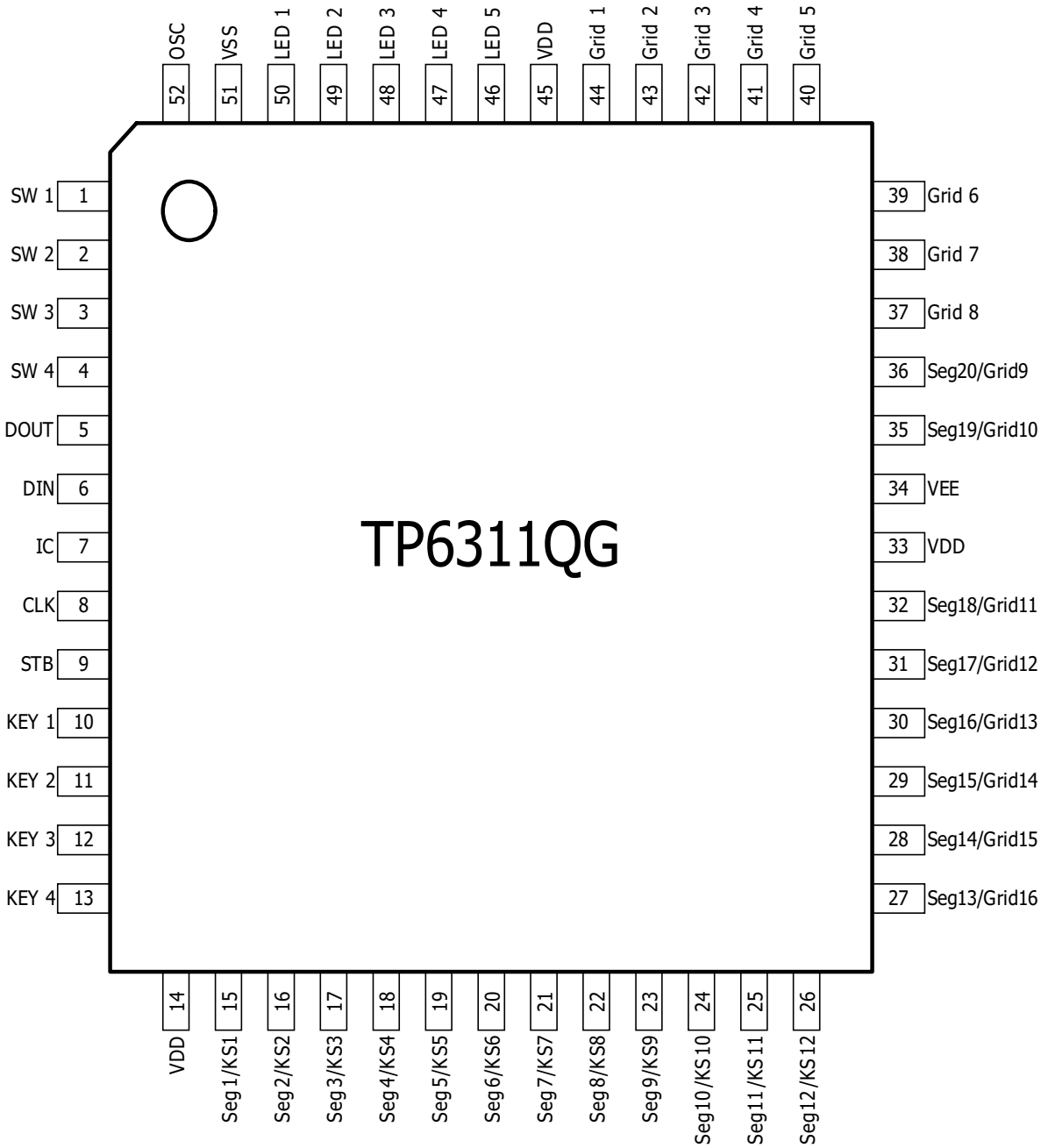
Pin Configurations and Package Type



Use all the power pins. Leave the IC pin open.

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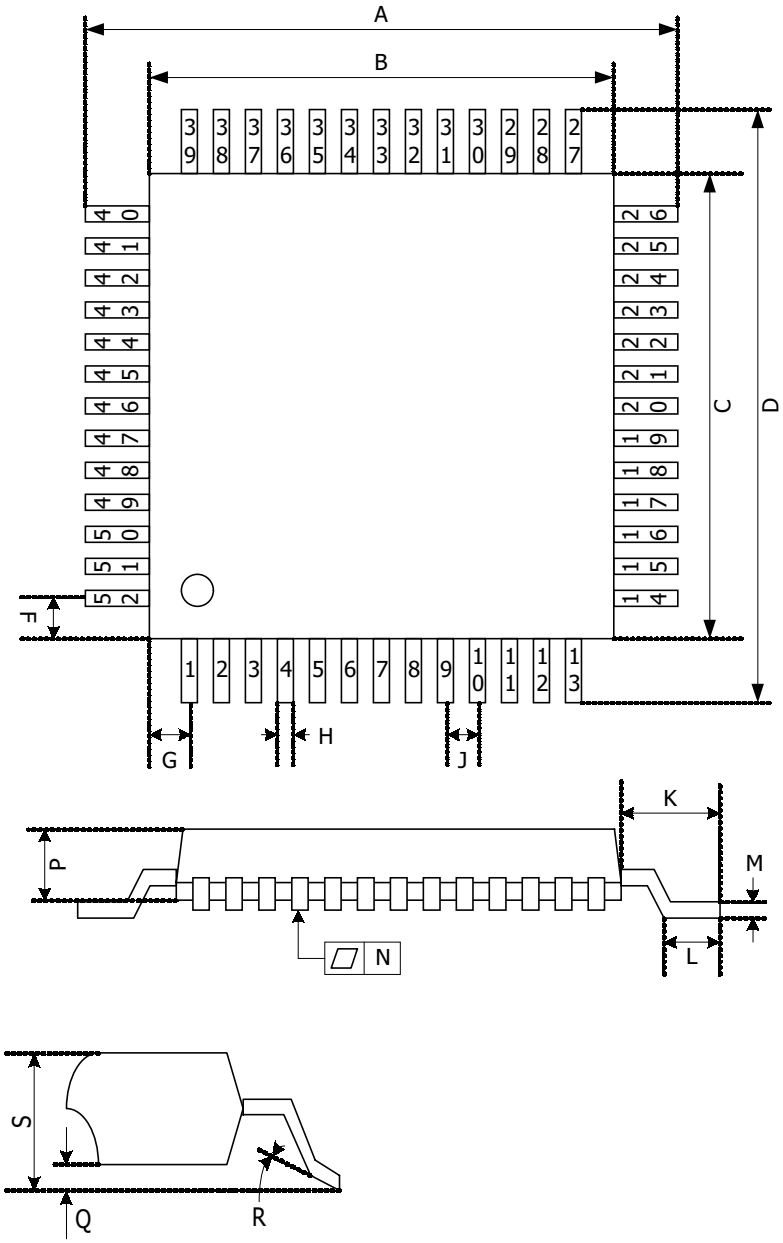
52 PIN PLASTIC QFP (14 × 14)



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ITEM	MILLMETERS	INCHES		ITEM	MILLMETERS		INCHES	
A	17.6± 0.4	0.693± 0.016		K	1.8± 0.2		0.071	+0.008 -0.009
B	14.0± 0.2	0.551	+0.009 -0.008	L	0.8± 0.2		0.031	+0.009 -0.008
C	14.0± 0.2	0.551	+0.009 -0.008	M	0.15	+0.10 -0.05	0.006	+0.004 -0.003
D	17.6± 0.4	0.693± 0.016		N	0.10		0.004	
F	1.0	0.039		P	2.6		0.102	
G	1.0	0.039		Q	0.1± 0.1		0.004± 0.004	
H	0.40± 0.10	0.016	+0.004 -0.005	R	5° ± 5°		5° ± 5°	
I	0.20	0.008		S	3.0 MAX.		0.119 MAX.	
J	1.0 (T.P.)	0.039 (T.P.).						

Pin Descriptions

Pin Function

Pin No	Symbol	Pin Name	Description
6	DIN	Date input	Input serial data at rising edge of shift clock, starting from lower bit.
5	DOUT	Date output	Outputs serial data at falling edge of shift clock, starting from lower bit. This is N-ch open-drain output pin.
9	STB	Strobe	Initializes serial interface at rising or falling edge to make TP6311QG waiting for reception of command. Data input after STB has fallen is processed as command. While command data is processed, current processing is stopped, and serial interface is initialized . While STB is high, CLK is ignored.
8	CLK	Clock input	Reads serial data at rising edge, and outputs data at falling edge.
52	OSC	Oscillator pin	Connect resistor for determining oscillation frequency to this pin.
15 to 26	Seg1/KS1 to Seg12/KS 12	High-voltage output (segment)	Segment output pins (Dual function as key source)
44 to 37	Grid1 to Grid8	High-voltage output (grid)	Grid output pins
27 to 32 35 to 36	Seg13/Gri d16 to Seg20/Gri d9	High-voltage output (segment/grid)	These pins are selectable for segment or grid output.
50 to 46	LED1 to LED5	LED output	CMOS output. +20 mA max
10 to 13	Key1 to Key4	Key data input	Data input to these pins is latched at end of display cycle.
1 to 4	SW1 to SW4	Switch input	These pins constitute 4-bit general-purpose input port.

14, 33,45	VDD	Logic power	5V ± 10%
51	VSS	Logic ground	Connect this pin to GND of system.
34	VEE	Pull-down level	VDD – 35 V max
7	IC	Internally connected	Be sure to leave this pin open (this pin is at VDD level).

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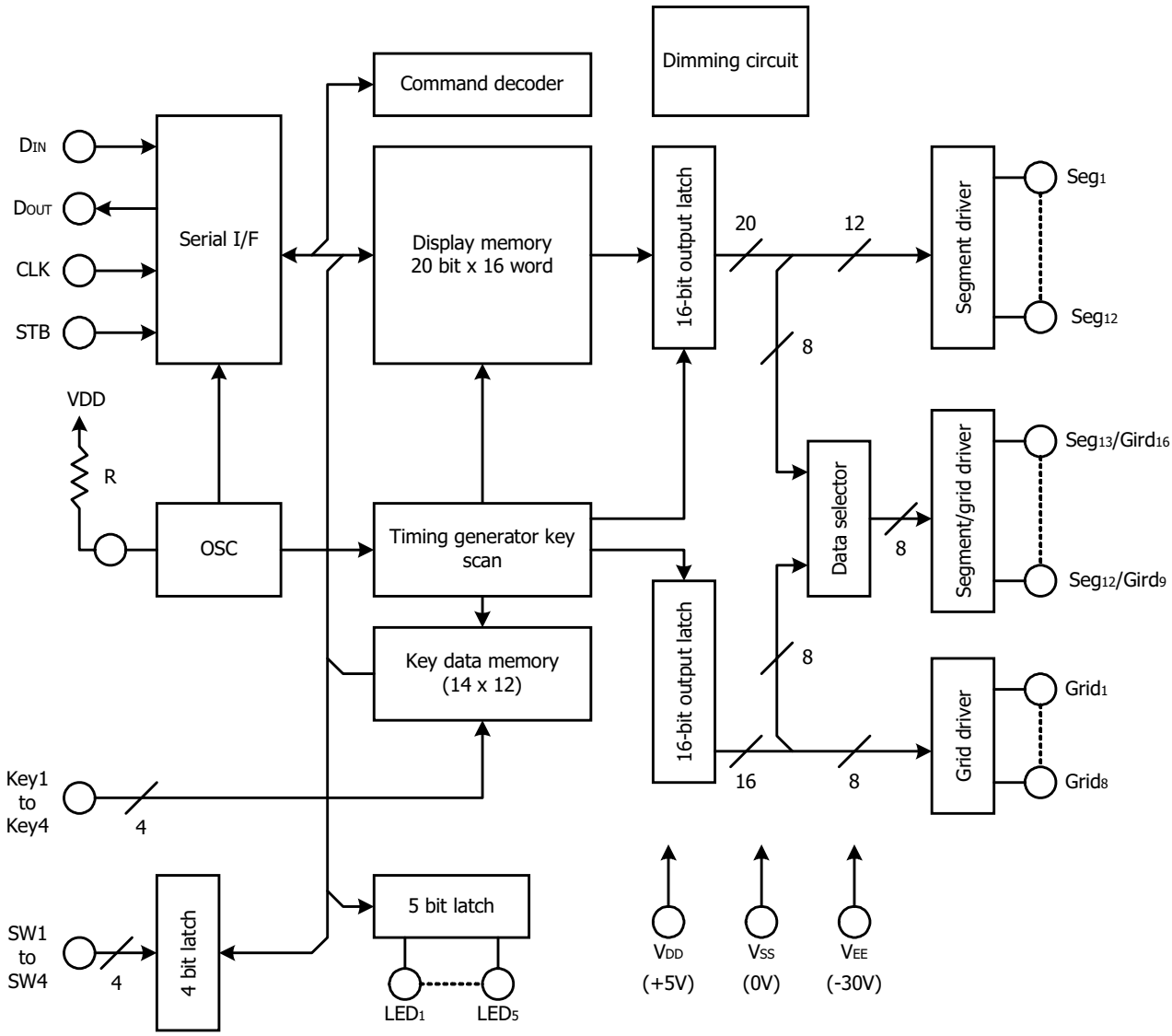
Functional Block Diagram



Function Descriptions

Display RAM Address and Display Mode

The display RAM stores the data transmitted from an external device to the TP6311QG through the serial interface, and is assigned addresses as follows, in units of 8 bits:

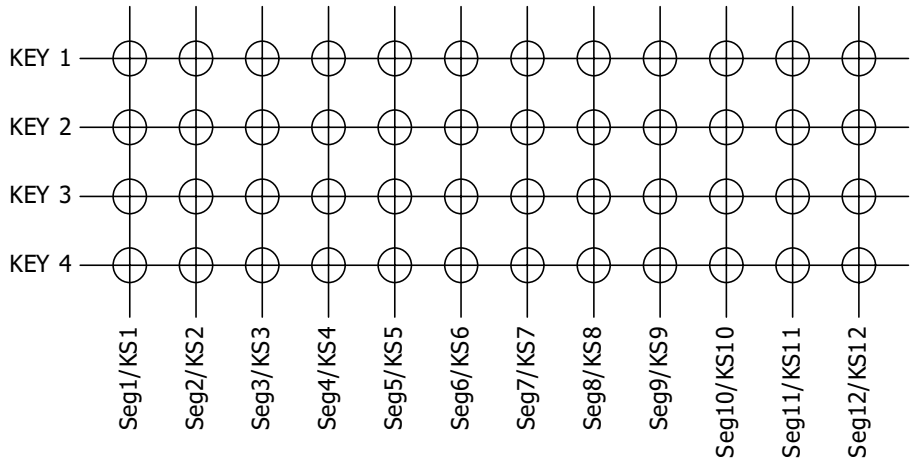
Seg_1	Seg_4	Seg_8	Seg_{12}	Seg_{16}	Seg_{20}	
$00H_L$	$00H_U$	$01H_L$	$01H_U$	$02H_L$		DIG1
$03H_L$	$03H_U$	$04H_L$	$04H_U$	$05H_L$		DIG2
$06H_L$	$06H_U$	$07H_L$	$07H_U$	$08H_L$		DIG3
$09H_L$	$09H_U$	$0AH_L$	$0AH_U$	$0BH_L$		DIG4
$0CH_L$	$0CH_U$	$0DH_L$	$0DH_U$	$0EH_L$		DIG5
$0FH_L$	$0FH_U$	$10H_L$	$10H_U$	$11H_L$		DIG
$12H_L$	$12H_U$	$13H_L$	$13H_U$	$14H_L$		DIG7
$15H_L$	$15H_U$	$16H_L$	$16H_U$	$17H_L$		DIG8
$18H_L$	$18H_U$	$19H_L$	$19H_U$	$1AH_L$		DIG9
$1BH_L$	$1BH_U$	$1CH_L$	$1CH_U$	$1DH_L$		DIG10
$1EH_L$	$1EH_U$	$1FH_L$	$1FH_U$	$20H_L$		DIG11
$21H_L$	$21H_U$	$22H_L$	$22H_U$	$23H_L$		DIG12
$24H_L$	$24H_U$	$25H_L$	$25H_U$	$26H_L$		DIG13
$27H_L$	$27H_U$	$28H_L$	$28H_U$	$29H_L$		DIG14
$2AH_L$	$2AH_U$	$2BH_L$	$2BH_U$	$2CH_L$		DIG15
$2DH_L$	$2DH_U$	$2EH_L$	$2EH_U$	$2FH_L$		DIG16

b_0	b_3 b_4	b_7
$XX\ H_L$	$XX\ H_U$	
Lower 4 bits	Higher 4 bits.	

Only the lower 4 bits of the addresses assigned to Seg17 through Seg20 are valid, and the higher 4 bits are ignored.

Key Matrix and Key-Input Data Storage RAM

The key matrix is of 12 × 4 configuration, as shown below.



The data of each key is stored as illustrated below, and is read by a read command, starting from the least significant bit.

KEY_1 …… KEY_4	KEY_1 …… KEY_4
Seg_1 / KS_1	Seg_2 / KS_2
Seg_3 / KS_3	Seg_4 / KS_4
Seg_5 / KS_5	Seg_6 / KS_6
Seg_7 / KS_7	Seg_8 / KS_8
Seg_9 / KS_9	Seg_{10} / KS_{10}
Seg_{11} / KS_{11}	Seg_{12} / KS_{12}

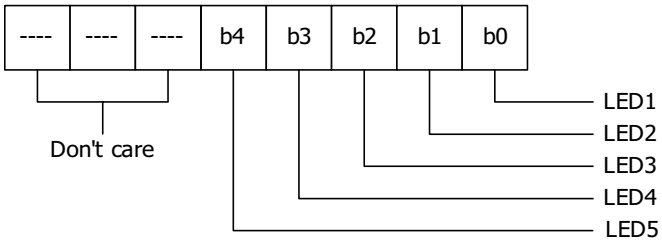
b0 …… b3 b4 …… b7

Reading sequenc

When the most significant bit if data (Seg12 b7) has been read, the least significant bit of the next data (Seg1 b0) is read.

LED PORT

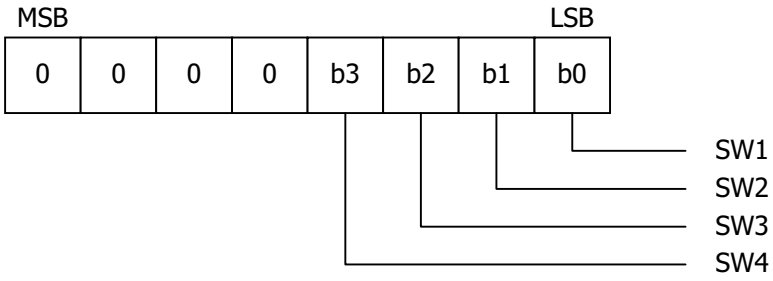
Data is written to the LED port by a write command, starting from the least significant bit of the port. When a bit of this port is 0, the corresponding LED lights ; when the bit is 1, the LED goes off. The data of bits 6 through 8 is ignored.



On power application, all the LEDs remain dark.

SW Data

The SW data is read by a read command, starting from the least significant bit. Bits 5 through 8 of the SW data are 0.



Command

A command sets the display mode and status of the FIP driver.

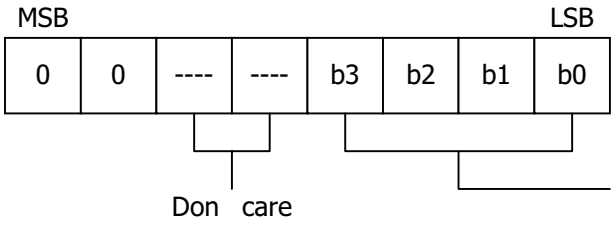
The first 1 byte input to the TP6311QG through the Din pin after the STB pin has fallen is regarded as a command.

If STB is made high while a command/data is transmitted, serial communication is initialized, and the command/data being transmitted is invalid (however, the command/data already transmitted remains valid).

(1) Display mode setting command

This command initializes the TP6311QG and selects the number of segments and number of grids (1/8 to 1/16 duty, 12 segments to 20 segments).

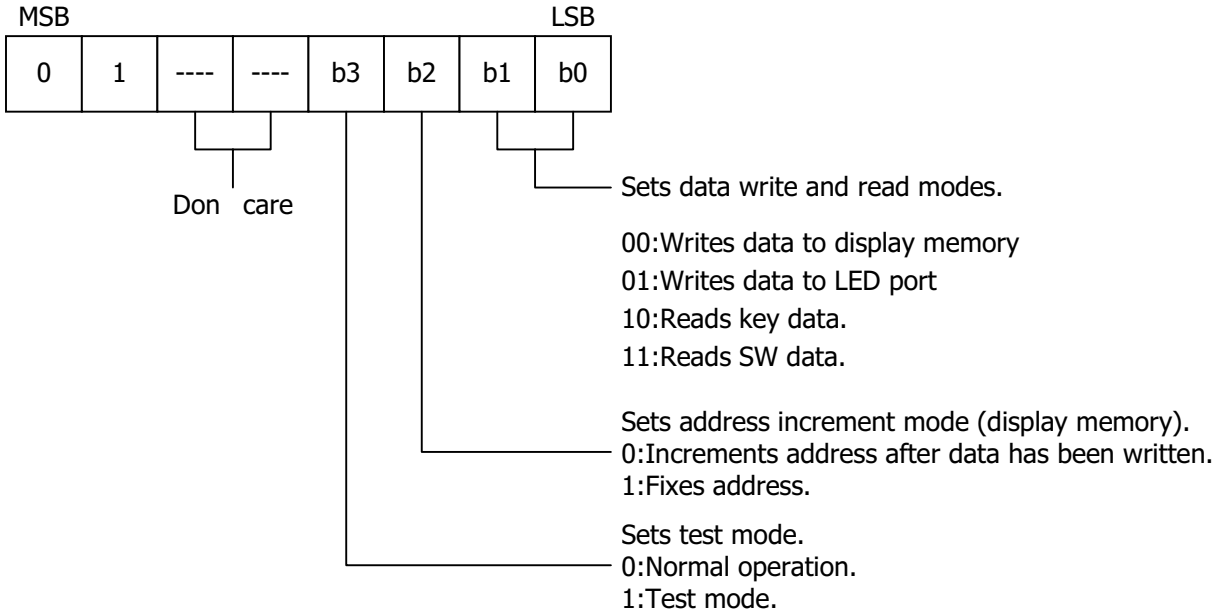
On power application, the 16-digit, 12-segment mode is selected.



0XXX : 8 digits, 20 segments
1000 : 9 digits, 19 segments
1001 : 10 digits, 18 segments
1010 : 11 digits, 17 segments
1011 : 12 digits, 16 segments
1100 : 13 digits, 15 segments
1101 : 14 digits, 14 segments
1110 : 15 digits, 13 segments
1111 : 16 digits, 12 segments

(2) Data setting command

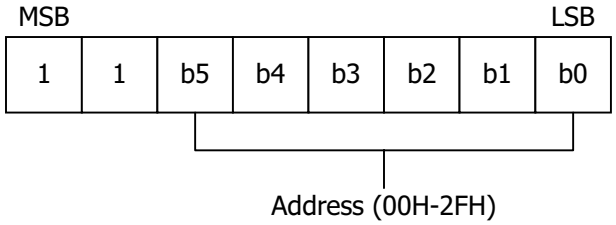
This command sets data write and read modes.



On power application, the normal operation mode and address increment mode set.

(3) Address setting command

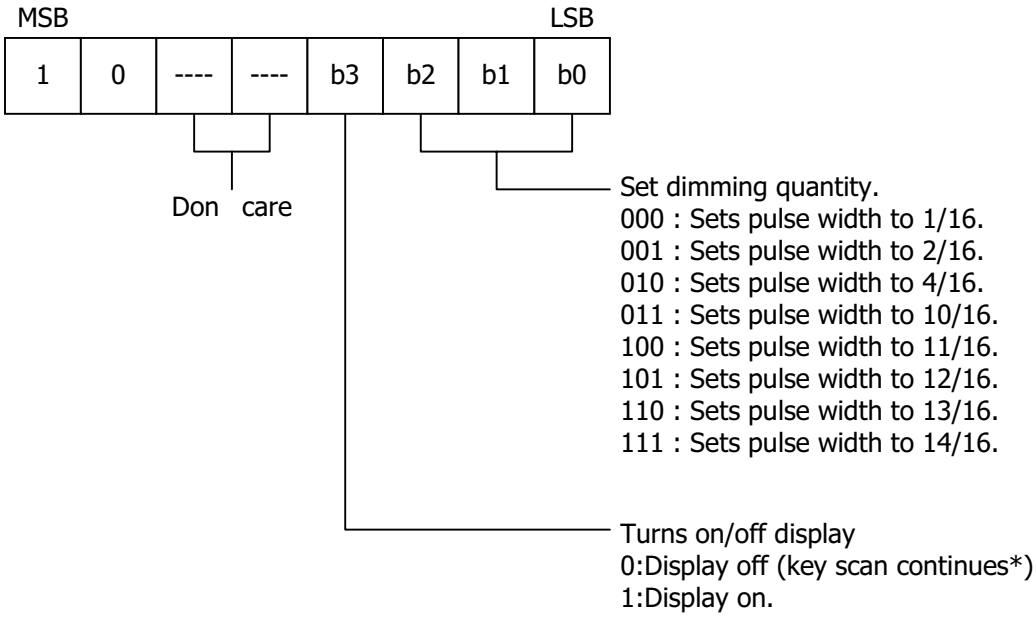
This command sets an address of the display memory.



If address 30H or higher is set, the data is ignored, unit a correct address is set.

On power application, the address is set to 00H.

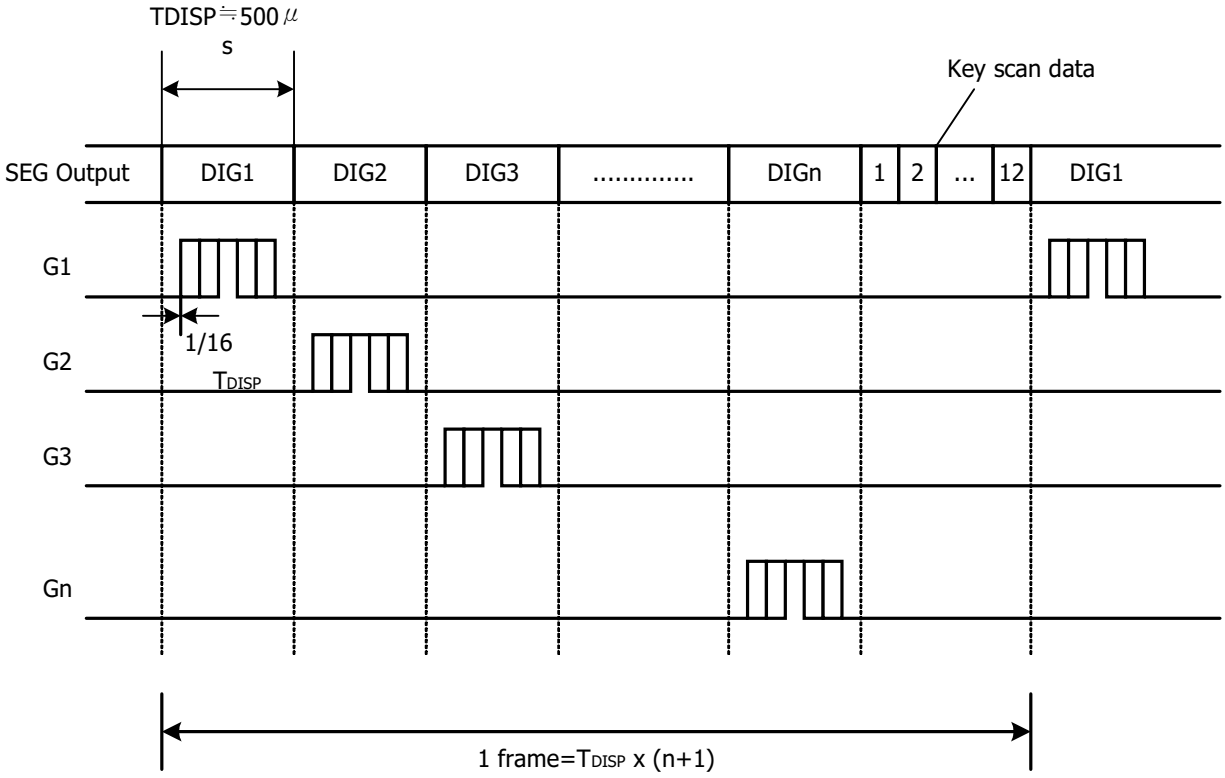
(4) Display control command



On power application, the 14/16-pulse width is set and the display is turned off.

* : On power application, key scanning is stopped..

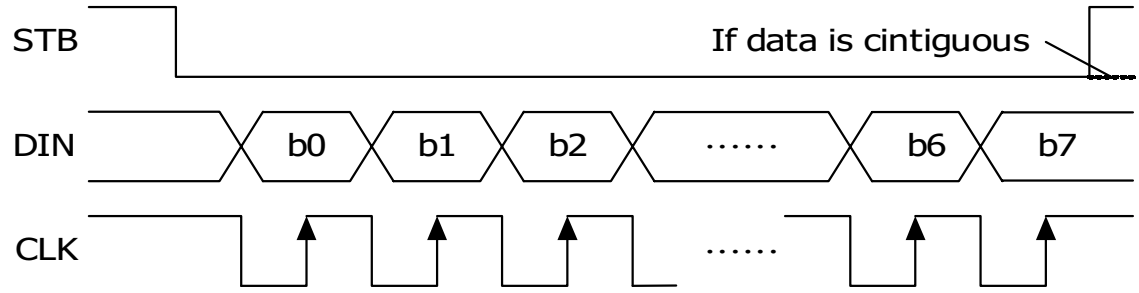
Key Scanning and Display Timing



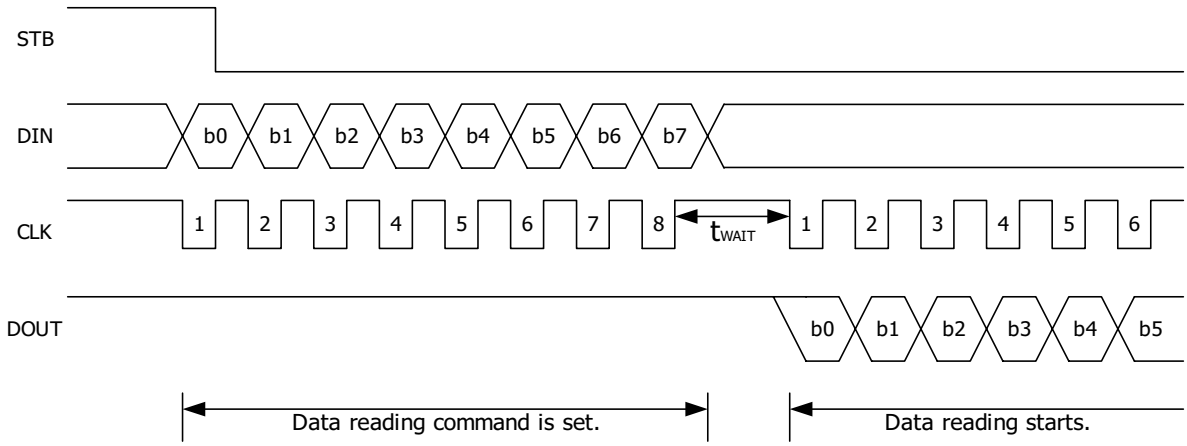
One cycle of key scanning consists of two frames, and data of 12 × 4 matrices is stored in RAM.

Serial Communication Format

Reception (command/data write)



Transmission (data read)



Because the DOUT pin is an N-ch, open-drain output pin, be sure to connect an external pull-up resistor to this pin (1kΩ to 10 kΩ).

*:When data is read, a wait time t_{WAIT} of 1μs is necessary since the rising of the eighth clock that has set the command, until the falling of the first clock that has read the data.

Absolute Maximum Ratings

ABSOLUTE MAXIMUM RATING (Ta=25℃, Vss=0 V)

PARAMETER	SYMBOL	RATINGS	UNIT
Logic Supply Voltage	V_{DD}	-0.5 to + 7.0	V
Driver Supply Voltage	V_{EE}	V_{DD} +0.5 to V_{DD} -40	V
Logic Input Voltage	V_{i1}	-0.5 to Vdd+0.5	V
FIP Driver Output Voltage	V_{o2}	V_{EE} –0.5 to V_{DD} +0.5	V
LED Driver Output Current	I_{o1}	25	mA
FIP Driver Output Current	I_{o2}	-40 (grid) -15 (segment)	mA
Power Dissipation	P_D	1200*	mW
Operating Ambient Temperature	T_{opt}	-40 to +85	℃
Storage Temperature	T_{stg}	-65 to +150	℃

* Derate at –9.6 mW/℃ at Ta=25℃ or higher.

DC Electrical Characteristic

RECOMMENDED OPERATING CONDITION (Ta=-20 to 70, Vss=0V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Logic Supply Voltage	VDD	4.5	5	5.5	V	
High-Level input Voltage	Vih	0.6VDD		VDD	V	
Low-Level input Voltage	Vil	0		0.3VDD	V	
Driver Supply Voltage	VEE	0		VDD-35	V	

Maximum power consumption Pmax.=FIP driver dissipation + R_L dissipation + LED driver dissipation + dynamic power consumption.

Where segment current = 3 mA, grid current = 15ma, and LED current = 20 mA,
FIP driver dissipation = number of segments x 6 + number of grids/(number of grids + 1) x 30 (mW)
R_L dissipation = $(V_{DD}-V_{EE})^2/50$ x (segment+1) (mW)
LED driver dissipation = number of LEDs x 20(mW)
Dynamic power consumption = V_{DD} x 5(mW)

Example

Where V_{EE} = -30 V, V_{DD} = 5 V, and in 16-segment and 12-digit modes,

FIP driver dissipation = 16 x 6 + 12/13 x 35 =	128
R_L dissipation = $35^2/50$ x 17 =	417
LED driver dissipation = 5 x 20 =	100
Dynamic power consumption = 5 x 5 =	25
Total	670 mW

ELECTRICAL SPECIFICATIONS(Ta= -20 to + 70°C ,VDD= 4.5 to 5.5V ,VS =0V,VEE =VDD - 35V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
High-Level Output Voltage	V_{OH1}	0.9 V_{DD}			V	LED_1 – LED_5, I_{OH1} = -1 mA
Low-Level Output Voltage	V_{OL1}			1	V	LED_1 – LED_5, I_{OL1} = 20 mA
Low-Level Output Voltage	V_{OL2}			0.4	V	D_{OUT}, I_{OL2} = 4 mA
High-Level Output Current	I_{OH21}	-3			mA	$V_O = V_{DD}$ –2V, Seg_1 to Seg_{12}
High-Level Output Current	I_{OH22}	-15			mA	$V_O = V_{DD}$ –2V,$Grid_1$ to $Grid_8$, Seg_{13}/Seg_{16} to Seg_{20}/Seg_9
Driver Leakage Current	I_{OLEAK}			-10	µA	$V_O = V_{DD}$ - 35V, Driver off
Output Pull-Down Resistor	R_L	50	100	150	kΩ	Driver output
Input Current	Ii			±1	µA	$V_I = V_{DD} – V_{SS}$
High-Level Output Voltage	V_{IH}	0.6 V_{DD}			V	
Low-Level Output Voltage	V_{IL}			0.3 V_{DD}	V	
Hysteresis Voltage	V_H		0.35		V	CLK, DIN, STB
Dynamic Current Consumption	I_{DDdyn}			5	mA	Under no load, display off

AC Electrical Characteristic

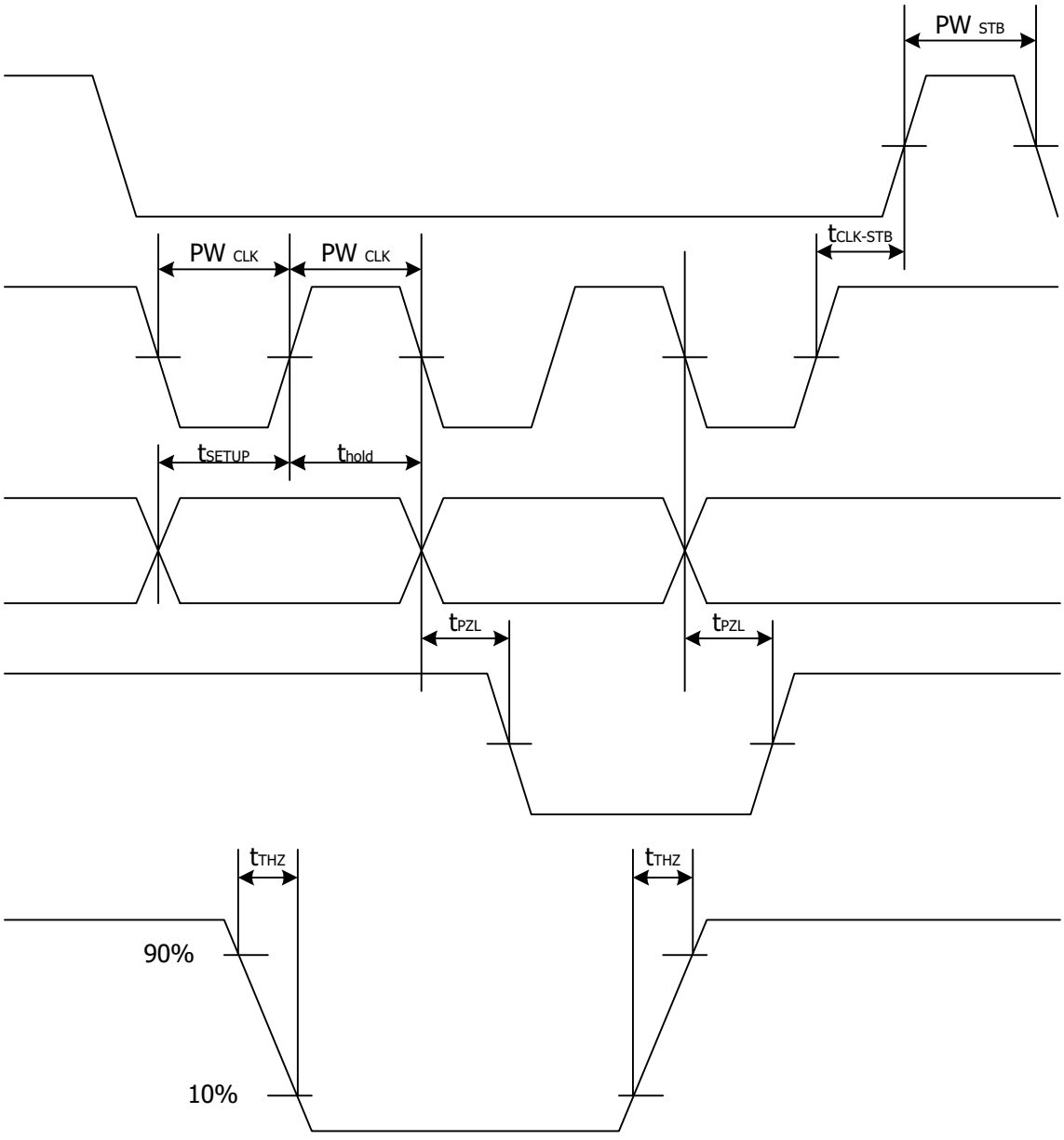
SWITCHING CHARACTERISTICS(Ta = -20 to +70°C, VDD = 4.5 to 5.5V, VEE = -30V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS	
Oscillation Frequency	t_{OSC}	350	500	650	kHz	R = 56kΩ	
Propagation Delay Time	t_{PLZ}			300	ns	CLK ⇒ DOUT CL = 15pF,RL = 10kΩ	
	t_{PZL}			100	ns		
Rise Time	t_{TZH1}			2	µs	CL = 300 PF	Seg1 to Seg12
	t_{TZH2}			0.5	µs		Grid1 to Grid8 Seg13/Grid15 to Seg20/Grid9
Fall Time	t_{THZ}			120	µs	CL = 300 pF, Segn, Gridn	
Maximum Clock Frequency	fmax	1			MHz	Duty = 50%	
Input Capacitance	C1			15	pF		

TIMING CONDITIONS(Ta = -20 to +70°C, VDD = 4.5 to 5.5V)

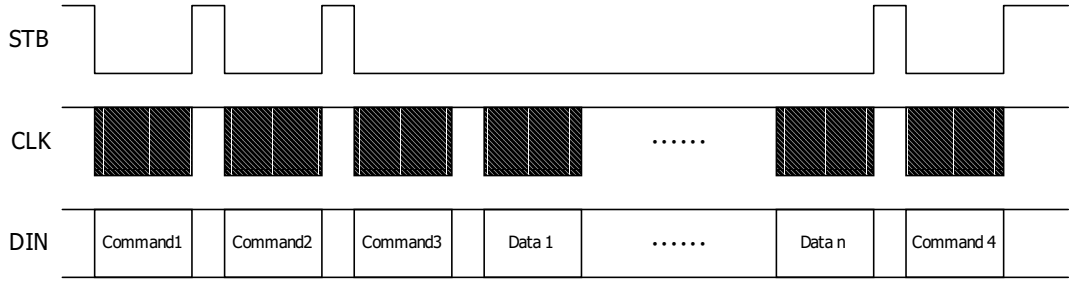
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
Clock Pulse Width	PW_{CLK}	400			ns	
Strobe Pulse Width	PW_{STB}	1			µs	
Data Setup Time	t_{SETUP}	100			ns	
Data Hold Time	t_{HOLD}	100			ns	
Clock-Strobe Time	$t_{CLK-STB}$	1			µs	CLK ↑ → STB ↑
Wait Time	t_{WAIT}	1			µs	CLK ↑ → CLK ↓

Switching Characteristic Waveform



Application Notes

Updating display memory by incrementing address.



Command1: sets display mode

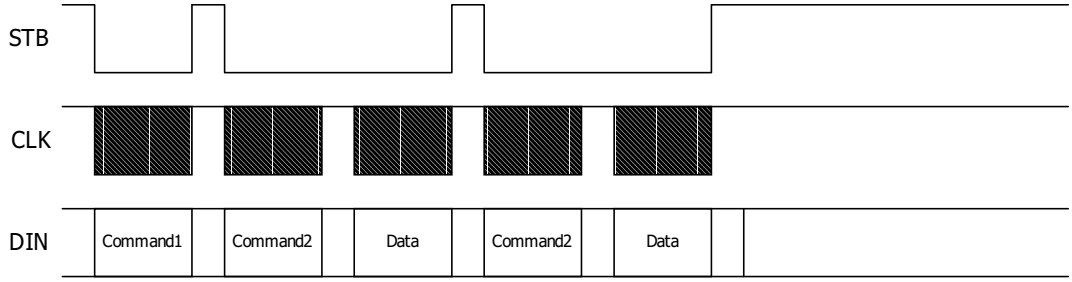
Command2: sets data

Command3: sets address

Data 1 to n : transfers display data (48 bytes max.)

Command4: controls display

Updating specific address



Command1: sets data

Command2: sets address

Data: display data