ECE284 FA25 Final Progress Report

Team : JOEVER

Item	Current Status	Status during Poster Presentation	Note
Part1	Complete	Complete	Vanilla version
Part2	Complete	Complete	2bit/4 bit Updated the mactile to have 2 MAC to process the 2 bit Activation signals - Works over 2 cycles. - Has control signal to toggle the mode in runtime - Signed W and unsigned Act
Part3	Complete	Complete	-WS/OS - Updated MAC tile , added IFIFO , SFU and SRAM loading logic
Alpha 1: ResNet	Complete	Complete	VGG v/s RESNET with QAT
Alpha 2 : Clock Gating	Complete	Complete	
Alpha 3 : Pruning	Complete	Complete	Combined Structured and Unstructured Pruning
Alpha 4 : Nij LUT and In Place PSUM	Complete	Complete	LUT design from optimising Nij from 36 to 16
Alpha 5 : FIFO Depth Reduction	Complete	Complete	FIFO Depth reduction from 64 to 16 and 8
Alpha 6 : Combined Part 2 + Part 3 (Part 4)	Complete	Complete	Added Control signal and updated MAC Tile to handle 4 bit and 2 bit Activations

			along with WS and OS modes. Update SPF , IFIFO , SRAM logic for the same
Alpha 7 : FPGA Mapping	Complete	In Progress	Actual Cyclone V FPGA implementation.
Alpha 8 : 2-bit Activation + 2-bit Weights	Complete	Addedly Newly for report and final submission	Modified Part 2. We Have designed 2 bit Activation and 2 bit Weight supported with 4 bit Activation and 4 bit weights in same design.