Flow Summary

<<Filter>>

Flow Status	Successful - Tue Dec 02 21:14:02 2025
Quartus Prime Version	20.1.0 Build 711 06/05/2020 SJ Lite Editio
Revision Name	core
Top-level Entity Name	core
Family	Cyclone V
Device	5CGXFC5C6F27C7
Timing Models	Final
Logic utilization (in ALMs)	6,407 / 29,080 (22 %)
Total registers	12049
Total pins	199 / 364 (55 %)
Total virtual pins	0
Total block memory bits	327,680 / 4,567,040 (7 %)
Total DSP Blocks	64 / 150 (43 %)
Total HSSI RX PCSs	0 / 6 (0 %)
Total HSSI PMA RX Deserializers	0 / 6 (0 %)
Total HSSI TX PCSs	0 / 6 (0 %)
Total HSSI PMA TX Serializers	0 / 6 (0 %)
Total PLLs	0 / 12 (0 %)
Total DLLs	0 / 4 (0 %)

Slow 1100mV 85C Model Fmax Summary

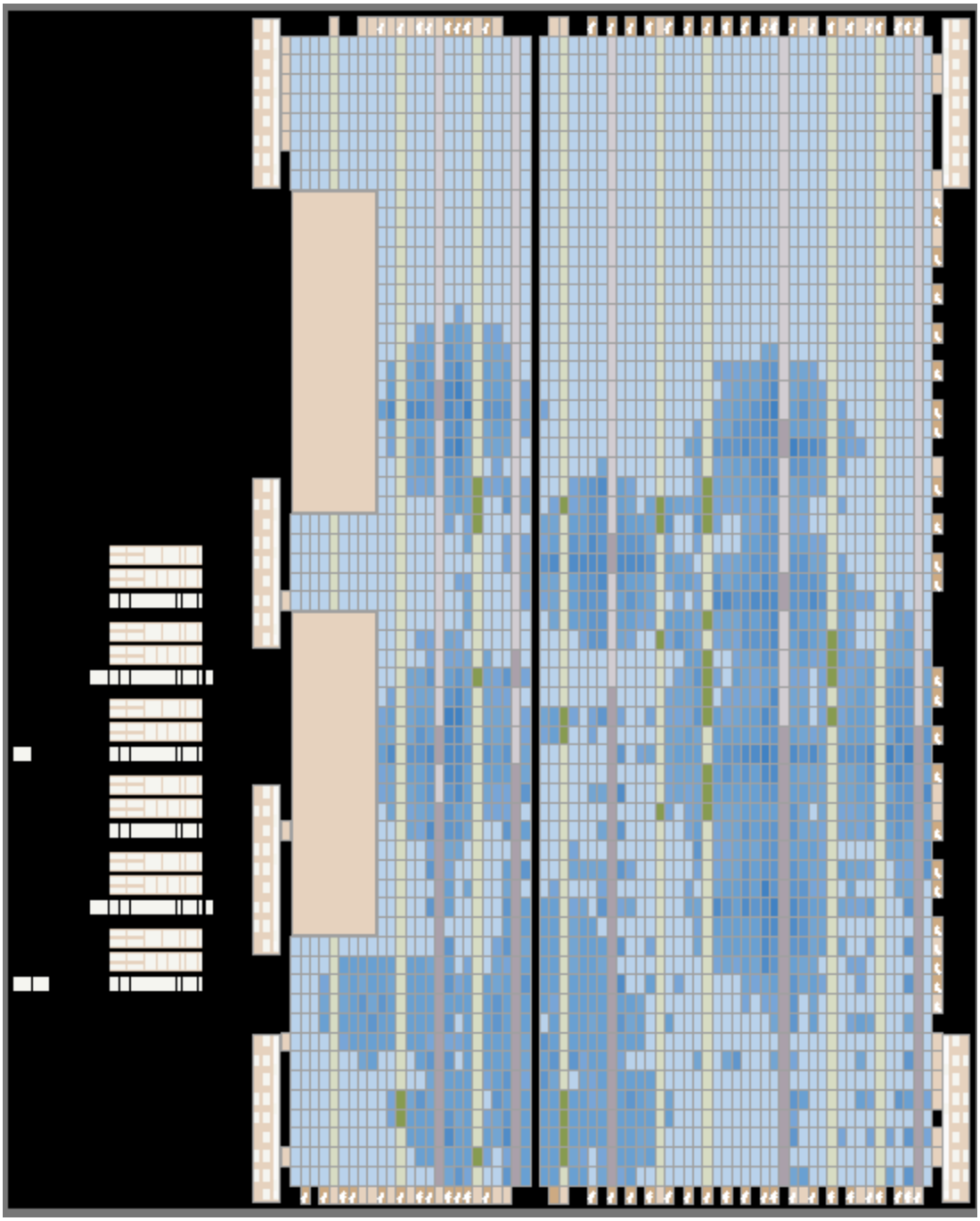
<<Filter>>

	Fmax	Restricted Fmax	Clock Name
1	99.29 MHz	99.29 MHz	clk

Power Analyzer Summary

<<Filter>>

Power Analyzer Status	Successful - Tue Dec 02 21:58:55 2025
Quartus Prime Version	20.1.0 Build 711 06/05/2020 SJ Lite Edition
Revision Name	core
Top-level Entity Name	core
Family	Cyclone V
Device	5CGXFC5C6F27C7
Power Models	Final
Total Thermal Power Dissipation	256.75 mW
Core Dynamic Thermal Power Dissipation	16.87 mW
Core Static Thermal Power Dissipation	227.32 mW
I/O Thermal Power Dissipation	12.56 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data



Top View - Wire Bond

Cyclone V - 5CGXFC5C6F27C7