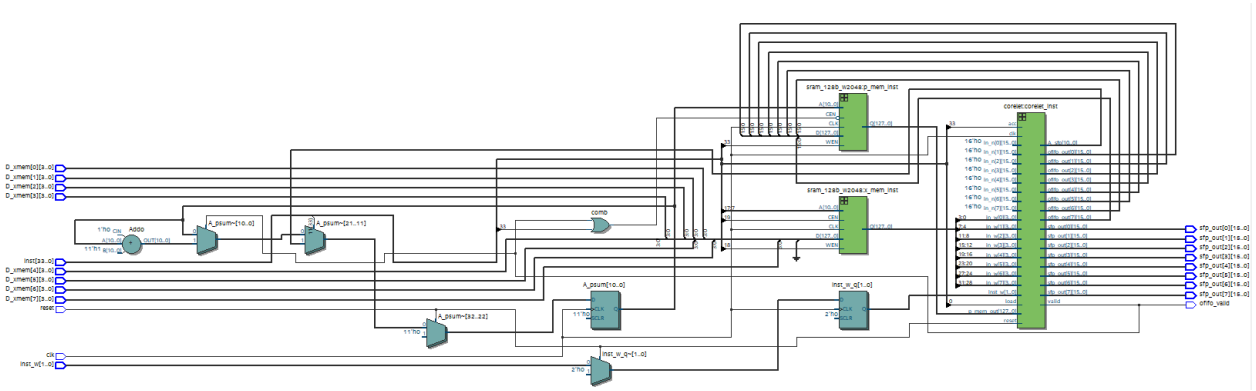
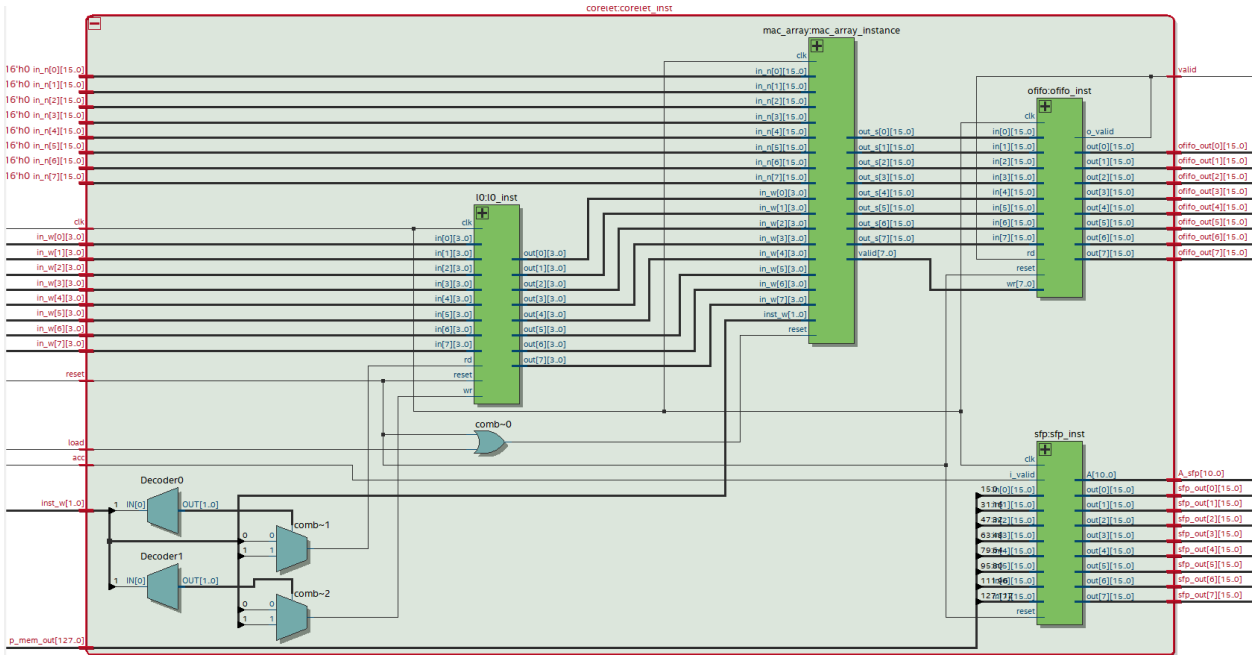
Design name: Vanilla Version (Part1)
Target Device: Cyclone IV GX



Top Level RTL of array



corelet

Logic Utilization/Memory

Fitter Summary

<<Filter>>

Fitter Status	Successful - Sat Dec 13 22:24:45 2025
Quartus Prime Version	20.1.0 Build 711 06/05/2020 SJ Lite Edition
Revision Name	corelet
Top-level Entity Name	corelet
Family	Cyclone IV GX
Device	EP4CGX30BF14C6
Timing Models	Final
Total logic elements	17,306 / 29,440 (59 %)
Total registers	12249
Total pins	0 / 81 (0 %)
Total virtual pins	562
Total memory bits	0 / 1,105,920 (0 %)
Embedded Multiplier 9-bit elements	0 / 160 (0 %)
Total GXB Receiver Channel PCS	0 / 2 (0 %)
Total GXB Receiver Channel PMA	0 / 2 (0 %)
Total GXB Transmitter Channel PCS	0 / 2 (0 %)
Total GXB Transmitter Channel PMA	0 / 2 (0 %)
Total PLLs	0 / 3 (0 %)

Analysis & Synthesis Resource Usage Summary

<<Filter>>

	Resource	Usage
1	Virtual pins	562
2	I/O pins	0
3		
4	DSP block 9-bit elements	0
5		
6	Maximum fan-out node	clk
7	Maximum fan-out	12249
8	Total fan-out	81869
9	Average fan-out	3.27

Max Frequency

Slow 1200mV 85C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name	Note
1	135.94 MHz	135.94 MHz	clk	

Power Estimates

Total Thermal Power Dissipation	244.05 mW
Core Dynamic Thermal Power Dissipation	34.93 mW
Core Static Thermal Power Dissipation	118.76 mW
I/O Thermal Power Dissipation	90.36 mW