Lab0：Verilog HDL 模擬器(Icarus Verilog 與 Vivado)之安裝與使用

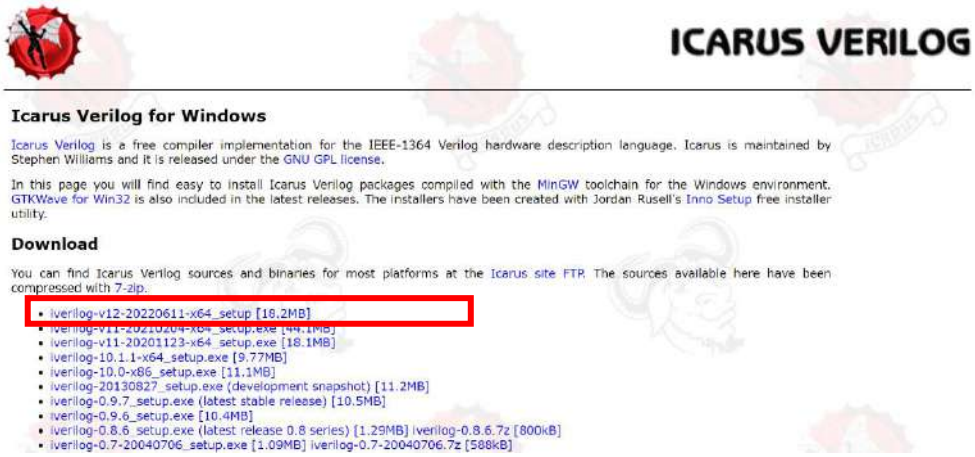
(The Setup and Use of Verilog Simulators, Icarus Verilog and Vivado)

A. Icarus Verilog (iVerilog) & GTKWave

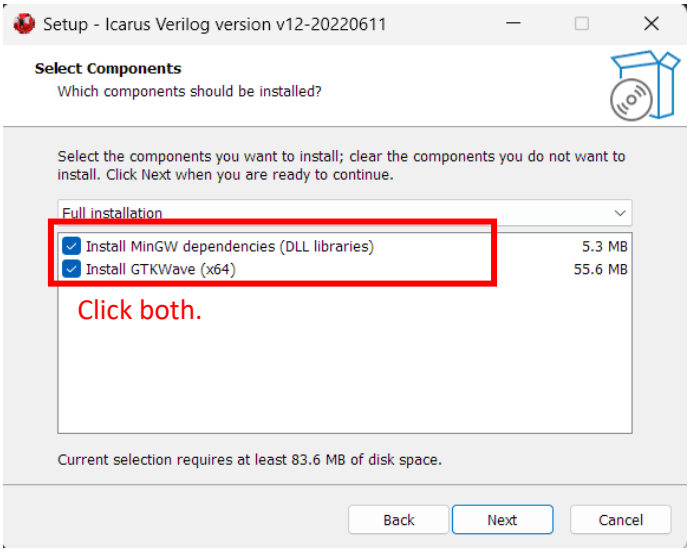
1. Windows 環境下的安裝 (Installation on Windows)

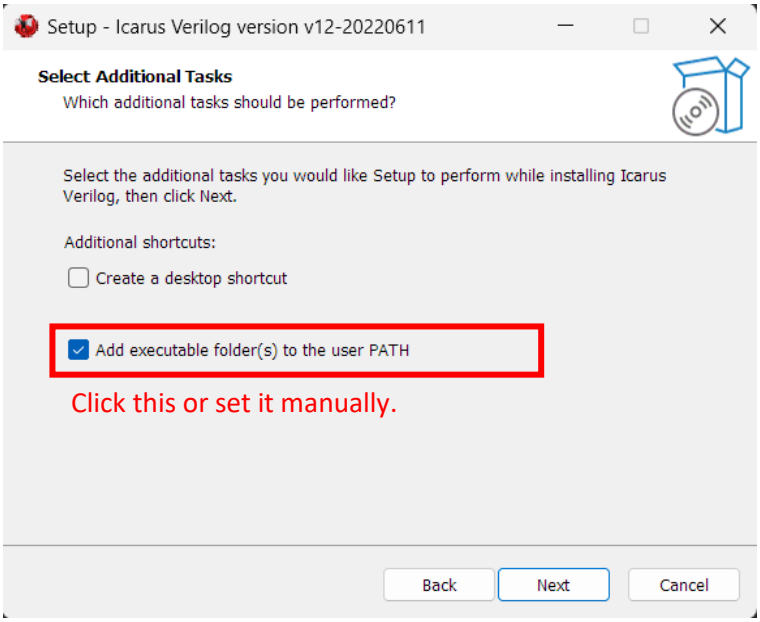
(a) 下載網址(Download here)：https://bleyer.org/icarus/

✓ 64 bit：iverilog-v12-20220611-x64_setup [18.2MB]



(b) 安裝步驟 (Installation Steps)

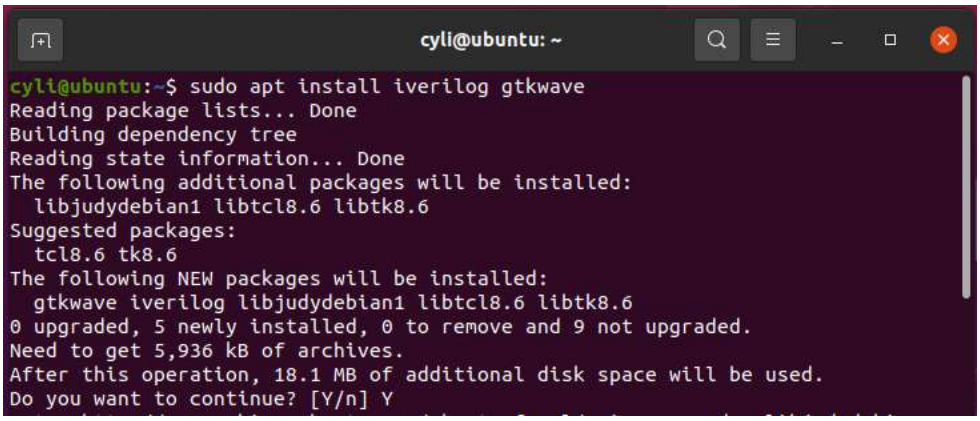




2. Linux 環境下的安裝 (Installation on Linux)

(a) Debian/Ubuntu 安裝 iVerilog & GTKWave (Install on Debian/Ubuntu)

✓ sudo apt install iverilog gtkwave



(b) Centos/Fedora 安裝 iVerilog & GTKWave (Install on Centos/Fedora)

✓ sudo yum install iverilog gtkwave

3. MacOS 環境下的安裝 (Installation on macOS)

(a) 安裝 iVerilog (Install iVerilog)

✓ Install Homebrew

$ /usr/bin/ruby -e "$(curl -fsSL https://raw.githubusercontent.com/Homebrew/install/master/install)"

✓ Install icarus-Verilog

$ brew install icarus-Verilog

✓ 版本過舊問題 (Version Error)

若安裝過程遇到 CLT (CommandLineTools) 版本過舊的問題，可以執行下面兩條指令解決

Following two commands can solve the CLT version Error

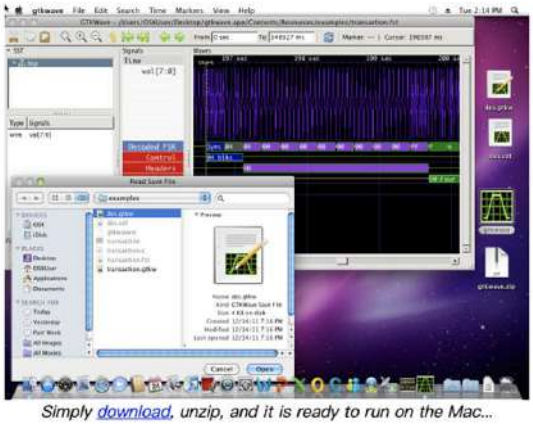
```
$ sudo rm -rf /Library/Developer/CommandLineTools
# 刪除原有的 CLT (delete own CLT)
$ sudo xcode-select --install        # 安裝新的 CLT (Install new CLT)
```

```
Error: Your CLT does not support macOS 11.2.
It is either outdated or was modified.
Please update your CLT or delete it if no updates are available.
```

(b) 安裝 GTKWave (Download GTKWave)

i. 下載網址 Download here：http://gtkwave.sourceforge.net/

點選 download (click **download**)



Simply download, unzip, and it is ready to run on the Mac...

ii. 解壓縮 gtkwave.zip，會看到應用程式 GTKWave

按住 **control**，打開 GTKWave

Unzip **gtkwave.zip** you'll see GTKWave.

Press **control** and open GTKWave.

iii. 接著會跳出警告視窗，點選打開
Click open on the warning window.

4. 撰寫 verilog 並編譯及執行的步驟 (Steps to compile Verilog code and run)

i. 使用任意文字編輯器撰寫 module 及 testbench 並將副檔名皆存成.v
Use any text editor to finish your module and testbench. Stores them as .v file
E.g. notepad++、VSCode…

ii. 撰寫 testbench 務必於 initial begin 之後加入
Remember to add following lines in testbench after initial begin
```
$dumpfile("filenameA.vcd");
$dumpvars;
```

iii. 打開命令提示字元，使用 cd [路徑]到達.v 所在資料夾
Open Command Prompt and move to the directory your .v files at
```
iverilog -o filenameB.vvp testbench_filename.v module_filename.v
vvp filenameB.vvp
gtkwave filenameA.vcd
```

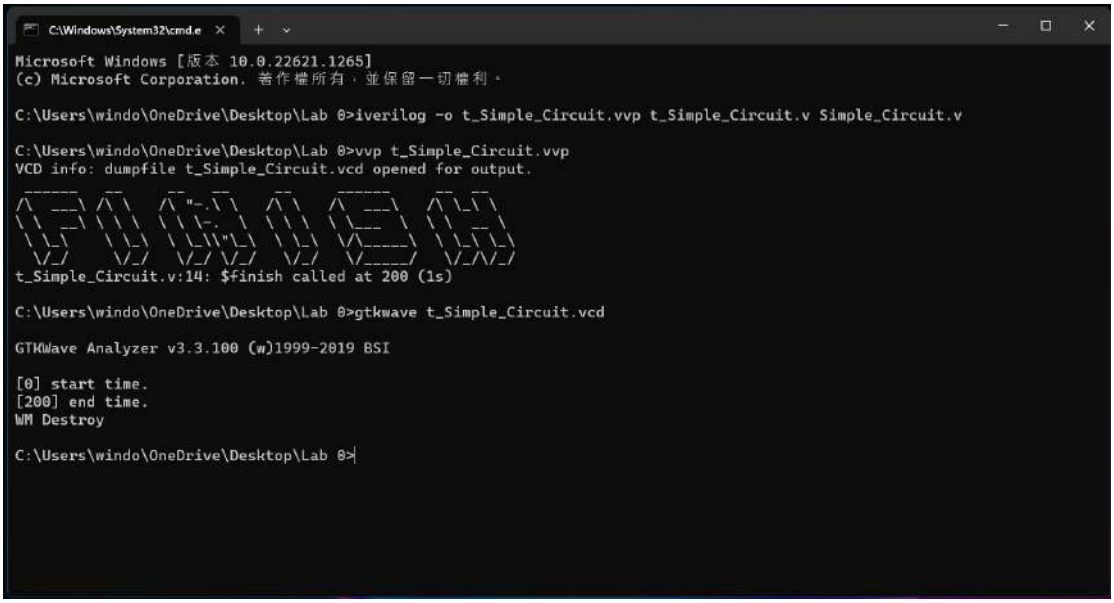
5. iVerilog 與 GTKWave 使用方式(Usage of iVerilog and GTKWave)

i. 下載 提供的兩個檔案: Simple_Circuit.v 和 t_Simple_Circuit.v
Download files provided on E3 (Simple_Circuit.v & t_Simple_Circuit.v)

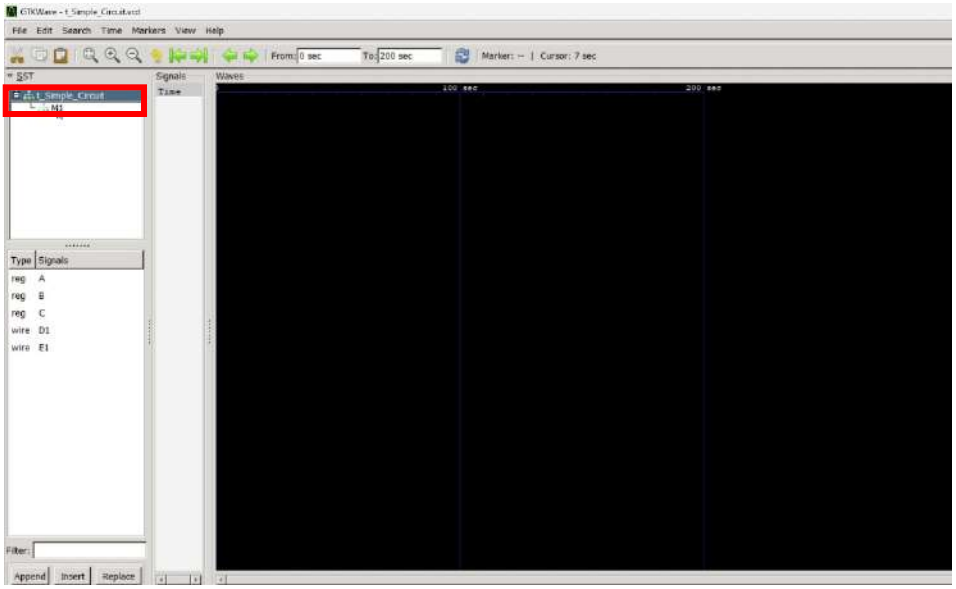
ii. 打開「命令提示字元」(終端機)
Open **Command Prompt**

iii. 使用 cd [路徑]到達 Simple_Circuit.v 和 t_Simple_Circuit.v 所在資料夾
Move to the directory your files at by using “cd <path>”.

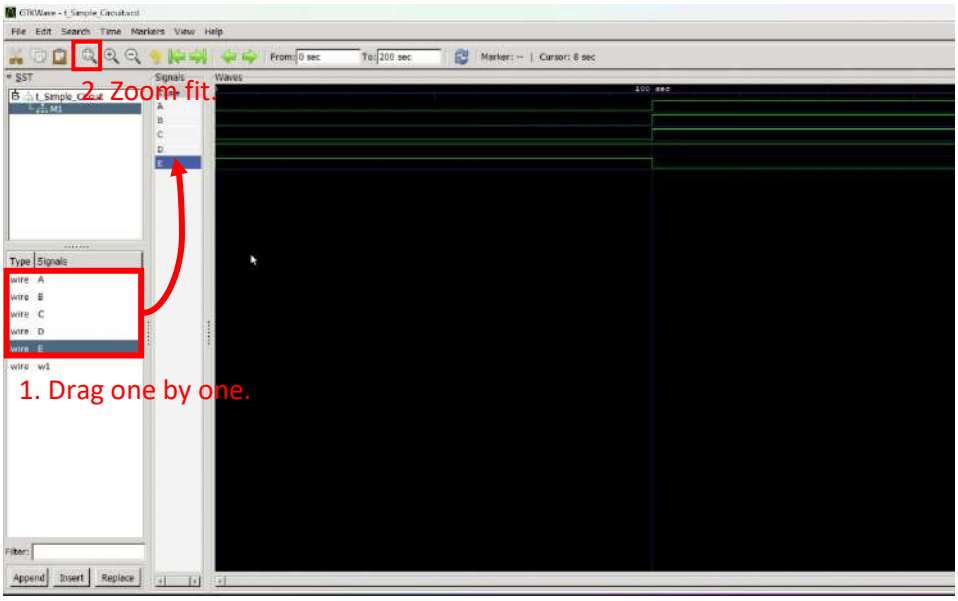
- ✓ iverilog -o t_Simple_Circuit.vvp t_Simple_Circuit.v Simple_Circuit.v
- ✓ vvp t_Simple_Circuit.vvp
- ✓ gtkwave t_Simple_Circuit.vcd



iv. GTKWave 視窗出現之後，點選 t_Simple_Circuit 旁邊的 ＋ 並點選 M1。
Click + next to t_Simple_Circuit and click M1.



vi. 將下方出現的五個變數拖至右側 Signals 欄。
點選左上方的  讓波型以最適合螢幕大小的方式顯示。
Drag variables below to the **Signals** section.
Click  so the waveform fit the window size properly.

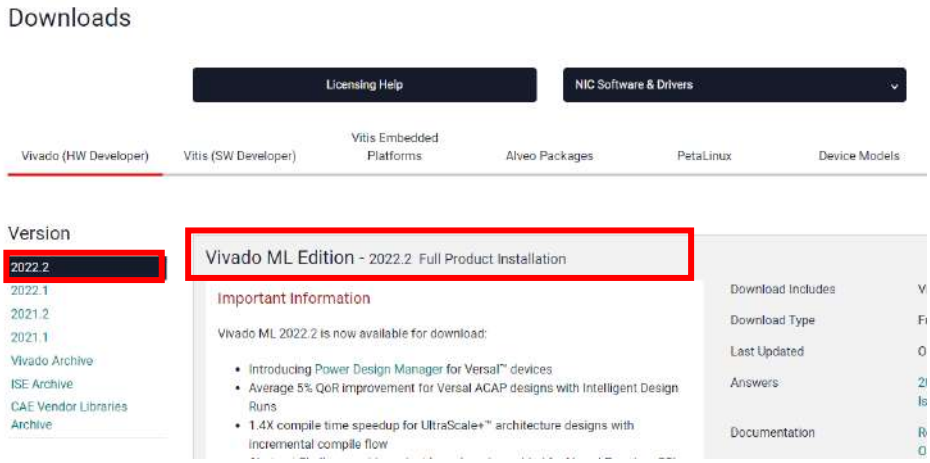


B. Vivado

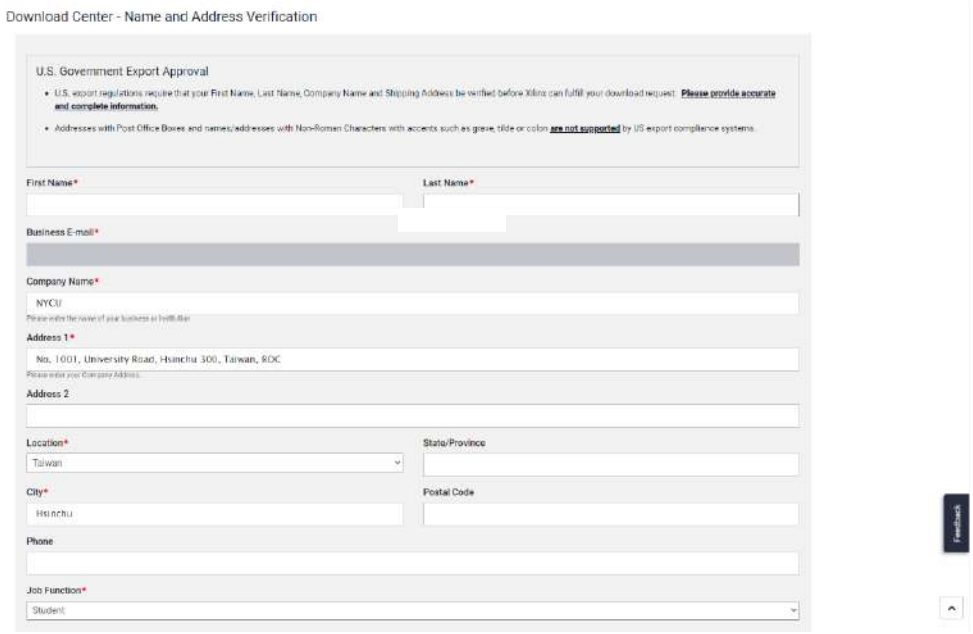
需在 Windows 系統下使用 (Only available on Windows)

1. Vivado 之下載及安裝 (Download and Installation of Vivado)

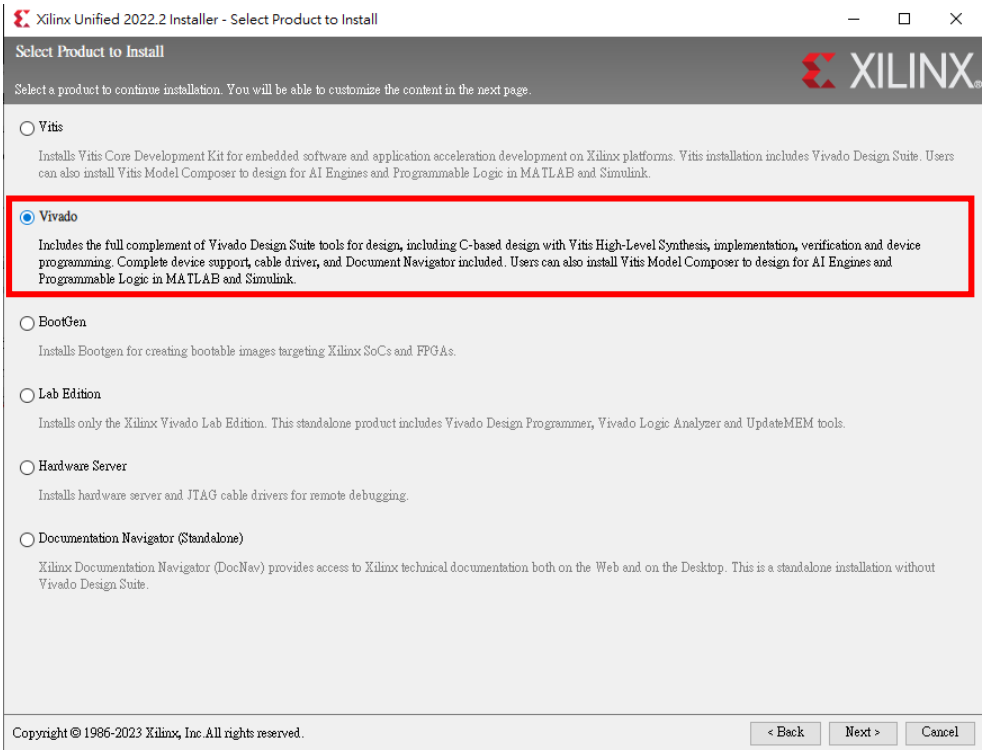
(a) 連結至「https://www.xilinx.com/support/download.html」，如下圖所示，並確定下載的是 2022.2 版本。
Connect to https://www.xilinx.com/support/download.html, and the following page will be shown, be sure to download 2022.2 version.



(b) 登入 Xilinx；若無帳號，則以學校的電子郵件註冊之。填寫認證資料。
Sign in to Xilinx, or register one with school's email if you don't have an account. Fill out your personal information in the page.

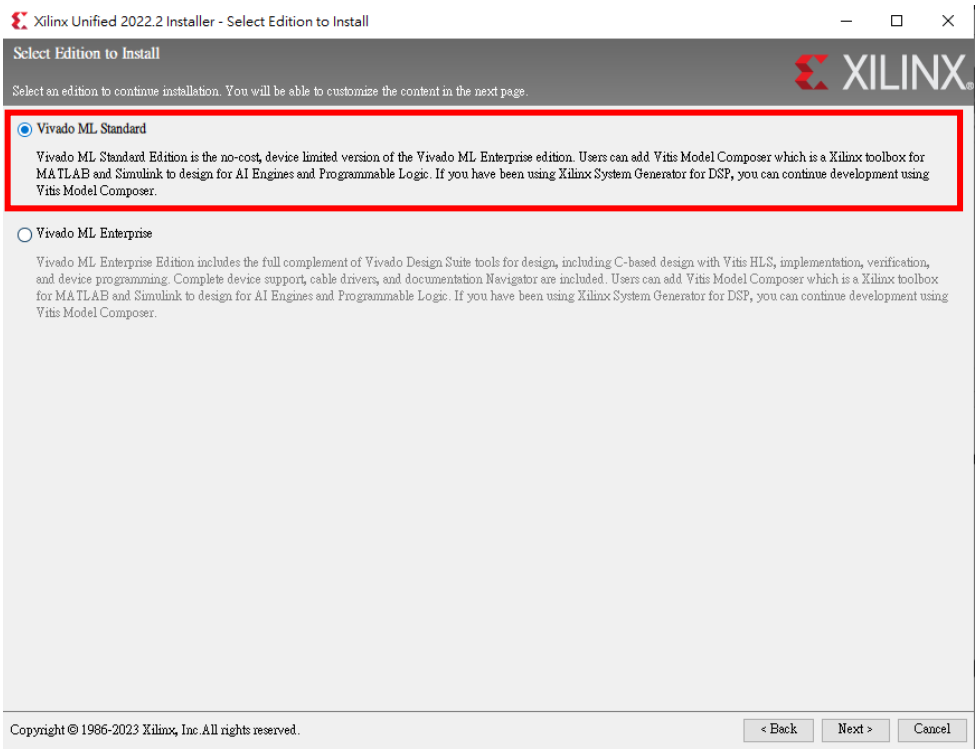


(c) 執行安裝程式。在產品選擇時選擇 Vivado。
Start to install. Choose Vivado at "Select Product to Install".



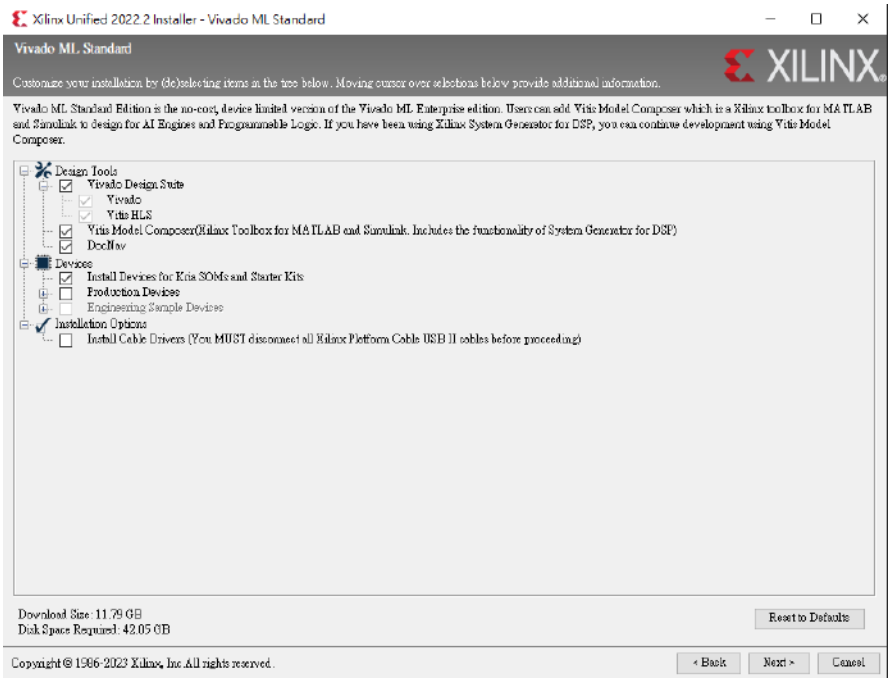
(d) 選擇版本時，請選 Vivado ML Standard Edition。

Choose Vivado ML Standard Edition at “Select Edition to Install”.



(e) 之後的選擇如下圖所示。因為這門課不會連到板子，所以 Device 可以任選一個。

After that, click your selection as shown in the following figure. Since we will not connect to any board in this course, you may choose any listed in the “Devices” part, and at least one should be selected.

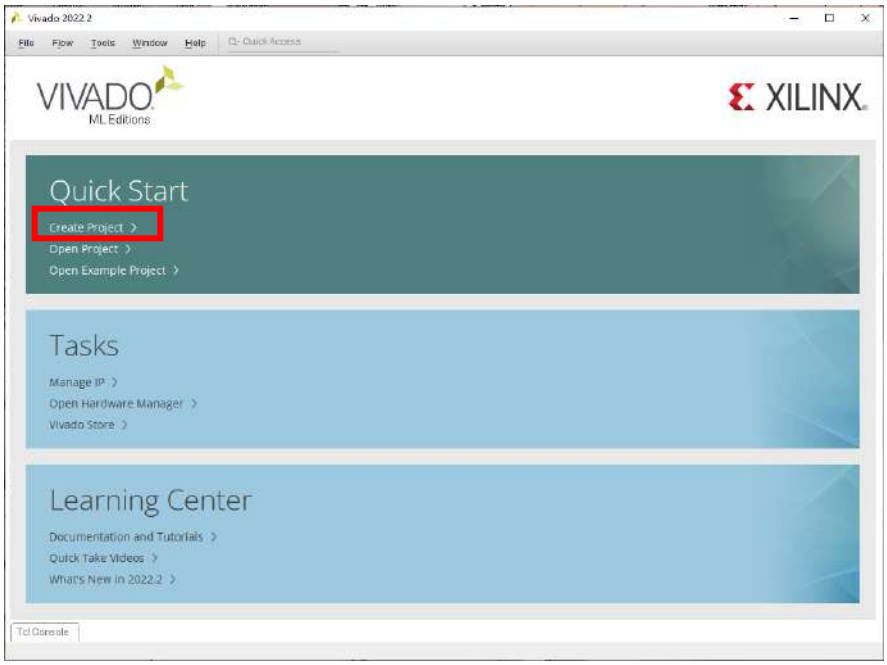


2. Vivado 之專案建立、程式編譯及執行模擬
(Project Creation, Program Compilation and Simulation in Vivado)

(a) 建立專案 (Project Creation)

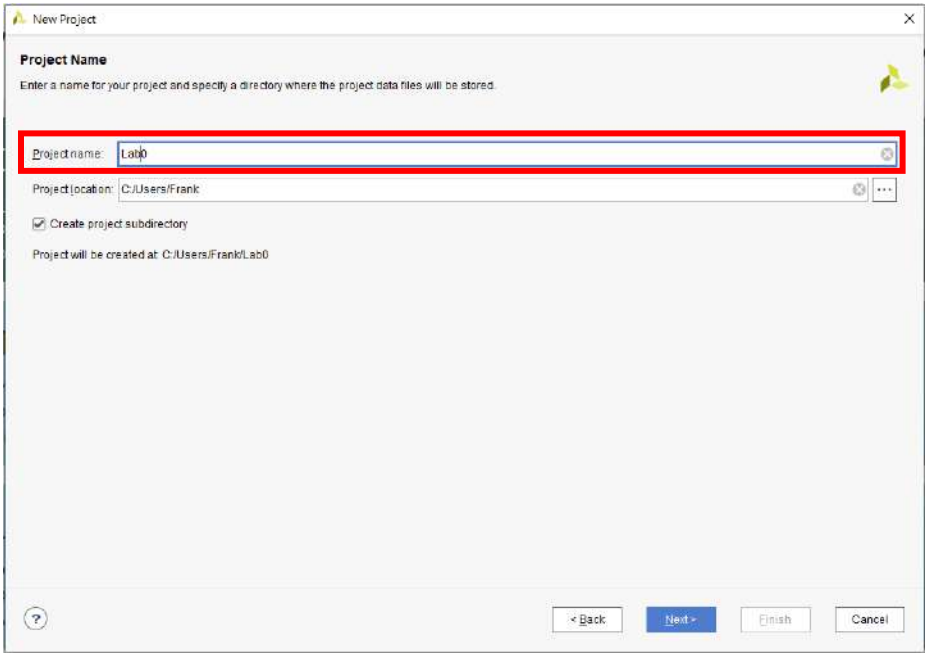
i. 新增專案。

Create a new project.



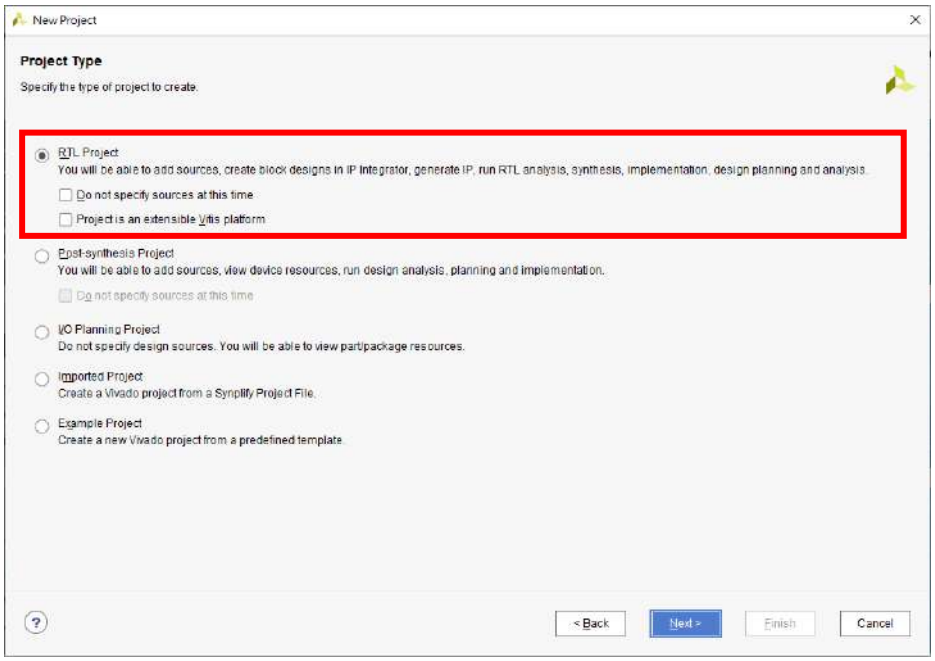
ii. 填寫專案名稱。

Name the new project.



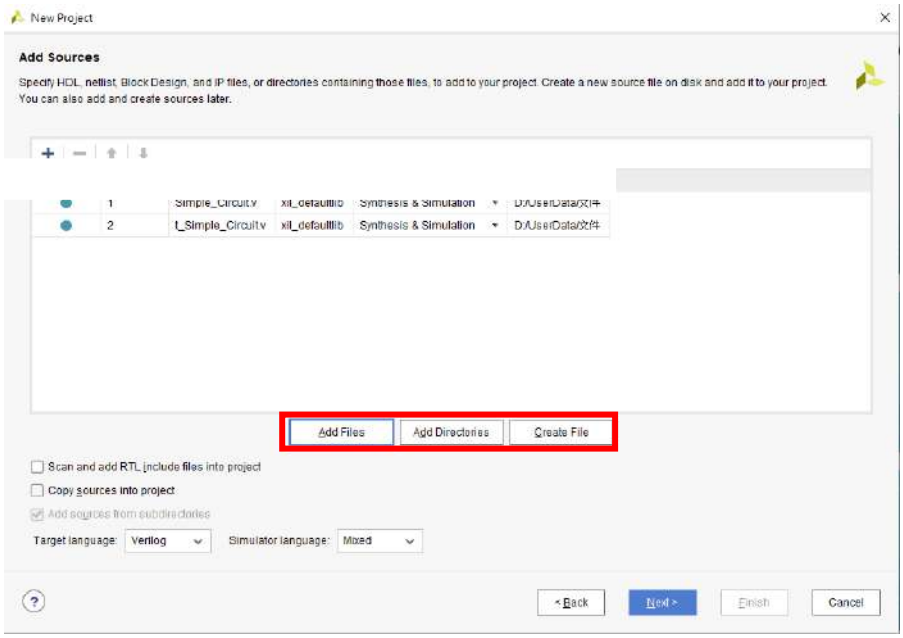
iii. 專案類型選擇 RTL Project。

Choose RTL Project at “Project Type”.

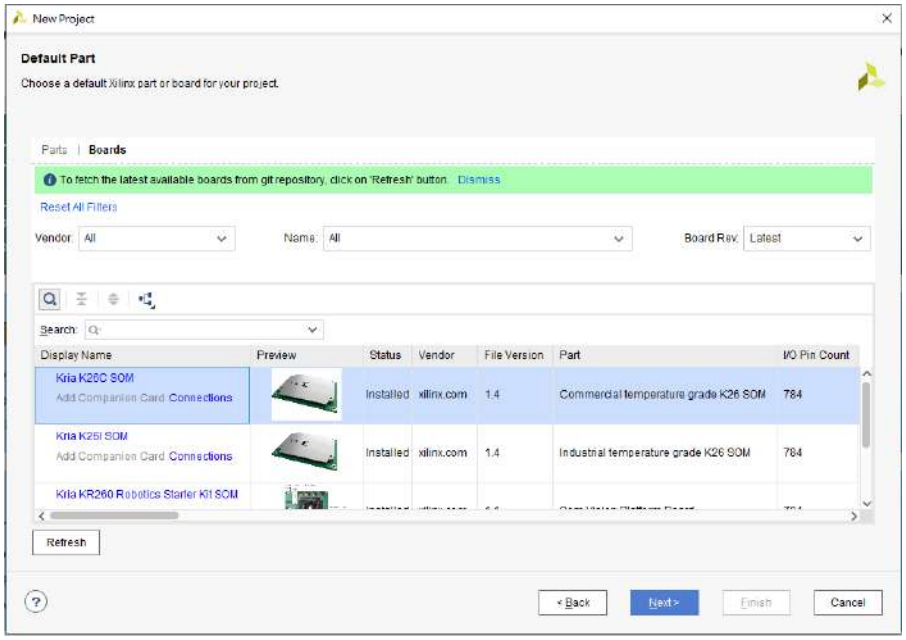


iv. 加入相關檔案或創建檔案

Add source files or create new files.

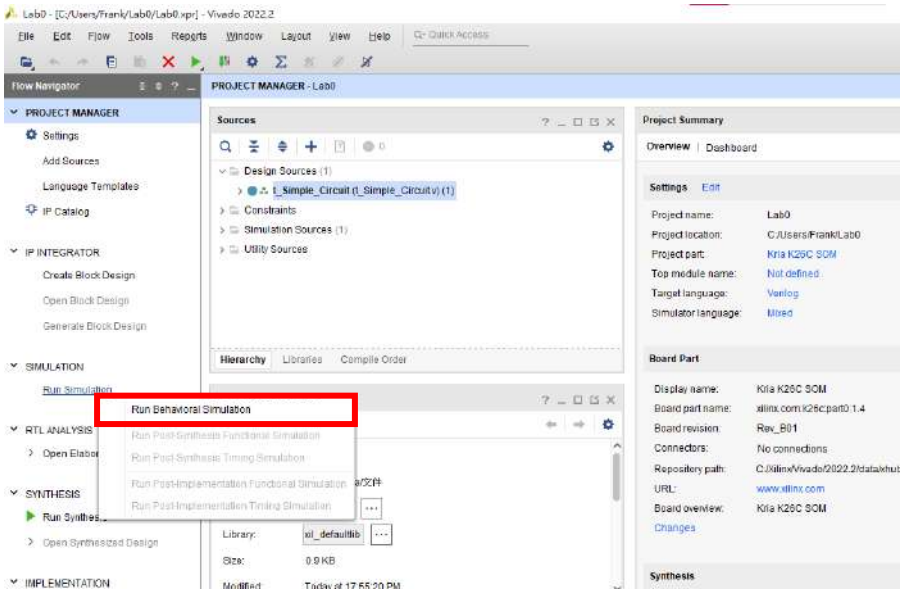


v. 任意選擇一個 Part/Board 作為 Default Part。
Choose any one of part/board in the “Default Part”.



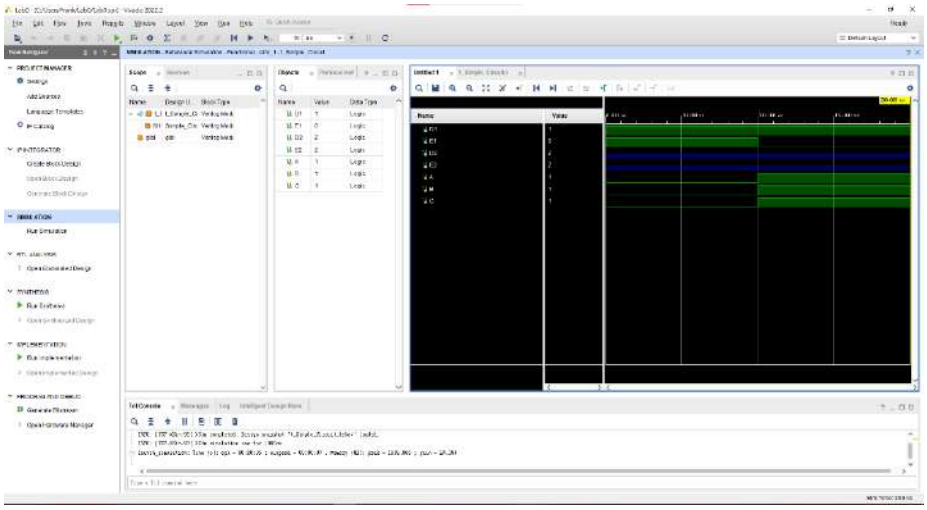
(b) 執行模擬 (Simulation)

i. 按下畫面左方工具列的 Run Simulation > Run Behavioral Simulation
Click Run Simulation > Run Behavioral Simulation.



ii. 完成模擬，觀察結果之波形圖。

Complete simulation and observe the waveform of simulation results.



注意：所有作業將使用 iVerilog 來進行批改，Lab Demo 環境也僅提供 iVerilog/GTKWave 給同學進行操作。同學仍然可以使用 Vivado 作為撰寫程式時所使用的 IDE，但必須熟悉如何通過指令操作 iVerilog，並確保繳交的程式碼能夠在 iVerilog 中正常運作。

Warning: We will use iVerilog to test your code, and the demo environment only provides iVerilog/GTKWave. You can still use Vivado as your IDE, but you must be familiar with how to operate iVerilog through the terminal and make sure your code could run correctly in iVerilog.