數位電路設計

Lab3 – 同步循序電路之 HDL 模組撰寫與測試

(Writing and Testing HDL Modules of Synchronous Sequential Circuit)

1. 目標(Goal)

在這次 Lab 中，我們希望同學們可以熟悉 Latch、正反器、同步循序電路的設計原理。以 **state-diagram-based model** 與 **structural model** 等不同方式撰寫同步循序電路之 Verilog HDL 電路模組，並撰寫測試模組。分別模擬後，繳交模組檔案與波形圖。

The main purpose of this Lab Unit is to be familiar with the design of latch, flip-flop, and synchronous sequential circuit. Please write the Verilog HDL circuit modules of synchronous sequential circuits by **state-diagram-based model** and **structural model**, and write the testbench for these circuit modules. After simulation, upload the files of the modules and the waveforms of the simulation results.

2. 撰寫 HDL 電路模組與測試模組(Design of the HDL Circuit Modules and Testbench)

A. D Latch with Control Input: 下圖為有控制輸入的 D Latch 之電路圖，請設計其 Verilog HDL 電路模組。

The circuit diagram of a D Latch with control input is shown in the following figure. Please write the Verilog circuit module for it.

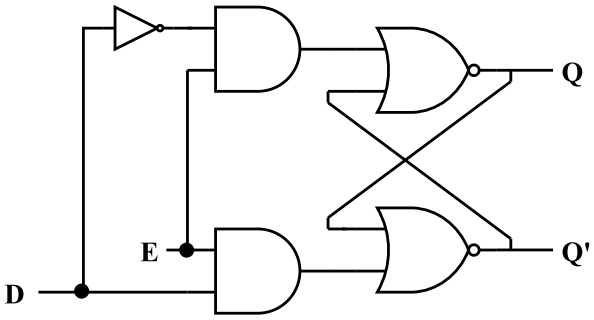

圖 1：具控制輸入的 D Latch 之電路圖

Figure 1: The circuit diagram of a D Latch with control input.

(a) 請根據上述電路圖(圖 1)，以 ***gate-level*** modeling 的方式撰寫其電路模組。假設每個 NOT、AND 及 NOR gate 的傳遞延遲皆為 1 ns。模組名稱與 port list 請訂為 Lab3_D_Latch_gatelevel (input D, E, output Q, Qb)，檔案則請命名為 Lab3_D_Latch_gatelevel.v。

According to the logic diagram shown in Figure 1, please write the Verilog circuit module in ***gate-level*** modeling. Assume that the propagation delay of each NOT, AND and NOR

gate is 1 ns. The circuit module and port list should be named as Lab3_D_Latch_gatelevel (input D, E, output Q, Qb), and its file should be named as Lab3_D_Latch_gatelevel.v.

(b) 請撰寫此 D Latch 之測試電路模組，必須至少包含下述指定之測資。請將此測試電路模組命名為 t_Lab3_D_Latch_gatelevel，檔案則命名為 t_Lab3_D_Latch_gatelevel.v。
Please write the testbench of the D Latch in which the test data shown in the following table must be included. The testbench module should be named as t_Lab3_D_Latch_gatelevel, and its file should be named as t_Lab3_D_Latch_gatelevel.v.

Time (ns)	D	E
0	0	0
5	0	1
10	0	0
15	1	0
20	1	1
25	0	0
30	0	1
35	0	0
50	1	1
51	1	0

B. Master-Slave D Flip-Flop: 下圖為一個 master-slave D flip-flop，請設計其 Verilog HDL 電路模組。
The circuit diagram of a master-slave D flip-flop is shown in the following figure. Please design the Verilog circuit module for it.

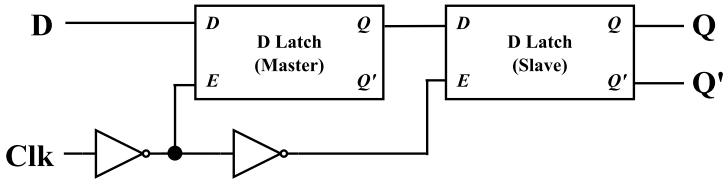

圖 2：Master-Slave D flip-flop 電路圖
Figure 2: The circuit diagram of a master-slave D flip-flop.

(a) 請根據上述電路圖(圖 2)，利用 A(a)的 module，以 ***gate-level*** modeling 的方式撰寫其電路模組。假設每個 NOT gate 的 delay 為 1 ns。模組名稱與 port list 請訂為 Lab3_D_FF_gatelevel(input D, Clk, output Q, Qb)，檔案則請命名為 Lab3_D_FF_gatelevel.v。
According to the logic diagram shown in Figure 2, please write the Verilog circuit module in ***gate-level*** modeling by using the module in A(a). Assume that the delay of a NOT gate is 1 ns. The circuit module and port list should be named as Lab3_D_FF_gatelevel(input D, Clk, output Q, Qb), and its file should be named as Lab3_D_FF_gatelevel.v.

(b) 請撰寫此 D flip-flop 之測試電路模組，時脈週期為 10 ns (先 5 ns 為 LOW、再 5 ns 為 HIGH)，且至少必須包含下述指定之測資。請將此測試電路模組命名為 t_Lab3_D_FF_gatelevel，檔案則命名為 t_Lab3_D_FF_gatelevel.v。

Please write the testbench of this D flip-flop in which the test data shown in the following table must be included. The period of the clock is 10 ns, LOW for 5 ns and then HIGH for 5 ns. The testbench should be named as t_Lab3_D_FF_gatelevel, and its file should be named as t_Lab3_D_FF_gatelevel.v.

Time(ns)	D
0	0
7	1
17	0
37	1
47	0
57	1
77	0
81	1

C. Mealy-Type Synchronous Sequential Circuit: 設計一個 ***Mealy-type*** 的同步循序電路，此電路為 Excess-3 轉 BCD 轉換器，有一個輸入變數(X)、一個輸出變數(Z)。此電路從最低有效位(least significant bit)開始，將欲轉換的 Excess-3 數字的每個位元輸入至 X，並從最低有效位開始，將轉換後的 BCD 數字的每個位元輸出至 Z。圖 3 為此順序電路之狀態圖(state diagram)，表 1 為其狀態表(state table)，表 2 為輸入輸出之範例。狀態 S_0 是電路的初始狀態。在本電路的設計中無需考慮 delay 的問題。

Design a ***Mealy-type*** synchronous sequential circuit which is an **Excess-3-to-BCD converter** with one input variable X and one output variable Z. This circuit sequentially inputs each bit of the Excess-3 number to be converted, starting from the least significant bit, into X, and sequentially outputs each bit of the converted BCD number, starting from the least significant bit, to Z. The state diagram of the sequential circuit is shown in Figure 3, its corresponding state table is shown in Table 1, and an example of its input/output is shown in Table 2. State S_0 is the initial state of the circuit. There is no need to consider the issue of delay in the design of this circuit.

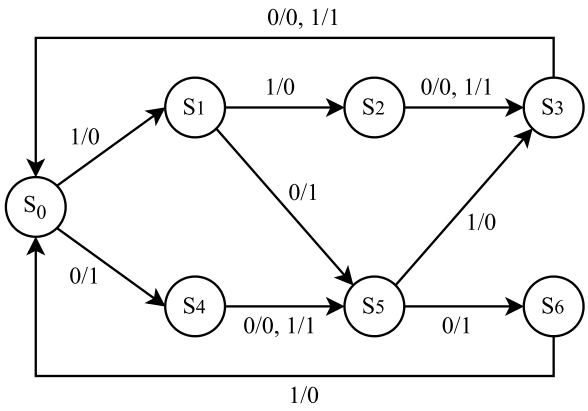

圖 3：Excess-3 轉 BCD 轉換器之狀態圖

Figure 3: The state diagram of the Excess-3-to-BCD converter

Present State	Next State		Output	
	X = 0	X = 1	X = 0	X = 1
S_0	S_4	S_1	1	0
S_1	S_5	S_2	1	0
S_2	S_3	S_3	0	1
S_3	S_0	S_0	0	1
S_4	S_5	S_5	0	1
S_5	S_6	S_3	1	0
S_6	-	S_0	-	0

表 1：Excess-3 轉 BCD 轉換器之狀態表

Table 1: The state table of the Excess-3-to-BCD converter.

Time	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	…
X	1	0	1	0	1	1	0	1	…
Z	0	1	0	0	0	0	0	1	…

表 2： Excess-3 轉 BCD 轉換器之輸入輸出範例

(說明：$1011\ 0101_{\text{Excess-3}} = 1000\ 0010_{\text{BCD}}$)

Table 2: An input/output example of the Excess-3-to-BCD converter

(Explanation: $1011\ 0101_{\text{Excess-3}} = 1000\ 0010_{\text{BCD}}$)

(a) 請根據此電路之狀態圖(圖 3)或狀態表(表 1)，以 **state-diagram-based** model 方式撰寫其 Verilog HDL 電路模組。各狀態之二元編碼為 $S_0 = 000$, $S_1 = 001$, $S_2 = 010$, $S_3 = 011$, $S_4 = 100$, $S_5 = 101$, $S_6 = 110$。假設此同步順序電路為正緣觸發(於 *Clk* 之正緣改變狀態)，且有 *Rst* 輸入訊號；*Rst* 為 Active LOW 的 reset 訊號，可設定電路至初始狀態 S_0 (000)。模組名稱與 port list 請訂為 Lab3_Converter_state_diagram (input X, Clk, Rst, output Z)，檔案則請命名為 Lab3_Converter_state_diagram.v。

According to the state diagram shown in Figure 3 or the state table shown in Table 1, write the Verilog circuit module for this synchronous sequential circuit by **state-diagram-based** model. The binary assignment of the states are $S_0 = 000$, $S_1 = 001$, $S_2 = 010$, $S_3 = 011$, $S_4 = 100$, $S_5 = 101$, $S_6 = 110$. Assume that this circuit is positive-edge triggered (changes state on the positive edge of *Clk*) and has an active-LOW *Rst* signal which resets the circuit to its initial state S_0 (000). The circuit module and port list should be named as Lab3_Converter_state_diagram (input X, Clk, Rst, output Z), and its file should be named as Lab3_Converter_state_diagram.v.

(b) 完成此同步順序電路之設計，以 D flip-flop 做為其儲存元件。根據推導出之電路圖，以 **structural model** 方式撰寫其 Verilog HDL 電路模組。各狀態之二元編碼同(a)所訂。假設此電路有 *Rst* 輸入訊號，可設定電路至初始狀態 S_0 (000)。模組名稱與 port list 請訂為 Lab3_Converter_structure (input X, Clk, Rst, output Z)，檔案則請命名為 Lab3_Converter_structure.v。請注意，此電路模組中需要用到有 asynchronous reset (又稱 direct reset) 之 D flip-flop 的電路模組，可自行撰寫或使用課本上之模組，模組名

稱與 port list 請訂為 D_FF_AR (input D, Clk, Rst, output Q)，檔案請命名為 D_FF_AR.v。此 flip-flop 為正緣觸發，*Rst* 為 Active-LOW 的 reset 訊號。

Complete the design of this synchronous sequential circuit by using D flip-flops. According to the circuit diagram derived, write the Verilog circuit module for this circuit by **structural model**. The binary assignments of the states are the same as that defined in (a). Assume that the circuit can be reset to its initial state S_0 (000) by input signal *Rst*. The circuit module and port list should be named as Lab3_Converter_structure (input X, Clk, Rst, output Z), and its file should be named as Lab3_Converter_structure.v . Note that this circuit module requires to instantiate the circuit module of a D flip-flop with *asynchronous reset*, also called as *direct reset*. You may design the D flip-flop module by yourself or apply the module provided in the textbook. The module and port list of the D flip-flop should be named as D_FF_AR (input D, Clk, Rst, output Q), and its file should be named as D_FF_AR.v. Assume that the flip-flop is positive-edge triggered and *Rst* is an active-LOW reset signal.

(c) 請撰寫一測試模組來充分測試上述兩個電路模組。請將此測試模組命名為 t_Lab3_Converter，檔案則請命名為 t_Lab3_Converter.v。

Please write a testbench to test the two circuit modules designed above sufficiently. The testbench module should be named as t_Lab3_Converter, and its file should be named as t_Lab3_Converter.v .

*** 注意事項：**

- 請用 Icarus Verilog 作為編譯器，以 vvp 執行，並以 GTKWave 觀察波形圖。
  Please compile your Verilog code by Icarus Verilog, execute the compiled code by vvp, and then observe the waveform by GTKWave.
- 請務必依照上述各項目之規定命名模組及檔案，違者至少扣 10 分。
  Be sure to name the modules and files as described above; otherwise, there will be 10 points penalty on your score at least.
- 禁止抄襲，違者(抄襲者與被抄襲者)以 0 分計算。
  Any assignment work by fraud will get a zero point.
- 助教會以其他測資去測試上述作業。
  TA will use similar testbench modules with different test data to verify the correctness of your design of the Verilog circuit modules.

3. 作業及 HDL 模組繳交(Hand in)

A. 作業報告繳交：pdf 檔，命名為 Lab3_學號

包含下列項目：

Hand in a pdf file, named Lab3_StudentID, including the following items:

(1) 2A 之模擬結果波形圖，並說明其模擬結果波形圖是否正確。若有輸出在 0 和 1 之間振盪的情況發生，請簡述理由。(20%)

Give the waveform of the simulation results in 2A, and explain whether it is correct or

not. If there is a situation where the output oscillates between 0 and 1, please briefly explain the reason.

(2) 2B 之模擬結果波形圖，觀察此 flip-flop 在何時改變狀態，並說明其模擬結果波形圖是否正確。(20%)
Give the waveform of the simulation results in 2B, observe when the flip-flop changes state, and explain whether the waveform is correct or not.

(3) 敘述 2C 之 Mealy-type 同步順序電路之設計過程，以 D flip-flop 為儲存元件，推導出 flip-flop input equations 及 output equation，並畫出其電路圖。而後，列出 2C 之模擬結果波形圖，並說明其 testbench 如何設計、針對 input stimulus 預期之狀態轉換與輸出值為何、及(a)與(b)兩種電路模組之模擬結果波形圖是否正確。(50%)
Describe the design of the Mealy-type synchronous sequential circuit in 2C by using D flip-flops based on the design procedure of synchronous sequential circuits. Derive the flip-flop input equations and output equation, and draw the logic circuit diagram of the circuit by using D flip-flops as basic building blocks. Then, give the waveform of the simulation results in 2C, explain how you design your testbench, show the state transitions and outputs for the input stimuli, and determine whether each of the two circuit modules designed by you is correct or not.

(4) 心得與感想、及遭遇到的問題或困難 (10%)
Describe what you have learned from this lab unit and discuss the problems or difficulties encountered in this lab.

B. Verilog modules 檔案繳交：eight .v files

Hand in the following Verilog modules: 8 .v files

Lab3_D_Latch_gatelevel.v、t_Lab3_D_Latch_gatelevel.v、
Lab3_D_FF_gatelevel.v、t_Lab3_D_FF_gatelevel.v、
Lab3_Converter_state_diagram.v、Lab3_Converter_structure.v、D_FF_AR.v、
t_Lab3_Converter.v

4. DEADLINE

- 本實驗單元為一人一組， 作業請上傳至 E3 平台。
  This lab unit is one student per group. Please upload your Lab Report (pdf file) and the corresponding HDL code (.v files) onto e-Campus platform.
- 請將上述作業報告及 Verilog 電路模組與測試模組檔案(.v)全部壓縮成一個 **zip 檔** (禁止上傳 rar 檔或是其他檔案格式)，並以「Lab3_學號」的方式命名，如：「Lab3_1111550001」。壓縮檔案時，**請選取好要求繳交的檔案執行壓縮，不要對整個資料夾壓縮。**
  Please compress the pdf file of lab report and the Verilog circuit modules and testbench described above all into one **zip** file (rar file or other format is not accepted), and name the zip file as "Lab3_StudentID", for example, "Lab3_111550001". When compressing files, please **select the requested files for compression**, and **do not compress the entire directory**.

- **作業繳交最後截止日期**為 **2023/6/11 (日) 23:55**。**不接受逾期繳交**。
  The final deadline for handing in lab report and Verilog files is **2023/6/11 (Sun) 23:55. No late hand-in is allowed.**
- **上機演示 Demo 時間**暫定為 **2023/6/6 (二)** 與 **2023/6/13 (二)** 兩天，之後會再發公告通知大家上網填寫 Demo 時間表。**若選擇 2023/6/6 Demo，則必須在 2023/6/4 (日) 23:55 前繳交作業**。
  The dates for **on-site demo** are arranged at **2023/6/6 (Tue)** and **2023/6/13 (Tue)** tentatively, and we will send an announcement to inform you to fill the Demo schedule online. **Students who register to Demo on 2023/6/6 (Tue) should submit their lab reports and Verilog files to e3 before 2023/6/4 (Sun) 23:55.**
- **未繳交作業者，將不予 Demo；有繳交作業但未 Demo 者，亦不予計分**。
  Those who have not hand-in their lab reports and Verilog files will not be able to demo their work, and those who have not demoed will not be scored neither.
- 程式碼請勿抄襲別人或讓別人抄襲，經查證後此次 lab 總分一律以 0 分計算。
  Any assignment work by fraud will get a zero point.