

Xilinx Vivado Installation Tutorial

Note

- The tool which we used in this class was usually Modelsim, but it is currently unavailable due to US federal regulations. We don't know when it will be available again. As a result, we choose to use Xilinx Vivado this semester.
- Xilinx Vivado is the same as Modelsim, which they only support **Windows** and **Linux** operating systems. For those who use MAC OS, we recommend you to install virtual machine with Windows or Linux OS and install Xilinx Vivado.
- The following installation tutorial is for Windows. You can install it on Linux OS, too.

Step 1

- Goto <https://www.xilinx.com/support/download.html>
- Download **Xilinx Unified Installer 2022.2: Windows Self Extracting Web Installer**

Windows

📄 Xilinx Unified Installer 2022.2: Windows Self Extracting Web Installer
(EXE - 209.61 MB)

MD5 SUM Value : 985168f6920c5ee2111c5d16573330e1

Download Verification ⓘ

Digests

Signature

Public Key

Linux

📄 Xilinx Unified Installer 2022.2: Linux Self Extracting Web Installer (BIN -
271.02 MB)

MD5 SUM Value : 9bf473b6be0b8531e70fd3d5c0fe4817

Download Verification ⓘ

Step2

- Create and activate an account



The AMD Login Form features the AMD logo at the top. Below it is the title "登入" (Login). The form includes two input fields: "電子郵件地址" (Email Address) and "密碼" (Password). A "登入" (Login) button is positioned below the password field. At the bottom, there is a "創建密碼" (Create Password) button and a link for "忘記/重設密碼?" (Forgot/Reset Password?). At the very bottom, there are links for "幫助" (Help), "隱私權" (Privacy), and "使用條款" (Terms of Use).



The AMD Account Creation Form is titled "AMD 帳戶創建" (AMD Account Creation). It includes instructions: "如需創建帳戶，請填寫以下表格。" (To create an account, please fill out the following form.) and "帶有訪問令牌的帳戶激活消息將通過電子郵件發送至您在下方預留的電子郵件地址。" (Account activation messages with access tokens will be sent via email to the email address you provide below.). The form contains three input fields: "名" (First Name), "姓" (Last Name), and "電子郵件" (Email). Below the email field, there is a note: "對於商業用戶，請提供您公司的電子郵件地址，以便完全訪問許可、技術支持和服務等專區內容。對於其他用戶，請使用您的個人電子郵件地址。" (For business users, please provide your company email address to fully access permissions, technical support, and service content. For other users, please use your personal email address.). There are two dropdown menus: "語言首選項" (Language Preference) with "英文" (English) selected, and "居住地" (Residence) with "選擇一個" (Select one) selected. At the bottom, a note states: "創建帳戶即表示您同意 AMD 使用條款和隱私政策。" (Creating an account indicates you agree to AMD's Terms of Use and Privacy Policy.).

Step 3

- Get US Government Export Approval

U.S. Government Export Approval

- U.S. export regulations require that your First Name, Last Name, Company Name and Shipping Address be verified before Xilinx can fulfill your download request. [Please provide accurate and complete information.](#)
- Addresses with Post Office Boxes and names/addresses with Non-Roman Characters with accents such as grave, tilde or colon **are not supported** by US export compliance systems.

First Name *

Yu-Cheng

Last Name *

Liu

Business E-mail *

benson.cs10@nycu.edu.tw

Company Name *

NYCU

Please enter the name of your business or institution.

Address 1 *

1001 University Road, Hsinchu, Taiwan 300, ROC

Please enter your Company Address.

Address 2

Location *

Taiwan

State/Province

City *

Hsinchu

Postal Code

Phone

Job Function *

Student

You can read about how we handle your personal data, your personal data rights, and how you can contact us in our [privacy policy](#).

Download


Step 4

- If it doesn't start downloading, close the page and press the link, fill the approval again.


ProductsCompanyAMD
XILINX

Chrome and Microsoft Edge web browsers.

- Starting with the Vivado ML 2021.1 release, this and newer releases offer only 2 Editions for Vivado ML. Please go to [product page](#) for more details.
- Vivado ML 2021.1 and later versions require upgrading your license server tools to the Flex 11.17.2.0 versions.




MD5 SUM Value : 985168f6920c5ee2111c5d16573330e1

Download Verification 


Digests

Signature

Public Key



MD5 SUM Value : 9bf473b6be0b8531e70fd3d5c0fe4817

Download Verification 

U.S. Government Export Approval

- U.S. export regulations require that your First Name, Last Name, Company Name and Shipping Address be verified before Xilinx can fulfill your download request. [Please provide accurate and complete information.](#)
- Addresses with Post Office Boxes and names/addressees with Non-Roman Characters with accents such as grave, tilde or colon **are not supported** by US export compliance systems.

For name and email, fill in your own information

First Name *

Last Name *

Business E-mail *

Company Name *

Address 1 *

Address 2

Location *

City *

Phone

Job Function *

NYCU

Please enter the name of your business or institution.

1001 University Road, Hsinchu, Taiwan 300, ROC

Please enter your Company Address.

Taiwan

Hsinchu

State/Province

Postal Code

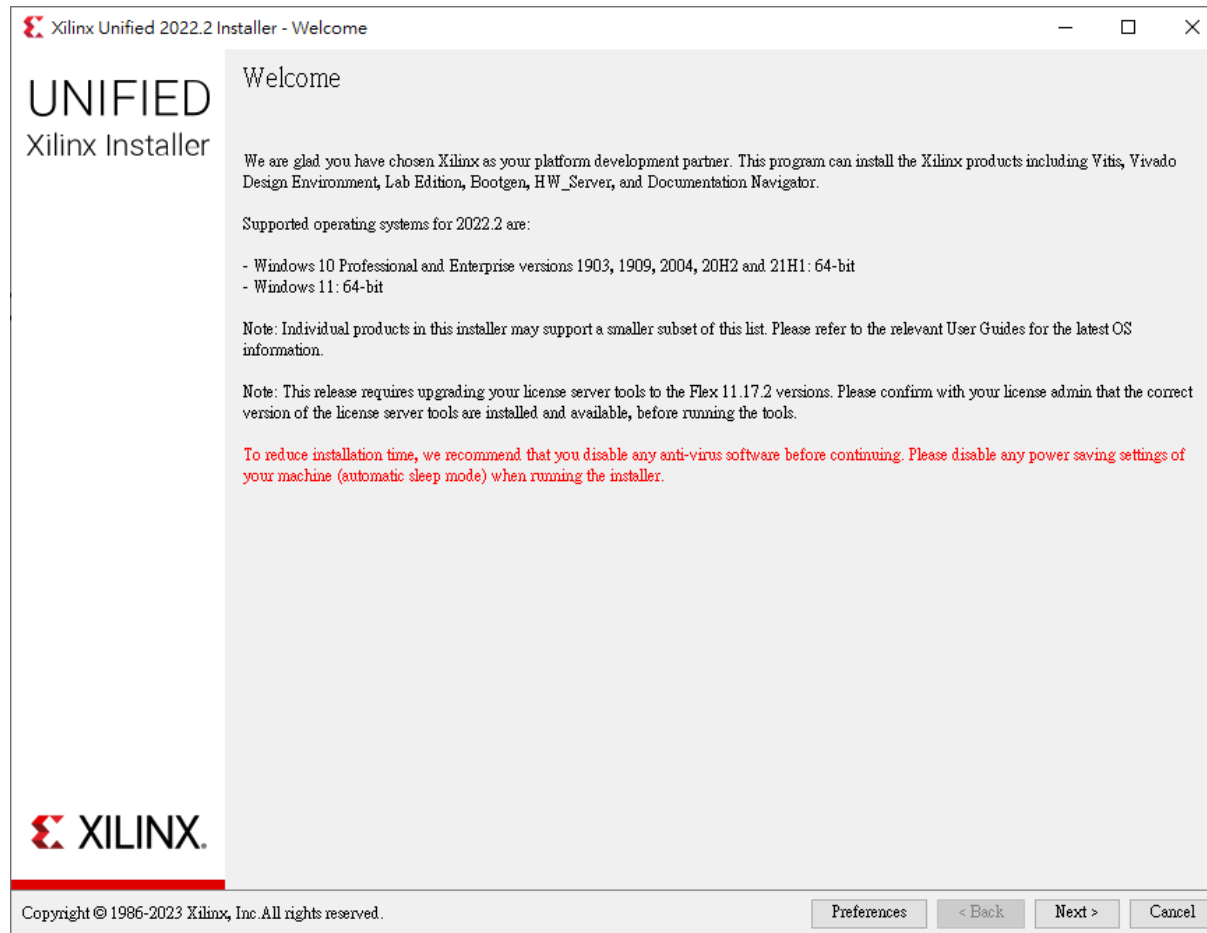
Student

These can be filled out with reference to the examples provided.

Download

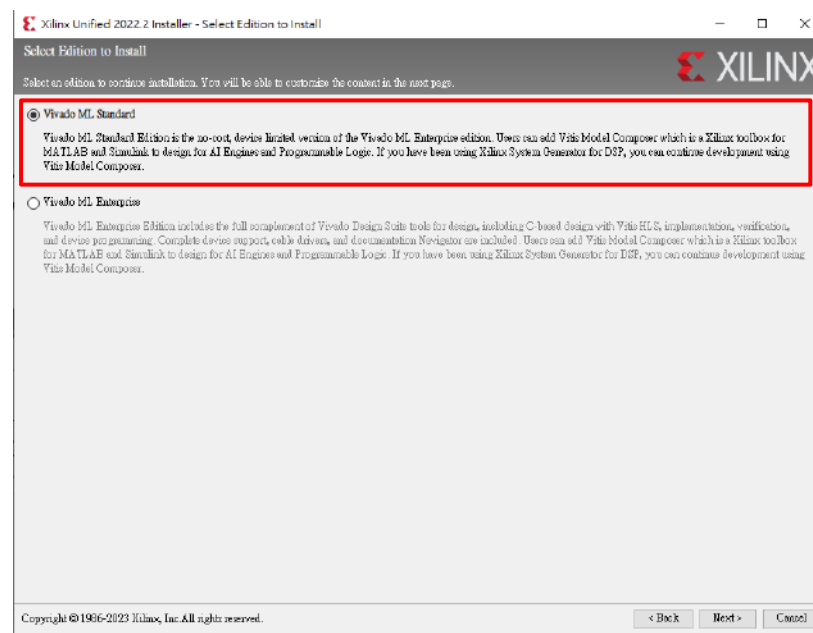
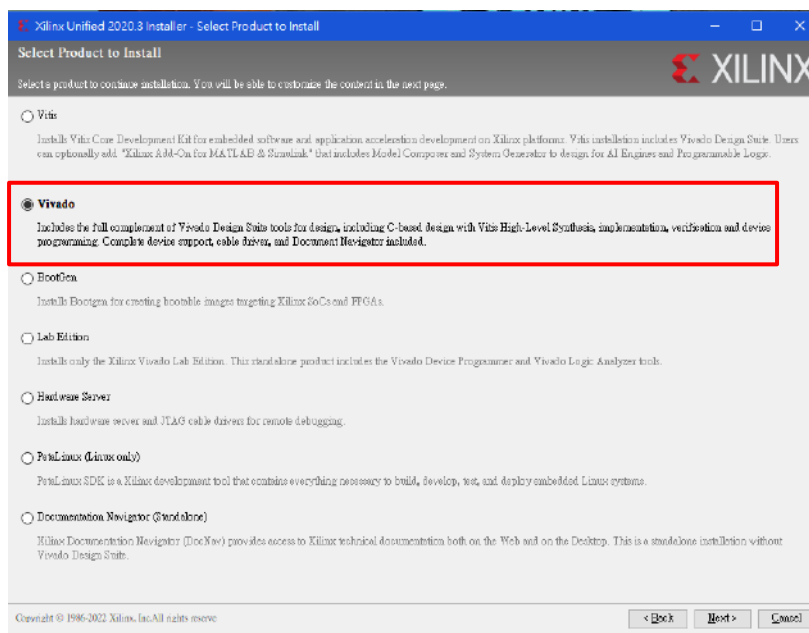
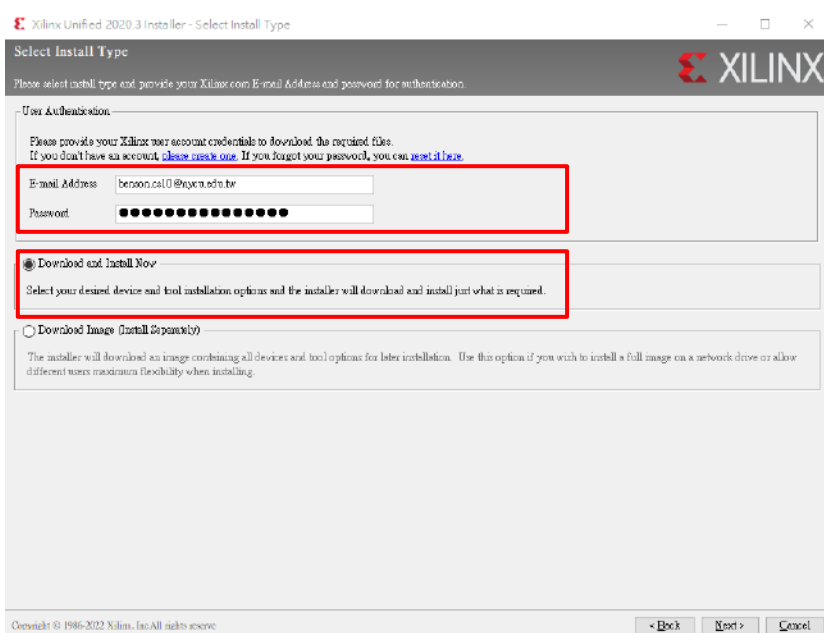
Step 5

- After downloading, run the installer.



Step 6

- Execute the file you download and choose the options like the following pictures.



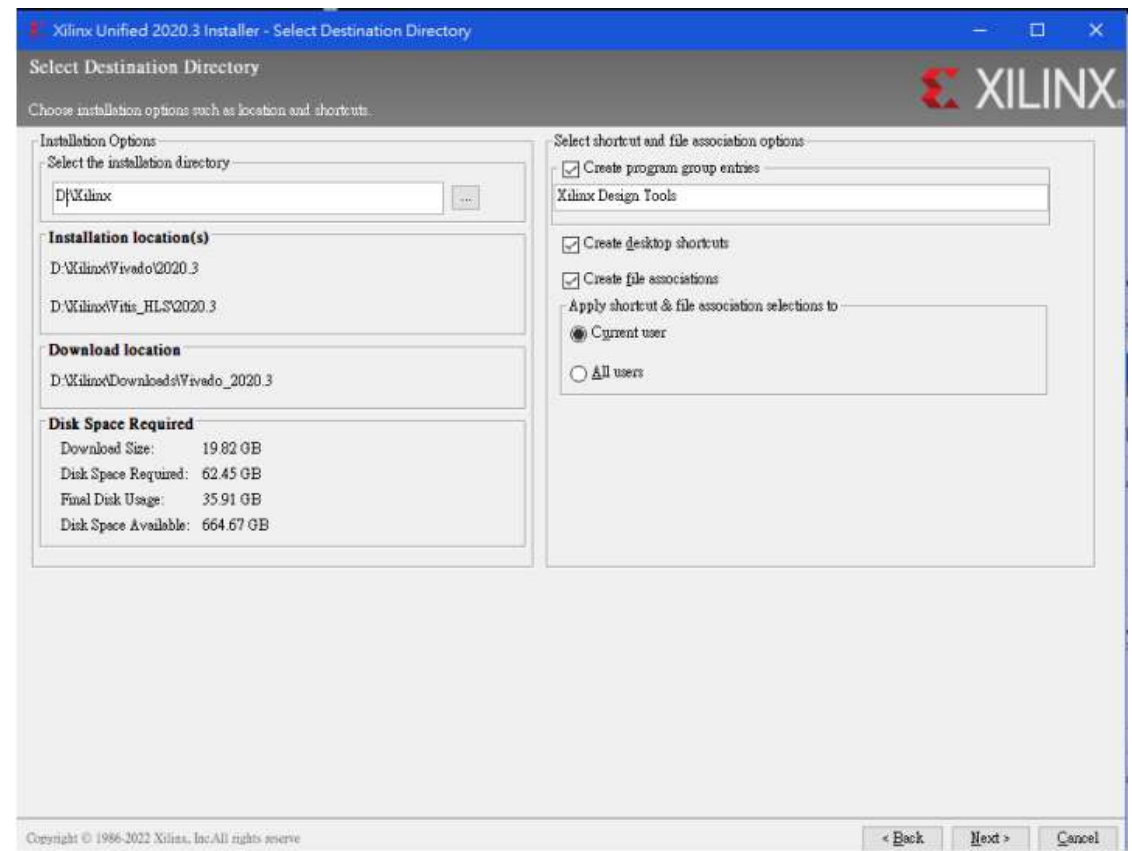
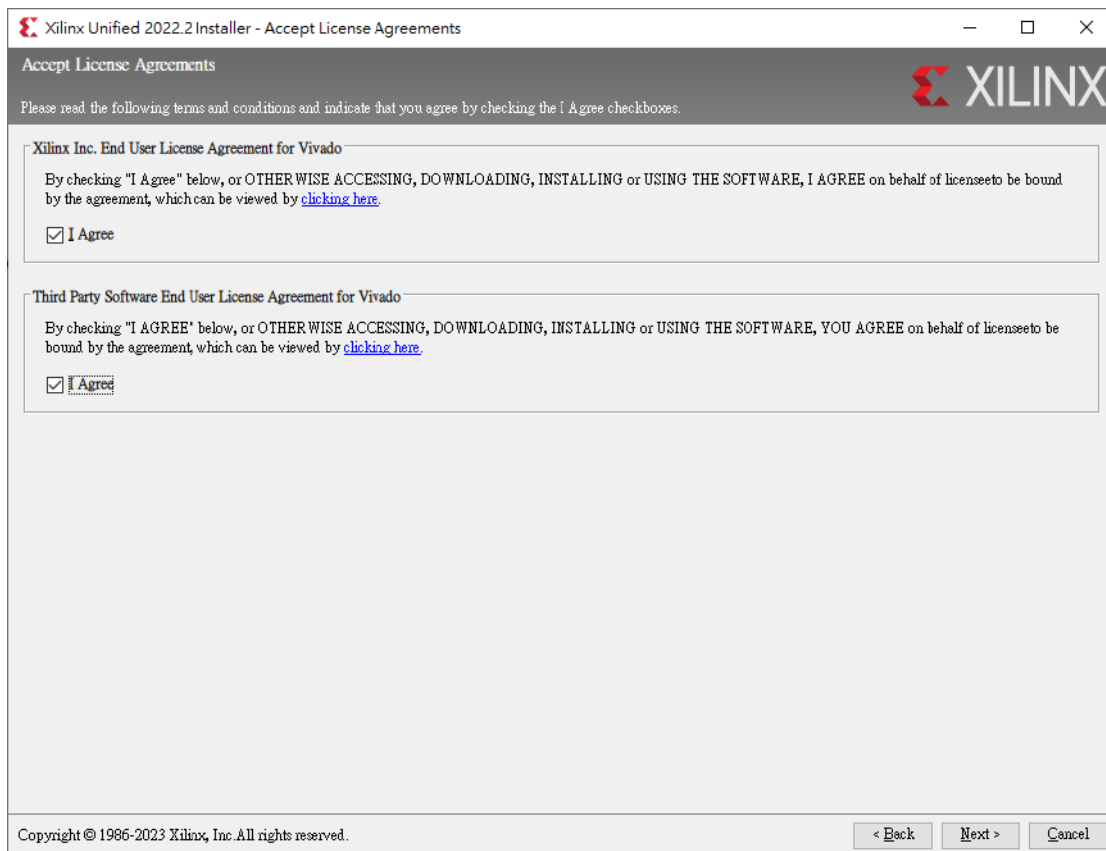
Step 7

- We only need behavioral simulation function, so I disabled other unnecessary functions.



Step 8

- You can decide your own installation directory.

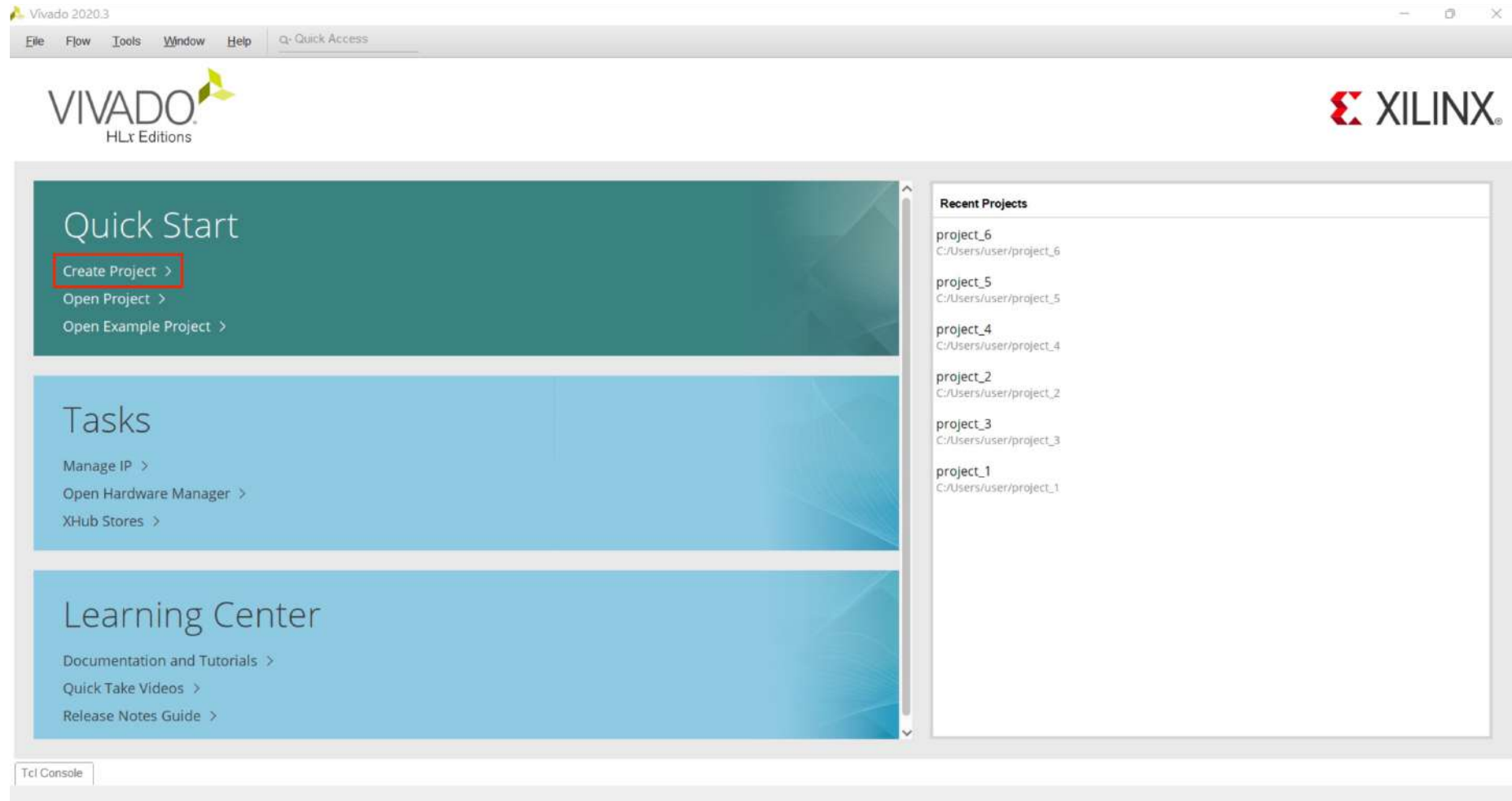


Step 9

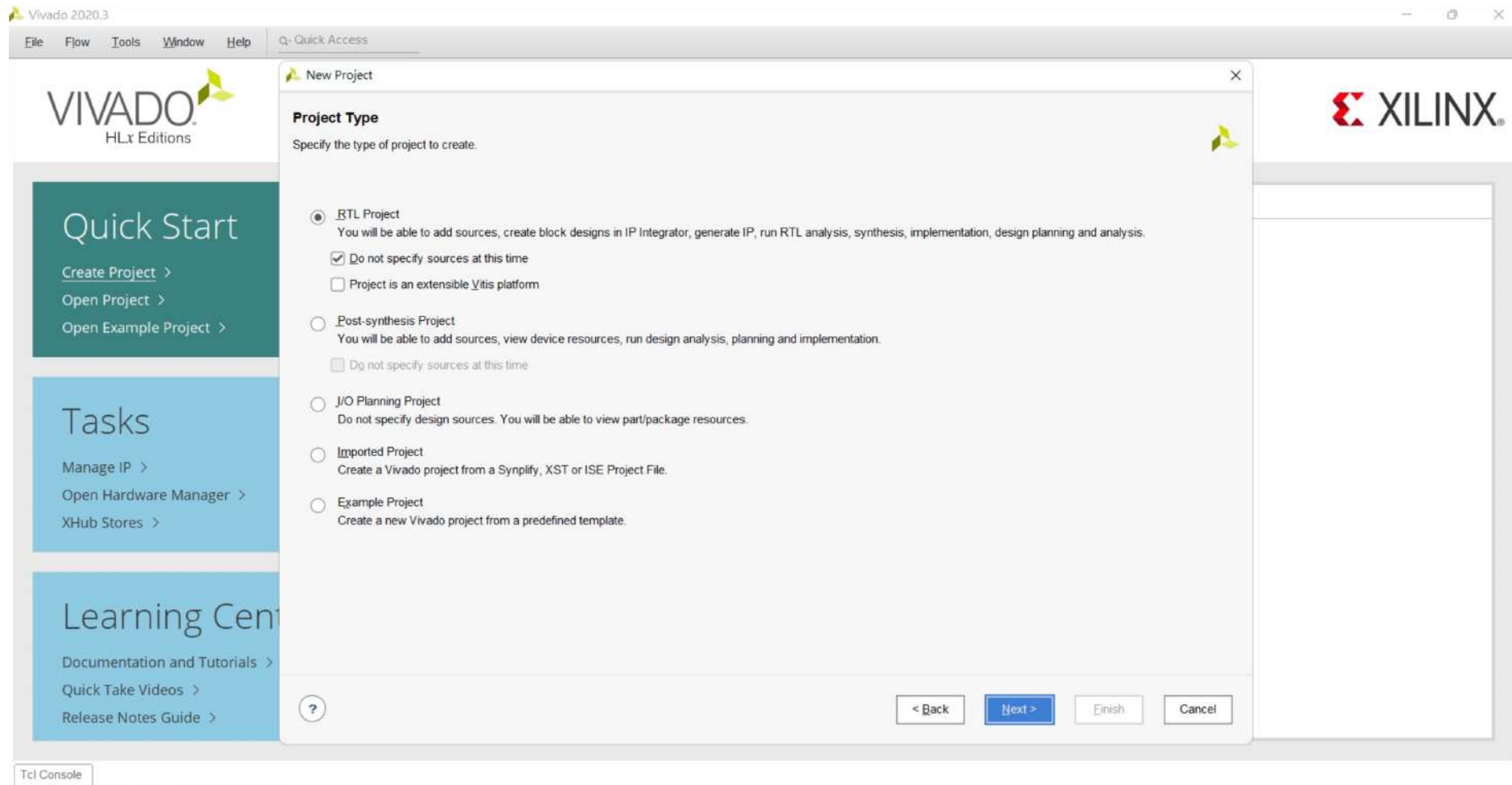
- Finally, wait for the installer to install the software. Note that the installer probably needs much time to install.
- You may need to reboot the computer after the installation.

Add Sources and Simulation

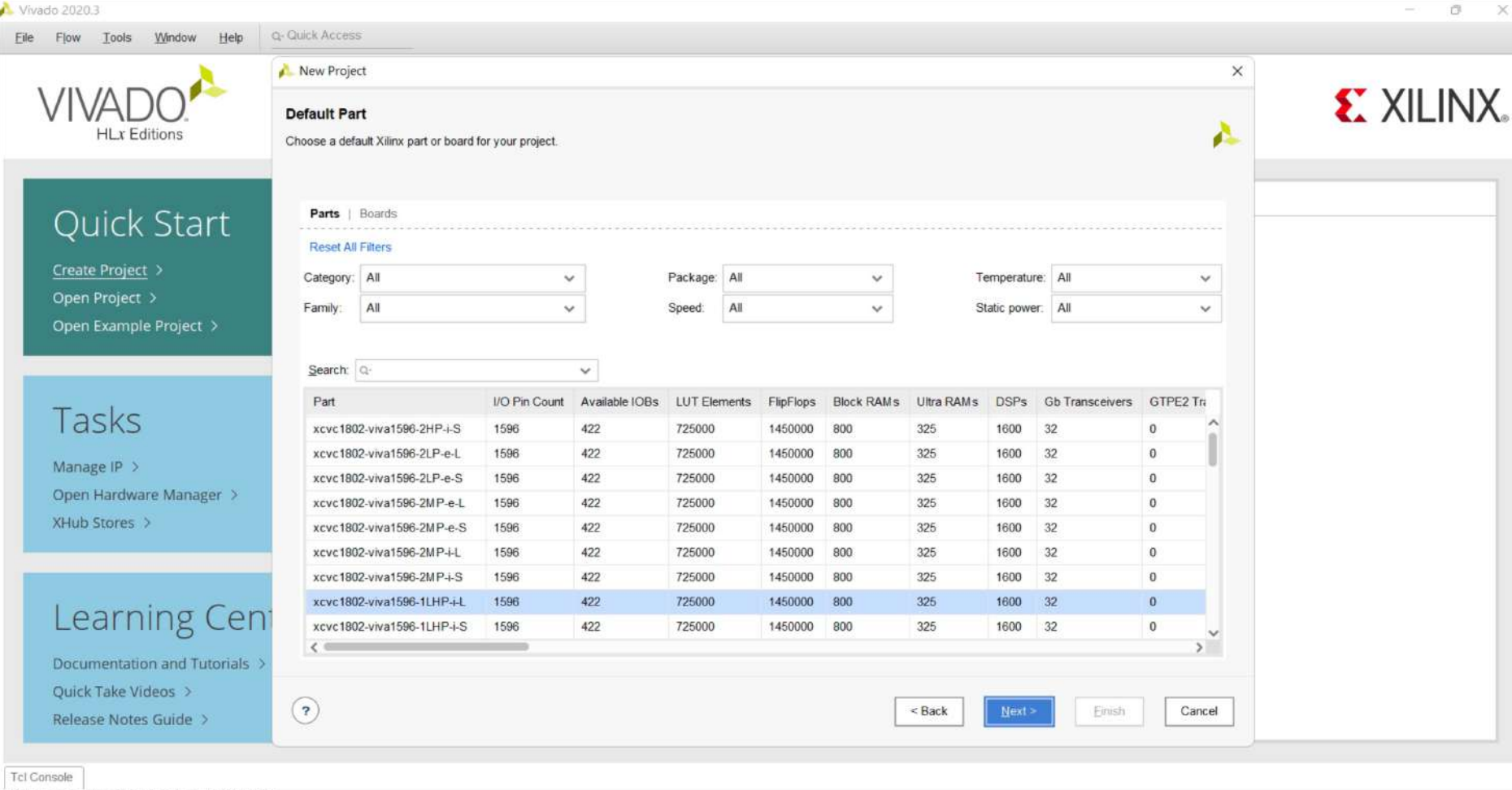
Create project



Select project type



Select default part



Vivado 2020.3

File Flow Tools Window Help Q: Quick Access

VIVADO
HLx Editions

Quick Start

- Create Project >
- Open Project >
- Open Example Project >

Tasks

- Manage IP >
- Open Hardware Manager >
- XHub Stores >

Learning Center

- Documentation and Tutorials >
- Quick Take Videos >
- Release Notes Guide >

New Project

Default Part
Choose a default Xilinx part or board for your project.

Parts | Boards

[Reset All Filters](#)

Category: All Package: All Temperature: All
Family: All Speed: All Static power: All

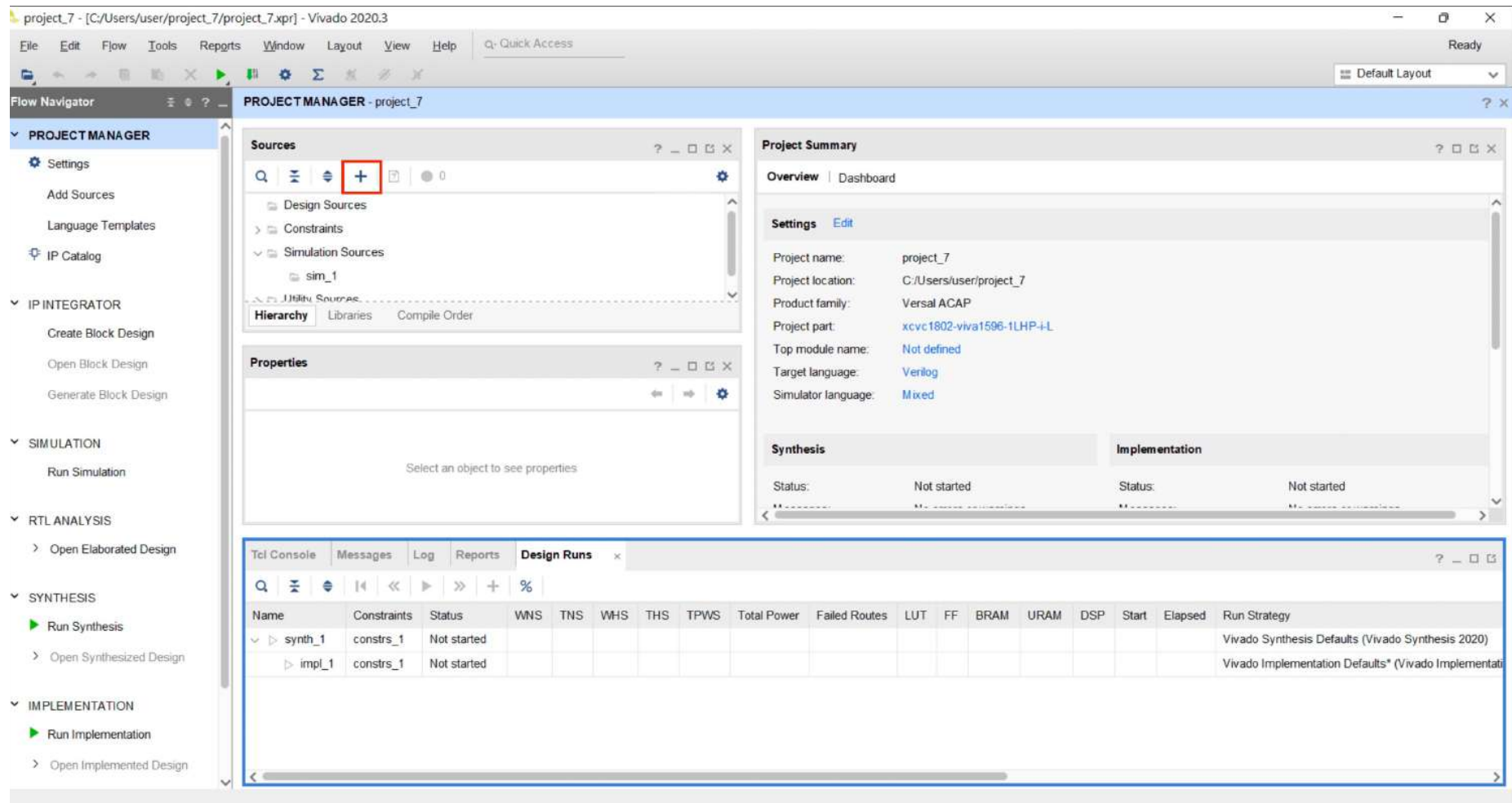
Search: Q:

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAM s	Ultra RAM s	DSPs	Gb Transceivers	GTPE2 Tri
xcvc1802-viva1596-2HP-i-S	1596	422	725000	1450000	800	325	1600	32	0
xcvc1802-viva1596-2LP-e-L	1596	422	725000	1450000	800	325	1600	32	0
xcvc1802-viva1596-2LP-e-S	1596	422	725000	1450000	800	325	1600	32	0
xcvc1802-viva1596-2MP-e-L	1596	422	725000	1450000	800	325	1600	32	0
xcvc1802-viva1596-2MP-e-S	1596	422	725000	1450000	800	325	1600	32	0
xcvc1802-viva1596-2MP-i-L	1596	422	725000	1450000	800	325	1600	32	0
xcvc1802-viva1596-2MP-i-S	1596	422	725000	1450000	800	325	1600	32	0
xcvc1802-viva1596-1LHP-i-L	1596	422	725000	1450000	800	325	1600	32	0
xcvc1802-viva1596-1LHP-i-S	1596	422	725000	1450000	800	325	1600	32	0

? < Back Next > Finish Cancel

Tcl Console

Add design sources



The screenshot displays the Vivado 2020.3 Project Manager interface for a project named 'project_7'. The 'Sources' panel on the left shows a tree view with 'Design Sources', 'Constraints', and 'Simulation Sources'. A red box highlights the '+' icon in the 'Sources' toolbar, indicating the action to add new design sources. The 'Project Summary' panel on the right provides an overview of the project settings, including the project name, location, product family, and target language. The 'Design Runs' panel at the bottom shows a table of design runs, including synthesis and implementation steps.

Project Summary

Overview | Dashboard

Settings [Edit](#)

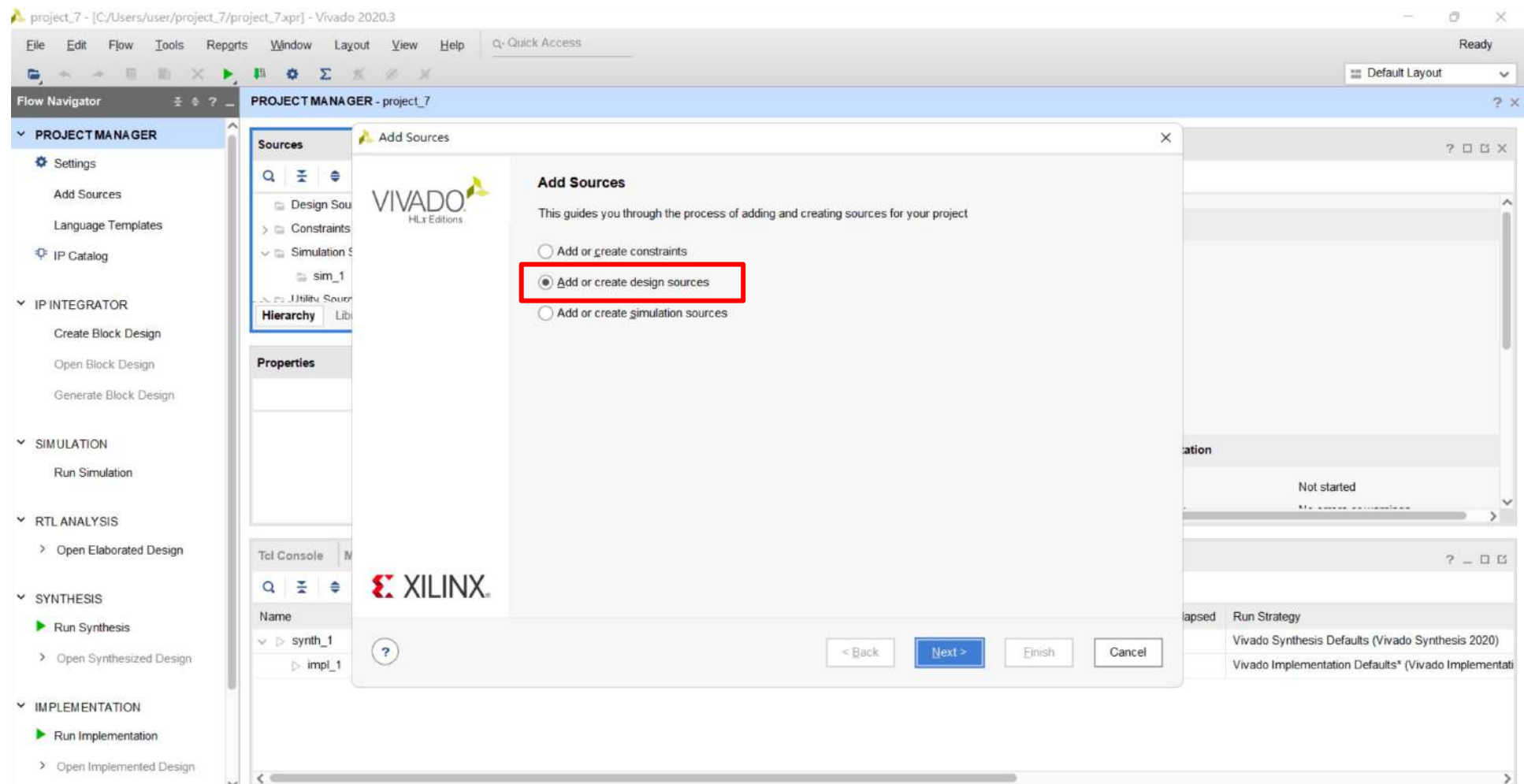
Project name: project_7
Project location: C:/Users/user/project_7
Product family: Versal ACAP
Project part: xcvc1802-vva1596-1LHP+L
Top module name: Not defined
Target language: Verilog
Simulator language: Mixed

Synthesis | **Implementation**

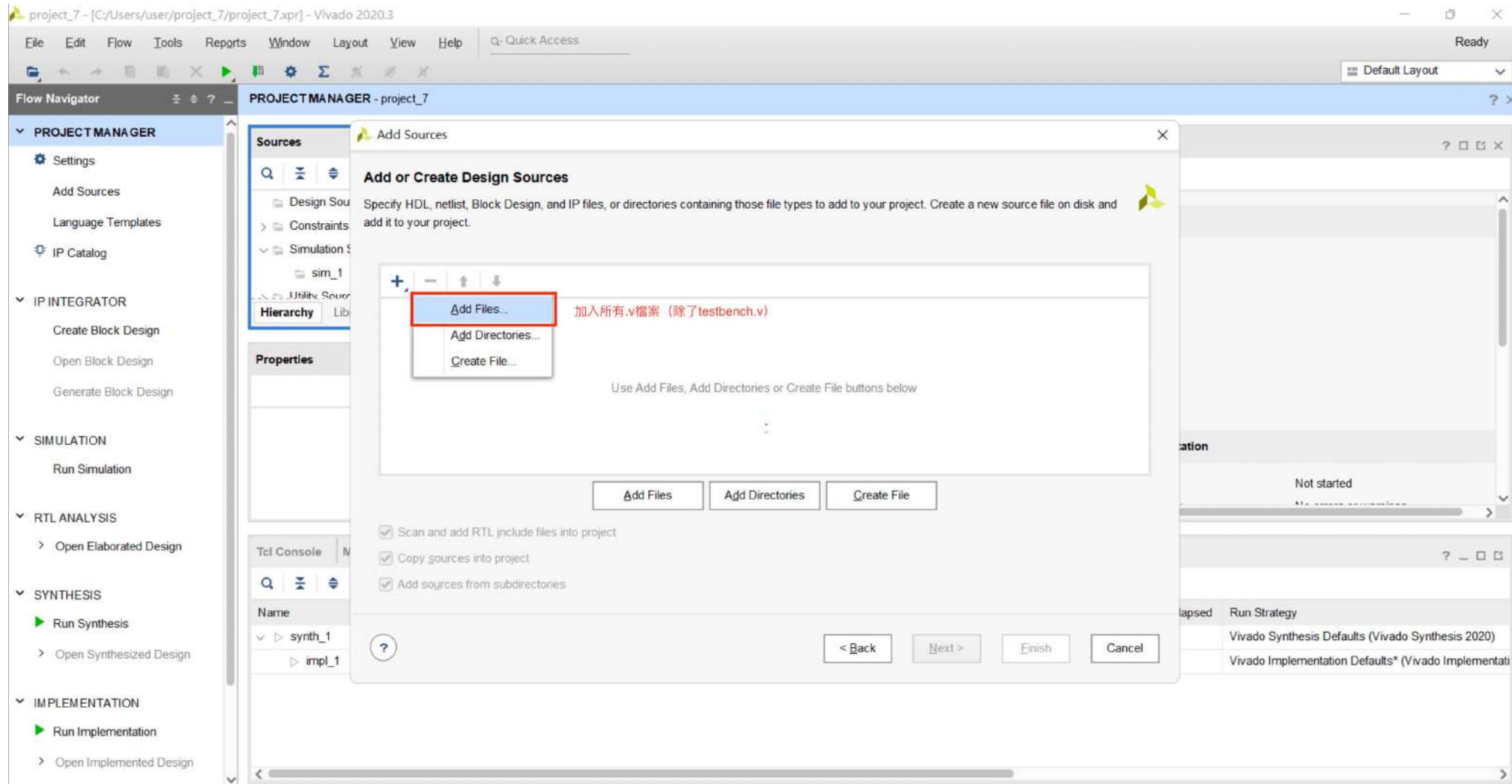
Status: Not started | Status: Not started

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2020)
impl_1	constrs_1	Not started															Vivado Implementation Defaults* (Vivado Implementation 2020)



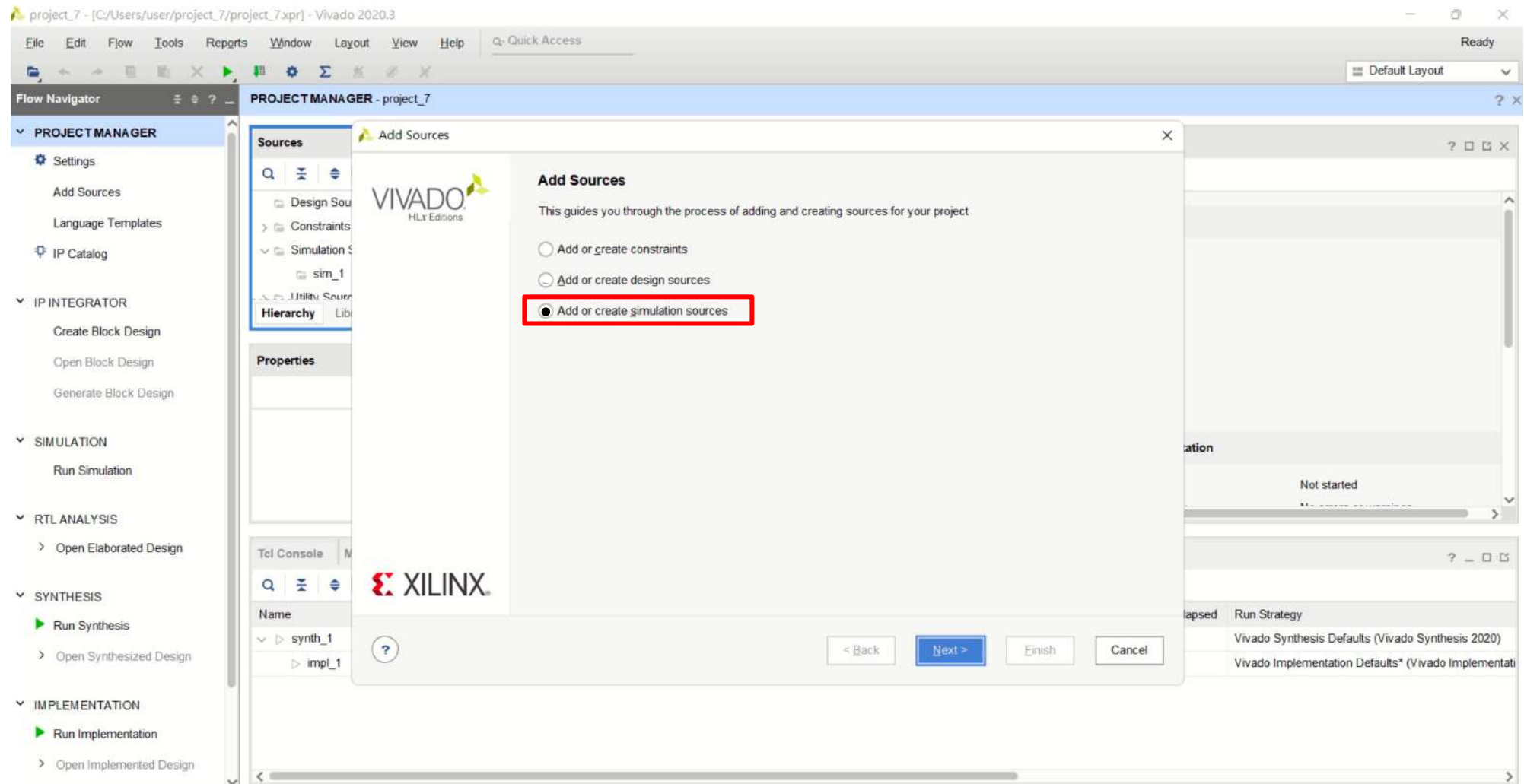
Add .v files (except TestBench.v)



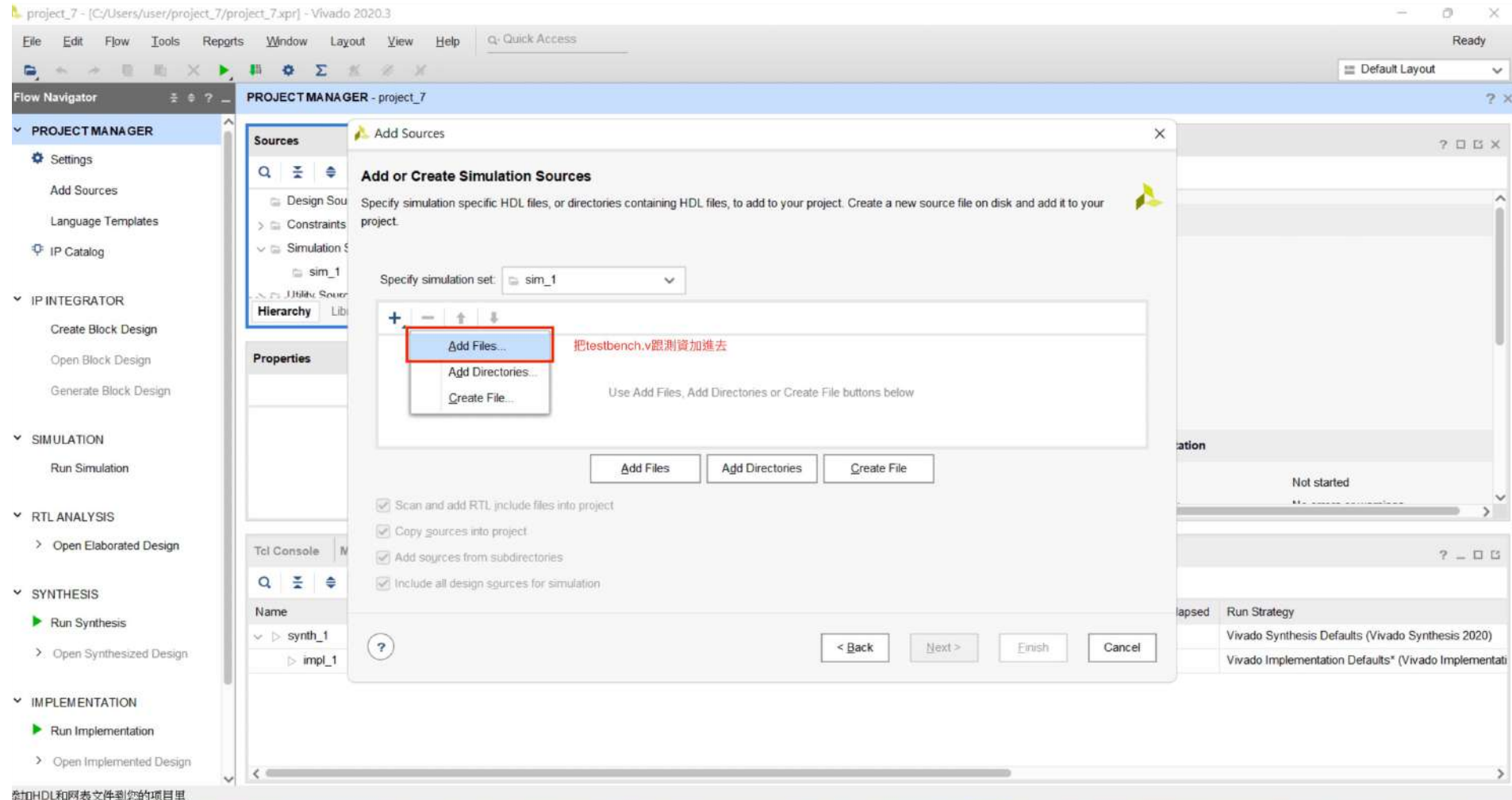
Add simulation sources

The screenshot shows the Vivado 2020.3 Project Manager interface for a project named 'project_7'. The 'Sources' tab is active, displaying a tree view of the project's sources. A red box highlights the '+' icon in the toolbar, which is used to add new sources. The 'Simulation Sources' folder is expanded, showing a sub-folder named 'sim_1'. The 'Properties' panel is empty, and the 'Project Summary' panel shows details about the project, including the project name, location, product family, and target language. The 'Design Runs' panel at the bottom shows a table of design runs, including synthesis and implementation runs.

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2020)
impl_1	constrs_1	Not started															Vivado Implementation Defaults* (Vivado Implementation 2020)



Add TestBench.v and test case file



Run Simulation

The screenshot shows the Vivado 2020.3 IDE interface. The left sidebar contains the 'Flow Navigator' with the following sections:

- PROJECT MANAGER
 - Settings
 - Add Sources
 - Language Templates
 - IP Catalog
- IP INTEGRATOR
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- SIMULATION
 - Run Simulation** (highlighted with a red box)
- RTL ANALYSIS
 - Open Elaborated Design
- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design

The main window is titled 'PROJECT MANAGER - project_7'. It contains several panels:

- Sources:** A tree view showing 'Design Sources' (Constraints, Simulation Sources) and 'Utility Sources'. 'sim_1' is listed under 'Simulation Sources'.
- Properties:** A panel for selecting an object to see properties.
- Project Summary:** A panel showing project details.
 - Overview | Dashboard:**
 - Settings (Edit)
 - Project name: project_7
 - Project location: C:/Users/user/project_7
 - Product family: Versal ACAP
 - Project part: xcvc1802-viva1596-1LHP-i-L
 - Top module name: Not defined
 - Target language: Verilog
 - Simulator language: Mixed
 - Synthesis:** Status: Not started
 - Implementation:** Status: Not started

- Design Runs:** A table showing the status of design runs.

The 'Design Runs' table has the following columns: Name, Constraints, Status, WNS, TNS, WHS, THS, TPWS, Total Power, Failed Routes, LUT, FF, BRAM, URAM, DSP, Start, Elapsed, Run Strategy.

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2020)
impl_1	constrs_1	Not started															Vivado Implementation Defaults* (Vivado Implementati

QA

- If you encounter any problems, please search for information online first. If you still can't solve the problem, then ask the TA through E3.