```
Inferred memory devices in process
        in routine core line 114 in file
                '/home/raid7_2/userb11/b11132/DSD/DSD_HW2/verilog/core.v'.
=================================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
=================================================================================
|       mem_reg       | Flip-flop | 1024  |  Y  | N  | N  | N  | N  | N  | N  |
=================================================================================
```

```
Inferred memory devices in process
        in routine core line 138 in file
                '/home/raid7_2/userb11/b11132/DSD/DSD_HW2/verilog/core.v'.
=================================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
=================================================================================
|       PC_reg        | Flip-flop |  32   |  Y  | N  | N  | N  | N  | N  | N  |
=================================================================================
```

```
Inferred memory devices in process
        in routine memory line 28 in file
                '/home/raid7_2/userb11/b11132/DSD/DSD_HW2/verilog/memory.v'.
=================================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
=================================================================================
|       mem_reg       | Flip-flop | 1024  |  Y  | N  | N  | N  | N  | N  | N  |
=================================================================================
```