

# DSD Final Project Scores

## 1. BrPred

(1) Total execution cycles of given I\_mem\_BrPred: 484

截圖:

```
Total cycle count: 484
----- Simulation FINISH !!-----
=====

\(^o^)/ CONGRATULATIONS!! The simulation result is PASS!!!

=====
$finish called from file "Final_tb.v", line 229.
$finish at simulation time          1303390
      V C S   S i m u l a t i o n   R e p o r t
Time: 1303390 ps
CPU Time:      2.430 seconds;      Data structure size:   9.0Mb
Wed Jun 11 00:31:26 2025
```

(2) Total execution cycles of given I\_mem\_hasHazard: 2307

截圖:

```
Total cycle count: 2307
----- Simulation FINISH !!-----
=====

\(^o^)/ CONGRATULATIONS!! The simulation result is PASS!!!

=====
$finish called from file "Final_tb.v", line 229.
$finish at simulation time          6133950
      V C S   S i m u l a t i o n   R e p o r t
Time: 6133950 ps
CPU Time:      5.600 seconds;      Data structure size:   9.0Mb
Wed Jun 11 00:29:58 2025
```

(3) Clock cycle for post-syn simulation (cycle in testbench, not cycle in sdc): 2.65(ns)

## 2. Compressed instructions

(1) Total Simulation Time of given I\_mem\_compression: 1455.01(ns)

截圖:

```

----- Simulation FINISH !!-----
=====

\(^o^)/ CONGRATULATIONS!! The simulation result is PASS!!!

=====
$finish called from file "Final_tb.v", line 221.
$finish at simulation time      1455010
      V C S   S i m u l a t i o n   R e p o r t
Time: 1455010 ps
CPU Time:      2.500 seconds;      Data structure size:   9.0Mb
Wed Jun 11 00:08:40 2025

```

(2) Clock cycle for post-syn simulation (cycle in testbench, not cycle in sdc): 2.65(ns)

### 3. Multiplication instructions

(1) Total Simulation Time of given Mul/I\_mem: 1207.63(ns)

截圖：

```

----- Simulation FINISH !!-----
=====

\(^o^)/ CONGRATULATIONS!! The simulation result is PASS!!!

=====
$finish called from file "Final_tb.v", line 221.
$finish at simulation time      1207630
      V C S   S i m u l a t i o n   R e p o r t
Time: 1207630 ps
CPU Time:      2.030 seconds;      Data structure size:   9.0Mb
Wed Jun 11 00:06:18 2025

```

(2) Clock cycle for post-syn simulation (cycle in testbench, not cycle in sdc): 2.65(ns)

### 4. Q\_sort & Conv

(1) Area: 491680.762215(um<sup>2</sup>)

截圖：

```

Total cell area:      491680.762215
Total area:           4938710.000130

```

(2) Total Simulation Time of Q\_Sort: 270870.45(ns)

(either using compressed or uncompressed instructions)

截圖：

```

----- Simulation FINISH !!-----
=====

\\(^o^)/ CONGRATULATIONS!! The simulation result is PASS!!!

=====
$finish called from file "Final_tb.v", line 221.
$finish at simulation time          270870450
      V C S   S i m u l a t i o n   R e p o r t
Time: 270870450 ps
CPU Time:    176.910 seconds;      Data structure size:   9.0Mb
Tue Jun 10 23:55:57 2025

```

(3) Total Simulation Time of Conv: 42419.01(ns)

(either using compressed or uncompressed instructions)

截圖：

```

----- Simulation FINISH !!-----
=====

\\(^o^)/ CONGRATULATIONS!! The simulation result is PASS!!!

=====
$finish called from file "Final_tb.v", line 221.
$finish at simulation time          42419010
      V C S   S i m u l a t i o n   R e p o r t
Time: 42419010 ps
CPU Time:    17.720 seconds;      Data structure size:   9.0Mb
Tue Jun 10 23:57:39 2025

```

(3) Area\*Total Simulation Time Q\_Sort\*Total Simulation Time of Conv: 5.6495e15  
( $\mu\text{m}^2 * \text{ns}^2$ )

(4) Clock cycle for post-syn simulation (cycle in testbench, not cycle in sdc): 2.65(ns)