Digital Circuit Lab 3 Report

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1 Introduction

In Lab 3, we designed an audio codec controller for recording and playback functionality. We also implemented two additional features: an LED display showing the current state of the controller in the top module, and a seven-segment hex display showing the speed mode (fast/slow) and speed value.

2 File Structure

The top module is written in the `Top.sv` file, and we added other `.sv` files corresponding to other modules. We also modified the `DE2_115.sv` file to add additional features of LED and seven-segment hex displays. The following image is the hierarchy of all files.

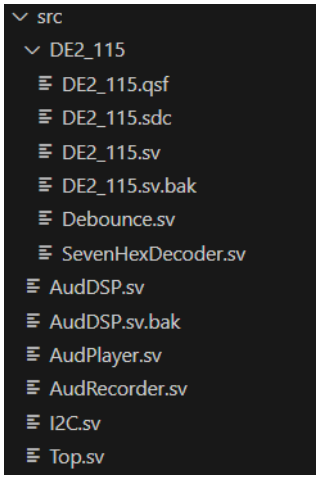


Figure 1: File structure

3 System Architecture

The detailed system architecture is illustrated in the figure below, showing all pin connections and signal interfaces between the top-level module and its constituent submodules.

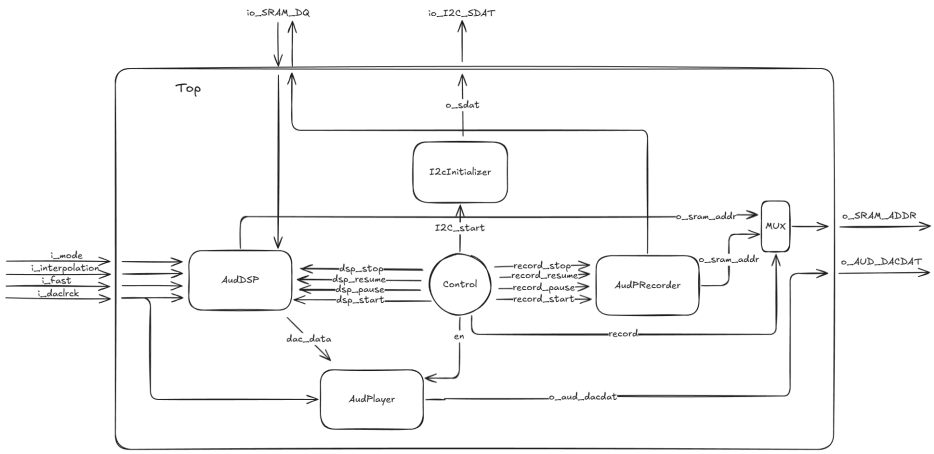


Figure 2: System architecture

4 Hardware Scheduling

We describe the top module and its submodules in the following subsections.

4.1 Top Module

The finite state machine (FSM) for the top module is shown in Figure 3.

After `i_key_2` resets the recorder, it will automatically enter the I2C state, which initializes the WM8731 chip. After initialization, the top module will enter IDLE state, waiting for input signals.

`i_key_0` acts as the record trigger and also provides pause/resume control while recording. `i_key_1` initiates playback and similarly supports pause/resume during playback. `i_key_2` terminates any active recording or playback operation and forces the FSM back to the `IDLE` state.

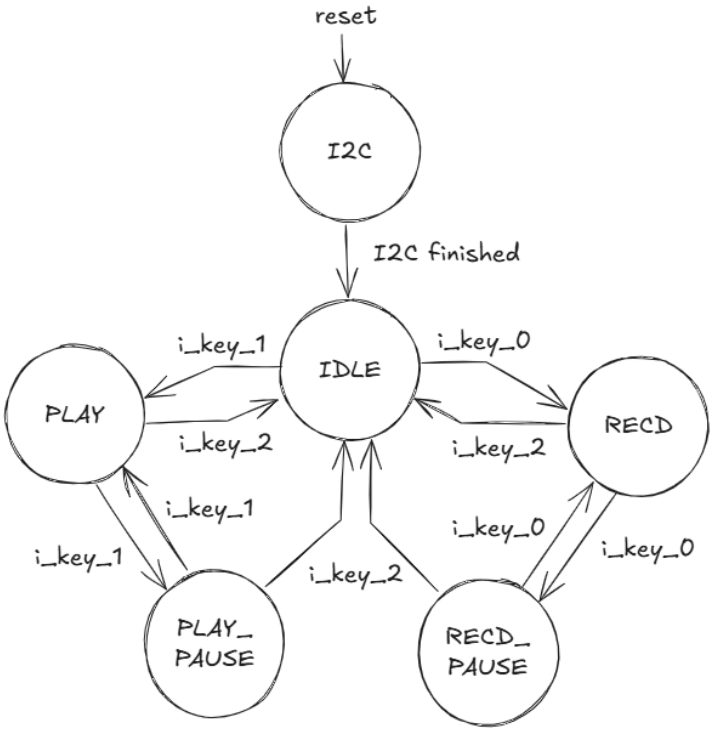


Figure 3: FSM of top module

4.2 12C Initializer

The `I2cInitializer` module sends a predefined sequence of register settings to the WM8731 codec through the I^{2}C interface. It ensures the audio chip is properly configured before recording or playback begins.

- When `i_start` is asserted, the module begins sending the first instruction.
- Each instruction is a 24-bit word that is shifted out MSB-first on SDA, synchronized with the generated I^{2}C clock `o_sclk`.
- Three ACK phases are included in each transfer, where the module releases SDA and waits for the codec to acknowledge.
- After one instruction finishes shifting, the next one will be prepared and sent until all ten instructions are completed.

- Once all configuration writes are done, `o_finished` is set to `1` to indicate that initialization is complete.

During reset, the I^2C lines return to their idle high state and the internal counters restart.

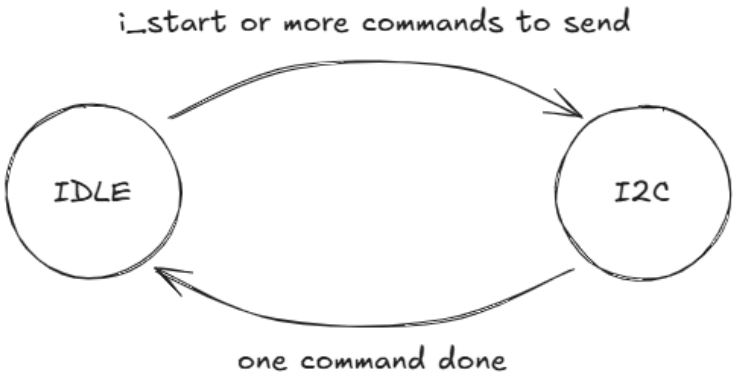


Figure 4: FSM of I2C initializer

4.3 AudRecorder

The `AudRecorder` module operates based on a five-state finite state machine (FSM) responsible for handling memory initialization, audio recording, pausing, and stopping. The states and transitions are shown in Figure 5 and are summarized as follows:

- `S_IDLE`
  Default state. The recorder remains idle until `i_start` is asserted. Upon receiving `i_start`, the FSM transitions to `S_CLEAR`.

- `S_CLEAR`
  The entire memory space is cleared by writing zeros sequentially across all addresses. After reaching `MAX_ADDR`, the FSM proceeds to `S_RECORD`.

- `S_RECORD`
  LEFT channel audio data is retrieved and stored into memory.
  State transitions:

  - `i_pause` → `S_PAUSE`
  - `i_stop` → `S_IDLE`
  - After one sample is written → `S_RETRIEVED`

- **`S_RETRIEVED`**
  Temporary state after one sample is stored.
  State transitions:
  - Next sample ready (left channel active) → `S_RECORD`
  - `i_pause` → `S_PAUSE`
  - `i_stop` → `S_IDLE`

- **`S_PAUSE`**
  Recording is halted but memory contents are preserved.
  State transitions:
  - `i_resume` → `S_RECORD`
  - `i_stop` → `S_IDLE`

Additionally, when the write address reaches `MAX_ADDR`, the `o_finish` signal is asserted for one cycle, indicating that the memory is full and recording should terminate.

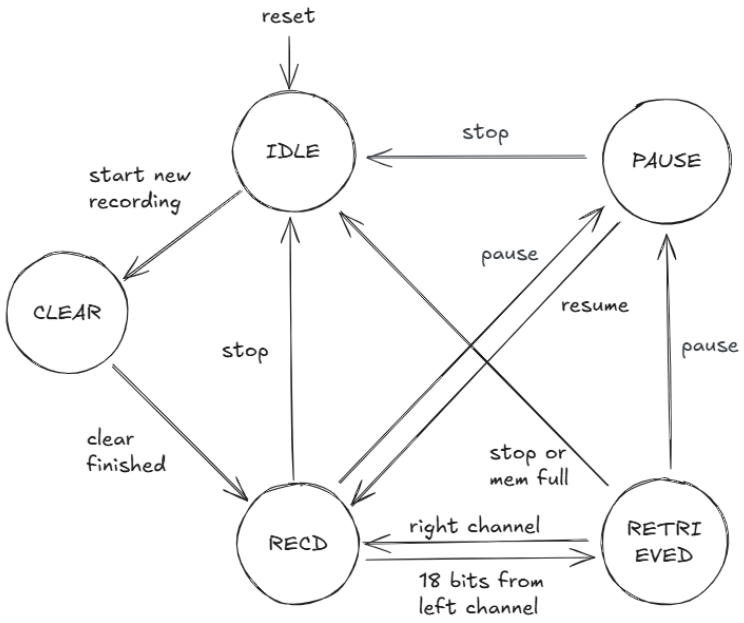


Figure 5: FSM of recorder

4.4 AudDSP

The `AudDSP` module processes audio samples from SRAM and outputs them to the DAC based on different playback modes (FAST, SLOW_0, SLOW_1) and adjustable playback speed. Playback can also be paused or stopped. The FSM with seven states controls memory request, sample capture, interpolation, and synchronization with `i_daclrck`. The states and their transitions are depicted in Figure 6 and are summarized as follows:

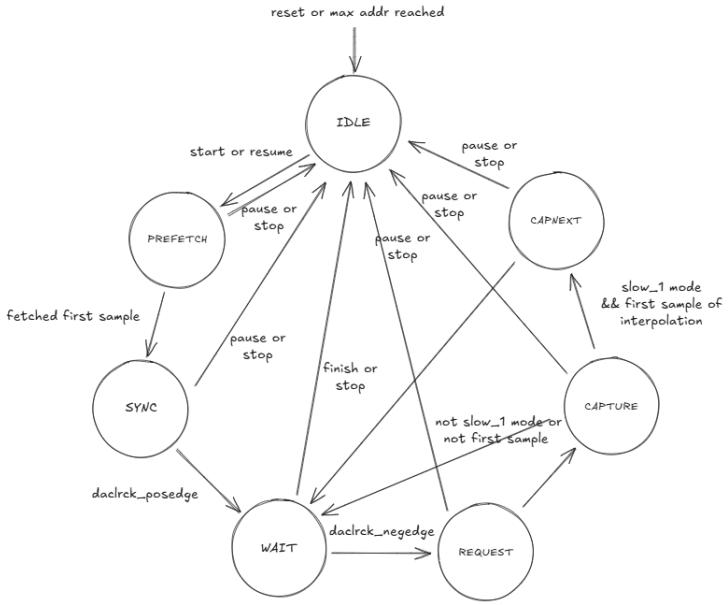


Figure 6: FSM of AudDSP

- `S_IDLE`
  Default state. Playback is halted. When `i_start` or `i_resume` is asserted, the address counters reset and the next sample fetch is prepared, transitioning to `S_PREFETCH`. If `i_stop` occurs, playback remains idle.

- `S_PREFETCH`
  The first audio sample is fetched from SRAM before synchronization. This ensures valid audio data is ready before DAC output begins. Next: `S_SYNC`.

- `S_SYNC`
  Waits for the first valid `i_daclrck` edge to align output timing with the DAC. Once synchronized, proceeds to `S_WAIT`.

- `S_REQUEST`
  Sets the correct SRAM address for the next sample fetch. Next: `S_CAPTURE`.

- `S_CAPTURE`
  Captures data from SRAM and sets the output sample depending on the selected mode:

  - **FAST mode:** directly output fetched sample.
  - **SLOW_0 mode:** hold each sample multiple DAC cycles.
  - **SLOW_1 mode:** prepare for interpolation by requesting the next sample.

  After processing, transitions to `S_WAIT`.

- `S_CAPNEXT`
  (SLOW_1 mode only) fetches the following sample to enable linear interpolation between two points. Then proceeds to `S_WAIT`.

- `S_WAIT`
  Waits for the next `i_daclrck` negative edge. Updates playback address and interpolation counter based on playback mode and speed. Next state: `S_REQUEST`.

Playback can be paused at any time using `i_pause`, returning the FSM to `S_IDLE` while preserving address values. When `i_stop` is asserted, addresses reset and playback returns to `S_IDLE`.

When the read address reaches the end of recorded data, `o_finish` is asserted and the module stops playback automatically.

4.5 AudPlayer

The `AudPlayer` module converts each 16-bit audio sample into a serial data stream for the DAC. It works in synchronization with the bit clock `i_bclk` and left/right channel clock `i_daclrck`.

- At the start of every LEFT channel frame, the next audio sample `i_dac_data` is loaded into a 16-bit shift register.
- When enabled and during the LEFT channel period (`i_daclrck=0`), bits are shifted out MSB-first on each rising edge of `i_bclk`.
- After 16 bits are shifted out, the module waits until the next LEFT frame to load new data.

- While in the RIGHT channel period or when disabled, the output `o_aud_dacdat` is placed in high-impedance state (`1'bz`), so the module does not drive the line.

On reset, the shift register, bit counter, and internal edge tracking are cleared.

5 Bonus

As part of the bonus, we implemented additional LED indicators to show the recorder's operating state, as well as FAST/SLOW mode and speed on the seven-segment displays, providing improved clarity and visibility of its configuration.

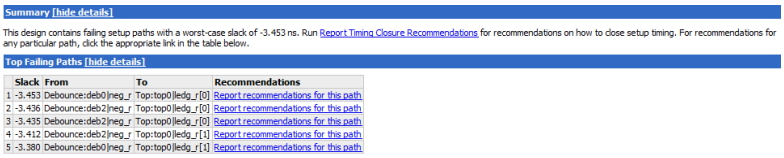
More specifically, each LED corresponds to a particular operating state of the recorder. From left to right, the states are: I2C, unused, unused, unused, play paused, play, record paused, record, and idle.

There are eight seven-segment displays on the FPGA board. The leftmost four display the current speed mode of the player, showing either FASt for fast mode or SLOU for slow mode. The rightmost seven-segment display shows the playback speed, ranging from 2 to 8 (i.e., 2× to 8× in fast mode, or 1/2× to 1/8× in slow mode). If the input speed exceeds this range, the value 1 is shown and the audio is played at normal speed.

6 Screen shot of Fitter Summary

Flow Status	Successful - Fri Oct 31 13:53:04 2025
Quartus II 64-Bit Version	15.0.0 Build 145 04/22/2015 SJ Full Version
Revision Name	DE2_115
Top-level Entity Name	DE2_115
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	1,156 / 114,480 (1 %)
Total combinational functions	1,141 / 114,480 (< 1 %)
Dedicated logic registers	265 / 114,480 (< 1 %)
Total registers	265
Total pins	518 / 529 (98 %)
Total virtual pins	0
Total memory bits	0 / 3,981,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 532 (0 %)
Total PLLs	1 / 4 (25 %)

7 Screen shot of Timing Analyzer



Summary [hide details]

This design contains failing setup paths with a worst-case slack of -3.453 ns. Run Report Timing Closure Recommendations for recommendations on how to close setup timing. For recommendations for any particular path, click the appropriate link in the table below.

Top Failing Paths [hide details]

	Slack	From	To	Recommendations
1	-3.453	Debounce:deb0|neg_r	Top:top0|ledg_r[0]	Report recommendations for this path
2	-3.436	Debounce:deb2|neg_r	Top:top0|ledg_r[0]	Report recommendations for this path
3	-3.435	Debounce:deb2|neg_r	Top:top0|ledg_r[0]	Report recommendations for this path
4	-3.412	Debounce:deb2|neg_r	Top:top0|ledg_r[1]	Report recommendations for this path
5	-3.380	Debounce:deb0|neg_r	Top:top0|ledg_r[1]	Report recommendations for this path

Slow 1200mV 85C Model Setup Summary

	Clock	Slack	End Point TNS
1	AUD_BCLK	-3.453	-41.732
2	pll0|altpll_0|sd1|pll7|clk[0]	80.602	0.000
3	pll0|altpll_0|sd1|pll7|clk[1]	9995.830	0.000

Slow 1200mV 85C Model Setup: 'AUD_BCLK'

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-3.453	Debounce:deb0|neg_r	Top:top0|ledg_r[0]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.182	5.544
2	-3.436	Debounce:deb2|neg_r	Top:top0|ledg_r[0]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.182	5.527
3	-3.412	Debounce:deb2|neg_r	Top:top0|ledg_r[1]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.182	5.503
4	-3.380	Debounce:deb0|neg_r	Top:top0|ledg_r[1]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.182	5.471
5	-3.372	Debounce:deb2|neg_r	Top:top0|ledg_r[2]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.126	5.407
6	-3.367	Debounce:deb0|neg_r	Top:top0|ledg_r[2]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.126	5.402
7	-3.322	Debounce:deb1|neg_r	Top:top0|ledg_r[0]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.182	5.413
8	-3.292	Debounce:deb2|neg_r	Top:top0|ledg_r[3]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.126	5.327
9	-3.284	Debounce:deb1|neg_r	Top:top0|ledg_r[1]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.182	5.375
10	-3.277	Debounce:deb0|neg_r	Top:top0|ledg_r[3]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.126	5.312
11	-3.256	Debounce:deb2|neg_r	Top:top0|ledg_r[4]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.126	5.291
12	-3.244	Debounce:deb1|neg_r	Top:top0|ledg_r[2]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.126	5.279
13	-3.208	Debounce:deb0|neg_r	Top:top0|ledg_r[4]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.126	5.243
14	-3.164	Debounce:deb1|neg_r	Top:top0|ledg_r[3]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.126	5.199
15	-3.150	Debounce:deb2|neg_r	Top:top0|ledg_r[8]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.191	5.250
16	-3.128	Debounce:deb1|neg_r	Top:top0|ledg_r[4]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.126	5.163
17	-3.081	Debounce:deb0|neg_r	Top:top0|ledg_r[8]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.191	5.181
18	-3.064	Debounce:deb1|neg_r	Top:top0|ledg_r[8]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.191	5.164
19	-2.672	Debounce:deb1|neg_r	Top:top0|state_r.S_I2C	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.191	4.772
20	-2.648	Debounce:deb2|neg_r	Top:top0|state_r.S_I2C	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.191	4.748
21	-2.609	Debounce:deb0|neg_r	Top:top0|record_pause_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.126	4.644
22	-2.582	Debounce:deb2|neg_r	Top:top0|dsp_stop_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.182	4.673
23	-2.579	Debounce:deb0|neg_r	Top:top0|state_r.S_I2C	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.191	4.679
24	-2.535	Debounce:deb0|neg_r	Top:top0|record_start_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.182	4.626
25	-2.510	Debounce:deb0|neg_r	Top:top0|record_resume_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.182	4.601
26	-2.508	Debounce:deb2|neg_r	Top:top0|record_stop_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.182	4.599
27	-2.428	Debounce:deb1|neg_r	Top:top0|dsp_resume_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.945	4.282
28	-2.325	Top:top0|I2cInitializer:init0|inst_count_r[1]	Top:top0|ledg_r[0]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	2.184	5.417
29	-2.319	Debounce:deb1|neg_r	Top:top0|dsp_pause_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.069	4.297
30	-2.314	Top:top0|I2cInitializer:init0|inst_count_r[3]	Top:top0|ledg_r[0]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	2.184	5.406
31	-2.302	Top:top0|I2cInitializer:init0|inst_count_r[1]	Top:top0|ledg_r[1]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	2.184	5.394
32	-2.291	Top:top0|I2cInitializer:init0|inst_count_r[3]	Top:top0|ledg_r[1]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	2.184	5.383
33	-2.262	Top:top0|I2cInitializer:init0|inst_count_r[1]	Top:top0|ledg_r[2]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	2.128	5.298
34	-2.251	Top:top0|I2cInitializer:init0|inst_count_r[3]	Top:top0|ledg_r[2]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	2.128	5.287
35	-2.206	Top:top0|I2cInitializer:init0|inst_count_r[2]	Top:top0|ledg_r[0]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	2.184	5.298
36	-2.185	Top:top0|I2cInitializer:init0|inst_count_r[0]	Top:top0|ledg_r[0]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	2.184	5.277
37	-2.182	Top:top0|I2cInitializer:init0|inst_count_r[1]	Top:top0|ledg_r[3]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	2.128	5.218

Slow 1200mV 85C Model Setup: 'AUD_BCLK'

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
37	-2.182	Top:top0|I2cInitializer:init0|inst_count_r[1]	Top:top0|ledg_r[3]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	2.128	5.218
38	-2.171	Top:top0|I2cInitializer:init0|inst_count_r[3]	Top:top0|ledg_r[3]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	2.128	5.207
39	-2.163	Debounce:deb1|neg_r	Top:top0|dsp_stop_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.182	4.254
40	-2.146	Top:top0|I2cInitializer:init0|inst_count_r[1]	Top:top0|ledg_r[4]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	2.128	5.182
41	-2.135	Top:top0|I2cInitializer:init0|inst_count_r[3]	Top:top0|ledg_r[4]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	2.128	5.171
42	-2.133	Top:top0|I2cInitializer:init0|inst_count_r[2]	Top:top0|ledg_r[1]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	2.184	5.225
43	-2.120	Top:top0|I2cInitializer:init0|inst_count_r[2]	Top:top0|ledg_r[2]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	2.128	5.156
44	-2.112	Top:top0|I2cInitializer:init0|inst_count_r[0]	Top:top0|ledg_r[1]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	2.184	5.204
45	-2.099	Top:top0|I2cInitializer:init0|inst_count_r[0]	Top:top0|ledg_r[2]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	2.128	5.135
46	-2.030	Top:top0|I2cInitializer:init0|inst_count_r[2]	Top:top0|ledg_r[3]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	2.128	5.066
47	-2.028	Top:top0|I2cInitializer:init0|inst_count_r[1]	Top:top0|ledg_r[8]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	2.193	5.129
48	-2.017	Top:top0|I2cInitializer:init0|inst_count_r[3]	Top:top0|ledg_r[8]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	2.193	5.118
49	-2.009	Top:top0|I2cInitializer:init0|inst_count_r[0]	Top:top0|ledg_r[3]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	2.128	5.045
50	-1.979	Debounce:deb0|neg_r	Top:top0|record_stop_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.182	4.070
51	-1.961	Top:top0|I2cInitializer:init0|inst_count_r[2]	Top:top0|ledg_r[4]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	2.128	4.997
52	-1.940	Top:top0|I2cInitializer:init0|inst_count_r[0]	Top:top0|ledg_r[4]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	2.128	4.976
53	-1.916	Top:top0|I2cInitializer:init0|inst_count_r[2]	Top:top0|ledg_r[8]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	2.193	5.017
54	-1.895	Top:top0|I2cInitializer:init0|inst_count_r[0]	Top:top0|ledg_r[8]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	2.193	4.996
55	-1.746	Top:top0|I2cInitializer:init0|inst_count_r[1]	Top:top0|state_r.S_I2C	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	2.193	4.847
56	-1.728	Top:top0|I2cInitializer:init0|inst_count_r[3]	Top:top0|state_r.S_I2C	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	2.193	4.829
57	-1.671	Top:top0|I2cInitializer:init0|inst_count_r[2]	Top:top0|state_r.S_I2C	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	2.193	4.772
58	-1.650	Top:top0|I2cInitializer:init0|inst_count_r[0]	Top:top0|state_r.S_I2C	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	2.193	4.751
59	-1.634	Debounce:deb1|neg_r	Top:top0|dsp_start_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.126	3.669
60	-1.284	Debounce:deb0|neg_r	Top:top0|dsp_start_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	2.126	3.319

Slow 1200mV 0C Model Setup Summary

	Clock	Slack	End Point TNS
1	AUD_BCLK	-3.210	-39.680
2	pll0|altpll_0|sd1|pll7|clk[0]	80.821	0.000
3	pll0|altpll_0|sd1|pll7|clk[1]	9996.216	0.000

Slow 1200mV 0C Model Setup: 'AUD_BCLK'

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-3.210	Debounce:deb2|neg_r	Top:top0|ledg_r[1]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.965	5.085
2	-3.200	Debounce:deb2|neg_r	Top:top0|ledg_r[0]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.965	5.075
3	-3.161	Debounce:deb0|neg_r	Top:top0|ledg_r[1]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.965	5.036
4	-3.160	Debounce:deb2|neg_r	Top:top0|ledg_r[2]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.907	4.977
5	-3.160	Debounce:deb0|neg_r	Top:top0|ledg_r[0]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.965	5.035
6	-3.111	Debounce:deb0|neg_r	Top:top0|ledg_r[2]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.907	4.928
7	-3.101	Debounce:deb1|neg_r	Top:top0|ledg_r[1]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.965	4.976
8	-3.094	Debounce:deb2|neg_r	Top:top0|ledg_r[3]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.907	4.911
9	-3.091	Debounce:deb1|neg_r	Top:top0|ledg_r[0]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.965	4.966
10	-3.066	Debounce:deb2|neg_r	Top:top0|ledg_r[4]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.907	4.883
11	-3.051	Debounce:deb1|neg_r	Top:top0|ledg_r[2]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.907	4.868
12	-3.045	Debounce:deb0|neg_r	Top:top0|ledg_r[3]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.907	4.862
13	-3.017	Debounce:deb0|neg_r	Top:top0|ledg_r[4]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.907	4.834
14	-2.985	Debounce:deb1|neg_r	Top:top0|ledg_r[3]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.907	4.802
15	-2.969	Debounce:deb2|neg_r	Top:top0|ledg_r[8]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.968	4.847
16	-2.957	Debounce:deb1|neg_r	Top:top0|ledg_r[4]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.907	4.774
17	-2.920	Debounce:deb0|neg_r	Top:top0|ledg_r[8]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.968	4.798
18	-2.918	Debounce:deb1|neg_r	Top:top0|ledg_r[8]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.968	4.796
19	-2.536	Debounce:deb2|neg_r	Top:top0|state_r.S_I2C	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.968	4.414
20	-2.504	Debounce:deb0|neg_r	Top:top0|record_pause_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.907	4.321
21	-2.484	Debounce:deb2|neg_r	Top:top0|dsp_stop_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.965	4.359
22	-2.462	Debounce:deb1|neg_r	Top:top0|state_r.S_I2C	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.968	4.340
23	-2.444	Debounce:deb0|neg_r	Top:top0|state_r.S_I2C	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.968	4.322
24	-2.429	Debounce:deb0|neg_r	Top:top0|record_start_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.965	4.304
25	-2.419	Debounce:deb0|neg_r	Top:top0|record_resume_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.965	4.294
26	-2.418	Debounce:deb2|neg_r	Top:top0|record_stop_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.965	4.293
27	-2.352	Debounce:deb1|neg_r	Top:top0|dsp_resume_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.742	4.004
28	-2.242	Debounce:deb1|neg_r	Top:top0|dsp_pause_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.856	4.008
29	-2.085	Top:top0|I2cInitializer:init0|inst_count_r[1]	Top:top0|ledg_r[0]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.968	4.962
30	-2.071	Top:top0|I2cInitializer:init0|inst_count_r[3]	Top:top0|ledg_r[0]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.968	4.948
31	-2.058	Top:top0|I2cInitializer:init0|inst_count_r[1]	Top:top0|ledg_r[1]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.968	4.935
32	-2.052	Top:top0|I2cInitializer:init0|inst_count_r[3]	Top:top0|ledg_r[1]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.968	4.929
33	-2.020	Debounce:deb1|neg_r	Top:top0|dsp_stop_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.965	3.895
34	-2.008	Top:top0|I2cInitializer:init0|inst_count_r[1]	Top:top0|ledg_r[2]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.910	4.827
35	-2.002	Top:top0|I2cInitializer:init0|inst_count_r[3]	Top:top0|ledg_r[2]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.910	4.821
36	-1.994	Top:top0|I2cInitializer:init0|inst_count_r[2]	Top:top0|ledg_r[0]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.968	4.871
37	-1.972	Top:top0|I2cInitializer:init0|inst_count_r[0]	Top:top0|ledg_r[0]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.968	4.849

Slow 1200mV 0C Model Setup: 'AUD_BCLK'

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
37	-1.972	Top:top0|I2cInitializer:init0|inst_count_r[0]	Top:top0|ledg_r[0]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.968	4.849
38	-1.942	Top:top0|I2cInitializer:init0|inst_count_r[1]	Top:top0|ledg_r[3]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.910	4.761
39	-1.936	Top:top0|I2cInitializer:init0|inst_count_r[3]	Top:top0|ledg_r[3]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.910	4.755
40	-1.914	Top:top0|I2cInitializer:init0|inst_count_r[1]	Top:top0|ledg_r[4]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.910	4.733
41	-1.912	Top:top0|I2cInitializer:init0|inst_count_r[2]	Top:top0|ledg_r[2]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.910	4.731
42	-1.908	Top:top0|I2cInitializer:init0|inst_count_r[3]	Top:top0|ledg_r[4]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.910	4.727
43	-1.903	Top:top0|I2cInitializer:init0|inst_count_r[2]	Top:top0|ledg_r[1]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.968	4.780
44	-1.898	Top:top0|I2cInitializer:init0|inst_count_r[0]	Top:top0|ledg_r[1]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.968	4.775
45	-1.890	Top:top0|I2cInitializer:init0|inst_count_r[0]	Top:top0|ledg_r[2]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.910	4.709
46	-1.854	Debounce:deb0|neg_r	Top:top0|record_stop_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.965	3.729
47	-1.845	Top:top0|I2cInitializer:init0|inst_count_r[2]	Top:top0|ledg_r[3]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.910	4.664
48	-1.827	Top:top0|I2cInitializer:init0|inst_count_r[1]	Top:top0|ledg_r[8]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.971	4.707
49	-1.823	Top:top0|I2cInitializer:init0|inst_count_r[0]	Top:top0|ledg_r[3]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.910	4.642
50	-1.813	Top:top0|I2cInitializer:init0|inst_count_r[3]	Top:top0|ledg_r[8]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.971	4.693
51	-1.754	Top:top0|I2cInitializer:init0|inst_count_r[0]	Top:top0|ledg_r[4]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.910	4.573
52	-1.736	Top:top0|I2cInitializer:init0|inst_count_r[2]	Top:top0|ledg_r[8]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.971	4.616
53	-1.728	Top:top0|I2cInitializer:init0|inst_count_r[2]	Top:top0|ledg_r[4]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.910	4.547
54	-1.714	Top:top0|I2cInitializer:init0|inst_count_r[0]	Top:top0|ledg_r[8]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.971	4.594
55	-1.655	Top:top0|I2cInitializer:init0|inst_count_r[1]	Top:top0|state_r.S_I2C	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.971	4.535
56	-1.641	Top:top0|I2cInitializer:init0|inst_count_r[3]	Top:top0|state_r.S_I2C	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.971	4.521
57	-1.597	Debounce:deb1|neg_r	Top:top0|dsp_start_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.907	3.414
58	-1.564	Top:top0|I2cInitializer:init0|inst_count_r[2]	Top:top0|state_r.S_I2C	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.971	4.444
59	-1.542	Top:top0|I2cInitializer:init0|inst_count_r[0]	Top:top0|state_r.S_I2C	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.971	4.422
60	-1.202	Debounce:deb0|neg_r	Top:top0|dsp_start_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.907	3.019

Fast 1200mV 0C Model Setup Summary

	Clock	Slack	End Point TNS
1	AUD_BCLK	-1.690	-22.083
2	pll0|altpll_0|sd1|pll7|clk[0]	81.998	0.000
3	pll0|altpll_0|sd1|pll7|clk[1]	9997.978	0.000

Fast 1200mV 0C Model Hold Summary

	Clock	Slack	End Point TNS
1	AUD_BCLK	-0.047	-0.047
2	pll0|altpll_0|sd1|pll7|clk[1]	0.174	0.000
3	pll0|altpll_0|sd1|pll7|clk[0]	0.182	0.000

Fast 1200mV 0C Model Setup: 'AUD_BCLK'

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-1.690	Debounce:deb0|neg_r	Top:top0|ledg_r[1]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.103	2.691
2	-1.687	Debounce:deb0|neg_r	Top:top0|ledg_r[2]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.076	2.661
3	-1.673	Debounce:deb0|neg_r	Top:top0|ledg_r[0]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.103	2.674
4	-1.653	Debounce:deb2|neg_r	Top:top0|ledg_r[1]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.103	2.654
5	-1.650	Debounce:deb2|neg_r	Top:top0|ledg_r[2]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.076	2.624
6	-1.636	Debounce:deb2|neg_r	Top:top0|ledg_r[0]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.103	2.637
7	-1.630	Debounce:deb0|neg_r	Top:top0|ledg_r[3]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.076	2.604
8	-1.601	Debounce:deb0|neg_r	Top:top0|ledg_r[4]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.076	2.575
9	-1.601	Debounce:deb1|neg_r	Top:top0|ledg_r[1]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.103	2.602
10	-1.598	Debounce:deb1|neg_r	Top:top0|ledg_r[2]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.076	2.572
11	-1.593	Debounce:deb2|neg_r	Top:top0|ledg_r[3]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.076	2.567
12	-1.584	Debounce:deb1|neg_r	Top:top0|ledg_r[0]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.103	2.585
13	-1.566	Debounce:deb0|neg_r	Top:top0|ledg_r[8]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.104	2.568
14	-1.564	Debounce:deb2|neg_r	Top:top0|ledg_r[4]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.076	2.538
15	-1.541	Debounce:deb1|neg_r	Top:top0|ledg_r[3]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.076	2.515
16	-1.529	Debounce:deb2|neg_r	Top:top0|ledg_r[8]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.104	2.531
17	-1.517	Debounce:deb1|neg_r	Top:top0|ledg_r[8]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.104	2.519
18	-1.512	Debounce:deb1|neg_r	Top:top0|ledg_r[4]	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.076	2.486
19	-1.482	Debounce:deb2|neg_r	Top:top0|dsp_stop_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.103	2.483
20	-1.461	Debounce:deb0|neg_r	Top:top0|record_pause_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.076	2.435
21	-1.443	Debounce:deb0|neg_r	Top:top0|record_start_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.103	2.444
22	-1.441	Debounce:deb2|neg_r	Top:top0|record_stop_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.103	2.442
23	-1.441	Debounce:deb2|neg_r	Top:top0|state_r.S_I2C	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.104	2.443
24	-1.415	Debounce:deb0|neg_r	Top:top0|record_resume_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.103	2.416
25	-1.396	Debounce:deb0|neg_r	Top:top0|state_r.S_I2C	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.104	2.398
26	-1.359	Debounce:deb1|neg_r	Top:top0|dsp_resume_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	0.992	2.249
27	-1.347	Debounce:deb1|neg_r	Top:top0|state_r.S_I2C	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.104	2.349
28	-1.315	Debounce:deb1|neg_r	Top:top0|dsp_pause_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.029	2.242
29	-1.089	Debounce:deb1|neg_r	Top:top0|dsp_stop_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.103	2.090
30	-0.999	Debounce:deb0|neg_r	Top:top0|record_stop_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.103	2.000
31	-0.879	Debounce:deb1|neg_r	Top:top0|dsp_start_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.076	1.853
32	-0.638	Top:top0|I2cInitialzer:init0|inst_count_r[1]	Top:top0|ledg_r[0]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.104	2.639
33	-0.631	Top:top0|I2cInitialzer:init0|inst_count_r[3]	Top:top0|ledg_r[0]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.104	2.632
34	-0.606	Top:top0|I2cInitialzer:init0|inst_count_r[1]	Top:top0|ledg_r[2]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.077	2.580
35	-0.599	Top:top0|I2cInitialzer:init0|inst_count_r[3]	Top:top0|ledg_r[2]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.077	2.573
36	-0.598	Debounce:deb0|neg_r	Top:top0|dsp_start_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.001	1.076	1.572
37	-0.581	Top:top0|I2cInitialzer:init0|inst_count_r[1]	Top:top0|ledg_r[1]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.104	2.582

Fast 1200mV 0C Model Setup: 'AUD_BCLK'

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
37	-0.581	Top:top0|I2cInitialzer:init0|inst_count_r[1]	Top:top0|ledg_r[1]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.104	2.582
38	-0.574	Top:top0|I2cInitialzer:init0|inst_count_r[3]	Top:top0|ledg_r[1]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.104	2.575
39	-0.548	Top:top0|I2cInitialzer:init0|inst_count_r[1]	Top:top0|ledg_r[3]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.077	2.522
40	-0.547	Top:top0|I2cInitialzer:init0|inst_count_r[1]	Top:top0|ledg_r[8]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.105	2.549
41	-0.541	Top:top0|I2cInitialzer:init0|inst_count_r[3]	Top:top0|ledg_r[3]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.077	2.515
42	-0.540	Top:top0|I2cInitialzer:init0|inst_count_r[3]	Top:top0|ledg_r[8]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.105	2.542
43	-0.519	Top:top0|I2cInitialzer:init0|inst_count_r[2]	Top:top0|ledg_r[1]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.104	2.520
44	-0.516	Top:top0|I2cInitialzer:init0|inst_count_r[2]	Top:top0|ledg_r[2]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.077	2.490
45	-0.509	Top:top0|I2cInitialzer:init0|inst_count_r[0]	Top:top0|ledg_r[1]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.104	2.510
46	-0.508	Top:top0|I2cInitialzer:init0|inst_count_r[1]	Top:top0|state_r.S_I2C	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.105	2.510
47	-0.506	Top:top0|I2cInitialzer:init0|inst_count_r[0]	Top:top0|ledg_r[2]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.077	2.480
48	-0.502	Top:top0|I2cInitialzer:init0|inst_count_r[2]	Top:top0|ledg_r[0]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.104	2.503
49	-0.501	Top:top0|I2cInitialzer:init0|inst_count_r[3]	Top:top0|state_r.S_I2C	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.105	2.503
50	-0.492	Top:top0|I2cInitialzer:init0|inst_count_r[0]	Top:top0|ledg_r[0]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.104	2.493
51	-0.484	Top:top0|I2cInitialzer:init0|inst_count_r[1]	Top:top0|ledg_r[4]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.077	2.458
52	-0.477	Top:top0|I2cInitialzer:init0|inst_count_r[3]	Top:top0|ledg_r[4]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.077	2.451
53	-0.459	Top:top0|I2cInitialzer:init0|inst_count_r[2]	Top:top0|ledg_r[3]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.077	2.433
54	-0.449	Top:top0|I2cInitialzer:init0|inst_count_r[0]	Top:top0|ledg_r[3]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.077	2.423
55	-0.430	Top:top0|I2cInitialzer:init0|inst_count_r[2]	Top:top0|ledg_r[4]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.077	2.404
56	-0.420	Top:top0|I2cInitialzer:init0|inst_count_r[0]	Top:top0|ledg_r[4]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.077	2.394
57	-0.402	Top:top0|I2cInitialzer:init0|inst_count_r[2]	Top:top0|ledg_r[8]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.105	2.404
58	-0.395	Top:top0|I2cInitialzer:init0|inst_count_r[0]	Top:top0|ledg_r[8]	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.105	2.397
59	-0.363	Top:top0|I2cInitialzer:init0|inst_count_r[2]	Top:top0|state_r.S_I2C	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.105	2.365
60	-0.356	Top:top0|I2cInitialzer:init0|inst_count_r[0]	Top:top0|state_r.S_I2C	pll0|altpll_0|sd1|pll7|clk[1]	AUD_BCLK	1.000	1.105	2.358

Fast 1200mV 0C Model Hold: 'AUD_BCLK'

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-0.047	Debounce:deb0|neg_r	Top:top0|dsp_start_r	pll0|altpll_0|sd1|pll7|clk[0]	AUD_BCLK	0.000	1.383	1.500

Multicorner Timing Analysis Summary

	Clock	Setup	Hold	Recovery	Removal	Minimum Pulse Width
1	Worst-case Slack	-3.453	-0.047	N/A	N/A	9.400
1	AUD_BCLK	-3.453	-0.047	N/A	N/A	40.692
2	CLOCK2_50	N/A	N/A	N/A	N/A	16.000
3	CLOCK3_50	N/A	N/A	N/A	N/A	16.000
4	CLOCK_50	N/A	N/A	N/A	N/A	9.400
5	pll0|altpll_0|sd1|pll7|clk[0]	80.602	0.182	N/A	N/A	41.374
6	pll0|altpll_0|sd1|pll7|clk[1]	9995.830	0.174	N/A	N/A	4999.693
2	Design-wide TNS	-41.732	-0.047	0.0	0.0	0.0
1	AUD_BCLK	-41.732	-0.047	N/A	N/A	0.000
2	CLOCK2_50	N/A	N/A	N/A	N/A	0.000
3	CLOCK3_50	N/A	N/A	N/A	N/A	0.000
4	CLOCK_50	N/A	N/A	N/A	N/A	0.000
5	pll0|altpll_0|sd1|pll7|clk[0]	0.000	0.000	N/A	N/A	0.000
6	pll0|altpll_0|sd1|pll7|clk[1]	0.000	0.000	N/A	N/A	0.000

Unconstrained Paths

	Property	Setup	Hold
1	Illegal Clocks	0	0
2	Unconstrained Clocks	0	0
3	Unconstrained Input Ports	29	29
4	Unconstrained Input Port Paths	568	568
5	Unconstrained Output Ports	68	68
6	Unconstrained Output Port Paths	233	233

8 Problems Encountered

We encountered several challenges during Lab 3. The first issue was the lack of detailed specifications regarding the I2C and I2S protocols, so we relied on trial and error to determine the correct data transmission behavior.

The second difficulty was debugging. Since the system cannot be fully verified in simulation and must be deployed on the FPGA for testing, debugging became more complicated. To overcome this, we used LED indicators to observe the internal FSM states of each module. However, the overall correctness could only be confirmed based on whether the final audio output was correct.