Quiz 2

BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI

Hyderabad Campus, Second Semester 2020-2021

CS/ ECE /EEE/ INSTR F241 Microprocessor Programming & Interfacing

Quiz-2 (Open Book)

Date: 01/04/21 Max Marks : 15
Day: Thursday Time :9.15 - 9.45 AM

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Not f20190506@hyderabad.bits-pilani.ac.in? Switch account

* Required

To have multiprocessing capabilities of the 8086 microprocessors, which of the following pins should be connected to the ground.	ch 1 point
O DEN'	
○ ALE	
○ INTR	
● MN/MX'	
Clear	r selection

Match the following

1 point

- (a) NMI
- (1) CLD
- (b) READY (2) CALL
- (c) ES
- ...(3) OUT
- (d) RET
- (4) ISR
- a-2, b-1, c-3, d-4
- a-1, b-4, c-3, d-2
- a-3, b-4, c-1, d-2
- a-4, b-3, c-1, d-2

Clear selection

Match the following

1 point

Type of Interrupt

- (a) NMI
- (b) Divide by zero
- (c) Overflow
- (d) Single step
- (a) a-3, b-1, c-4, d-2
-) a-3, b-2, c-4, d-1
- a-4, b-3, c-1, d-2
- a-1, b-2, c-3, d-4

Physical address of CS

- __(1) 00002H
 - (2) 00006H
 - (3) 0000AH
 - (4) 00012H

Clear selection

What will be the OP Code for the following instruction?	1 point
Address Instruction 0139 JMP 11E	
○ EB E2	
○ EB E3	
● EB E4	
○ EB E5	
None of the above	
	Clear selection
The Programmable interrupt controller is used to	1 point
Handle one interrupt request	
Handle one or more interrupt requests at a time	
Handle one or more interrupt requests with a delay	
Handle no interrupt request	
	Clear selection
If a 30 MHz Crystal is connected to 8284 A, and with F/C' conground, the (i) EFI output, (ii) Peripheral Clock output and (ii) for 8086 will be	
30 MHz, 15 MHz and 15 MHz respectively	
15 MHz, 10 MHz and 5 MHz respectively	
30 MHz, 5 MHz and 10 MHz respectively	
30 MHz, 7.5 MHz and 15 MHz respectively	
Other:	

If a processor is working at 5 MHz and the memory access time is 750ns. The number of wait states required will be, considering an address set-up time of 110ns, data set-up time of 40 ns with a latching and buffer delays of 30ns. 1 2 3 4 None of the above Match the following: (a) Size of IP	16	
address set-up time of 110ns, data set-up time of 40 ns with a latching and buffer delays of 30ns. 1 2 3 4 None of the above Match the following: (a) Size of IP (b) Size of ALU (c) Word length (c) Size of ALU (d) Size of AL (d) Internal address bus a-1, b-2, c-4, d-3 a-3, b-2, c-1, d-4 a-4, b-2, c-1, d-3 A-4, b-1, c-2, d-3 Which of the following interrupt request in independent of IF flag status? NMI TRAP DIVIDE BY ZERO ALL OF THESE		1 point
☐ 1 ☐ 2 ☐ 3 ☐ 4 ☐ None of the above Match the following: (a) Size of IP		
O 2 O 3 O 4 O None of the above Match the following: (a) Size of IP (b) Size of ALU (c) Size of accessible memory (d) Size of AL (e) Size of AL (f) Internal address bus (h) Size of AL (h) (h) Si	buffer delays of 30ns.	
	O 1	
Match the following: (a) Size of IP (1) External address bus (b) Size of ALU (c) Size of accessible memory (d) Size of AL (d) Size of AL (e) Size of AL (f) Internal address bus a-1, b-2, c-4, d-3 a-3, b-2, c-1, d-4 a-4, b-2, c-1, d-3 Which of the following interrupt request in independent of IF flag status? NMI TRAP DIVIDE BY ZERO ALL OF THESE	O 2	
Match the following: (a) Size of IP (b) Size of ALU (c) Size of Accessible memory (d) Size of AL (e) Size of AL (f) Internal address bus (g) Word length (g) Size of AL (g) Size of AL (g) Word length (g) Size of AL (g) Word length (g) Size of AL (O 3	
Match the following: (a) Size of IP (b) Size of ALU (c) Size of ACCESSIBLE memory (d) Size of AL (d) Internal address bus (e) Size of AL (f) Internal address bus (g) Size of AL (h) Internal address bus (h) Size of AL (h) Internal address bus (h) Internal address bus	O 4	
Match the following: (a) Size of IP (b) Size of ALU (c) Size of accessible memory (d) Size of AL (e) Size of AL (f) Internal data bus/2 (d) Size of AL (e) Size of AL (f) Internal data bus/2 (g) Word length (g) Size of AL (g) Word length (g) Size of AL (h) Internal data bus/2 (h) Internal address bus (o) a-1, b-2, c-4, d-3 (o) a-3, b-2, c-1, d-4 (o) a-4, b-2, c-1, d-3 (o) a-4, b-1, c-2, d-3 Which of the following interrupt request in independent of IF flag status? (o) NMI (o) TRAP (o) DIVIDE BY ZERO (o) ALL OF THESE	None of the above	
(a) Size of IP (b) Size of ALU (c) Size of accessible memory (d) Size of AL (d) Size of AL (e) Size of AL (f) Internal address bus (o) Size of AL (d) Size of AL (e) Size of AL (f) Internal address bus (o) a-1, b-2, c-4, d-3 (o) a-3, b-2, c-1, d-4 (o) a-4, b-2, c-1, d-3 (o) a-4, b-1, c-2, d-3 Which of the following interrupt request in independent of IF flag status? (o) NMI (o) TRAP (o) DIVIDE BY ZERO (o) ALL OF THESE	Match the following	1 point
(b) Size of ALU (c) Size of accessible memory (d) Size of AL a-1, b-2, c-4, d-3 a-3, b-2, c-1, d-4 a-4, b-2, c-1, d-3 Which of the following interrupt request in independent of IF flag status? NMI TRAP DIVIDE BY ZERO ALL OF THESE	Match the following:	
(c) Size of accessible memory (d) Size of AL (4) Internal data bus/2 (4) Size of AL (4) Internal address bus a-1, b-2, c-4, d-3 a-3, b-2, c-1, d-4 a-4, b-2, c-1, d-3 a-4, b-1, c-2, d-3 Which of the following interrupt request in independent of IF flag status? 1 point NMI TRAP DIVIDE BY ZERO ALL OF THESE	(a) Size of IP (1) External address bus	
 □ a-1, b-2, c-4, d-3 □ a-3, b-2, c-1, d-4 □ a-4, b-2, c-1, d-3 □ a-4, b-1, c-2, d-3 Which of the following interrupt request in independent of IF flag status? 1 point NMI TRAP □ DIVIDE BY ZERO ● ALL OF THESE 	(c) Size of accessible memory (3) Internal data bus/2	
 a-3, b-2, c-1, d-4 a-4, b-2, c-1, d-3 a-4, b-1, c-2, d-3 Which of the following interrupt request in independent of IF flag status? 1 point NMI TRAP DIVIDE BY ZERO ALL OF THESE	(d) Size of AL (4) Internal address bus	
 a-4, b-2, c-1, d-3 a-4, b-1, c-2, d-3 Which of the following interrupt request in independent of IF flag status? 1 point NMI TRAP DIVIDE BY ZERO ALL OF THESE 	a-1, b-2, c-4, d-3	
 a-4, b-1, c-2, d-3 Which of the following interrupt request in independent of IF flag status? 1 point NMI TRAP DIVIDE BY ZERO ALL OF THESE 	a-3, b-2, c-1, d-4	
Which of the following interrupt request in independent of IF flag status? NMI TRAP DIVIDE BY ZERO ALL OF THESE	a-4, b-2, c-1, d-3	
 NMI TRAP DIVIDE BY ZERO ALL OF THESE 	a-4, b-1, c-2, d-3	
TRAPDIVIDE BY ZEROALL OF THESE	Which of the following interrupt request in independent of IF flag status?	1 point
DIVIDE BY ZEROALL OF THESE	○ NMI	
ALL OF THESE	○ TRAP	
	O DIVIDE BY ZERO	
	ALL OF THESE	

For an 8086 processor, if the clock is operated at 5 MHz, the 1 cycle completes in sec.	machine 1 point
200 ns	
O 400 ns	
O 600 ns	
O 800 ns	
Other:	
	Clear selection
What will be the OP Code for the following instruction?	1 point
Address Instruction 0161 JMP 1AA	
○ EB 43	
○ EB 45	
○ EB 47	
● EB 49	
O NONE OF THE ABOVE	
	Clear selection

What is the duration of the bus cycle in an 8088 based microcomputer if 1 point the clock is 8 MHz and two wait states are inserted? 500 ns 750 ns 250 ns 800 ns Clear selection Processor senses an interrupt 1 point Immediately when the interrupt signal occurs After each machine cycle After each instruction cycle After an interval as set by the programmer Clear selection List the memory control signals together with their active logic levels that occur when a word of data is written to memory address A000016 in a minimum-mode 8086 microcomputer system. BHE' = 0, A0 = 0, WR' = 0, M/IO' = 1, DT/R' = 1, BHE' = 1, A0 = 0, WR' = 0, M/IO' = 1, DT/R' = 1, BHE' = 0, A0 = 0, WR' = 0, M/IO' = 1, DT/R' = 0 BHE' =1, A0 = 0, WR' = 0, M/IO' = 1, DT/R' = 0

The physical memory address in the vector table corresponding to INT 50 1 point is:-
IP: 000C8h, CS: 000CAh
OS: 000C8h, IP: 000CAh
O IP: 00032h, CS: 00034h
CS: 00032h, IP: 00034h
Clear selection
Name *
Sai Anoop
ID*
2019A8PS0506H
Send me a copy of my responses.
Submit
Never submit passwords through Google Forms.
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