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Bipolar Transistor

The Bipolar Junction Transistor is a semiconductor device which can be used for switching or amplification.

Unlike semiconductor diodes which are made up from two pieces of semiconductor material to form one simple pn-junction. The bipolar transistor uses one more layer of semiconductor material to produce a device with properties and characteristics of an amplifier.

If we join together two individual signal diodes back-to-back, this will give us two PN-junctions connected together in series which would share a common Positive, (P) or Negative, (N) terminal. The fusion of these two diodes produces a three layer, two junction, three terminal device forming the basis of a **Bipolar Junction Transistor**, or **BJT** for short.

Transistors are three terminal active devices made from different semiconductor materials that can act as either an insulator or a conductor by the application of a small signal voltage. The transistor's ability to change between these two states enables it to have two basic functions: "switching" (digital electronics) or "amplification" (analogue electronics). Then bipolar transistors have the ability to operate within three different regions:

- ✔ Active Region – the transistor operates as an amplifier and $I_C = \beta * I_B$
- ✔ Saturation – the transistor is "Fully-ON" operating as a switch and Ic = I(saturation)
- ✔ Cut-off – the transistor is "Fully-OFF" operating as a switch and $I_C = 0$

The word Transistor is a combination of the two words Transfer Varistor which describes their mode of operation way back in their early days of electronics development. There are two basic types of bipolar transistor construction, PNP and NPN, which basically describes the physical arrangement of the P-type and N-type semiconductor materials from which they are made.

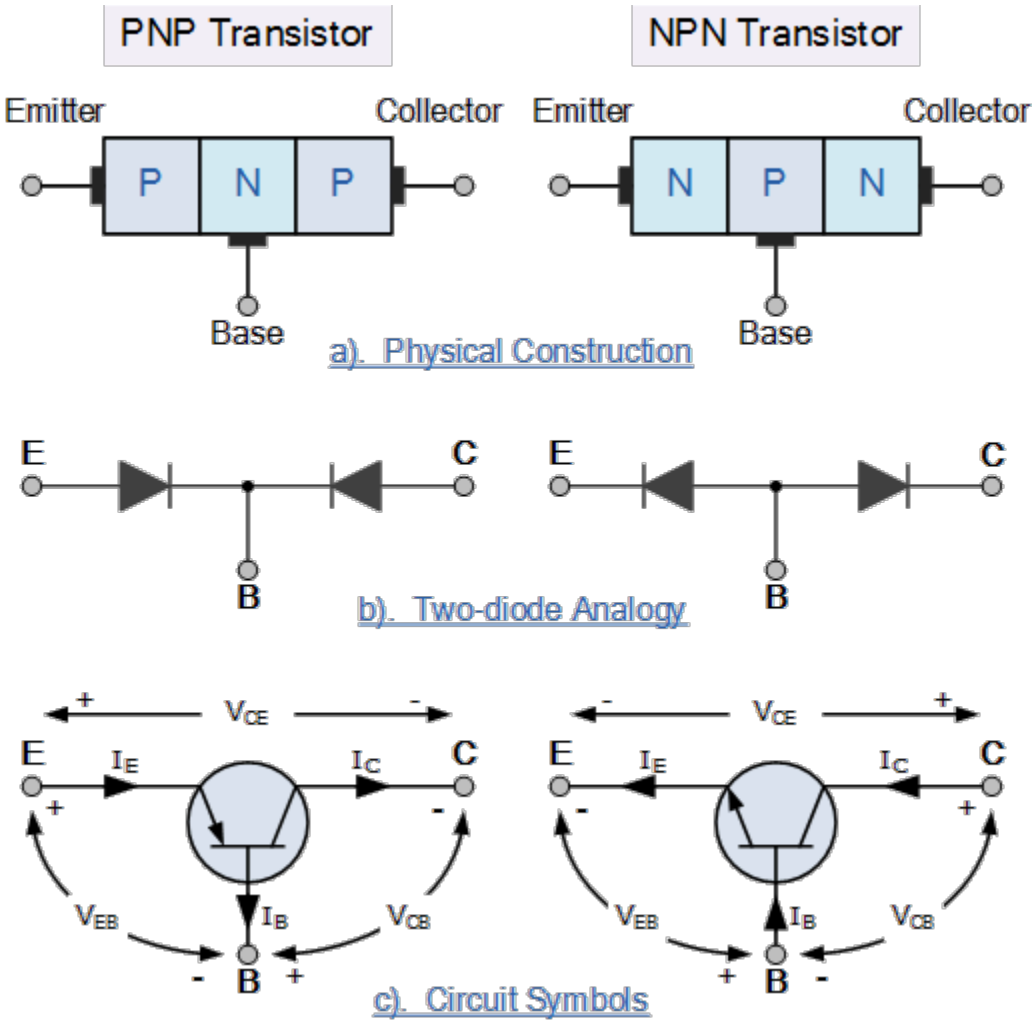
A Typical Bipolar Transistor

The **Bipolar Transistor** basic construction consists of two PN-junctions producing three connecting terminals with each terminal being given a name to identify it from the other two. These three terminals are known and labelled as the Emitter (E), the Base (B) and the Collector (C) respectively.

Bipolar Transistors are current regulating devices that control the amount of current flowing through them from the Emitter to the Collector terminals in proportion to the amount of biasing voltage applied to their base terminal, thus acting like a current-controlled switch. As a small current flowing into the base terminal controls a much larger collector current forming the basis of transistor action.

The principle of operation of the two transistor types PNP and NPN, is exactly the same the only difference being in their biasing and the polarity of the power supply for each type.

Bipolar Transistor Construction



The construction and circuit symbols for both the PNP and NPN bipolar transistor are given above with the arrow in the circuit symbol always showing the direction of “conventional current flow” between the base terminal and its emitter terminal. The direction of the arrow always points from the positive P-type region to the negative N-type region for both transistor types, exactly the same as for the standard diode symbol.

Bipolar Transistor Configurations

As the **Bipolar Transistor** is a three terminal device, there are basically three possible ways to connect it within an electronic circuit with one terminal being common to both the input and output signals. Each method of connection responding differently to its input signal within a circuit as the static characteristics of the transistor vary with each circuit arrangement.

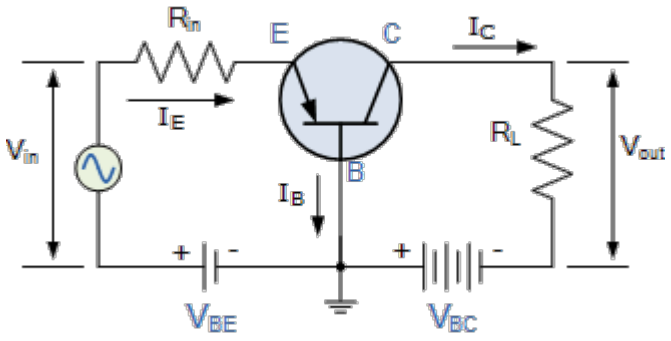
- ✔ Common Base Configuration – has Voltage Gain but no Current Gain.
- ✔ Common Emitter Configuration – has both Current and Voltage Gain.
- ✔ Common Collector Configuration – has Current Gain but no Voltage Gain.

The Common Base (CB) Configuration

As its name suggests, in the **Common Base** or grounded base configuration, the BASE connection is common to both the input signal AND the output signal. The input signal is applied between the transistors base and the emitter terminals, while the corresponding output signal is taken from between the base and the collector terminals as shown. The base terminal is grounded or can be connected to some fixed reference voltage point.

The input current flowing into the emitter is quite large as its the sum of both the base current and collector current respectively therefore, the collector current output is less than the emitter current input resulting in a current gain for this type of circuit of “1” (unity) or less, in other words the common base configuration “attenuates” the input signal.

The Common Base Transistor Circuit



This type of amplifier configuration is a non-inverting voltage amplifier circuit, in that the signal voltages Vin and Vout are “in-phase”. This type of transistor arrangement is not very common due to its unusually high voltage gain characteristics. Its input characteristics represent that of a forward biased diode while the output characteristics represent that of an illuminated photo-diode.

Also this type of bipolar transistor configuration has a high ratio of output to input resistance or more importantly “load” resistance (R_L) to “input” resistance (R_{IN}) giving it a value of “Resistance Gain”. Then the voltage gain (A_V) for a common base configuration is therefore given as:

Common Base Voltage Gain

$$A_V = \frac{Vout}{Vin} = \frac{I_C \times R_L}{I_E \times R_{IN}}$$

Where: I_C/I_E is the current gain, alpha (α) and R_L/R_{IN} is the resistance gain.

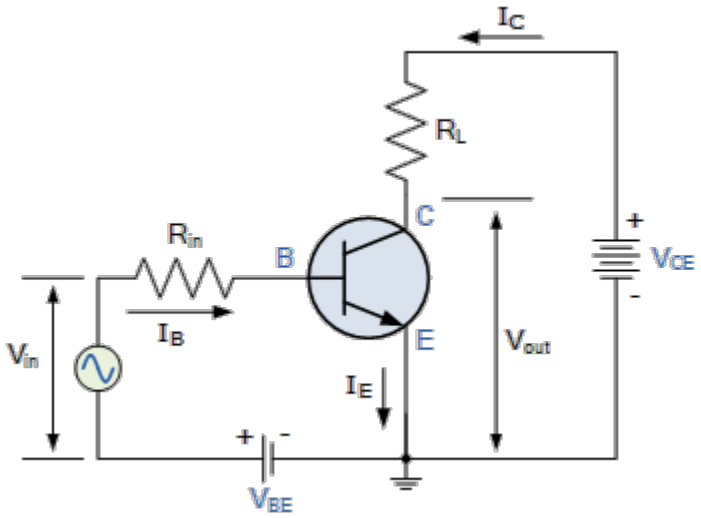
The common base circuit is generally only used in single stage amplifier circuits such as microphone pre-amplifier or radio frequency (Rf) amplifiers due to its very good high frequency response.

The Common Emitter (CE) Configuration

In the **Common Emitter** or grounded emitter configuration, the input signal is applied between the base and the emitter, while the output is taken from between the collector and the emitter as shown. This type of configuration is the most commonly used circuit for transistor based amplifiers and which represents the “normal” method of bipolar transistor connection.

The common emitter amplifier configuration produces the highest current and power gain of all the three bipolar transistor configurations. This is mainly because the input impedance is LOW as it is connected to a forward biased PN-junction, while the output impedance is HIGH as it is taken from a reverse biased PN-junction.

The Common Emitter Amplifier Circuit



In this type of configuration, the current flowing out of the transistor must be equal to the currents flowing into the transistor as the emitter current is given as $I_E = I_C + I_B$.

As the load resistance (R_L) is connected in series with the collector, the current gain of the common emitter transistor configuration is quite large as it is the ratio of I_C/I_B. A transistors current gain is given the Greek symbol of Beta, (β).

As the emitter current for a common emitter configuration is defined as $I_E = I_C + I_B$, the ratio of I_C/I_E is called Alpha, given the Greek symbol of α. Note: that the value of Alpha will always be less than unity.

Since the electrical relationship between these three currents, I_B, I_C and I_E is determined by the physical construction of the transistor itself, any small change in the base current (I_B), will result in a much larger change in the collector current (I_C).

Then, small changes in current flowing in the base will thus control the current in the emitter-collector circuit. Typically, Beta has a value between 20 and 200 for most general purpose transistors. So if a transistor has a Beta value of say 100, then one electron will flow from the base terminal for every 100 electrons flowing between the emitter-collector terminal.

By combining the expressions for both Alpha, α and Beta, β the mathematical relationship between these parameters and therefore the current gain of the transistor can be given as:

$$\text{Alpha},(\alpha) = \frac{I_C}{I_E} \quad \text{and} \quad \text{Beta},(\beta) = \frac{I_C}{I_B}$$

$$\therefore I_C = \alpha . I_E = \beta . I_B$$

$$\text{as:}\ \alpha = \frac{\beta}{\beta + 1} \qquad \beta = \frac{\alpha}{1 - \alpha}$$

$$I_E = I_C + I_B$$

Where: I_C is the current flowing into the collector terminal, I_B is the current flowing into the base terminal and “Ie” is the current flowing out of the emitter terminal.

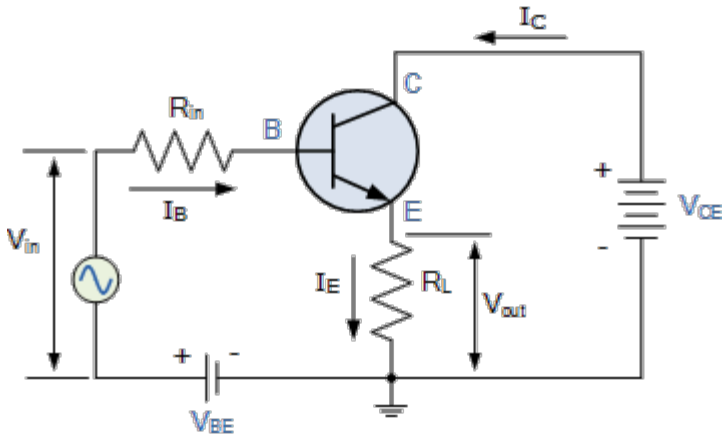
Then to summarise a little. This type of bipolar transistor configuration has a greater input impedance, current and power gain than that of the common base configuration but its voltage gain is much lower. The common emitter configuration is an inverting amplifier circuit. This means that the resulting output signal has a 180º phase-shift with regards to the input voltage signal.

The Common Collector (CC) Configuration

In the **Common Collector** or grounded collector configuration, the collector is connected to ground through the supply, thus the collector terminal is common to both the input and the output. The input signal is connected directly to the base terminal, while the output signal is taken from across the emitter load resistor as shown. This type of configuration is commonly known as a **Voltage Follower** or **Emitter Follower** circuit.

The common collector, or emitter follower configuration is very useful for impedance matching applications because of its very high input impedance, in the region of hundreds of thousands of Ohms while having a relatively low output impedance.

The Common Collector Transistor Circuit



The common emitter configuration has a current gain approximately equal to the β value of the transistor itself. However in the common collector configuration, the load resistance is connected in series with the emitter terminal so its current is equal to that of the emitter current.

As the emitter current is the combination of the collector AND the base current combined, the load resistance in this type of transistor configuration also has both the collector current and the input current of the base flowing through it. Then the current gain of the circuit is given as:

The Common Collector Current Gain

$$I_E = I_C + I_B$$

$$A_i = \frac{I_E}{I_B} = \frac{I_C + I_B}{I_B}$$

$$A_i = \frac{I_C}{I_B} + 1$$

$$A_i = \beta + 1$$

This type of bipolar transistor configuration is a non-inverting circuit in that the signal voltages of Vin and Vout are “in-phase”. The common collector configuration has a voltage gain of about “1” (unity gain). Thus it can considered as a voltage-buffer since the voltage gain is unity.

The load resistance of the common collector transistor receives both the base and collector currents giving a large current gain (as with the common emitter configuration) therefore, providing good current amplification with very little voltage gain.

Having looked at the three different types of bipolar transistor configurations, we can now summarise the various relationships between the transistors individual DC currents flowing through each leg and its DC current gains given above in the following table.

Relationship between DC Currents and Gains

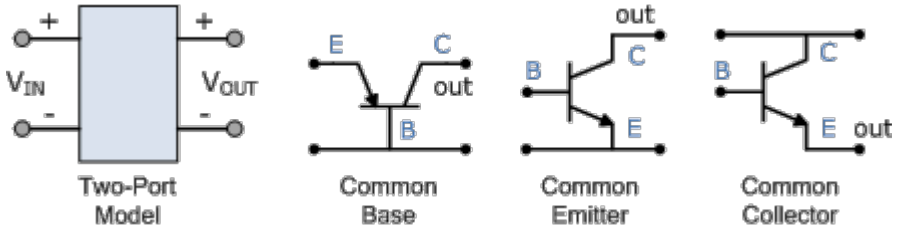
$I_E = I_B + I_C$ $I_C = I_E - I_B$ $I_B = I_E - I_C$	$\alpha = \frac{I_C}{I_E} = \frac{\beta}{1+\beta}$ $\beta = \frac{I_C}{I_B} = \frac{\alpha}{1-\alpha}$
$I_B = \frac{I_C}{\beta} = \frac{I_E}{1+\beta} = I_E(1-\alpha)$	
$I_C = \beta . I_B = \alpha . I_E$	$I_E = \frac{I_C}{\alpha} = I_B(1+\beta)$

Note that although we have looked at *NPN Bipolar Transistor* configurations here, PNP transistors are just as valid to use in each configuration as the calculations will all be the same, as for the non-inverting of the amplified signal. The only difference will be in the voltage polarities and current directions.

Bipolar Transistor Summary

Then to summarise, the behaviour of the bipolar transistor in each one of the above circuit configurations is very different and produces different circuit characteristics with regards to input impedance, output impedance and gain whether this is voltage gain, current gain or power gain and this is summarised in the table below.

Bipolar Transistor Configurations



with the generalised characteristics of the different transistor configurations given in the following table:

Characteristic	Common Base	Common Emitter	Common Collector
Input Impedance	Low	Medium	High
Output Impedance	Very High	High	Low
Phase Shift	0^o	180^o	0^o
Voltage Gain	High	Medium	Low
Current Gain	Low	Medium	High
Power Gain	Low	Very High	Medium

In the next tutorial about Bipolar Transistors, we will look at the NPN Transistor in more detail when used in the common emitter configuration as an amplifier as this is the most widely used configuration due to its flexibility and high gain. We will also plot the output characteristics curves commonly associated with amplifier circuits as a function of the collector current to the base current.

https://www.electronics-tutorials.ws/transistor/tran_2.html

NPN Transistor

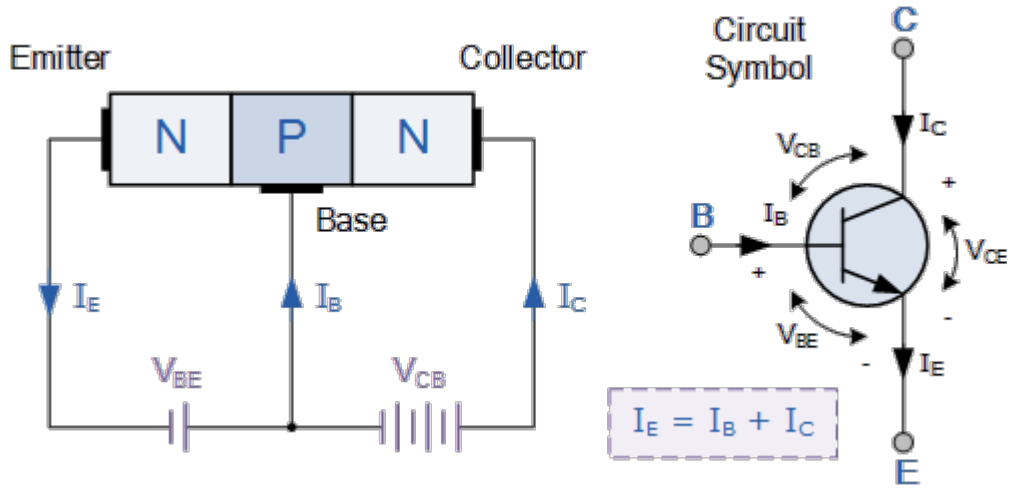
NPN Transistors are three-terminal, three-layer devices that can function as either amplifiers or electronic switches.

In the previous tutorial we saw that the standard **Bipolar Transistor** or BJT, comes in two basic forms. An **NPN** (**N**egative-**P**ositive-**N**egative) configuration and a **PNP** (**P**ositive-**N**egative-**P**ositive) configuration. That is: an NPN transistor and a PNP transistor types.

The most commonly used transistor configuration is the **NPN Transistor**. We also learnt that the junctions of the bipolar transistor can be biased in one of three different ways – **Common Base**, **Common Emitter** and **Common Collector**.

In this tutorial about bipolar transistors we will look more closely at the "Common Emitter" configuration using the **Bipolar NPN Transistor** with an example of the construction of a NPN transistor along with the transistors current flow characteristics is given below.

A Bipolar NPN Transistor Configuration

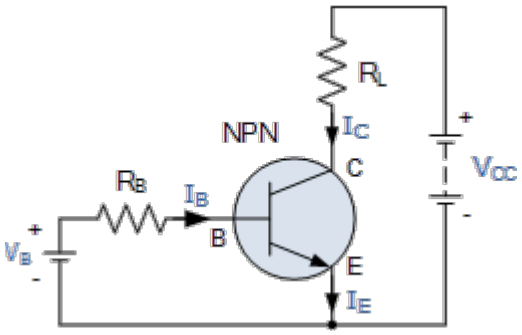


(Note: Arrow defines the emitter and conventional current flow, "out" for a Bipolar NPN Transistor.)

The construction and terminal voltages for a bipolar NPN transistor are shown above. The voltage between the Base and Emitter (V_{BE}), is positive at the Base and negative at the Emitter because for an NPN transistor, the Base terminal is always positive with respect to the Emitter. The Collector supply voltage must also be more positive with respect to the Emitter (V_{CE}).

Therefore, for a bipolar NPN transistor to conduct correctly, the Collector must always more positive with respect to both the Base and the Emitter terminals.

Then the voltage sources are connected to an NPN transistor as shown. The Collector is connected to the supply voltage V_{CC} via the load resistor, R_L which also acts to limit the maximum current flowing through the device.



NPN Transistor Connection

The Base supply voltage V_B is connected to the Base resistor R_B, which again is used to limit the maximum Base current.

So in a NPN Transistor it is the movement of negative current carriers (electrons) through the Base region that constitutes transistor action, since these mobile electrons provide the link between the Collector and Emitter circuits. This link between the input and output circuits is the main feature of transistor action because the transistors amplifying properties come from the consequent control which the Base exerts upon the Collector to Emitter current.

Then we can see that the transistor is a current operated device (Beta model) and that a large current (I_C) flows freely through the device between the collector and the emitter terminals when the transistor is switched “fully-ON”. However, this only happens when a small biasing current (I_B) is flowing into the base terminal of the transistor at the same time thus allowing the Base to act as a sort of current control input.

The current in a bipolar NPN transistor is the ratio of these two currents (I_C/I_B), called the *DC Current Gain* of the device and is given the symbol of hfe or nowadays Beta, (β).

The value of β can be large up to 200 for standard transistors, and it is this large ratio between Ic and Ib that makes the bipolar NPN transistor a useful amplifying device when used in its active region as Ib provides the input and Ic provides the output. Note that Beta has no units as it is a ratio.

Also, the current gain of the transistor from the Collector terminal to the Emitter terminal, I_C/I_E, is called Alpha, (α), and is a function of the transistor itself (electrons diffusing across the junction).

As the emitter current I_E is the sum of a very small base current plus a very large collector current, the value of alpha (α), is very close to unity, and for a typical low-power signal transistor this value ranges from about 0.950 to 0.999

α and β Relationship in a NPN Transistor

$$\text{DC Current Gain} = \frac{\text{Output Current}}{\text{Input Current}} = \frac{I_C}{I_B}$$

$$I_E = I_B + I_C \ldots\ldots \text{(KCL)} \quad \text{and} \quad \frac{I_C}{I_E} = \alpha$$

$$\text{Thus:} \quad I_B = I_E - I_C$$

$$I_B = I_E - \alpha I_E$$

$$I_B = I_E(1-\alpha)$$

$$\therefore \ \beta = \frac{I_C}{I_B} = \frac{I_C}{I_E(1-\alpha)} = \frac{\alpha}{1-\alpha}$$

By combining the two parameters α and β we can produce two mathematical expressions that gives the relationship between the different currents flowing in the transistor.

$$\alpha = \frac{\beta}{\beta+1} \quad \text{or} \quad \alpha = \beta(1-\alpha)$$

$$\beta = \frac{\alpha}{1-\alpha} \quad \text{or} \quad \beta = \alpha(1+\beta)$$

$$\text{If} \quad \alpha = 0.99 \qquad \beta = \frac{0.99}{0.01} = 99$$

The values of Beta vary from about 20 for high current power transistors to well over 1000 for high frequency low power type bipolar transistors. The value of Beta for most standard NPN transistors can be found in the manufactures data sheets but generally range between 50 – 200.

The equation above for Beta can also be re-arranged to make Ic as the subject, and with a zero base current ($I_B = 0$) the resultant collector current Ic will also be zero, (β*0).

Also note that when the base current is high the corresponding collector current will also be high resulting in the base current controlling the collector current. One of the most important properties of the **Bipolar Junction Transistor** is that a small base current can control a much larger collector current. Consider the following example.

NPN Transistor Example No1

A bipolar NPN transistor has a DC current gain, (Beta) value of 200. Calculate the base current Ib required to switch a resistive load of 4mA.

$$I_B = \frac{I_C}{\beta} = \frac{4 \times 10^{-3}}{200} = 20\mu A$$

Therefore, β = 200, I_C = 4mA and I_B = 20μA.

One other point to remember about **Bipolar NPN Transistors**. The collector voltage, (V_C) must be greater and positive with respect to the emitter voltage, (V_E) to allow current to flow through the transistor between the collector-emitter junctions. There is also a voltage drop between the Base and the Emitter terminal of about 0.7V (one diode volt drop) for silicon devices as the input characteristics of an NPN Transistor are of a forward biased diode.

Then the base voltage, (V_{BE}) of a NPN transistor must be greater than this 0.7V otherwise the transistor will not conduct with the base current given as :

$$I_B = \frac{V_B - V_{BE}}{R_B}$$

Where: I_B is the base current, V_B is the base bias voltage, V_{BE} is the base-emitter volt drop (0.7v) and R_B is the base input resistor. Increasing Ib, Vbe slowly increases to 0.7V but I_C rises exponentially.

NPN Transistor Example No2

An NPN Transistor has a DC base bias voltage, V_B of 10v and an input base resistor, R_B of 100kΩ. What will be the value of the base current into the transistor.

$$I_B = \frac{V_B - V_{BE}}{R_B} = \frac{10 - 0.7}{100k\Omega} = 93\mu A$$

Therefore, I_B = 93μA.

The Common Emitter Configuration.

As well as being used as a semiconductor switch to turn load currents “ON” or “OFF” by controlling the Base signal to the transistor in either its saturation or cut-off regions, **Bipolar NPN Transistors** can also be used in its active region to produce a circuit which will amplify any small AC signal applied to its Base terminal with the Emitter grounded.

If a suitable DC “biasing” voltage is firstly applied to the transistors Base terminal thus allowing it to always operate within its linear active region, an inverting amplifier circuit called a single stage common emitter amplifier is produced.

One such *Common Emitter Amplifier* configuration of an NPN transistor is called a Class A Amplifier. A “Class A Amplifier” operation is one where the transistors Base terminal is biased in such a way as to forward bias the Base-emitter junction.

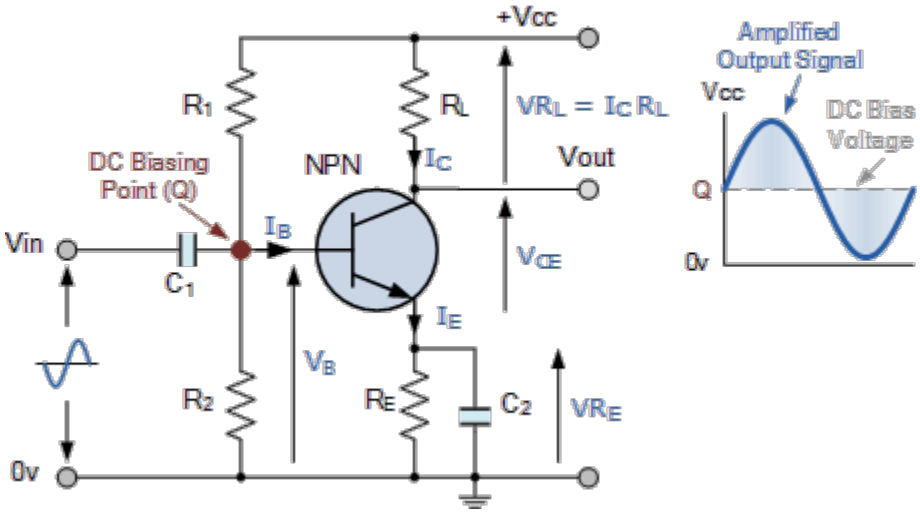
The result is that the transistor is always operating halfway between its cut-off and saturation regions, thereby allowing the transistor amplifier to accurately reproduce the positive and negative halves of any AC input signal superimposed upon this DC biasing voltage.

Without this “Bias Voltage” only one half of the input waveform would be amplified. This common emitter amplifier configuration using an NPN transistor has many applications but is commonly used in audio circuits such as pre-amplifier and power amplifier stages.

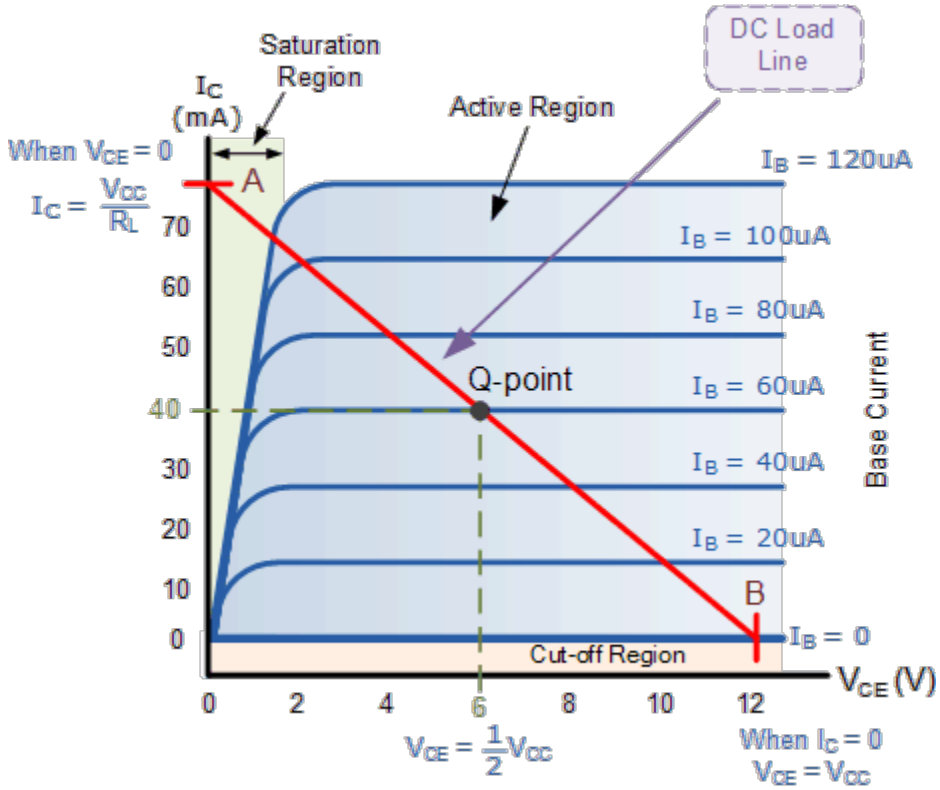
With reference to the common emitter configuration shown below, a family of curves known as the **Output Characteristics Curves**, relates the output collector current, (I_C) to the collector voltage, (V_{CE}) when different values of Base current, (I_B). Output characteristics curves are applied to the transistor for transistors with the same β value.

A DC “Load Line” can also be drawn onto the output characteristics curves to show all the possible operating points when different values of base current are applied. It is necessary to set the initial value of V_{CE} correctly to allow the output voltage to vary both up and down when amplifying AC input signals and this is called setting the operating point or Quiescent Point, **Q-point** for short and this is shown below.

Single Stage Common Emitter Amplifier Circuit



Output Characteristics Curves of a Typical Bipolar Transistor



The most important factor to notice is the effect of Vce upon the collector current I_C when V_{CE} is greater than about 1.0 volts. We can see that I_C is largely unaffected by changes in V_{CE} above this value and instead it is almost entirely controlled by the base current, I_B. When this happens we can say then that the output circuit represents that of a “Constant Current Source”.

It can also be seen from the common emitter circuit above that the emitter current Ie is the sum of the collector current, Ic and the base current, Ib, added together so we can also say that $I_E = I_C + I_B$ for the common emitter (CE) configuration.

By using the output characteristics curves in our example above and also Ohm´s Law, the current flowing through the load resistor, (R_L), is equal to the collector current, Ic entering the transistor which in turn corresponds to the supply voltage, (V_{CC}) minus the voltage drop between the collector and the emitter terminals, (V_{CE}) and is given as:

$$\text{Collector Current, } I_C = \frac{V_{CC} - V_{CE}}{R_L}$$

Also, a straight line representing the **Dynamic Load Line** of the transistor can be drawn directly onto the graph of curves above from the point of “Saturation” (A) when Vce = 0 to the point of “Cut-off” (B) when Ic = 0 thus giving us the “Operating” or **Q-point** of the transistor. These two points are joined together by a straight line and any position along this straight line represents the “Active Region” of the transistor. The actual position of the load line on the characteristics curves can be calculated as follows:

$$\text{When: } (V_{CE} = 0) \quad I_C = \frac{V_{CC} - 0}{R_L}, \quad I_C = \frac{V_{CC}}{R_L}$$

$$\text{When: } (I_C = 0) \quad 0 = \frac{V_{CC} - V_{CE}}{R_L}, \quad V_{CC} = V_{CE}$$

Then, the collector or output characteristics curves for **Common Emitter NPN Transistors** can be used to predict the Collector current, I_C, when given V_{CE} and the Base current, I_B. A Load Line can also be constructed onto the curves to determine a suitable Operating or **Q-point** which can be set by adjustment of the base current. The slope of this load line is equal to the reciprocal of the load resistance which is given as: $-1/R_L$

Then we can define a **NPN Transistor** as being normally “OFF” but a small input current and a small positive voltage at its Base (B) relative to its Emitter (E) will turn it “ON” allowing a much large Collector-Emitter current to flow. NPN transistors conduct when Vc is much greater than V_E.

In the next tutorial about **Bipolar Transistors**, we will look at the opposite or complementary form of the NPN Transistor called the PNP Transistor and show that the PNP Transistor has very similar characteristics to the bipolar NPN transistor except that the polarities (or biasing) of the current and voltage directions are reversed.

https://www.electronics-tutorials.ws/transistor/tran_3.html

PNP Transistor

The PNP Transistor is the exact opposite to the NPN Transistor device we looked at in the previous tutorial.

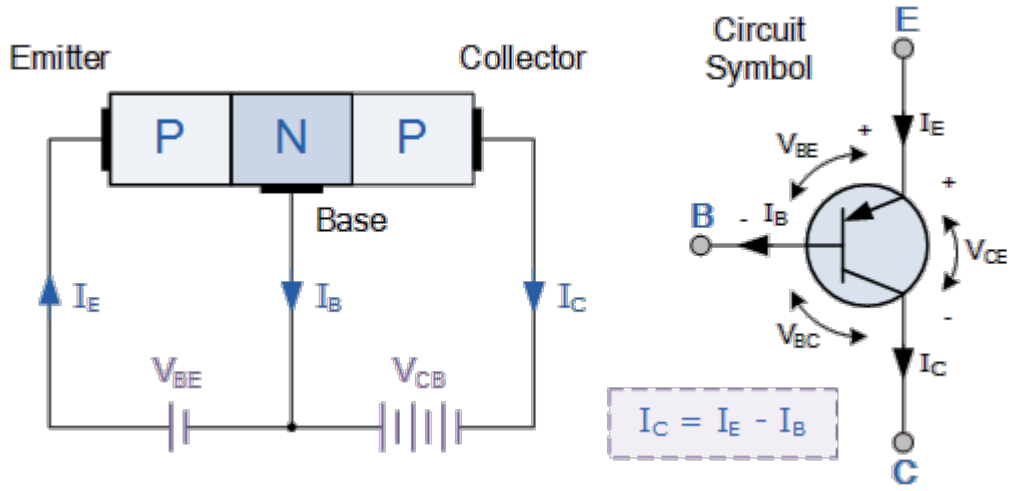
Basically, in this type of PNP transistor construction, the two interconnected diodes are reversed with respect to the previous NPN transistor. This produces a **P**ositive-**N**egative-**P**ositive type of configuration, with the arrow which also defines the Emitter terminal pointing inwards in the PNP transistor symbol.

Also, all the polarities for a PNP *transistor* are reversed which means that it "sinks" current into its Base as opposed to the NPN transistor which "sources" current through its Base. The main difference between the two types of transistors is that holes are the more important carriers for PNP transistors, whereas electrons are the important carriers for NPN transistors.

Then, PNP transistors use a small base current and a negative base voltage to control a much larger emitter-collector current. In other words for a PNP transistor, the Emitter is more positive with respect to the Base and also with respect to the Collector.

The construction of a "PNP transistor" consists of two P-type semiconductor materials either side of an N-type material as shown below.

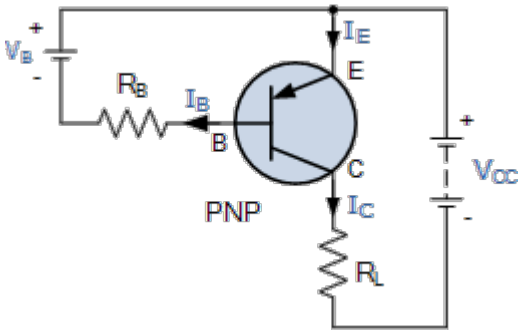
A PNP Transistor Configuration



(Note: Arrow defines the emitter and conventional current flow, "in" for a PNP transistor.)

The construction and terminal voltages for an NPN transistor are shown above. The **PNP Transistor** has very similar characteristics to their NPN bipolar cousins, except that the polarities (or biasing) of

the current and voltage directions are reversed for any one of the possible three configurations looked at in the first tutorial, Common Base, Common Emitter and Common Collector.



PNP Transistor Connection

The voltage between the Base and Emitter (V_{BE}), is now negative at the Base and positive at the Emitter because for a PNP transistor, the Base terminal is always biased negative with respect to the Emitter.

Also the Emitter supply voltage is positive with respect to the Collector (V_{CE}). So for a PNP transistor to conduct the Emitter is always more positive with respect to both the Base and the Collector.

The voltage sources are connected to a PNP transistor are as shown. This time the Emitter is connected to the supply voltage V_{CC} with the load resistor, R_L which limits the maximum current flowing through the device connected to the Collector terminal. The Base voltage V_B which is biased negative with respect to the Emitter and is connected to the Base resistor R_B, which again is used to limit the maximum Base current.

To cause the Base current to flow in a PNP transistor the Base needs to be more negative than the Emitter (current must leave the base) by approx 0.7 volts for a silicon device or 0.3 volts for a germanium device with the formulas used to calculate the Base resistor, Base current or Collector current are the same as those used for an equivalent NPN transistor and is given as :

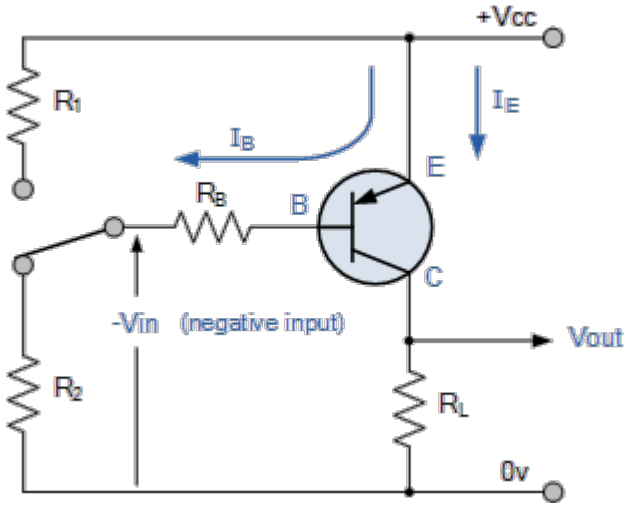
$$I_C = I_E - I_B$$

$$I_C = \beta . I_B \qquad I_B = \frac{I_C}{\beta}$$

We can see that the fundamental differences between a NPN Transistor and a PNP Transistor is the proper biasing of the transistors junctions as the current directions and voltage polarities are always opposite to each other. So for the circuit above: $I_C = I_E - I_B$ as current must leave the Base.

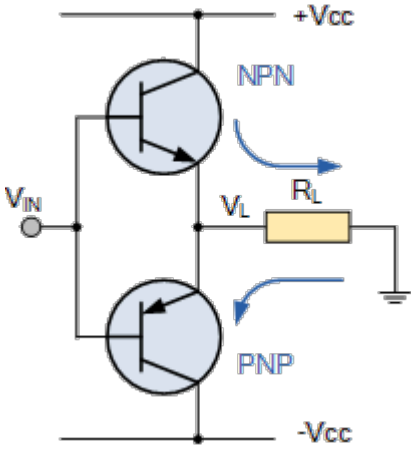
Generally, the PNP transistor can replace NPN transistors in most electronic circuits, the only difference is the polarities of the voltages, and the directions of the current flow. PNP transistors can also be used as switching devices and an example of a PNP transistor switch is shown below.

A PNP Transistor Circuit



The **Output Characteristics Curves** for a PNP transistor look very similar to those for an equivalent NPN transistor except that they are rotated by 180º to take account of the reverse polarity voltages and currents, (that is for a PNP transistor, electron current flows out of the base and collector towards the battery). The same dynamic load line can be drawn onto the I-V curves to find the PNP transistors operating points.

Transistor Matching



Complementary Transistors

You may think what is the point of having a PNP Transistor, when there are plenty of NPN Transistors available that can be used as an amplifier or solid-state switch?. Well, having two different types of transistors “PNP” and “NPN”, can be a great advantage when designing power amplifier circuits such as the Class B Amplifier.

Class-B amplifiers uses “Complementary” or “Matched Pair” (that is one PNP and one NPN connected together) transistors in its output stage or in reversible H-Bridge motor control circuits where we want to control the flow of current evenly through the motor in both directions at different times for forward and reverse motion.

A pair of corresponding NPN and PNP transistors with near identical characteristics to each other are called **Complementary Transistors** for example, a TIP3055 (NPN transistor) and the TIP2955 (PNP transistor) are good examples of complementary or matched pair silicon power transistors. They both have a DC current gain, Beta, (I_C/I_B) matched to within 10% and high Collector current of about 15A making them ideal for general motor control or robotic applications.

Also, class B amplifiers use complementary NPN and PNP in their power output stage design. The NPN transistor conducts for only the positive half of the signal while the PNP transistor conducts for negative half of the signal.

This allows the amplifier to drive the required power through the load loudspeaker in both directions at the stated nominal impedance and power resulting in an output current which is likely to be in the order of several amps shared evenly between the two complementary transistors.

Identifying the PNP Transistor

We saw in the first tutorial of this transistors section, that transistors are basically made up of two Diodes connected together back-to-back.

We can use this analogy to determine whether a transistor is of the PNP type or NPN type by testing its Resistance between the three different leads, Emitter, Base and Collector. By testing each pair of transistor leads in both directions with a multimeter will result in six tests in total with the expected resistance values in Ohm's given below.

1. Emitter-Base Terminals – The Emitter to Base should act like a normal diode and conduct one way only.
2. Collector-Base Terminals – The Collector-Base junction should act like a normal diode and conduct one way only.
3. Emitter-Collector Terminals – The Emitter-Collector should not conduct in either direction.

Terminal Resistance Values for PNP and NPN Transistors

Between Transistor Terminals		PNP	NPN
Collector	Emitter	R_{HIGH}	R_{HIGH}
Collector	Base	R_{LOW}	R_{HIGH}
Emitter	Collector	R_{HIGH}	R_{HIGH}
Emitter	Base	R_{LOW}	R_{HIGH}
Base	Collector	R_{HIGH}	R_{LOW}
Base	Emitter	R_{HIGH}	R_{LOW}

Then we can define a **PNP Transistor** as being normally “OFF” but a small output current and negative voltage at its Base (B) relative to its Emitter (E) will turn it “ON” allowing a much large Emitter-Collector current to flow. PNP transistors conduct when V_E is much greater than V_C.

In other words, a **Bipolar PNP Transistor** will ONLY conduct if both the Base and Collector terminals are negative with respect to the Emitter

In the next tutorial about Bipolar Transistors instead of using the transistor as an amplifying device, we will look at the operation of the transistor in its saturation and cut-off regions when used as a solid-state switch.

Bipolar transistor switches are used in many applications to switch a DC current “ON” or “OFF”, from LED’s which require only a few milliamps of switching current at low DC voltages, or motors and relays which may require higher currents at higher voltages.

https://www.electronics-tutorials.ws/transistor/tran_4.html

Transistor as a Switch

Transistor switches can be used to switch a low voltage DC device (e.g. LED's) ON or OFF by using a transistor in its saturated or cut-off state.

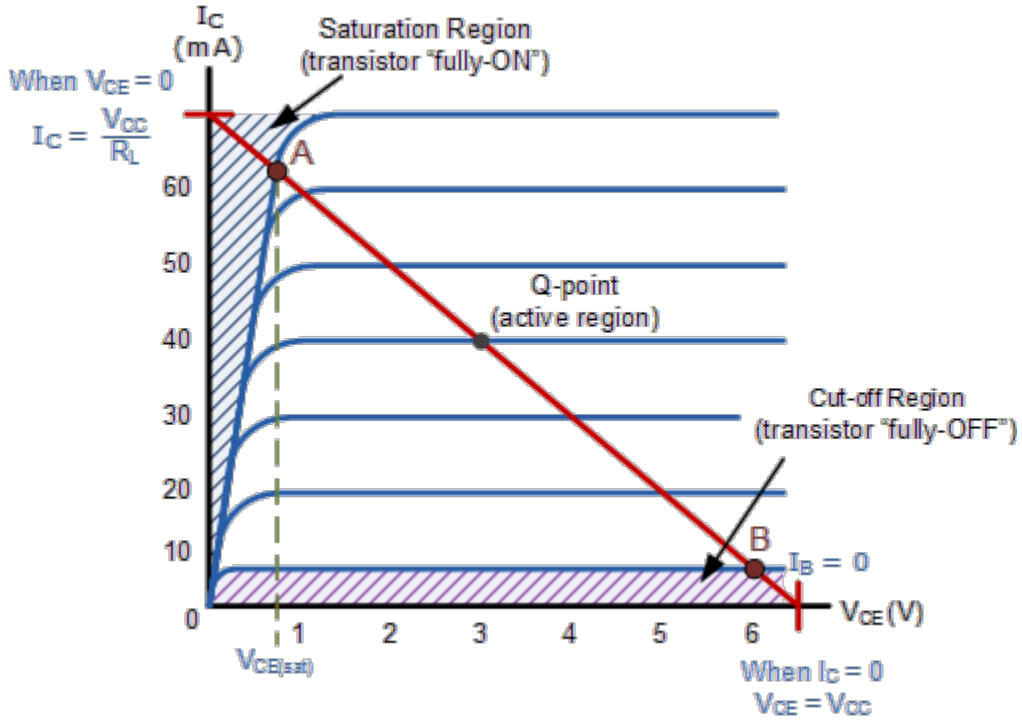
When used as an AC signal amplifier, the transistors Base biasing voltage is applied in such a way that it always operates within its "active" region, that is the linear part of the output characteristics curves are used. However, both the NPN & PNP type bipolar transistors can be made to operate as "ON/OFF" type solid state switch by biasing the transistors Base terminal differently operating the transistor as a switch.

Solid state switches are one of the main applications for the use of transistor to switch a DC output "ON" or "OFF". Some output devices, such as LED's only require a few milliamps at logic level DC voltages and can therefore be driven directly by the output of a logic gate. However, high power devices such as motors, solenoids or lamps, often require more power than that supplied by an ordinary logic gate so transistor switches are used.

If the circuit uses the Bipolar Transistor as a Switch, then the biasing of the transistor, either NPN or PNP is arranged to operate the transistor at both sides of the " I-V " characteristics curves we have seen previously.

The areas of operation for a transistor switch are known as the Saturation Region and the Cut-off Region. This means then that we can ignore the operating Q-point biasing and voltage divider circuitry required for amplification, and use the transistor as a switch by driving it back and forth between its “fully-OFF” (cut-off) and “fully-ON” (saturation) regions as shown below.

Operating Regions

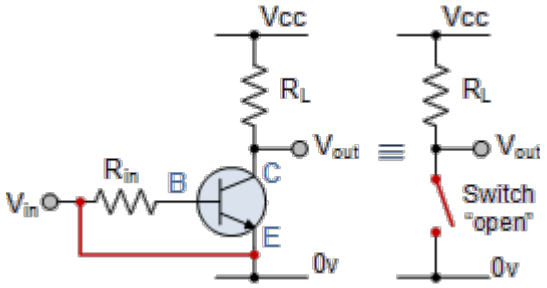


The pink shaded area at the bottom of the curves represents the “Cut-off” region while the blue area to the left represents the “Saturation” region of the transistor. Both these transistor regions are defined as:

1. Cut-off Region

Here the operating conditions of the transistor are zero input base current (I_B), zero output collector current (I_C) and maximum collector voltage (V_{CE}) which results in a large depletion layer and no current flowing through the device. Therefore the transistor is switched “Fully-OFF”.

Cut-off Characteristics

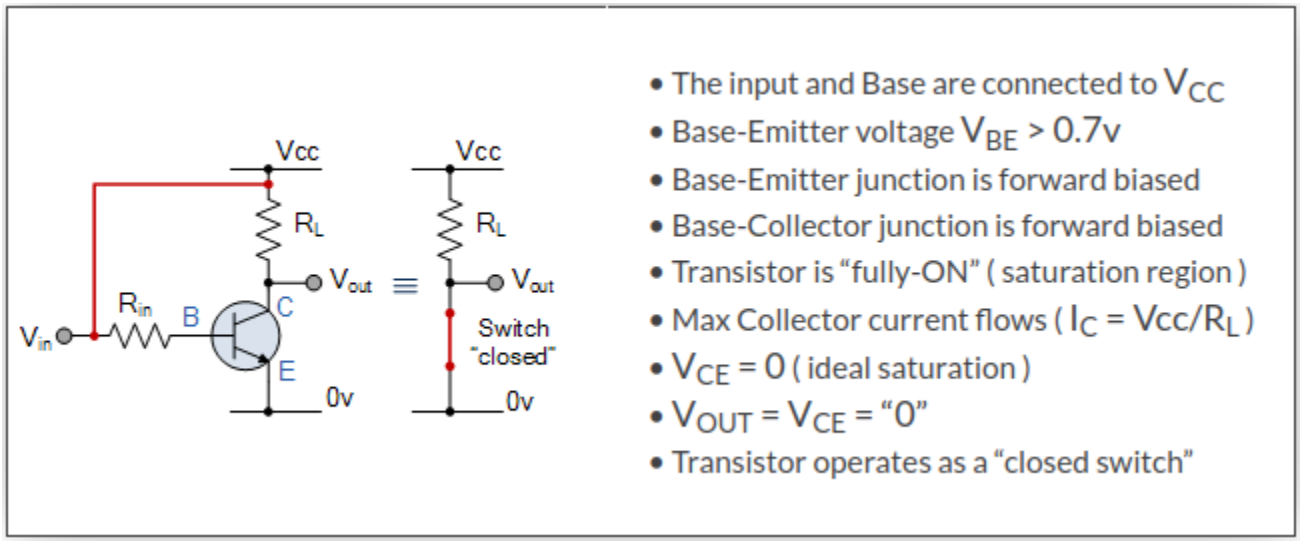


Then we can define the “cut-off region” or “OFF mode” when using a bipolar transistor as a switch as being, both junctions reverse biased, $V_B < 0.7v$ and $I_C = 0$. For a PNP transistor, the Emitter potential must be negative with respect to the Base.

2. Saturation Region

Here the transistor will be biased so that the maximum amount of base current is applied, resulting in maximum collector current resulting in the minimum collector emitter voltage drop which results in the depletion layer being as small as possible and maximum current flowing through the transistor. Therefore the transistor is switched “Fully-ON”.

Saturation Characteristics



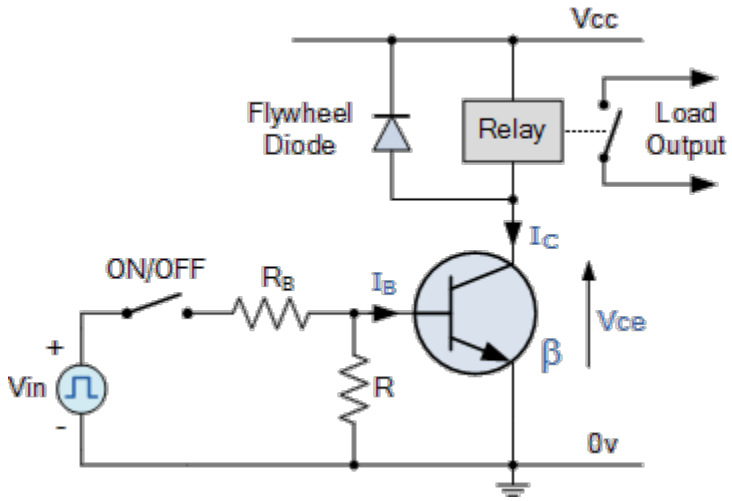
Then we can define the “saturation region” or “ON mode” when using a bipolar transistor as a switch as being, both junctions forward biased, $V_B > 0.7v$ and I_C = Maximum. For a PNP transistor, the Emitter potential must be positive with respect to the Base.

Then the transistor operates as a “single-pole single-throw” (SPST) solid state switch. With a zero signal applied to the Base of the transistor it turns “OFF” acting like an open switch and zero collector current flows. With a positive signal applied to the Base of the transistor it turns “ON” acting like a closed switch and maximum circuit current flows through the device.

The simplest way to switch moderate to high amounts of power is to use the transistor with an open-collector output and the transistors Emitter terminal connected directly to ground. When used in this way, the transistors open collector output can thus “sink” an externally supplied voltage to ground thereby controlling any connected load.

An example of an NPN Transistor as a switch being used to operate a relay is given below. With inductive loads such as relays or solenoids a flywheel diode is placed across the load to dissipate the back EMF generated by the inductive load when the transistor switches “OFF” and so protect the transistor from damage. If the load is of a very high current or voltage nature, such as motors, heaters etc, then the load current can be controlled via a suitable relay as shown.

Basic NPN Transistor Switching Circuit



The circuit resembles that of the *Common Emitter* circuit we looked at in the previous tutorials. The difference this time is that to operate the transistor as a switch the transistor needs to be turned either fully “OFF” (cut-off) or fully “ON” (saturated).

An ideal transistor switch would have infinite circuit resistance between the Collector and Emitter when turned “fully-OFF” resulting in zero current flowing through it and zero resistance between the Collector and Emitter when turned “fully-ON”, resulting in maximum current flow.

In practice when the transistor is turned “OFF”, small leakage currents flow through the transistor and when fully “ON” the device has a low resistance value causing a small saturation voltage (V_{CE}) across it. Even though the transistor is not a perfect switch, in both the cut-off and saturation regions the power dissipated by the transistor is at its minimum.

In order for the Base current to flow, the Base input terminal must be made more positive than the Emitter by increasing it above the 0.7 volts needed for a silicon device. By varying this Base-Emitter voltage V_{BE}, the Base current is also altered and which in turn controls the amount of Collector current flowing through the transistor as previously discussed.

When maximum Collector current flows the transistor is said to be **Saturated**. The value of the Base resistor determines how much input voltage is required and corresponding Base current to switch the transistor fully "ON".

Transistor as a Switch Example No1

Using the transistor values from the previous tutorials of: β = 200, I_C = 4mA and I_B = 20uA, find the value of the Base resistor (R_B) required to switch the load fully "ON" when the input terminal voltage exceeds 2.5v.

$$R_B = \frac{V_{in} - V_{BE}}{I_B} = \frac{2.5v - 0.7v}{20x10^{-6}} = 90k\Omega$$

The next lowest preferred value is: 82kΩ, this guarantees the transistor switch is always saturated.

Transistor as a Switch Example No2

Again using the same values, find the minimum Base current required to turn the transistor "fully-ON" (saturated) for a load that requires 200mA of current when the input voltage is increased to 5.0V. Also calculate the new value of R_B.

Transistor Base current:

$$I_B = \frac{I_C}{\beta} = \frac{200mA}{200} = 1mA$$

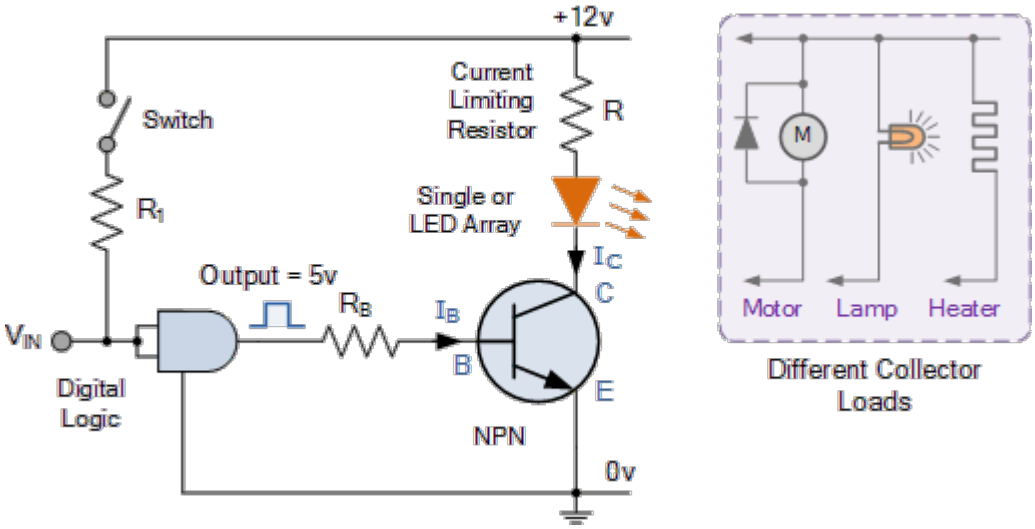
Transistor Base resistance:

$$R_B = \frac{V_{in} - V_{BE}}{I_B} = \frac{5.0v - 0.7v}{1\times10^{-3}} = 4.3k\Omega$$

Transistor switches are used for a wide variety of applications such as interfacing large current or high voltage devices like motors, relays or lamps to low voltage digital IC's or logic gates like AND gates or OR gates.

Here, the output from a digital logic gate is only +5v but the device to be controlled may require a 12 or even 24 volts supply. Or the load such as a DC Motor may need to have its speed controlled using a series of pulses (Pulse Width Modulation). transistor switches will allow us to do this faster and more easily than with conventional mechanical switches.

Digital Logic Transistor Switch

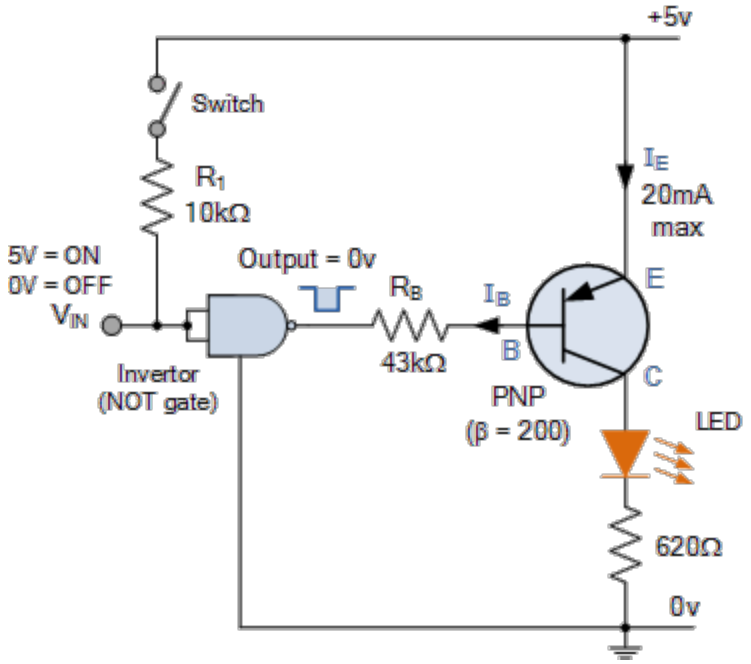


The base resistor, R_B is required to limit the output current from the logic gate.

PNP Transistor Switch

We can also use the PNP Transistors as a switch, the difference this time is that the load is connected to ground (0v) and the PNP transistor switches the power to it. To turn the PNP transistor operating as a switch “ON”, the Base terminal is connected to ground or zero volts (LOW) as shown.

PNP Transistor Switching Circuit



The equations for calculating the Base resistance, Collector current and voltages are exactly the same as for the previous NPN transistor switch. The difference this time is that we are switching power with

a PNP transistor (sourcing current) instead of switching ground with an NPN transistor (sinking current).

Darlington Transistor Switch

Sometimes the DC current gain of the bipolar transistor is too low to directly switch the load current or voltage, so multiple switching transistors are used. Here, one small input transistor is used to switch “ON” or “OFF” a much larger current handling output transistor.

To maximise the signal gain, the two transistors are connected in a “Complementary Gain Compounding Configuration” or what is more commonly called a “**Darlington Configuration**” were the amplification factor is the product of the two individual transistors.

Darlington Transistors simply contain two individual bipolar NPN or PNP type transistors connected together so that the current gain of the first transistor is multiplied with that of the current gain of the second transistor to produce a device which acts like a single transistor with a very high current gain for a much smaller Base current.

The overall current gain Beta (β) or hfe value of a Darlington device is the product of the two individual gains of the transistors and is given as:

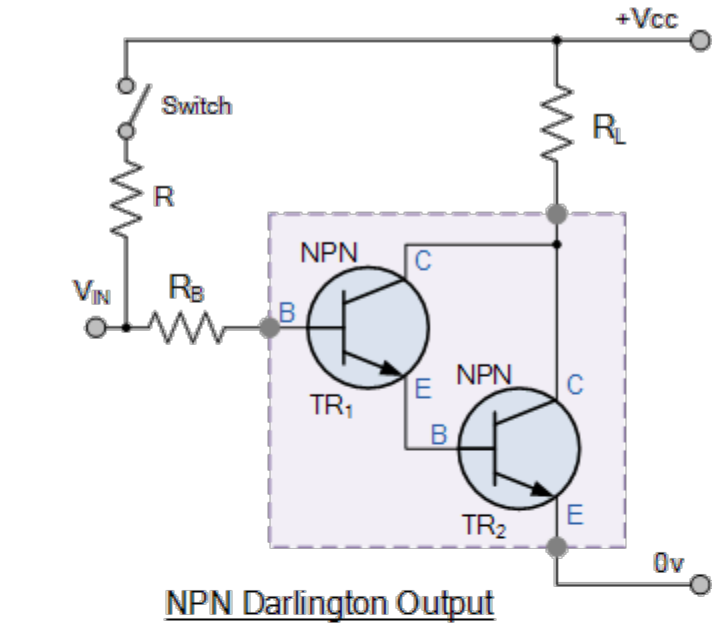
$$\beta_{TOTAL} = \beta_1 \times \beta_2$$

So Darlington Transistors with very high β values and high Collector currents are possible compared to a single transistor switch. For example, if the first input transistor has a current gain of 100 and the second switching transistor has a current gain of 50 then the total current gain will be 100 * 50 = 5000.

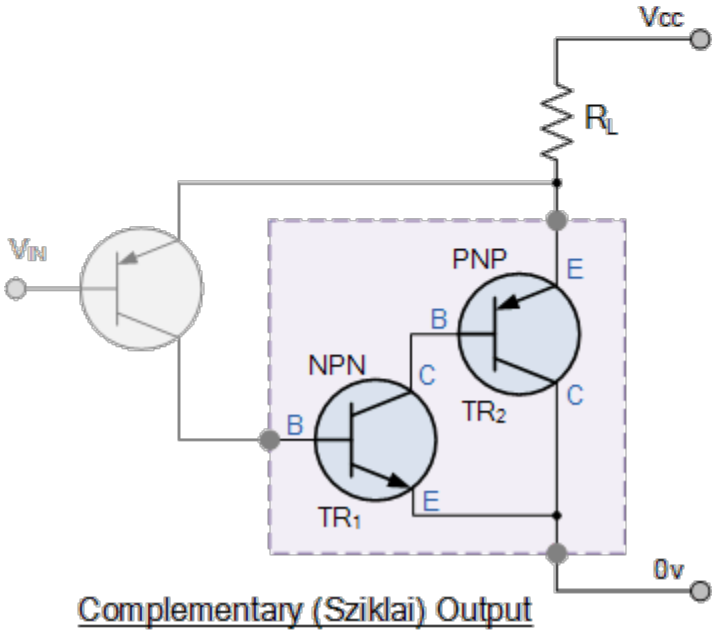
So for example, if our load current from above is 200mA, then the darlington base current is only 200mA/5000 = 40uA. A huge reduction from the previous 1mA for a single transistor.

An example of the two basic types of Darlington transistor configurations are given below.

Darlington Transistor Configurations



NPN Darlington Output



Complementary (Sziklai) Output

The above NPN Darlington transistor switch configuration shows the Collectors of the two transistors connected together with the Emitter of the first transistor connected to the Base terminal of the second transistor therefore, the Emitter current of the first transistor becomes the Base current of the second transistor switching it “ON”.

The first or “input” transistor receives the input signal to its Base. This transistor amplifies it in the usual way and uses it to drive the second larger “output” transistors. The second transistor amplifies the

signal again resulting in a very high current gain. One of the main characteristics of **Darlington Transistors** is their high current gains compared to single bipolar transistors.

As well as its high increased current and voltage switching capabilities, another advantage of a “Darlington Transistor Switch” is in its high switching speeds making them ideal for use in inverter circuits, lighting circuits and DC motor or stepper motor control applications.

One difference to consider when using Darlington transistors over the conventional single bipolar types when using the transistor as a switch is that the Base-Emitter input voltage (V_{BE}) needs to be higher at approx 1.4v for silicon devices, due to the series connection of the two PN junctions.

Transistor as a Switch Summary

Then to summarise when using a Transistor as a Switch the following conditions apply:

- ✔ Transistor switches can be used to switch and control lamps, relays or even motors.
- ✔ When using the bipolar transistor as a switch they must be either “fully-OFF” or “fully-ON”.
- ✔ Transistors that are fully “ON” are said to be in their Saturation region.
- ✔ Transistors that are fully “OFF” are said to be in their Cut-off region.
- ✔ When using the transistor as a switch, a small Base current controls a much larger Collector load current.
- ✔ When using transistors to switch inductive loads such as relays and solenoids, a “Flywheel Diode” is used.
- ✔ When large currents or voltages need to be controlled, Darlington Transistors can be used.

In the next tutorial about Transistors, we will look at the operation of the junction field effect transistor known commonly as an JFET. We will also plot the output characteristics curves commonly associated with JFET amplifier circuits as a function of Source voltage to Gate voltage.

https://www.electronics-tutorials.ws/transistor/tran_5.html

Junction Field Effect Transistor

The Junction Field Effect Transistor, or JFET, is a voltage controlled three terminal unipolar semiconductor device available in N-channel and P-channel configurations.

The Junction Field Effect Transistor is a unipolar device in which current flow between its two electrodes is controlled by the action of an electric field at a reverse biased pn-junction.

In the *Bipolar Junction Transistor* tutorials, we saw that the output Collector current of the transistor is proportional to input current flowing into the Base terminal of the device. This makes the bipolar transistor a “CURRENT” operated device (Beta model) as a smaller current can be used to switch a larger load current.

The **Field Effect Transistor**, or simply **FET** however, uses the voltage that is applied to their input terminal, called the Gate to control the current flowing through them resulting in the output current being proportional to the input voltage. As their operation relies on an electric field (hence the name field effect) generated by the input Gate voltage, this then makes the **Field Effect Transistor** a “VOLTAGE” operated device.

The **Field Effect Transistor** is a three terminal unipolar semiconductor device that has very similar characteristics to those of their *Bipolar Transistor* counterparts. For example, high efficiency, instant operation, robust and cheap and can be used in most electronic circuit applications to replace their equivalent bipolar junction transistors (BJT) cousins.

Typical Field Effect Transistor

Field effect transistors can be made much smaller than an equivalent BJT transistor and along with their low power consumption and power dissipation makes them ideal for use in integrated circuits such as the CMOS range of digital logic chips.

We remember from the previous tutorials that there are two basic types of bipolar transistor construction, NPN and PNP, which basically describes the physical arrangement of the P-type and N-type semiconductor materials from which they are made. This is also true of FET’s as there are also two basic classifications of Field Effect Transistor, called the N-channel FET and the P-channel FET.

The field effect transistor is a three terminal device that is constructed with no PN-junctions within the main current carrying path between the Drain and the Source terminals. These terminals correspond in function to the Collector and the Emitter respectively of the bipolar transistor. The current path between these two terminals is called the “channel” which may be made of either a P-type or an N-type semiconductor material.

The control of current flowing in this channel is achieved by varying the voltage applied to the Gate. As their name implies, Bipolar Transistors are “Bipolar” devices because they operate with both types of charge carriers, Holes and Electrons. The Field Effect Transistor on the other hand is a “Unipolar” device that depends only on the conduction of electrons (N-channel) or holes (P-channel).

The **Field Effect Transistor** has one major advantage over its standard bipolar transistor cousins, in that their input impedance, (Rin) is very high, (thousands of Ohms), while the BJT is comparatively low. This very high input impedance makes them very sensitive to input voltage signals, but the price of this high sensitivity also means that they can be easily damaged by static electricity.

There are two main types of field effect transistor, the **Junction Field Effect Transistor** or **JFET** and the **Insulated-gate Field Effect Transistor** or **IGFET**), which is more commonly known as the standard **Metal Oxide Semiconductor Field Effect Transistor** or MOSFET for short.

The Junction Field Effect Transistor

We saw previously that a bipolar junction transistor is constructed using two PN-junctions in the main current carrying path between the Emitter and the Collector terminals. The **Junction Field Effect Transistor** (JUGFET or JFET) has no PN-junctions but instead has a narrow piece of high resistivity semiconductor material forming a “Channel” of either N-type or P-type silicon for the majority carriers to flow through with two ohmic electrical connections at either end commonly called the Drain and the Source respectively.

There are two basic configurations of junction field effect transistor, the N-channel JFET and the P-channel JFET. The N-channel JFET’s channel is doped with donor impurities meaning that the flow of current through the channel is negative (hence the term N-channel) in the form of electrons.

Likewise, the P-channel JFET’s channel is doped with acceptor impurities meaning that the flow of current through the channel is positive (hence the term P-channel) in the form of holes. N-channel JFET’s have a greater channel conductivity (lower resistance) than their equivalent P-channel types, since electrons have a higher mobility through a conductor compared to holes. This makes the N-channel JFET’s a more efficient conductor compared to their P-channel counterparts.

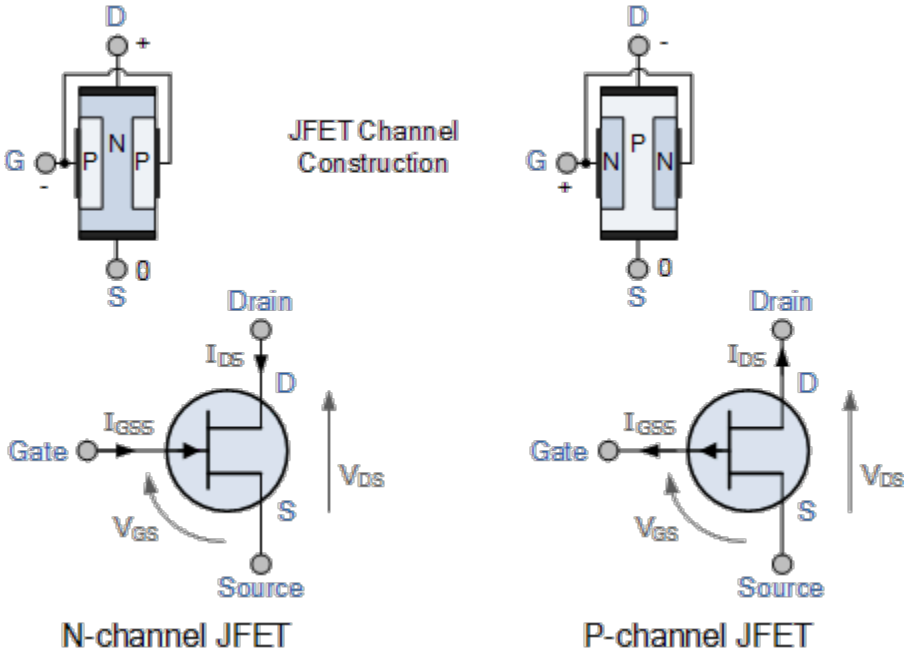
We have said previously that there are two ohmic electrical connections at either end of the channel called the Drain and the Source. But within this channel there is a third electrical connection which is called the Gate terminal and this can also be a P-type or N-type material forming a PN-junction with the main channel.

The relationship between the connections of a junction field effect transistor and a bipolar junction transistor are compared below.

Comparison of Connections between a JFET and a BJT

Bipolar Transistor (BJT)	Field Effect Transistor (FET)
Emitter – (E) >> Source – (S)	
Base – (B) >> Gate – (G)	
Collector – (C) >> Drain – (D)	

The symbols and basic construction for both configurations of JFETs are shown below.



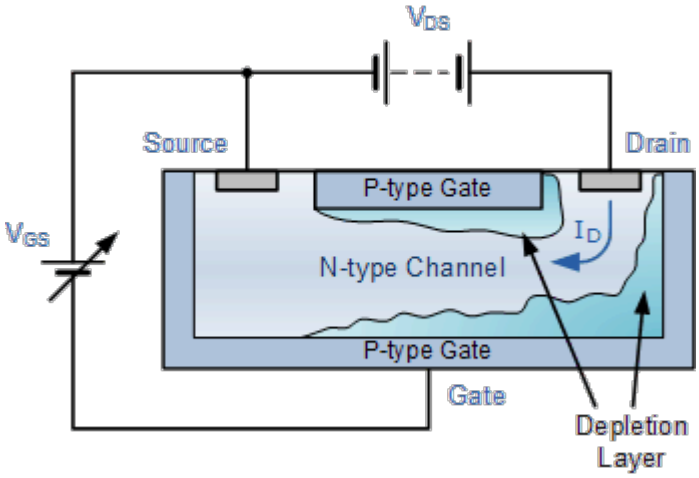
The semiconductor “channel” of the **Junction Field Effect Transistor** is a resistive path through which a voltage V_{DS} causes a current I_D to flow and as such the junction field effect transistor can conduct current equally well in either direction. As the channel is resistive in nature, a voltage gradient is thus formed down the length of the channel with this voltage becoming less positive as we go from the Drain terminal to the Source terminal.

The result is that the PN-junction therefore has a high reverse bias at the Drain terminal and a lower reverse bias at the Source terminal. This bias causes a “depletion layer” to be formed within the channel and whose width increases with the bias.

The magnitude of the current flowing through the channel between the Drain and the Source terminals is controlled by a voltage applied to the Gate terminal, which is a reverse-biased. In an N-channel JFET this Gate voltage is negative while for a P-channel JFET the Gate voltage is positive.

The main difference between the JFET and a BJT device is that when the JFET junction is reverse-biased the Gate current is practically zero, whereas the Base current of the BJT is always some value greater than zero.

Biasing of an N-channel Junction Field Effect Transistor



The cross sectional diagram above shows an N-type semiconductor channel with a P-type region called the Gate diffused into the N-type channel forming a reverse biased PN-junction and it is this junction which forms the *depletion region* around the Gate area when no external voltages are applied. JFETs are therefore known as depletion mode devices.

This depletion region produces a potential gradient which is of varying thickness around the PN-junction and restrict the current flow through the channel by reducing its effective width and thus increasing the overall resistance of the channel itself.

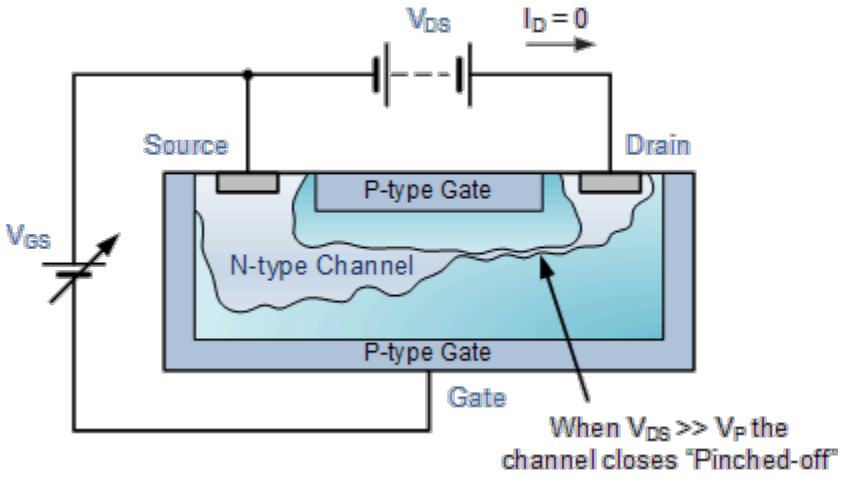
Then we can see that the most-depleted portion of the depletion region is in between the Gate and the Drain, while the least-depleted area is between the Gate and the Source. Then the JFET's channel conducts with zero bias voltage applied (ie, the depletion region has near zero width).

With no external Gate voltage ($V_G = 0$), and a small voltage (V_{DS}) applied between the Drain and the Source, maximum saturation current (I_{DSS}) will flow through the channel from the Drain to the Source restricted only by the small depletion region around the junctions.

If a small negative voltage ($-V_{GS}$) is now applied to the Gate the size of the depletion region begins to increase reducing the overall effective area of the channel and thus reducing the current flowing through it, a sort of "squeezing" effect takes place. So by applying a reverse bias voltage increases the width of the depletion region which in turn reduces the conduction of the channel.

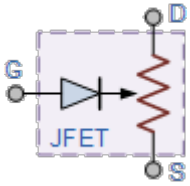
Since the PN-junction is reverse biased, little current will flow into the gate connection. As the Gate voltage ($-V_{GS}$) is made more negative, the width of the channel decreases until no more current flows between the Drain and the Source and the FET is said to be “pinched-off” (similar to the cut-off region for a BJT). The voltage at which the channel closes is called the “pinch-off voltage”, (V_P).

Junction Field effect Transistor Channel Pinched-off



In this pinch-off region the Gate voltage, VGS controls the channel current and VDS has little or no effect.

The result is that the FET acts more like a voltage controlled resistor which has zero resistance when $V_{GS} = 0$ and maximum “ON” resistance (R_{DS}) when the Gate voltage is very negative. Under normal operating conditions, the JFET gate is always negatively biased relative to the source.



JFET Model

It is essential that the Gate voltage is never positive since if it is all the channel current will flow to the Gate and not to the Source, the result is damage to the JFET. Then to close the channel:

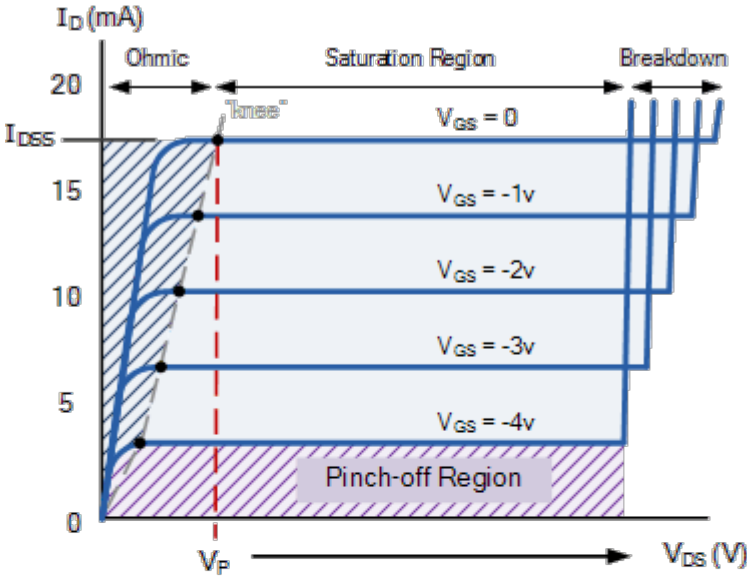
- No Gate Voltage (V_{GS}) and V_{DS} is increased from zero.
- No V_{DS} and Gate control is decreased negatively from zero.
- V_{DS} and V_{GS} varying.

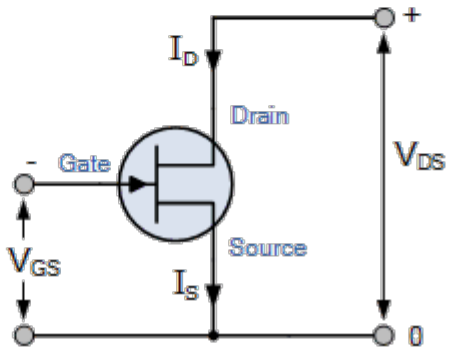
The P-channel **Junction Field Effect Transistor** operates exactly the same as the N-channel above, with the following exceptions:

1. Channel current is positive due to holes
2. The polarity of the biasing voltage needs to be reversed.

The output characteristics of an N-channel JFET with the gate short-circuited to the source is given as:

Output characteristic V-I curves of a typical junction FET





The voltage V_{GS} applied to the Gate controls the current flowing between the Drain and the Source terminals. V_{GS} refers to the voltage applied between the Gate and the Source while V_{DS} refers to the voltage applied between the Drain and the Source.

Because a **Junction Field Effect Transistor** is a voltage controlled device, "**NO current flows into the gate!**" then the Source current (I_S) flowing out of the device equals the Drain current flowing into it and therefore ($I_D = I_S$).

The characteristics curves example shown above, shows the four different regions of operation for a JFET and these are given as:

- ✔ Ohmic Region – When V_{GS} = 0 the depletion layer of the channel is very small and the JFET acts like a voltage controlled resistor.
- ✔ Cut-off Region – This is also known as the pinch-off region were the Gate voltage, V_{GS} is sufficient to cause the JFET to act as an open circuit as the channel resistance is at maximum.
- ✔ Saturation or Active Region – The JFET becomes a good conductor and is controlled by the Gate-Source voltage, (V_{GS}) while the Drain-Source voltage, (V_{DS}) has little or no effect.
- ✔ Breakdown Region – The voltage between the Drain and the Source, (V_{DS}) is high enough to causes the JFET's resistive channel to break down and pass uncontrolled maximum current.

The characteristics curves for a P-channel junction field effect transistor are the same as those above, except that the Drain current I_D decreases with an increasing positive Gate-Source voltage, V_{GS}.

The Drain current is zero when $V_{GS} = V_P$. For normal operation, V_{GS} is biased to be somewhere between V_P and 0. Then we can calculate the Drain current, I_D for any given bias point in the saturation or active region as follows:

Drain current in the active region

$$I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]^2$$

Note that the value of the Drain current will be between zero (pinch-off) and I_{DSS} (maximum current). By knowing the Drain current I_D and the Drain-Source voltage V_{DS} the resistance of the channel (R_{DS}) is given as:

Drain-Source Channel Resistance

$$R_{DS} = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1}{g_m}$$

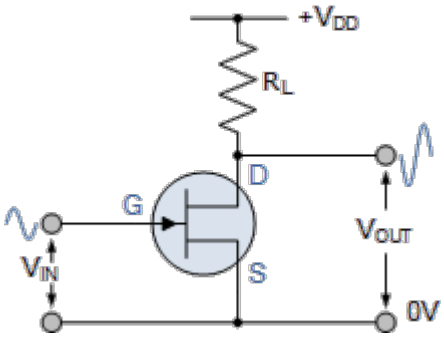
Where: g_m is the "transconductance gain" since the JFET is a voltage controlled device and which represents the rate of change of the Drain current with respect to the change in Gate-Source voltage.

Modes of FET's

Like the bipolar junction transistor, the field effect transistor being a three terminal device is capable of three distinct modes of operation and can therefore be connected within a circuit in one of the following configurations.

Common Source (CS) Configuration

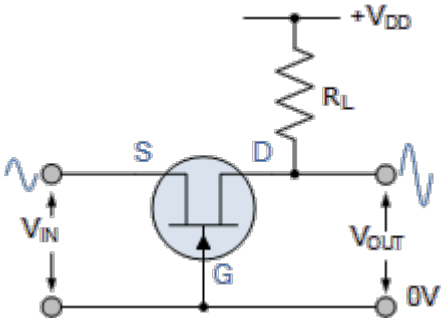
In the Common Source configuration (similar to common emitter), the input is applied to the Gate and its output is taken from the Drain as shown. This is the most common mode of operation of the FET due to its high input impedance and good voltage amplification and as such Common Source amplifiers are widely used.



The common source mode of FET connection is generally used audio frequency amplifiers and in high input impedance pre-amps and stages. Being an amplifying circuit, the output signal is 180o "out-of-phase" with the input.

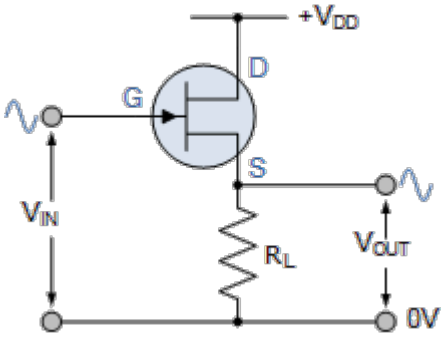
Common Gate (CG) Configuration

In the Common Gate configuration (similar to common base), the input is applied to the Source and its output is taken from the Drain with the Gate connected directly to ground (0v) as shown. The high input impedance feature of the previous connection is lost in this configuration as the common gate has a low input impedance, but a high output impedance.



This type of FET configuration can be used in high frequency circuits or in impedance matching circuits were a low input impedance needs to be matched to a high output impedance. The output is "in-phase" with the input.

Common Drain (CD) Configuration



In the **Common Drain** configuration (similar to common collector), the input is applied to the Gate and its output is taken from the Source. The common drain or "source follower" configuration has a high input impedance and a low output impedance and near-unity voltage gain so is therefore used in buffer amplifiers. The voltage gain of the source follower configuration is less than unity, and the output signal is "in-phase", 0º with the input signal.

This type of configuration is referred to as "Common Drain" because there is no signal available at the drain connection, the voltage present, $+V_{DD}$ just provides a bias. The output is in-phase with the input.

The Junction Field Effect Transistor Amplifier

Just like the bipolar junction transistor, JFET's can be used to make single stage class A amplifier circuits with the JFET common source amplifier and characteristics being very similar to the BJT common emitter circuit. The main advantage JFET amplifiers have over BJT amplifiers is their high input impedance which is controlled by the Gate biasing resistive network formed by R1 and R2 as shown.

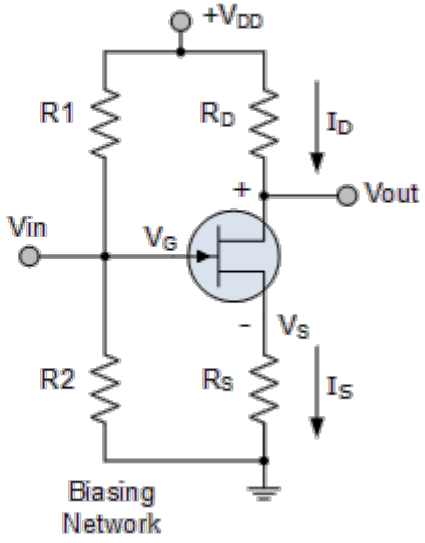
Biasing of the Junction Field Effect Transistor Amplifier

$$V_S = I_D R_S = \frac{V_{DD}}{4}$$

$$V_S = V_G - V_{GS}$$

$$V_G = \left(\frac{R2}{R1 + R2} \right) V_{DD}$$

$$I_D = \frac{V_S}{R_S} = \frac{V_G - V_{GS}}{R_S}$$



This common source (CS) amplifier circuit is biased in class "A" mode by the voltage divider network formed by resistors R1 and R2. The voltage across the Source resistor R_S is generally set to be about one quarter of V_{DD}, (V_{DD} /4) but can be any reasonable value.

The required Gate voltage can then be calculated from this R_S value. Since the Gate current is zero, (I_G = 0) we can set the required DC quiescent voltage by the proper selection of resistors R1 and R2.

The control of the Drain current by a negative Gate potential makes the **Junction Field Effect Transistor** useful as a switch and it is essential that the Gate voltage is never positive for an N-channel JFET as the channel current will flow to the Gate and not the Drain resulting in damage to the JFET. The principals of operation for a P-channel JFET are the same as for the N-channel JFET, except that the polarity of the voltages need to be reversed.

In the next tutorial about **Transistors**, we will look at another type of Field Effect Transistor called a *MOSFET* whose Gate connection is completely isolated from the main current carrying channel.

https://www.electronics-tutorials.ws/transistor/tran_6.html

The MOSFET

MOSFET's operate the same as JFET's but have a gate terminal that is electrically isolated from the conductive channel.

As well as the Junction Field Effect Transistor (JFET), there is another type of Field Effect Transistor available whose Gate input is electrically insulated from the main current carrying channel. The MOSFET is a type of semiconductor device called an **Insulated Gate Field Effect Transistor**.

The most common type of insulated gate FET which is used in many different types of electronic circuits is called the **Metal Oxide Semiconductor Field Effect Transistor** or **MOSFET** for short.

The **IGFET** or **MOSFET** is a voltage controlled field effect transistor that differs from a JFET in that it has a "Metal Oxide" Gate electrode which is electrically insulated from the main semiconductor n-channel or p-channel by a very thin layer of insulating material usually silicon dioxide, commonly known as glass.

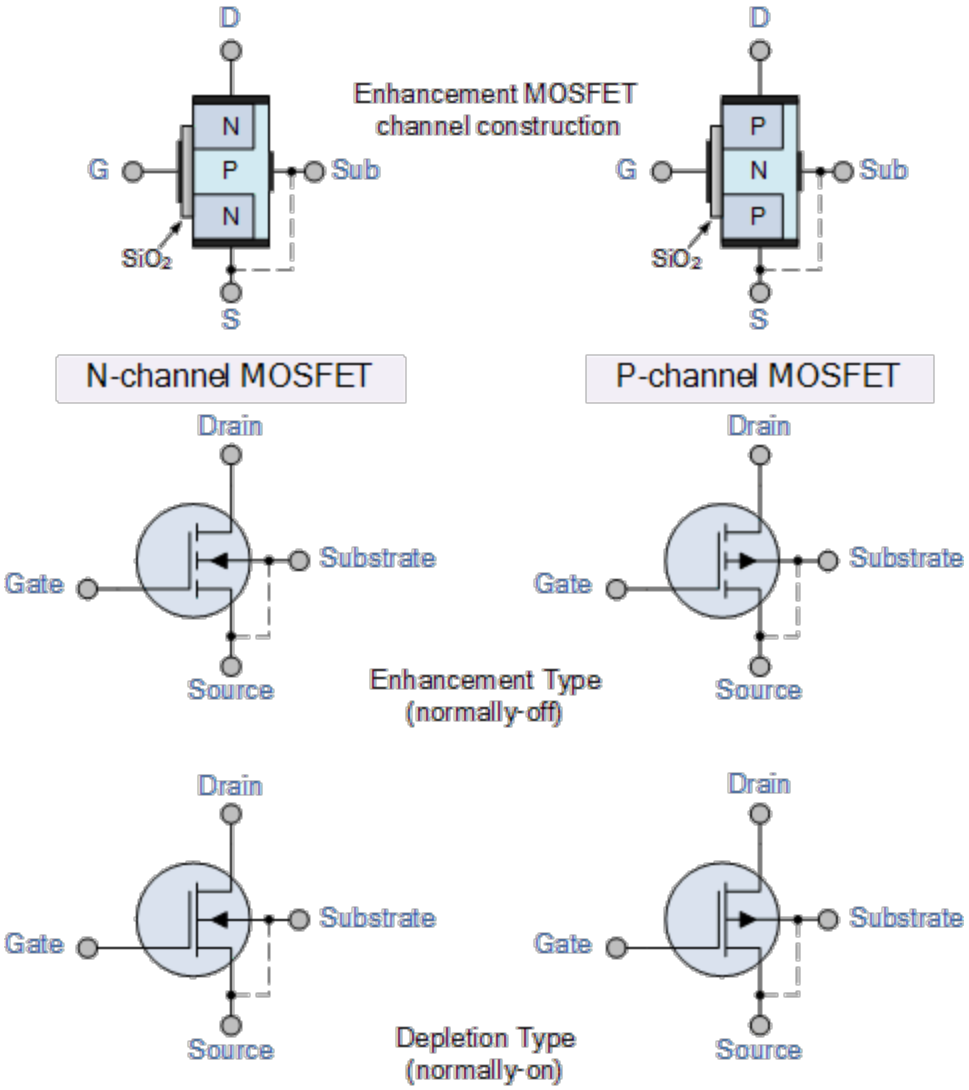
This ultra thin insulated metal gate electrode can be thought of as one plate of a capacitor. The isolation of the controlling Gate makes the input resistance of the **MOSFET** extremely high way up in the Mega-ohms (MΩ) region thereby making it almost infinite.

As the Gate terminal is electrically isolated from the main current carrying channel between the drain and source, "**NO current flows into the gate**" and just like the JFET, the MOSFET also acts like a voltage controlled resistor where the current flowing through the main channel between the Drain and Source is proportional to the input voltage. Also like the JFET, the MOSFETs very high input resistance can easily accumulate large amounts of static charge resulting in the **MOSFET** becoming easily damaged unless carefully handled or protected.

Like the previous JFET tutorial, MOSFETs are three terminal devices with a Gate, Drain and Source and both P-channel (PMOS) and N-channel (NMOS) MOSFETs are available. The main difference this time is that MOSFETs are available in two basic forms:

- ✔ Depletion Type – the transistor requires the Gate-Source voltage, (V_{GS}) to switch the device "OFF". The depletion mode MOSFET is equivalent to a "Normally Closed" switch.
- ✔ Enhancement Type – the transistor requires a Gate-Source voltage, (V_{GS}) to switch the device "ON". The enhancement mode MOSFET is equivalent to a "Normally Open" switch.

The symbols and basic construction for both configurations of MOSFETs are shown below.



The four MOSFET symbols above show an additional terminal called the Substrate and is not normally used as either an input or an output connection but instead it is used for grounding the substrate. It connects to the main semiconductive channel through a diode junction to the body or metal tab of the MOSFET.

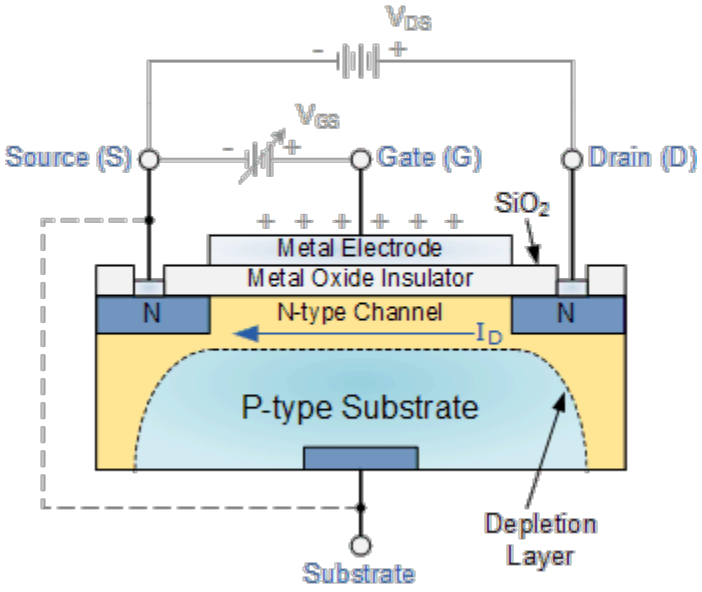
Usually in discrete type MOSFETs, this substrate lead is connected internally to the source terminal. When this is the case, as in enhancement types it is omitted from the symbol for clarification.

The line in the MOSFET symbol between the drain (D) and source (S) connections represents the transistors semiconductive channel. If this channel line is a solid unbroken line then it represents a “Depletion” (normally-ON) type MOSFET as drain current can flow with zero gate biasing potential.

If the channel line is shown as a dotted or broken line, then it represents an “Enhancement” (normally-OFF) type MOSFET as zero drain current flows with zero gate potential. The direction of the arrow

pointing to this channel line indicates whether the conductive channel is a P-type or an N-type semiconductor device.

Basic MOSFET Structure and Symbol



The construction of the Metal Oxide Semiconductor FET is very different to that of the Junction FET. Both the Depletion and Enhancement type MOSFETs use an electrical field produced by a gate voltage to alter the flow of charge carriers, electrons for n-channel or holes for P-channel, through the semiconductive drain-source channel. The gate electrode is placed on top of a very thin insulating layer and there are a pair of small n-type regions just under the drain and source electrodes.

We saw in the previous tutorial, that the gate of a junction field effect transistor, JFET must be biased in such a way as to reverse-bias the pn-junction. With a insulated gate MOSFET device no such limitations apply so it is possible to bias the gate of a MOSFET in either polarity, positive (+ve) or negative (-ve).

This makes the MOSFET device especially valuable as electronic switches or to make logic gates because with no bias they are normally non-conducting and this high gate input resistance means that very little or no control current is needed as MOSFETs are voltage controlled devices. Both the p-channel and the n-channel MOSFETs are available in two basic forms, the **Enhancement** type and the **Depletion** type.

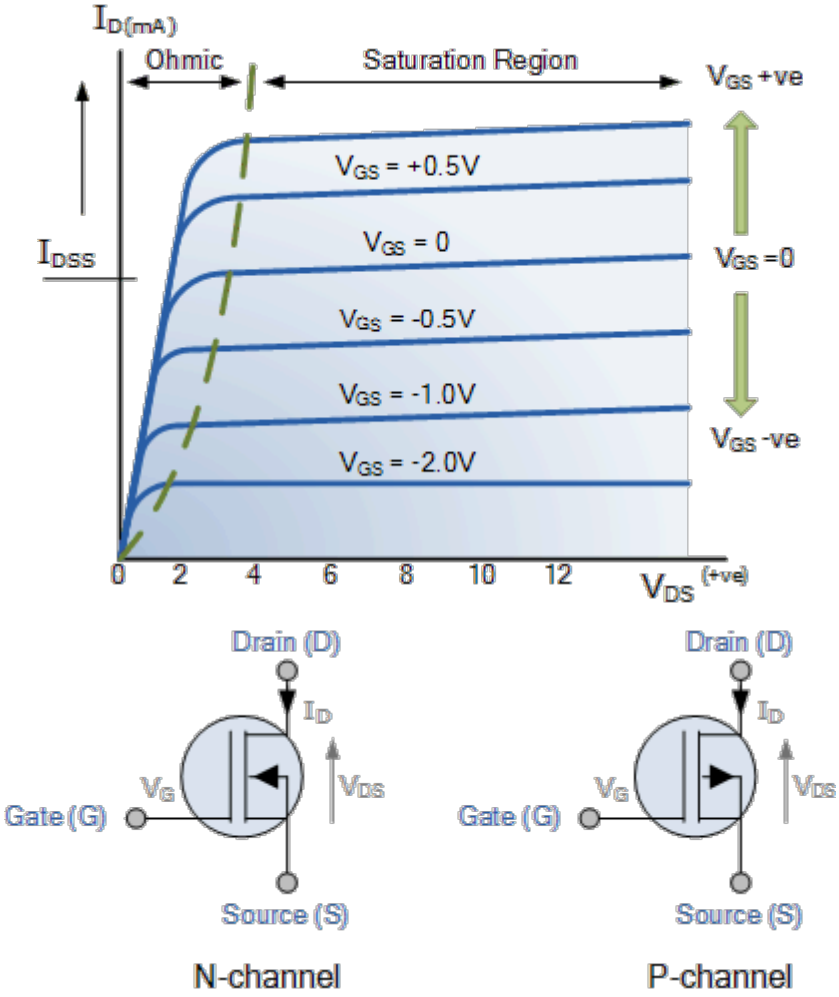
Depletion-mode MOSFET

The Depletion-mode MOSFET, which is less common than the enhancement mode types is normally switched “ON” (conducting) without the application of a gate bias voltage. That is the channel conducts when $V_{GS} = 0$ making it a “normally-closed” device. The circuit symbol shown above for a depletion MOS transistor uses a solid channel line to signify a normally closed conductive channel.

For the n-channel depletion MOS transistor, a negative gate-source voltage, $-V_{GS}$ will deplete (hence its name) the conductive channel of its free electrons switching the transistor “OFF”. Likewise for a p-channel depletion MOS transistor a positive gate-source voltage, $+V_{GS}$ will deplete the channel of its free holes turning it “OFF”.

In other words, for an n-channel depletion mode MOSFET: $+V_{GS}$ means more electrons and more current. While a $-V_{GS}$ means less electrons and less current. The opposite is also true for the p-channel types. Then the depletion mode MOSFET is equivalent to a “normally-closed” switch.

Depletion-mode N-Channel Circuit Symbols



The depletion-mode MOSFET is constructed in a similar way to their JFET transistor counterparts were the drain-source channel is inherently conductive with the electrons and holes already present within the n-type or p-type channel. This doping of the channel produces a conducting path of low resistance between the Drain and Source with zero Gate bias.

Enhancement-mode MOSFET

The more common **Enhancement-mode MOSFET** or eMOSFET, is the reverse of the depletion-mode type. Here the conducting channel is lightly doped or even undoped making it non-conductive. This results in the device being normally “OFF” (non-conducting) when the gate bias voltage, V_{GS} is equal to zero. The circuit symbol shown above for an enhancement MOS transistor uses a broken channel line to signify a normally open non-conducting channel.

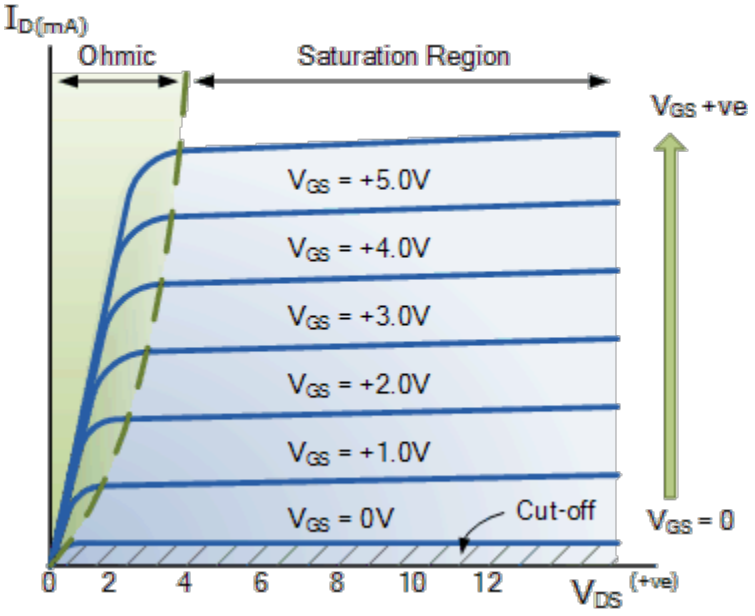
For the n-channel enhancement MOS transistor a drain current will only flow when a gate voltage (V_{GS}) is applied to the gate terminal greater than the threshold voltage (V_{TH}) level in which conductance takes place making it a transconductance device.

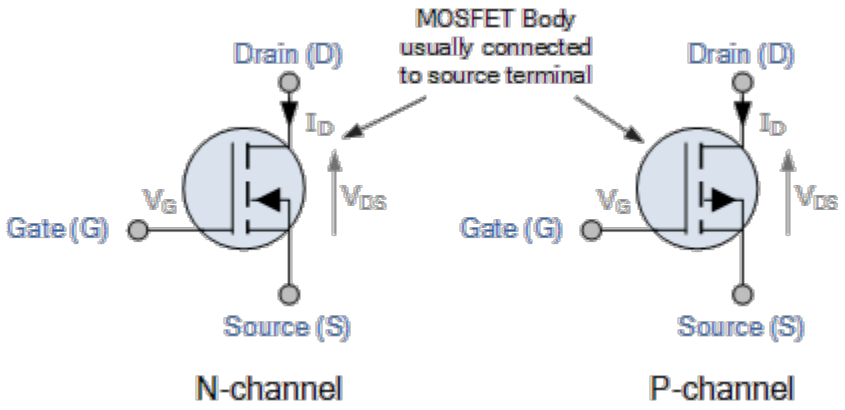
The application of a positive (+ve) gate voltage to a n-type eMOSFET attracts more electrons towards the oxide layer around the gate thereby increasing or enhancing (hence its name) the thickness of the channel allowing more current to flow. This is why this kind of transistor is called an enhancement mode device as the application of a gate voltage enhances the channel.

Increasing this positive gate voltage will cause the channel resistance to decrease further causing an increase in the drain current, ID through the channel. In other words, for an n-channel enhancement mode MOSFET: $+V_{GS}$ turns the transistor “ON”, while a zero or $-V_{GS}$ turns the transistor “OFF”. Thus the enhancement-mode MOSFET is equivalent to a “normally-open” switch.

The reverse is true for the p-channel enhancement MOS transistor. When $V_{GS} = 0$ the device is “OFF” and the channel is open. The application of a negative (-ve) gate voltage to the p-type eMOSFET enhances the channels conductivity turning it “ON”. Then for an p-channel enhancement mode MOSFET: $+V_{GS}$ turns the transistor “OFF”, while $-V_{GS}$ turns the transistor “ON”.

Enhancement-mode N-Channel Circuit Symbols





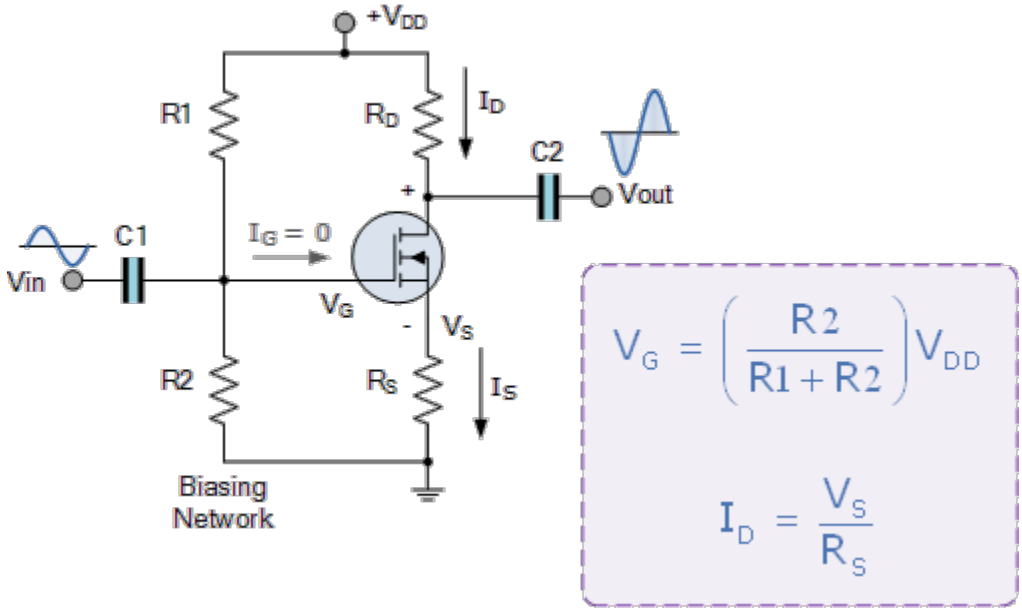
Enhancement-mode MOSFETs make excellent electronics switches due to their low “ON” resistance and extremely high “OFF” resistance as well as their infinitely high input resistance due to their isolated gate. Enhancement-mode MOSFETs are used in integrated circuits to produce CMOS type *Logic Gates* and power switching circuits in the form of as PMOS (P-channel) and NMOS (N-channel) gates. CMOS actually stands for *Complementary* MOS meaning that the logic device has both PMOS and NMOS within its design.

The MOSFET Amplifier

Just like the previous Junction Field Effect transistor, MOSFETs can be used to make single stage class “A” amplifier circuits with the enhancement mode n-channel MOSFET common source amplifier being the most popular circuit. Depletion mode MOSFET amplifiers are very similar to the JFET amplifiers, except that the MOSFET has a much higher input impedance.

This high input impedance is controlled by the gate biasing resistive network formed by R1 and R2. Also, the output signal for the enhancement mode common source MOSFET amplifier is inverted because when VG is low the transistor is switched “OFF” and V_D (Vout) is high. When V_G is high the transistor is switched “ON” and VD (Vout) is low as shown.

Enhancement-mode N-Channel Amplifier



The DC biasing of this common source (CS) MOSFET amplifier circuit is virtually identical to the JFET amplifier. The MOSFET circuit is biased in class A mode by the voltage divider network formed by resistors R1 and R2. The AC input resistance is given as $R_{IN} = R_G = 1M\Omega$.

Metal Oxide Semiconductor Field Effect Transistors are three terminal active devices made from different semiconductor materials that can act as either an insulator or a conductor by the application of a small signal voltage.

The MOSFETs ability to change between these two states enables it to have two basic functions: “switching” (digital electronics) or “amplification” (analogue electronics). Then MOSFETs have the ability to operate within three different regions:

1. Cut-off Region : with VGS < Vthreshold the gate-source voltage is much lower than the transistors threshold voltage so the MOSFET transistor is switched “fully-OFF” thus, $I_D = 0$, with the transistor acting like an open switch regardless of the value of VDS.
2. Linear (Ohmic) Region : with $V_{GS} > V_{threshold}$ and $V_{DS} < V_{GS}$ the transistor is in its constant resistance region behaving as a voltage-controlled resistance whose resistive value is determined by the gate voltage, V_{GS} level.
3. Saturation Region : with $V_{GS} >$ Vthreshold and $V_{DS} > V_{GS}$ the transistor is in its constant current region and is therefore “fully-ON”. The Drain current I_D = Maximum with the transistor acting as a closed switch.

MOSFET Tutorial Summary

The Metal Oxide Semiconductor Field Effect Transistor, or **MOSFET** for short, has an extremely high input gate resistance with the current flowing through the channel between the source and drain being controlled by the gate voltage. Because of this high input impedance and gain, MOSFETs can be easily damaged by static electricity if not carefully protected or handled.

MOSFET's are ideal for use as electronic switches or as common-source amplifiers as their power consumption is very small. Typical applications for metal oxide semiconductor field effect transistors are in Microprocessors, Memories, Calculators and Logic CMOS Gates etc.

Also, notice that a dotted or broken line within the symbol indicates a normally "OFF" enhancement type showing that "NO" current can flow through the channel when zero gate-source voltage V_{GS} is applied.

A continuous unbroken line within the symbol indicates a normally "ON" Depletion type showing that current "CAN" flow through the channel with zero gate voltage. For p-channel types the symbols are exactly the same for both types except that the arrow points outwards. This can be summarised in the following switching table.

MOSFET type	V_{GS} = +ve	V_{GS} = 0	V_{GS} = -ve
N-Channel Depletion	ON	ON	OFF
N-Channel Enhancement	ON	OFF	OFF
P-Channel Depletion	OFF	ON	ON
P-Channel Enhancement	OFF	OFF	ON

So for n-type enhancement type MOSFETs, a positive gate voltage turns "ON" the transistor and with zero gate voltage, the transistor will be "OFF". For a p-channel enhancement type MOSFET, a negative gate voltage will turn "ON" the transistor and with zero gate voltage, the transistor will be "OFF". The voltage point at which the MOSFET starts to pass current through the channel is determined by the threshold voltage V_{TH} of the device.

In the next tutorial about **Field Effect Transistors** instead of using the transistor as an amplifying device, we will look at the operation of the transistor in its saturation and cut-off regions when used as a solid-state switch. Field effect transistor switches are used in many applications to switch a DC current "ON" or "OFF" such as LED's which require only a few milliamps at low DC voltages, or motors which require higher currents at higher voltages.

https://www.electronics-tutorials.ws/transistor/tran_7.html

MOSFET as a Switch

MOSFET's make very good electronic switches for controlling loads and in CMOS digital circuits as they operate between their cut-off and saturation regions.

We saw previously, that the N-channel, Enhancement-mode MOSFET (e-MOSFET) operates using a positive input voltage and has an extremely high input resistance (almost infinite) making it possible to use the MOSFET as a switch when interfaced with nearly any logic gate or driver capable of producing a positive output.

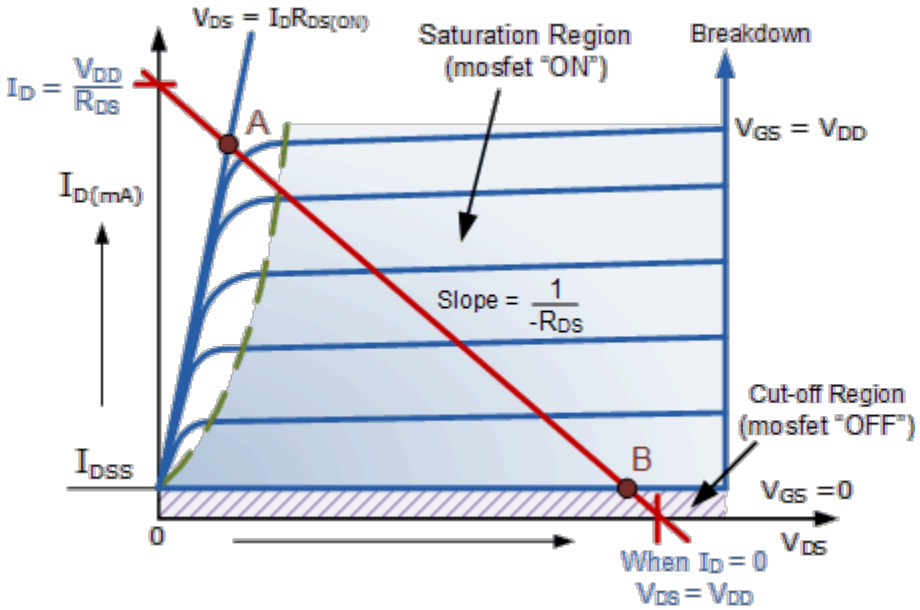
We also saw that due to this very high input (Gate) resistance we can safely parallel together many different MOSFETS until we achieve the current handling capacity that we required.

While connecting together various MOSFETS in parallel may enable us to switch high currents or high voltage loads, doing so becomes expensive and impractical in both components and circuit board space. To overcome this problem **Power Field Effect Transistors** or Power FET's where developed.

We now know that there are two main differences between field effect transistors, depletion-mode only for JFET's and both enhancement-mode and depletion-mode for MOSFETs. In this tutorial we will look at using the *Enhancement-mode MOSFET as a Switch* as these transistors require a positive gate voltage to turn "ON" and a zero voltage to turn "OFF" making them easily understood as switches and also easy to interface with logic gates.

The operation of the enhancement-mode MOSFET, or e-MOSFET, can best be described using its I-V characteristics curves shown below. When the input voltage, (V_{IN}) to the gate of the transistor is zero, the MOSFET conducts virtually no current and the output voltage (V_{OUT}) is equal to the supply voltage V_{DD}. So the MOSFET is "OFF" operating within its "cut-off" region.

MOSFET Characteristics Curves



The minimum ON-state gate voltage required to ensure that the MOSFET remains “ON” when carrying the selected drain current can be determined from the V-I transfer curves above. When V_{IN} is HIGH or equal to V_{DD}, the MOSFET Q-point moves to point A along the load line.

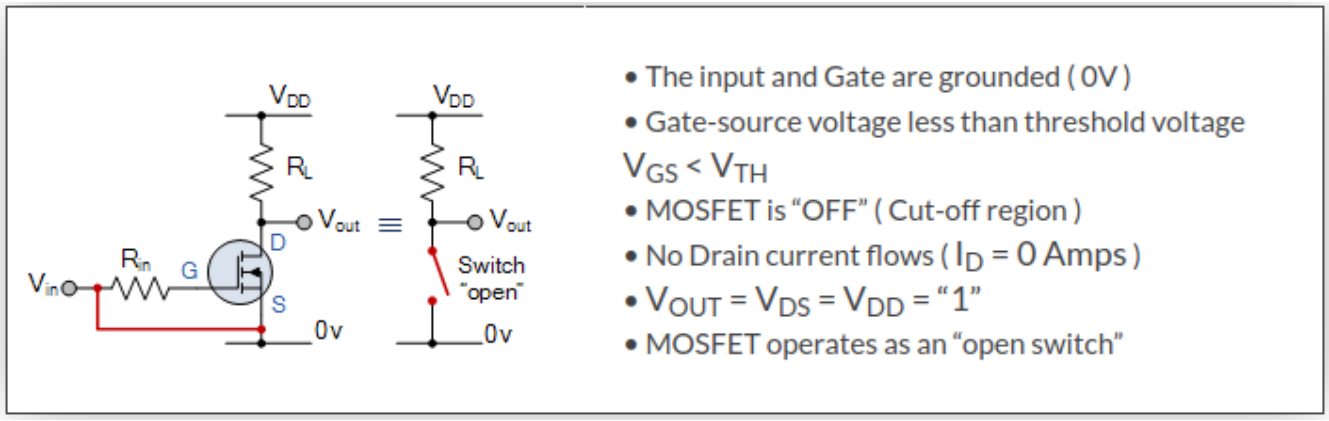
The drain current I_D increases to its maximum value due to a reduction in the channel resistance. I_D becomes a constant value independent of VDD, and is dependent only on V_{GS}. Therefore, the transistor behaves like a closed switch but the channel ON-resistance does not reduce fully to zero due to its $R_{DS(on)}$ value, but gets very small.

Likewise, when V_{IN} is LOW or reduced to zero, the MOSFET Q-point moves from point A to point B along the load line. The channel resistance is very high so the transistor acts like an open circuit and no current flows through the channel. So if the gate voltage of the MOSFET toggles between two values, HIGH and LOW the MOSFET will behave as a “single-pole single-throw” (SPST) solid state switch and this action is defined as:

1. Cut-off Region

Here the operating conditions of the transistor are zero input gate voltage (VIN), zero drain current ID and output voltage VDS = VDD. Therefore for an enhancement type MOSFET the conductive channel is closed and the device is switched “OFF”.

Cut-off Characteristics

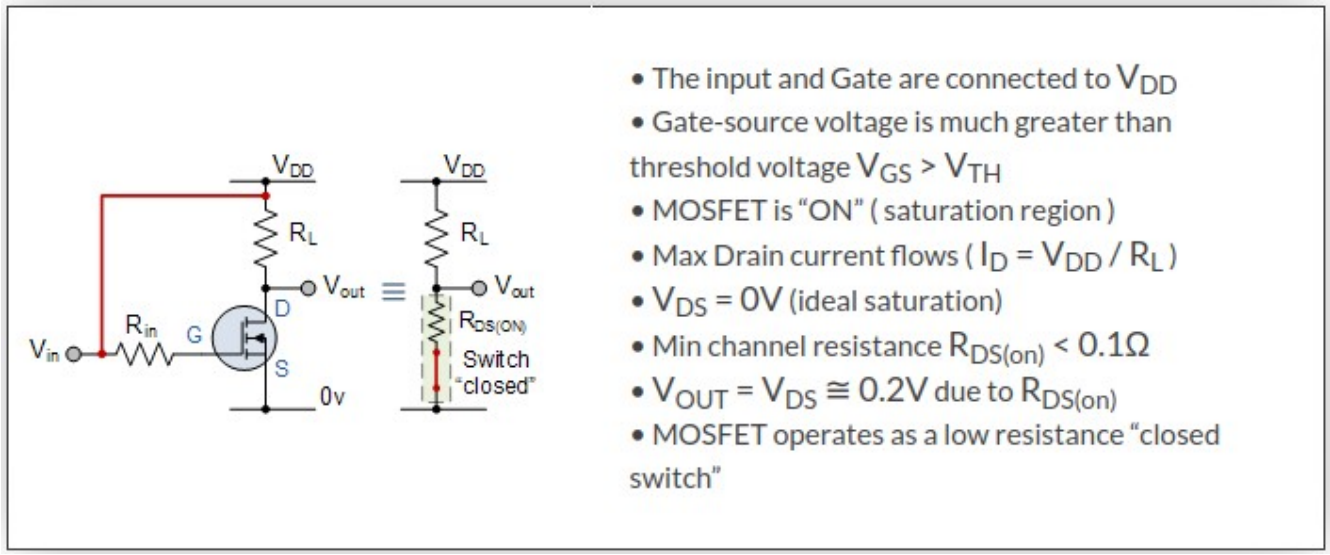


Then we can define the cut-off region or “OFF mode” when using an e-MOSFET as a switch as being, gate voltage, $V_{GS} < V_{TH}$ thus $I_D = 0$. For a P-channel enhancement MOSFET, the Gate potential must be more positive with respect to the Source.

2. Saturation Region

In the saturation or linear region, the transistor will be biased so that the maximum amount of gate voltage is applied to the device which results in the channel resistance $R_{DS(on)}$ being as small as possible with maximum drain current flowing through the MOSFET switch. Therefore for the enhancement type MOSFET the conductive channel is open and the device is switched “ON”.

Saturation Characteristics

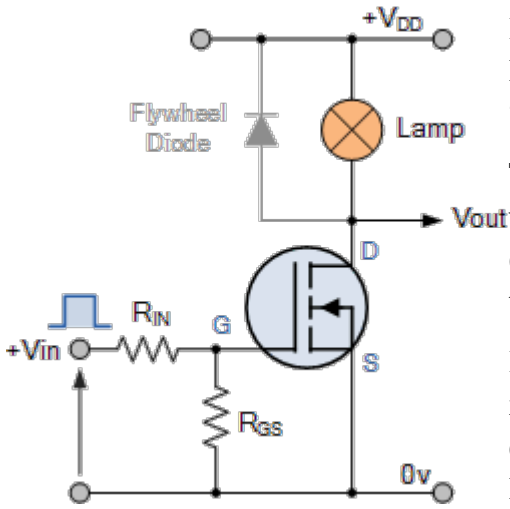


Then we can define the saturation region or “ON mode” when using an e-MOSFET as a switch as gate-source voltage, $V_{GS} > V_{TH}$ thus I_D = Maximum. For a P-channel enhancement MOSFET, the Gate potential must be more negative with respect to the Source.

By applying a suitable drive voltage to the gate of an FET, the resistance of the drain-source channel, $R_{DS(on)}$ can be varied from an “OFF-resistance” of many hundreds of kΩ, effectively an open circuit, to an “ON-resistance” of less than 1Ω, effectively acting as a short circuit.

When using the MOSFET as a switch we can drive the MOSFET to turn “ON” faster or slower, or pass high or low currents. This ability to turn the power MOSFET “ON” and “OFF” allows the device to be used as a very efficient switch with switching speeds much faster than standard bipolar junction transistors.

An example of using the MOSFET as a switch



In this circuit arrangement an Enhancement-mode N-channel MOSFET is being used to switch a simple lamp “ON” and “OFF” (could also be an LED).

The gate input voltage V_{GS} is taken to an appropriate positive voltage level to turn the device and therefore the lamp load either “ON”, (V_{GS} = +ve) or at a zero voltage level that turns the device “OFF”, (V_{GS} = 0V).

If the resistive load of the lamp was to be replaced by an inductive load such as a coil, solenoid or relay a “flywheel diode” would be required in parallel with the load to protect the MOSFET from any self generated back-emf.

Above shows a very simple circuit for switching a resistive load such as a lamp or LED. But when using power MOSFETs to switch either inductive or capacitive loads some form of protection is required to prevent the MOSFET device from becoming damaged. Driving an inductive load has the opposite effect from driving a capacitive load.

For example, a capacitor without an electrical charge is a short circuit, resulting in a high “inrush” of current and when we remove the voltage from an inductive load we have a large reverse voltage build up as the magnetic field collapses, resulting in an induced back-emf in the windings of the inductor.

Then we can summarise the switching characteristics of both the N-channel and P-channel type MOSFET within the following table.

MOSFET Type	$V_{GS} \ll 0$	$V_{GS} = 0$	$V_{GS} \gg 0$
N-channel Enhancement	OFF	OFF	ON
N-channel Depletion	OFF	ON	ON
P-channel Enhancement	ON	OFF	OFF
P-channel Depletion	ON	ON	OFF

Note that unlike the N-channel MOSFET whose gate terminal must be made more positive (attracting electrons) than the source to allow current to flow through the channel, the conduction through the P-channel MOSFET is due to the flow of holes. That is the gate terminal of a P-channel MOSFET must be made more negative than the source and will only stop conducting (cut-off) until the gate is more positive than the source.

So for the enhancement type power MOSFET to operate as an analogue switching device, it needs to be switched between its “Cut-off Region” where: V_{GS} = 0V (or V_{GS} = -ve) and its “Saturation Region” where: $V_{GS(on)}$ = +ve. The power dissipated in the MOSFET (P_D) depends upon the current flowing through the channel ID at saturation and also the “ON-resistance” of the channel given as $R_{DS(on)}$. For example.

MOSFET as a Switch Example No1

Lets assume that the lamp is rated at 6v, 24W and is fully “ON”, the standard MOSFET has a channel on-resistance ($R_{DS(on)}$) value of 0.1ohms. Calculate the power dissipated in the MOSFET switching device.

The current flowing through the lamp is calculated as:

$$P = V \times I_D$$

$$\therefore I_D = \frac{P}{V} = \frac{24}{6} = 4.0\,\text{amps}$$

Then the power dissipated in the MOSFET will be given as:

$$P = I^2.R$$

$$P_D = I_D^2 \times R_{DS}$$

$$\therefore P_D = 4^2 \times 0.1 = 1.6\,\text{watts}$$

You may be sat there thinking, well so what!, but when using the MOSFET as a switch to control DC motors or electrical loads with high inrush currents the “ON” Channel resistance ($R_{DS(on)}$) between the drain and the source is very important. For example, MOSFETs that control DC motors, are subjected to a high in-rush current when the motor first begins to rotate, because the motors starting current is only limited by the very low resistance value of the motors windings.

As the basic power relationship is: $P = I^2R$, then a high $R_{DS(on)}$ channel resistance value would simply result in large amounts of power being dissipated and wasted within the MOSFET itself resulting in an excessive temperature rise, which if not controlled could result in the MOSFET becoming very hot and damaged due to a thermal overload.

A lower $R_{DS(on)}$ value for the channel resistance is also a desirable parameter as it helps to reduce the channels effective saturation voltage ($V_{DS(sat)} = I_D * R_{DS(on)}$) across the MOSFET and will therefore

operate at a cooler temperature. Power MOSFETs generally have a $R_{DS(on)}$ value of less than 0.01Ω which allows them to run cooler, extending their operational life span.

One of the main limitations when using a MOSFET as a switching device is the maximum drain current it can handle. So the $R_{DS(on)}$ parameter is an important guide to the switching efficiency of the MOSFET and is simply given as the ratio of V_{DS} / I_D when the transistor is switched “ON”.

When using a MOSFET or any type of field effect transistor for that matter as a solid-state switching device it is always advisable to select ones that have a very low $R_{DS(on)}$ value or at least mount them onto a suitable heatsink to help reduce any thermal runaway and damage. Power MOSFETs used as a switch generally have surge-current protection built into their design, but for high-current applications the bipolar junction transistor is a better choice.

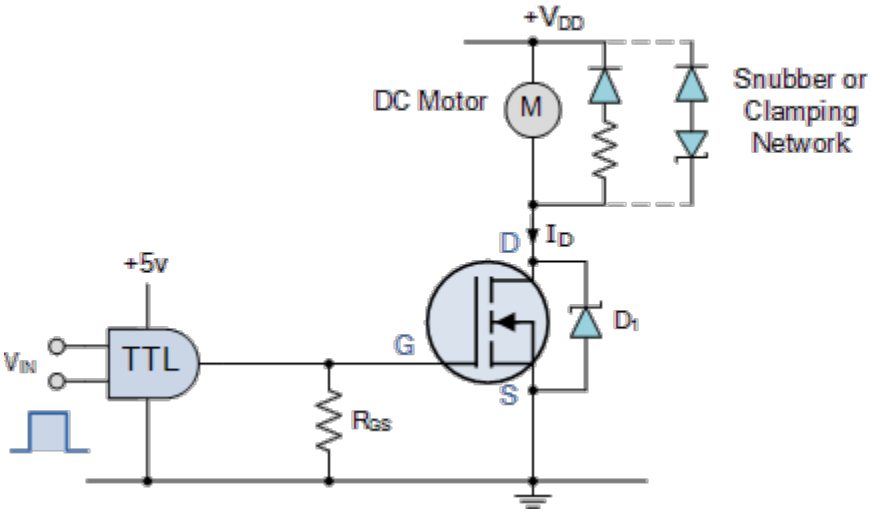
Power MOSFET Motor Control

Because of the extremely high input or gate resistance that the MOSFET has, its very fast switching speeds and the ease at which they can be driven makes them ideal to interface with op-amps or standard logic gates. However, care must be taken to ensure that the gate-source input voltage is correctly chosen because when using the **MOSFET as a switch** the device must obtain a low $R_{DS(on)}$ channel resistance in proportion to this input gate voltage.

Low threshold type power MOSFETs may not switch “ON” until a least 3V or 4V has been applied to its gate and if the output from the logic gate is only +5V logic it may be insufficient to fully drive the MOSFET into saturation. Using lower threshold MOSFETs designed for interfacing with TTL and CMOS logic gates that have thresholds as low as 1.5V to 2.0V are available.

Power MOSFETs can be used to control the movement of DC motors or brushless stepper motors directly from computer logic or by using pulse-width modulation (PWM) type controllers. As a DC motor offers high starting torque and which is also proportional to the armature current, MOSFET switches along with a PWM can be used as a very good speed controller that would provide smooth and quiet motor operation.

Simple Power MOSFET Motor Controller

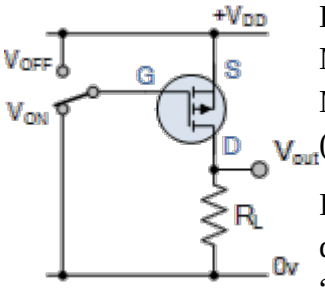


As the motor load is inductive, a simple flywheel diode is connected across the inductive load to dissipate any back emf generated by the motor when the MOSFET turns it “OFF”. A clamping network formed by a zener diode in series with the diode can also be used to allow for faster switching and better control of the peak reverse voltage and drop-out time.

For added security an additional silicon or zener diode D1 can also be placed across the channel of a MOSFET switch when using inductive loads, such as motors, relays, solenoids, etc, for suppressing over voltage switching transients and noise giving extra protection to the MOSFET switch if required. Resistor R_{GS} is used as a pull-down resistor to help pull the TTL output voltage down to 0V when the MOSFET is switched “OFF”.

P-channel MOSFET as a Switch

Thus far we have looked at the N-channel MOSFET as a switch were the MOSFET is placed between the load and the ground. This also allows for the MOSFET’s gate drive or switching signal to be referenced to ground (low-side switching).



P-channel MOSFET Switch

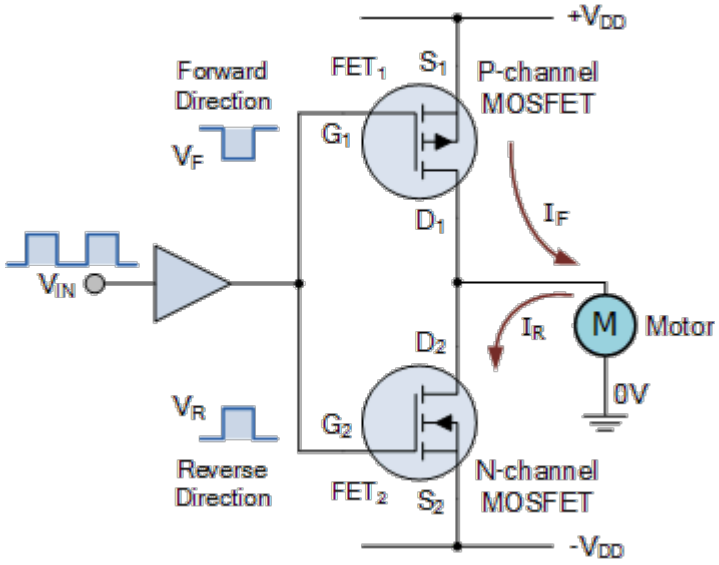
But in some applications we require the use of P-channel enhancement-mode MOSFET were the load is connected directly to ground. In this instance the MOSFET switch is connected between the load and the positive supply rail (high-side switching) as we do with PNP transistors.

In a P-channel device the conventional flow of drain current is in the negative direction so a negative gate-source voltage is applied to switch the transistor “ON”.

This is achieved because the P-channel MOSFET is “upside down” with its source terminal tied to the positive supply $+V_{DD}$. Then when the switch goes LOW, the MOSFET turns “ON” and when the switch goes HIGH the MOSFET turns “OFF”.

This upside down connection of a P-channel enhancement mode MOSFET switch allows us to connect it in series with a N-channel enhancement mode MOSFET to produce a complementary or CMOS switching device as shown across a dual supply.

Complementary MOSFET as a Switch Motor Controller



The two MOSFETs are configured to produce a bi-directional switch from a dual supply with the motor connected between the common drain connection and ground reference. When the input is LOW the P-channel MOSFET is switched-ON as its gate-source junction is negatively biased so the motor rotates in one direction. Only the positive $+V_{DD}$ supply rail is used to drive the motor.

When the input is HIGH, the P-channel device switches-OFF and the N-channel device switches-ON as its gate-source junction is positively biased. The motor now rotates in the opposite direction because the motors terminal voltage has been reversed as it is now supplied by the negative $-V_{DD}$ supply rail.

Then the P-channel MOSFET is used to switch the positive supply to the motor for forward direction (high-side switching) while the N-channel MOSFET is used to switch the negative supply to the motor for reverse direction (low-side switching).

There are a variety of configurations for driving the two MOSFETs with many different applications. Both the P-channel and the N-channel devices can be driven by a single gate drive IC as shown.

However, to avoid cross conduction with both MOSFETS conducting at the same time across the two polarities of the dual supply, fast switching devices are required to provide some time difference between them turning “OFF” and the other turning “ON”. One way to overcome this problem is to drive both MOSFETS gates separately. This then produces a third option of “STOP” to the motor when both MOSFETS are “OFF”.

MOSFET as a Switch Motor Control Table

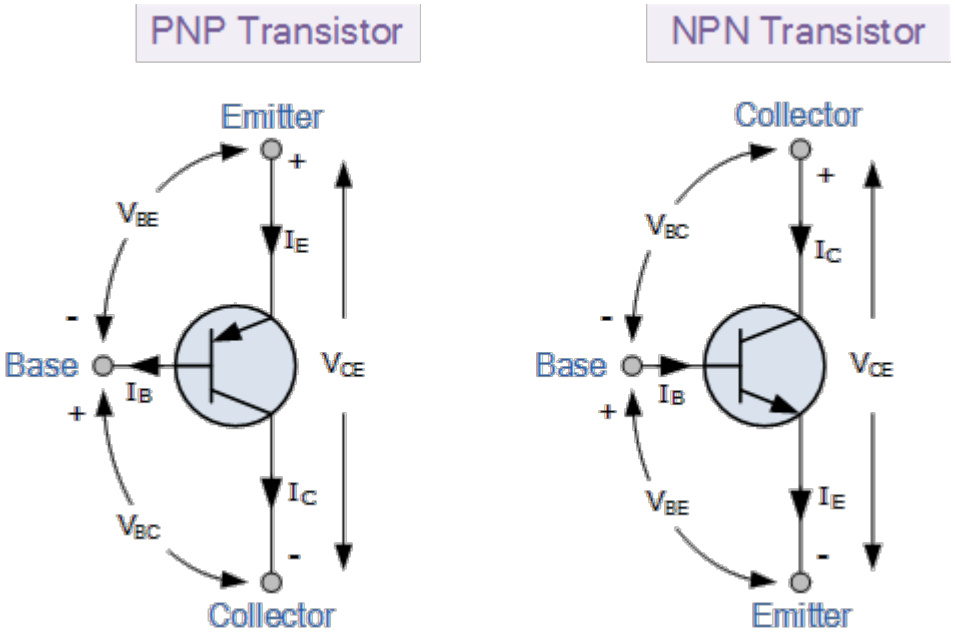
MOSFET 1	MOSFET 2	Motor Function
OFF	OFF	Motor Stopped (OFF)
ON	OFF	Motor Rotates Forward
OFF	ON	Motor Rotates Reverse
ON	ON	NOT ALLOWED

Please note it is important that there are no other combination of inputs allowed at the same time as this may cause the power supply to become shorted out, as both MOSFETS, FET_1 and FET_2 could be switched “ON” together resulting in: (fuse = bang!), be warned.

https://www.electronics-tutorials.ws/transistor/tran_8.html

Transistor Tutorial Summary

Having looked at the construction and operation of NPN and PNP bipolar junctions transistors (BJT's) as well as field effect transistors (FET's), both junction and insulated gate, we can summarise the main points of these transistor tutorial as outlined below:



- The Bipolar Junction Transistor (BJT) is a three layer device constructed form two semiconductor diode junctions joined together, one forward biased and one reverse biased.
- There are two main types of bipolar junction transistors, (BJT) the NPN and the PNP transistor.
- Bipolar junction transistors are "Current Operated Devices" where a much smaller Base current causes a larger Emitter to Collector current, which themselves are nearly equal, to flow.
- The arrow in a transistor symbol represents conventional current flow.
- The most common transistor connection is the Common Emitter (CE) configuration but Common Base (CB) and Common Collector (CC) are also available.
- Requires a Biasing voltage for AC amplifier operation.
- The Base-Emitter junction is always forward biased whereas the Collector-Base junction is always reverse biased.
- The standard equation for currents flowing in a transistor is given as: $I_E = I_B + I_C$
- The Collector or output characteristics curves can be used to find either I_B, I_C or β to which a load line can be constructed to determine a suitable operating point, Q with variations in base current determining the operating range.

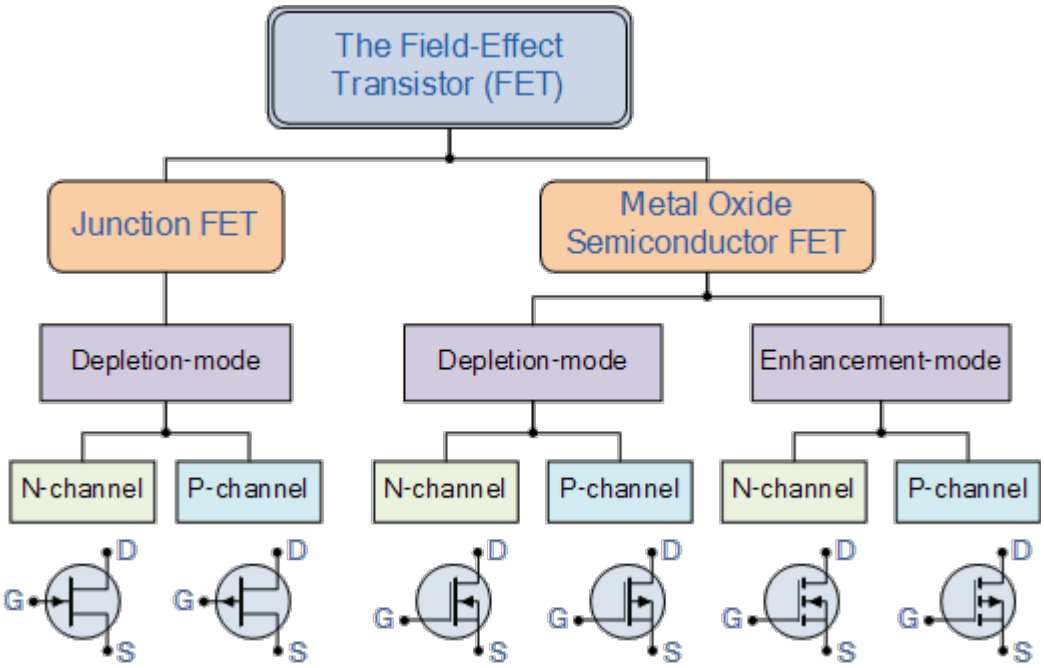
- A transistor can also be used as an electronic switch between its saturation and cut-off regions to control devices such as lamps, motors and solenoids etc.
- Inductive loads such as DC motors, relays and solenoids require a reverse biased “Flywheel” diode placed across the load. This helps prevent any induced back emf’s generated when the load is switched “OFF” from damaging the transistor.
- The NPN transistor requires the Base to be more positive than the Emitter while the PNP type requires that the Emitter is more positive than the Base.

Transistor Tutorial – The Field Effect Transistor

- Field Effect Transistors, or FET’s are “Voltage Operated Devices” and can be divided into two main types: Junction-gate devices called JFET’s and Insulated-gate devices called IGFET´s or more commonly known as MOSFETs.
- Insulated-gate devices can also be sub-divided into Enhancement types and Depletion types. All forms are available in both N-channel and P-channel versions.
- FET’s have very high input resistances so very little or no current (MOSFET types) flows into the input terminal making them ideal for use as electronic switches.
- The input impedance of the MOSFET is even higher than that of the JFET due to the insulating oxide layer and therefore static electricity can easily damage MOSFET devices so care needs to be taken when handling them.
- When no voltage is applied to the gate of an enhancement FET the transistor is in the “OFF” state similar to an “open switch”.
- The depletion FET is inherently conductive and in the “ON” state when no voltage is applied to the gate similar to a “closed switch”.
- FET’s have much higher current gains compared to bipolar junction transistors.
- The most common FET connection is the Common Source (CS) configuration but Common Gate (CG) and Common Drain (CD) configurations are also available.
- MOSFETS can be used as ideal switches due to their very high channel “OFF” resistance, low “ON” resistance.
- To turn the N-channel JFET transistor “OFF”, a negative voltage must be applied to the gate.
- To turn the P-channel JFET transistor “OFF”, a positive voltage must be applied to the gate.
- N-channel depletion MOSFETs are in the “OFF” state when a negative voltage is applied to the gate to create the depletion region.
- P-channel depletion MOSFETs, are in the “OFF” state when a positive voltage is applied to the gate to create the depletion region.

- N-channel enhancement MOSFETs are in the “ON” state when a “+ve” (positive) voltage is applied to the gate.
- P-channel enhancement MOSFETs are in the “ON” state when “-ve” (negative) voltage is applied to the gate.

The Field Effect Transistor Chart



Biasing of the Gate for both the junction field effect transistor, (JFET) and the metal oxide semiconductor field effect transistor, (MOSFET) configurations are given as:

Type	Junction FET		Metal Oxide Semiconductor FET			
	Depletion Mode		Depletion Mode		Enhancement Mode	
Bias	ON	OFF	ON	OFF	ON	OFF
N-channel	0V	-ve	0V	-ve	+ve	0V
P-channel	0V	+ve	0V	+ve	-ve	0V

Transistor Tutorial – Differences between a FET and a BJT

Field Effect Transistors can be used to replace normal Bipolar Junction Transistors in electronic circuits. A simple comparison in this transistor tutorial between FET's and Transistors stating both their advantages and their disadvantages is given below.

	Field Effect Transistor (FET)	Bipolar Junction Transistor (BJT)
1	Low voltage gain	High voltage gain
2	High current gain	Low current gain
3	Very high input impedance	Low input impedance
4	High output impedance	Low output impedance
5	Low noise generation	Medium noise generation
6	Fast switching time	Medium switching time
7	Easily damaged by static	Robust
8	Some require an input to turn it "OFF"	Requires zero input to turn it "OFF"
9	Voltage controlled device	Current controlled device
10	Exhibits the properties of a Resistor	
11	More expensive than bipolar	Cheap
12	Difficult to bias	Easy to bias

Below is a list of complementary bipolar transistors which can be used for the general–purpose switching of low-current relays, driving LED's and lamps, and for amplifier and oscillator applications.

Complementary NPN and PNP Transistors

NPN	PNP	V_{CE}	$I_{C(max)}$	P_d
BC547	BC557	45v	100mA	600mW
BC447	BC448	80v	300mA	625mW
2N3904	2N3906	40v	200mA	625mW
2N2222	2N2907	30v	800mA	800mW
BC140	BC160	40v	1.0A	800mW
TIP29	TIP30	100v	1.0A	3W
BD137	BD138	60v	1.5A	1.25W
TIP3055	TIP2955	60v	15A	90W

https://www.electronics-tutorials.ws/transistor/darlington-transistor.html

Darlington Transistors

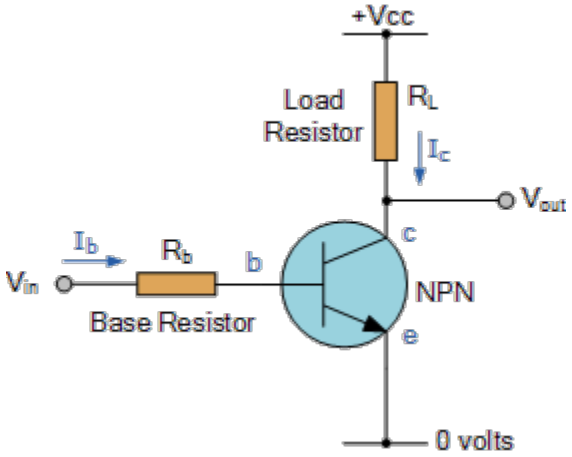
The Darlington Transistor configuration of two bipolar transistors offers increased current switching for a given base current.

The **Darlington Transistor** named after its inventor, Sidney Darlington is a special arrangement of two standard NPN or PNP bipolar junction transistors (BJT) connected together. The Emitter of one transistor is connected to the Base of the other to produce a more sensitive transistor with a much larger current gain being useful in applications where current amplification or switching is required.

Darlington Transistor pairs can be made from two individually connected bipolar transistors or a one single device commercially made in a single package with the standard: Base, Emitter and Collector connecting leads and are available in a wide variety of case styles and voltage (and current) ratings in both NPN and PNP versions.

As we saw in our Transistor as a Switch tutorial, as well as being used as an amplifier, the bipolar junction transistor, (BJT) can be made to operate as an ON-OFF switch as shown.

Bipolar Transistor as a Switch



When the base terminal of the NPN transistor is grounded (0 volts), zero current flows into the base therfore Ib = 0. As the base terminal is grounded, no current flows from the collector to the emitter terminals therefore the non-conducting NPN transistor is switched “OFF” (cut-off). If we now forward biased the base terminal with respect to the emitter by using a voltage source greater than 0.7 volts, transistor action occurs causing in a much larger current to flow through the transistor between its collector and emitter terminals. The transistor is now said to be switched “ON” (conducting). If we operate the transistor between these two modes of cut-off and conduction, the transistor can be made to operate as an electronic switch.

However, the transistors base terminal needs to be switched between zero and some positive value much greater than 0.7 volts for the transistor to fully conduct. A higher voltage causes an increased

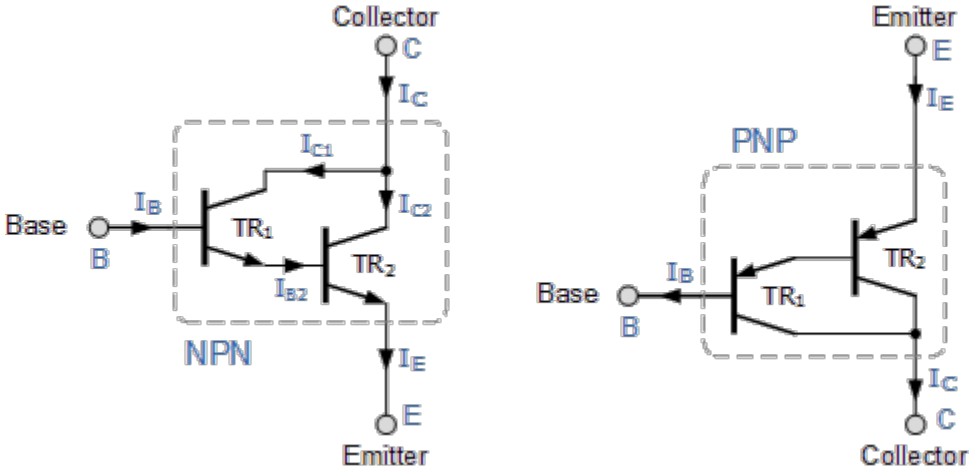
base current, Ib to flows into the device resulting in collector current Ic becoming large while the voltage drop across the colletor and emitter terminals, Vce becomes smaller. Then we can see that a smaller current flowing into the base terminal can cause a much larger current to flow between the collector and the emitter.

The ratio of collector current to base current (β) is known as the current gain of the transistor. A typical value of β for a standard bipolar transistor may be in the range of 50 to 200 and varies even between transistors of the same part number. In some cases where the current gain of a single transistor is too low to directly drive a load, one way to increase the gain is to use a Darlington pair.

A **Darlington Transistor** configuration, also known as a “Darlington pair” or “super-alpha circuit”, consist of two NPN or PNP transistors connected together so that the emitter current of the first transistor TR1 becomes the base current of the second transistor TR2. Then transistor TR1 is connected as an emitter follower and TR2 as a common emitter amplifier as shown below.

Also note that in this Darlington pair configuration, the collector current of the slave or control transistor, TR1 is “in-phase” with that of the master switching transistor TR2.

Basic Darlington Transistor Configuration



Using the NPN Darlington pair as the example, the collectors of two transistors are connected together, and the emitter of TR1 drives the base of TR2. This configuration achieves β multiplication because for a Base current ib, the collector current is $\beta * I_B$ where the current gain is greater than one, or unity and this is defined as:

$$I_C = I_{C1} + I_{C2}$$

$$I_C = \beta_1 . I_B + \beta_2 . I_{B2}$$

But the base current, I_{B2} is equal to transistor TR1 emitter current, I_{E1} as the emitter of TR1 is connected to the base of TR2. Therefore:

$$I_{B2} = I_{E1} = I_{C1} + I_B = \beta_1.I_B + I_B = (\beta_1 + 1).I_B$$

Then substituting in the first equation:

$$I_C = \beta_1.I_B + \beta_2.(\beta_1 + 1).I_B$$

$$I_C = \beta_1.I_B + \beta_2.\beta_1.I_B + \beta_2.I_B$$

$$I_C = \left(\beta_1 + (\beta_2.\beta_1) + \beta_2\right).I_B$$

Where β1 and β2 are the gains of the individual transistors.

This means that the overall current gain, β is given by the gain of the first transistor multiplied by the gain of the second transistor as the current gains of the two transistors multiply. In other words, a pair of bipolar transistors combined together to make a single Darlington transistor pair can be regarded as a single transistor with a very high value of β and consequently a high input resistance.

Darlington Transistor Example No1

Two NPN transistors are connected together in the form of a **Darlington Pair** to switch a 12V 75W halogen lamp. If the forward current gain of the first transistor is 25 and the forward current gain (Beta) of the second transistor is 80. Ignoring any voltage drops across the two transistors, calculate the maximum base current required to switch the lamp fully-ON.

Firstly, the current drawn by the lamp will be equal to the Collector current of the second transistor, then:

$$I_C = I_{LAMP}$$

$$\therefore I_{LAMP} = \frac{P}{V} = \frac{75}{12} = 6.25\,\text{Amps}$$

Using the equation above, the base current is given as:

$$\beta_1 = 25, \quad \beta_2 = 80$$

$$I_C = \left(\beta_1 + (\beta_2.\beta_1) + \beta_2\right).I_B$$

$$\therefore I_B = \frac{I_C}{\beta_1 + (\beta_2.\beta_1) + \beta_2} = \frac{6.25}{2105} = 3.0\,mA$$

Then we can see that a very small base current of only 3.0mA, such as that supplied by a digital logic gate or the output port of a micro-controller, can be used to switch the 75 Watt lamp “ON” and “OFF”.

If two identical bipolar transistors are used to make a single Darlington device then β1 is equal to β2 and the overall current gain will be given as:

$$\text{If } \beta_1 = \beta_2$$

$$I_C = \left(\beta_1 + (\beta_2.\beta_1) + \beta_2\right).I_B$$

$$\therefore I_C = \left(\beta^2 + 2\beta\right).I_B$$

Generally the value of β^2 is much greater than that of 2β, in which case it can be ignored to simplify the maths a little. Then the final equation for two identical transistors configured as a Darlington pair can be written as:

Identical Darlington Transistors

$$I_C = \left(\beta^2 \times I_B\right)$$

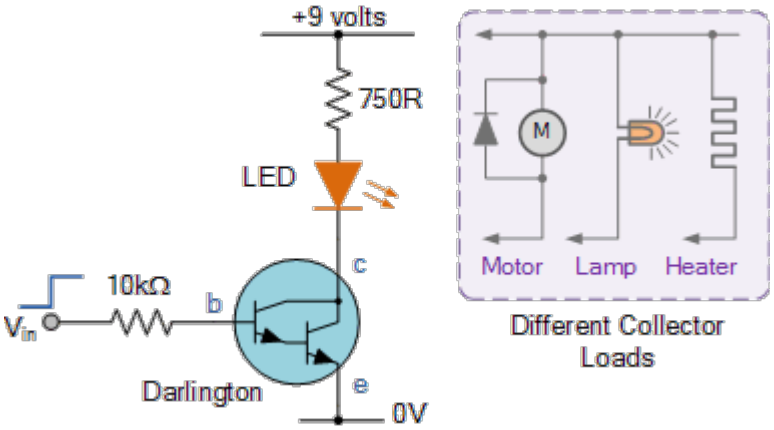
Then we can see that for two identical transistors, β^2 is used instead of β acting like one big transistor with a huge amount of gain. Darlington transistor pairs with current gains of more than a thousand with maximum collector currents of several amperes are easily available. For example: the NPN TIP120 and its PNP equivalent the TIP125.

The advantage of using an arrangement such as this, is that the switching transistor is much more sensitive as only a tiny base current is required to switch a much larger load current as the typical gain

of a Darlington configuration can be over 1,000 whereas normally a single transistor stage produces a gain of about 50 to 200.

Then we can see that a darlington pair with a gain of 1,000:1, could switch an output current of 1 ampere in the collector-emitter circuit with an input base current of just 1mA. This then makes darlington transistors ideal for interfacing with relays, lamps and motors to low power microcontroller, computer or logic controllers as shown.

Darlington Transistor Applications



The base of the Darlington transistor is sufficiently sensitive to respond to any small input current from a switch or directly from a TTL or 5V CMOS logic gate. The maximum collector current $I_{C(max)}$ for any Darlington pair is the same as that for the main switching transistor, TR2 so can be used to operate relays, DC motors, solenoids and lamps, etc.

One of the main disadvantage of a Darlington transistor pair is the minimum voltage drop between the base and emitter when fully saturated. Unlike a single transistor which has a saturated voltage drop of between 0.3v and 0.7v when fully-ON, a Darlington device has twice the base-emitter voltage drop (1.2 V instead of 0.6 V) as the base-emitter voltage drop is the sum of the base-emitter diode drops of the two individual transistors which can be between 0.6v to 1.5v depending on the current through the transistor.

This high base-emitter voltage drop means that the Darlington transistor can get hotter than a normal bipolar transistor for a given load current and therefore requires good heat sinking. Also, Darlington transistors have slower ON-OFF response times as it takes longer for the slave transistor TR1 to turn the master transistor TR2 either fully-ON or fully-OFF.

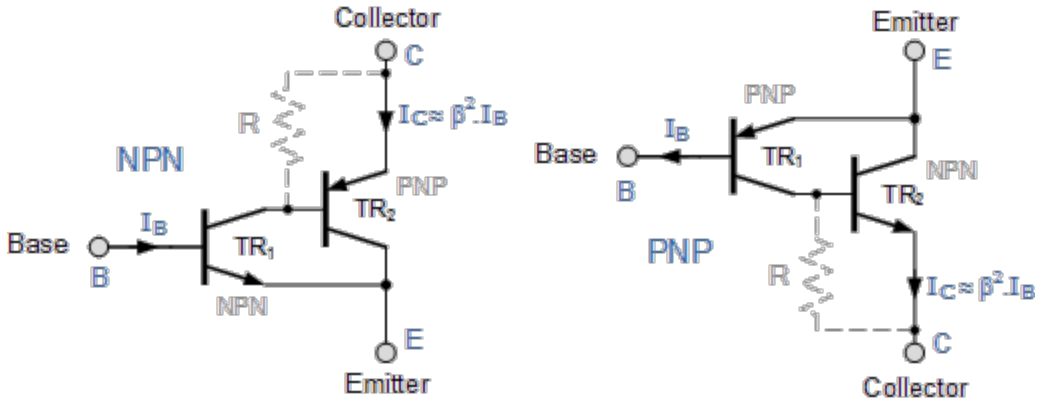
To overcome the slow response, increased voltage drop and thermal disadvantages of a standard **Darlington Transistor** device, complementary NPN and PNP transistors can be used in the same cascaded arrangement to produce another type of Darlington transistor called a **Sziklai Configuration**.

Sziklai Transistor Pair

The **Sziklai Darlington Pair**, named after its Hungarian inventor George Sziklai, is a complementary or compound Darlington device that consists of separate NPN and PNP complementary transistors connected together as shown below.

This cascaded combination of NPN and PNP transistors has the advantage that the Sziklai pair performs the same basic function of a Darlington pair except that it only requires 0.6v for it to turn-ON and like the standard Darlington configuration, the current gain is equal to β^2 for equally matched transistors or is given by the product of the two current gains for unmatched individual transistors.

Sziklai Darlington Transistor Configuration



We can see that the base-emitter voltage drop of the Sziklai device is equal to the diode drop of a single transistor in the signal path. However, the Sziklai configuration can not saturate to less than one whole diode drop, i.e. 0.7v instead of the usual 0.2v.

Also, as with the Darlington pair, the Sziklai pair have slower response times than a single transistor. Sziklai pair complementary transistors are commonly used in push-pull and class AB audio amplifier output stages allowing for one polarity of output transistor only. Both the Darlington and Sziklai transistor pairs are available in both NPN and PNP configurations.

Darlington Transistor IC's

In most electronics applications it is sufficient for the controlling circuit to switch a DC output voltage or current "ON" or "OFF" directly as some output devices such as LED's or displays only require a few milliamps to operate at low DC voltages and can therefore be driven directly by the output of a standard logic gate.

However as we have seen above, sometimes more power is required to operate the output device such as a DC motor than can be supplied by an ordinary logic gate or micro-controller. If the digital logic device cannot supply sufficient current then additional circuitry will be required to drive the device.

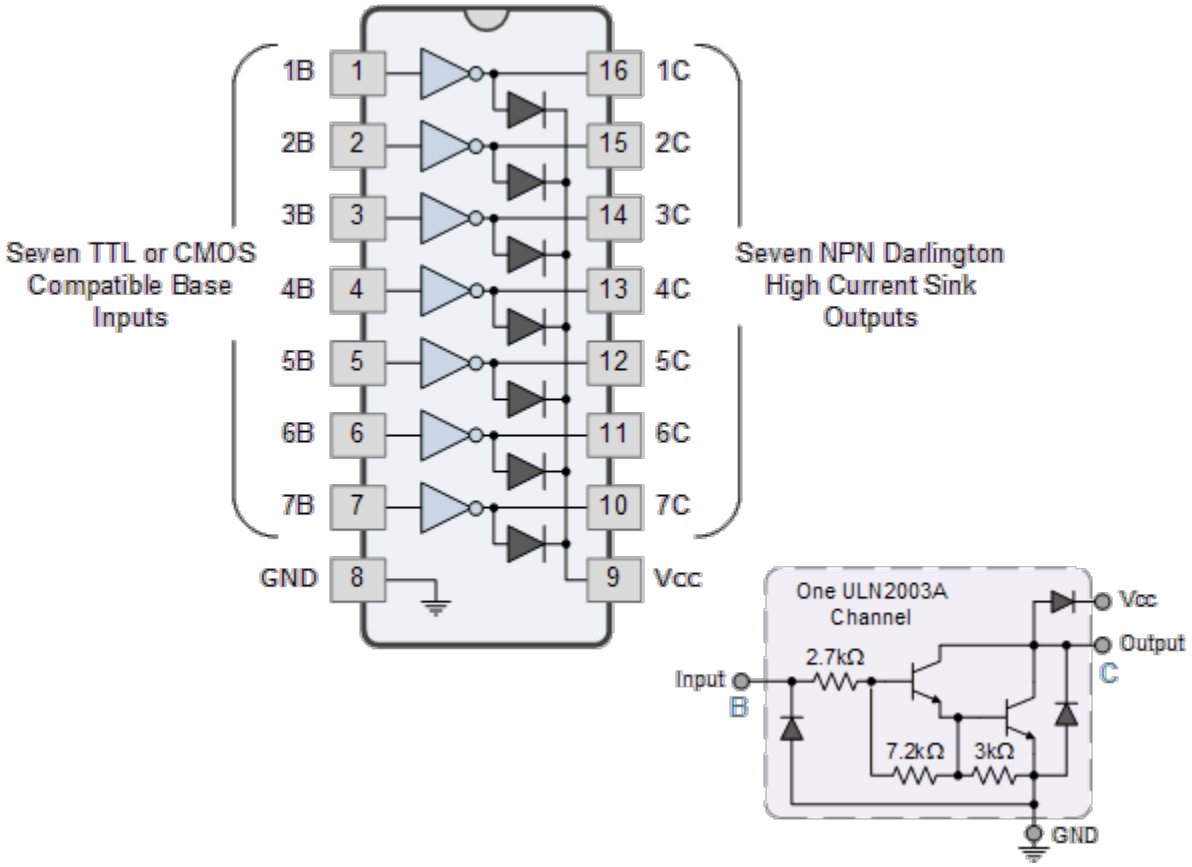
One such commonly used Darlington transistor chip is the **ULN2003** array. The family of darlington arrays consist of the ULN2002A, ULN2003A and the ULN2004A which are all high voltage, high current darlington arrays each containing seven open collector darlington pairs within a single IC package.

Each channel of the array is rated at 500mA and can withstand peak currents of up to 600mA making it ideal for controlling small motors or lamps or the gates and bases of high power semiconductors. Additional suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify the connections and board layout.

The ULN2003A Darlington Transistor Array

The ULN2003A is a inexpensive unipolar darlington transistor array with high efficiency and low power consumption making it useful for driving a wide range of loads including solenoids, relays DC Motor's and LED displays or filament lamps. The ULN2003A contains seven darlington transistor pairs each with an input pin on the left and an output pin opposite it on the right as shown.

ULN2003A Darlington Transistor Array



The ULN2003A Darlington driver has an extremely high input impedance and current gain which can be driven directly from either a TTL or +5V CMOS logic gate. For +15V CMOS logic use the ULN2004A and for higher switching voltages up to 100V it is better to use the SN75468 Darlington array.

When an input (pins 1 to 7) is driven "HIGH" the corresponding output will switch "LOW" sinking current. Likewise, when the input is driven "LOW" the corresponding output switches to a high impedance state. This high impedance "OFF" state blocks load current and reduces leakage current through the device improving efficiency.

Pin 8, (GND) is connected to the loads ground or 0 volts, while pin 9 (Vcc) connects to the loads supply. Then any load needs to be connected between +Vcc and an output pin, pins 10 to 16. For inductive loads such as motors, relays and solenoids, etc, pin 9 should always be connected to Vcc.

The ULN2003A is capable of switching 500mA (0.5A) per channel but if more switching current capability is required then both the Darlington pairs inputs and outputs can be paralleled together for higher current capability. For example, input pins 1 and 2 connected together and output pins 16 and 15 connected together to switch the load.

Darlington Transistor Summary

The Darlington Transistor is a high power semiconductor device with individual current and voltage ratings many times higher than a conventional small signal junction transistors.

The DC current gain values for standard high power NPN or PNP transistors are relatively low, as low as 20 or even less, compared to small signal switching transistors. This means that large base currents are required to switch a given load.

The Darlington arrangement uses two transistors back to back, one of which is the main current carrying transistor, while the other being a much smaller “switching” transistor provides the base current to drive the main transistor. As a result, a smaller base current can be used to switch a much larger load current as the DC current gains of the two transistors are multiplied together. Then the two transistor combination can be regarded as one single transistor with a very high value of β and consequently a high input resistance.

As well as standard PNP and NPN Darlington transistor pairs, complementary Sziklai Darlington transistors are also available which consist of separate matching NPN and PNP complementary transistors connected together within the same Darlington pair to improve efficiency.

Also Darlington arrays such as the ULN2003A are available which allow high power or inductive loads such as lamps, solenoids and motors to be safely driven by microprocessor and micro-controller devices in robotic and mechatronic type applications.

https://www.electronics-tutorials.ws/transistor/fet-current-source.html

FET Current Source

FET constant current sources use JFETs and MOSFETs to deliver a load current which remains constant despite changes in load resistance or supply voltage.

An **FET Current Source** is a type of active circuit which uses a *Field Effect Transistor* to supply a constant amount of current to a circuit. But why would you want a constant current? *Constant current sources* and current sinks, (a current sink is the reverse of a current source) are a very simple way of forming biasing circuits or voltage references with a constant value of current, for example, 100uA, 1mA or 20mA using just a single FET and resistor.

Constant current sources are commonly used in capacitor charging circuits for accurate timing purposes or in rechargeable battery charging applications, as well as linear LED circuits for driving strings of LED's at a constant brightness.

Resistive voltage references can also be formed using constant current sources, because if you know the value of the resistance and the current flowing through it is constant and steady, then you can simply use Ohm's law to find the voltage drop.

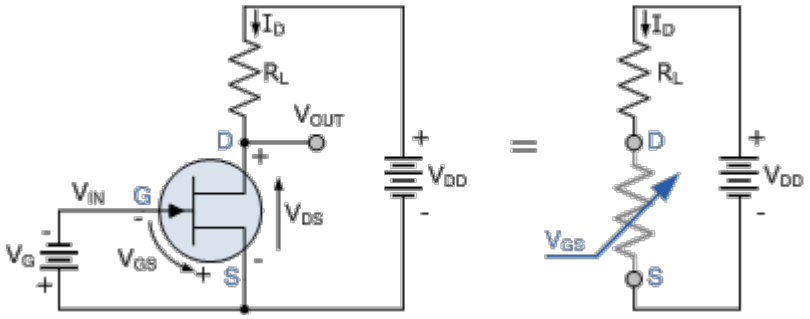
However, the key to creating an accurate and reliable FET based constant current source depends on using low transconductance FET's as well as precision resistor values to convert the current into a precise and stable voltage.

Field-effect transistors are commonly used to create a current source with Junction-FET's (JFET's) and Metal-oxide Semiconductor MOSFET's already being used in low current-source applications. In its simplest form, the JFET can be used as a voltage-controlled resistor where a small gate voltage controls the conduction of its channel.

Biasing the Junction FET

We saw in our tutorial about JFET's that JFET's are depletion devices and that the N-channel JFET is a "normally-ON" device, until the gate-to-source voltage (V_{GS}) becomes negative enough to turn it "OFF". The P-channel JFET which is also a "normally-ON" depletion device requires the gate voltage to become positive enough to turn it "OFF".

N-channel JFET Biasing



The image shows the standard arrangement and connections for a common source configured N-channel JFET with normal biasing when used in its active region. Here the gate-source voltage V_{GS} is equal to the gate supply, or input voltage V_G which sets the reverse bias between the gate and the source, while V_{DD} provides the drain-to-source voltage and current flow from the supply from drain to source. This current entering the JFET drain terminal is labelled I_D.

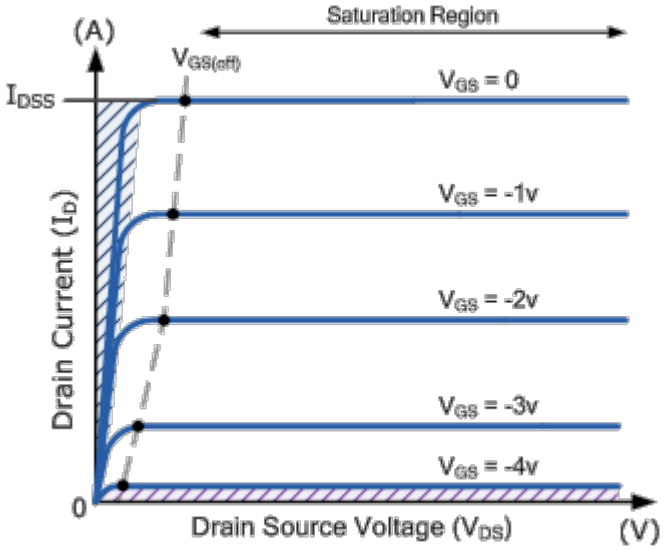
The drain-source voltage V_{DS} is the JFET's forward voltage drop and is a function of the drain current, I_D for different gate-source values of V_{GS}. When V_{DS} is at its minimum value, the JFET's conductive channel is fully open and I_D is at its maximum value which is called the drain-to-source saturation current $I_{D(sat)}$ or simply I_{DSS}.

When V_{DS} is at its maximum value, the JFET's conductive channel is fully closed, (pinched-off) so I_D reduces to zero with the drain-to-source voltage, V_{DS} being equal to the drain supply voltage V_{DD}. The gate voltage, V_{GS} at which the JFET's channel stops conducting is referred to as the gate cut-off voltage $V_{GS(off)}$.

This common source biasing arrangement of the N-channel JFET determines the steady state operation of the JFET in the absence of any input signal, V_{IN} as V_{GS} and I_D are steady state quantities, that is the quiescent state of the JFET.

Thus for a common-source JFET, the gate-source voltage V_{GS} controls how much current will flow through the JFET's conductive channel between the drain and source making the JFET a voltage-controlled device because its input voltage controls its channel current. As a result we can develop a set of output characteristic curves by plotting I_D versus V_{GS} for any given JFET device.

N-channel JFET Output Characteristic

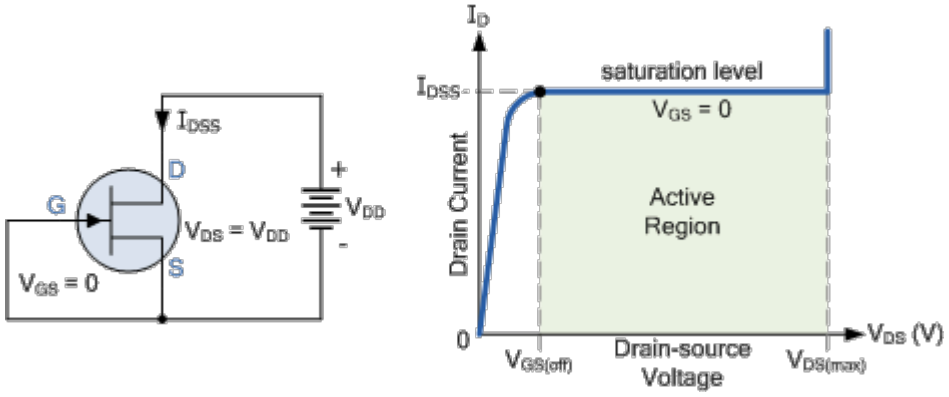


The JFET as a Constant Current Source

Then we could use this as the n-channel JFET is a normally-ON device and if V_{GS} is sufficiently negative enough, the drain-source conductive channel closes (cut-off) and the drain current reduces to zero. For the n-channel JFET, the closing of the conductive channel between drain and source is caused by the widening of the p-type depletion region around the gate until it completely closes the channel. N-type depletion regions close the channel for a p-channel JFET.

So by setting the gate-source voltage to some pre-determined fixed negative value, we can cause the JFET to conduct current through its channel at a certain value between zero amperes and I_{DSS} respectively making it an ideal FET current source. Consider the circuit below.

JFET Zero-voltage Biasing



We saw that the JFET's output characteristics curves are a plot of ID versus V_{GS} for a constant V_{DS}. But we also noticed that the JFET's curves do not change very much with large changes in V_{DS}, and this parameter can be very useful in establishing a fixed operating point of the conductive channel.

The simplest constant FET current source is with the JFET's gate terminal shorted to its source terminal as shown, the JFET's conductive channel is open so the flow of current through it will be close to its maximum I_{DSS} value due to the JFET being operated in its saturated current region.

However, the operation and performance of such a constant current configuration is fairly poor as the JFET is constantly in full conduction with the I_{DSS} current value depending completely on device type.

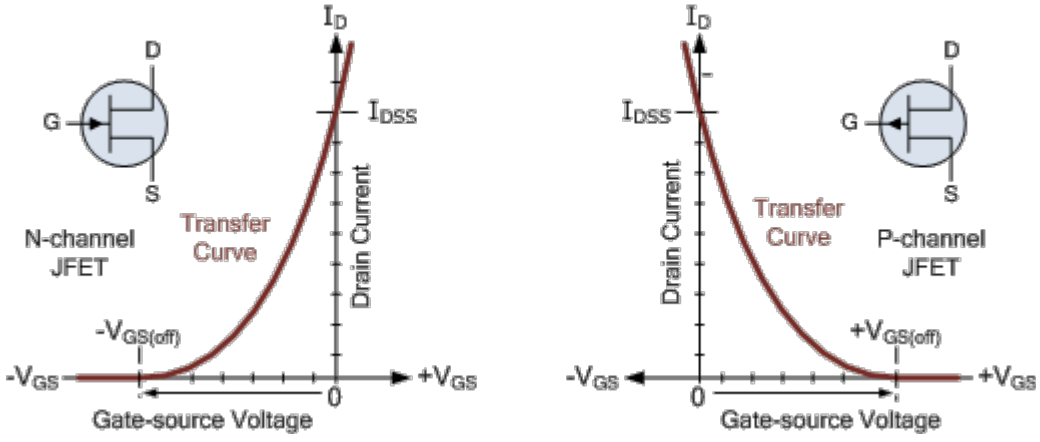
For example, the 2N36xx or the 2N43xx n-channel JFET series is only a few mill-amperes (mA), whereas the larger n-channel J1xx or PN4xxx series can be several ten's of milli-amperes. Also note that I_{DSS} will vary alot between devices of the same part number as manufacturers quote on their data sheets, minimum and maximum values of this zero gate voltage drain current, I_{DSS}.

Another point to note is that an FET is basically a voltage-controlled resistor whose conductive channel has a resistive value in series with the drain and source terminals. This channel resistance is called R_{DS}. As we have seen, when $V_{GS} = 0$, maximum drain-to-source current flows, therefore the JFET's channel resistance, R_{DS} must be at its minimum, and this is true.

However, the channel resistance is not completely zero but at some low ohmic value defined by the manufacturing geometry of the FET and which can be as high as 50 or so Ohms. When an FET is conducting, this channel resistance is commonly known as $R_{DS(ON)}$ and is at its minimum resistive value when $V_{GS} = 0$. Thus a high $R_{DS(ON)}$ value results in a low I_{DSS} and vice versa.

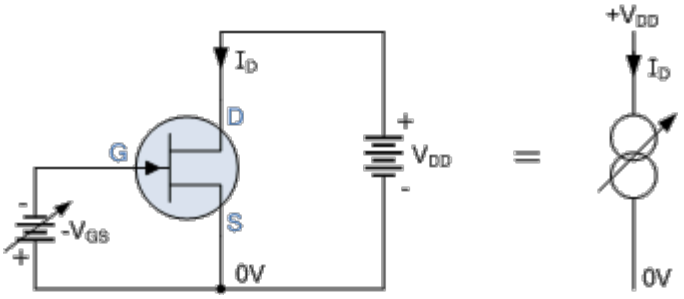
So a JFET can be biased to operate as an FET current source device at any current value below its saturation current, I_{DSS} when V_{GS} equals zero volts. When V_{GS} is at its $V_{GS(off)}$ cut-off voltage level there will be zero drain current, ($I_D = 0$) as the channel is closed. Thus the channels drain current, I_D will always flow as long as the JFET device is operated within its active region as shown.

JFET Transfer Curve



Note that for a P-channel JFET, the $V_{GS(off)}$ cut-off voltage will be a positive voltage but its saturation current, I_{DSS} obtained when V_{GS} equals zero volts will be the same as for an N-channel device. Also notice that the transfer curve is nonlinear because the drain current is increasing faster through the opening channel as V_{GS} approaches zero volts.

JFET Negative-voltage Biasing



We remember that the JFET is a depletion mode device which is always “ON”, so requires a negative gate voltage for N-channel JFET’s, and a positive gate voltage for P-channel JFET’s to turn them “OFF”. Biasing an N-channel JFET with a positive voltage, or biasing a P-channel JFET with a negative voltage will open the conductive channel even further forcing the channel current, I_D beyond I_{DSS}.

But if we use the characteristic curves of I_D against V_{GS}, we can set V_{GS} to some negative voltage level, say -1V, -2V or -3V too create a fixed JFET constant current source of whatever current level we require between zero and I_{DSS}.

But for a more accurate constant current source with improved regulation, it is better to bias the JFET at about 10% to 50% of its maximum I_{DSS} value. This also helps with I^2*R power losses through the resistive channel and therefore reduced heating effect.

So we can see that by biasing a JFET’s gate terminal with some negative voltage value, or a positive voltage for a P-channel JFET, we can establish its operating point allowing the channel to conduct and pass a certain value of drain current, I_D. For different values of V_{GS}, a JFET drain current I_D can be expressed mathematically as being:

JFET Drain Current Equation

$$I_D \cong I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

FET Constant Current Source Example No1

The manufacturers datasheet for a J107 N-channel switching JFET shows that it has an I_{DSS} of 40mA when V_{GS} = 0, and a maximum $V_{GS(off)}$ value of -6.0 volts. Using these declared values, calculate the JFET's drain current value when, V_{GS} = 0, V_{GS} = -2 volts, and when V_{GS} = -5 volts. Also show the J107's transfer characteristic curve.

1). When V_{GS} = 0V

When V_{GS} = 0V the conductive channel is open and maximum drain current flows.

Thus $I_D = I_{DSS}$ = 40mA.

2). When V_{GS} = -2V

$$I_D \cong I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2 = 40mA\left[1 - \frac{-2}{-6}\right]^2$$

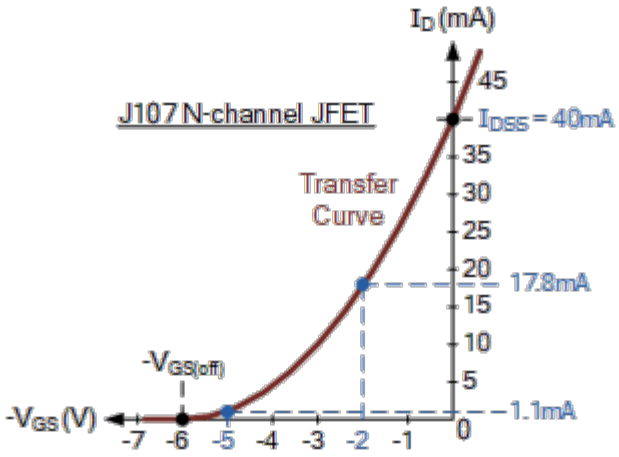
$$I_D = 0.04(1-0.333)^2 = 0.04(0.444) = 17.78mA$$

3). When V_{GS} = -5V

$$I_D \cong I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2 = 40mA\left[1 - \frac{-5}{-6}\right]^2$$

$$I_D = 0.04(1-0.833)^2 = 0.04(0.0278) = 1.11mA$$

4). J107 Transfer Characteristic Curve



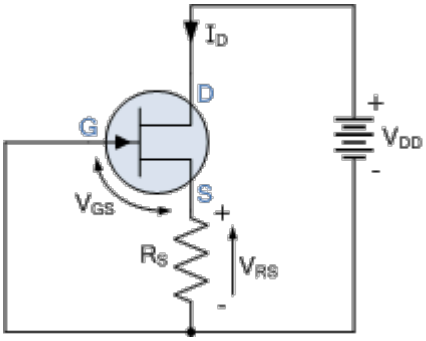
Thus we can see that as the gate-source voltage, V_{GS} approaches the gate-source cut-off voltage, $V_{GS(off)}$ the drain current, I_D decreases. In this simple example, we calculated the drain current at two points, but calculating using additional values of V_{GS} between zero and cut-off would give us a more accurate shape of the curve.

JFET Current Source

A JFET can be made to operate as a voltage controlled constant current source whenever its gate-source junction is reverse biased, and for an N-channel device we need a $-V_{GS}$ and for a P-channel device we need a $+V_{GS}$. The problem here is that the JFET requires two separate voltage supplies, one for VDD and another for V_{GS}.

However if we place a resistor between the source and ground (0 volts), we can achieve the necessary V_{GS} self-biasing arrangement for the JFET to operate as a constant current source using only the VDD supply voltage. Consider the circuit below.

JFET Current Source



At first glance you may think that this configuration looks very similar to a JFET common drain (source follower) circuit we saw in the **JFET tutorial**.

However the difference this time is that while the FET's gate terminal is still tied directly to ground ($V_G = 0$), the source terminal is at some voltage level above zero voltage ground due to the voltage drop across the source resistor, R_S.

Therefore, with a channel current flowing through the external source resistor, the gate-to-source voltage of the JFET will be less than (more negative than) zero ($V_{GS} < 0$).

The external source resistor, R_S provides a feedback voltage which is used to self-bias the JFET's gate terminal keeping the drain current constant through the channel despite any changes in the drain-source voltage. Thus the only voltage source we need is the supply voltage VDD to provide the drain current and bias.

So the JFET uses the voltage drop across source resistor (V_{RS}) to set the gate bias voltage V_{GS} and therefore the channel current as we have seen above. Thus, increasing the resistive value of R_S will decrease the channels drain current I_D, and vice versa. But if we wanted to construct a JFET constant current source circuit, what would be a suitable value for this external source resistor, R_S.

Manufacturers data sheets for a particular N-channel JFET will give us the values of $V_{GS(off)}$ and I_{DSS}. Knowing the values of these two parameters we can transpose the above JFET equation for the drain current, I_D to find the value of V_{GS} for any given value of drain current, I_D between zero and I_{DSS} as shown.

JFET Gate to Source Voltage Equation

$$I_D = I_{DSS}\left[1 - \frac{-V_{GS}}{-V_{GS(off)}}\right]^2$$

$$\therefore V_{GS} = -V_{GS(off)}\left[1 - \sqrt{\frac{I_D}{I_{DSS}}}\right]$$

Having found the gate-to-source voltage required for a given drain current, the value of the source biasing resitor value required is found by simply using Ohm's law, as R = V/I. Thus:

JFET Source Resistor Equation

$$R_S = \frac{V_{GS}}{I_D} \ (\Omega\text{'s})$$

FET Constant Current Source Example No2

Using the J107 N-channel JFET device from above which has an I_{DSS} of 40mA when $V_{GS} = 0$, and a maximum $V_{GS(off)}$ value of -6.0 volts. Calculate the value of the external source resistor required to produce a constant channel current of 20mA and again for constant current of 5mA.

1). V_{GS} for $I_D = 20mA$

$$V_{GS} = -V_{GS(off)}\left[1 - \sqrt{\frac{I_D}{I_{DSS}}}\right]$$

$$V_{GS} = -6\left[1 - \sqrt{\frac{20\,mA}{40\,mA}}\right] = -6(1 - 0.7071)$$

$$\therefore V_{GS} = -6 \times 0.2929 = -1.75\,volts$$

$$R_{DS} = \frac{V_{GS}}{I_D} = \frac{1.75V}{20mA} = \frac{1.75}{0.02} = 87.5\,\Omega$$

2). V_{GS} for I_D = 5mA

$$V_{GS} = -V_{GS(off)}\left[1 - \sqrt{\frac{I_D}{I_{DSS}}}\right]$$

$$V_{GS} = -6\left[1 - \sqrt{\frac{5mA}{40mA}}\right] = -6(1 - 0.3536)$$

$$\therefore V_{GS} = -6 \times 0.6464 = -3.88 \text{ volts}$$

$$R_{DS} = \frac{V_{GS}}{I_D} = \frac{3.88V}{5mA} = \frac{3.88}{0.005} = 776\,\Omega$$

Thus when $V_{GS(off)}$ and I_{DSS} are both known, we can use the above equations to find the source resistance required to bias the gate voltage for a particular drain current, and in our simple example this was 87.5Ω at 20mA, and 776Ω at 5mA. So the addition of an external source resistor allows for the adjustment of the current source output.

If we was to replace the fixed value resistors with a potentiometer we can make the JFET constant current source fully adjustable. For example, we could replace the two source resistors in the above example with one 1kΩ potentiometer, or trimmer. Also as well as being fully adjustable, this JFET constant current source circuits drain current will remain constant even with changes in V_{DS}.

FET Constant Current Source Example No3

An N-channel JFET is required to vary the brightness of a 5mm round red LED load between 8mA and 15mA. If the JFET constant current source circuit is fed from a 15 volt DC supply, calculate the JFET's source resistance required to illuminated the LED between minumum and maximum brightness when the switching JFET has a maximum $V_{GS(off)}$ value of -4.0 volts and an I_{DSS} of 20mA when V_{GS} = 0. Draw the circuit diagram.

1). V_{GS} for I_D = 8mA

$$V_{GS} = -V_{GS(off)}\left[1-\sqrt{\frac{I_D}{I_{DSS}}}\right]$$

$$V_{GS} = -4\left[1-\sqrt{\frac{8mA}{20mA}}\right] = -4(1-0.6325)$$

$$V_{GS}\,(8mA) = -4\times 0.3675 = -1.47\,\text{volts}$$

$$\therefore R_{DS(8mA)} = \frac{V_{GS}}{I_D} = \frac{1.47V}{8mA} = \frac{1.47}{0.008} = 184\Omega$$

2). V_{GS} for I_D = 15mA

$$V_{GS} = -V_{GS(off)}\left[1 - \sqrt{\frac{I_D}{I_{DSS}}}\right]$$

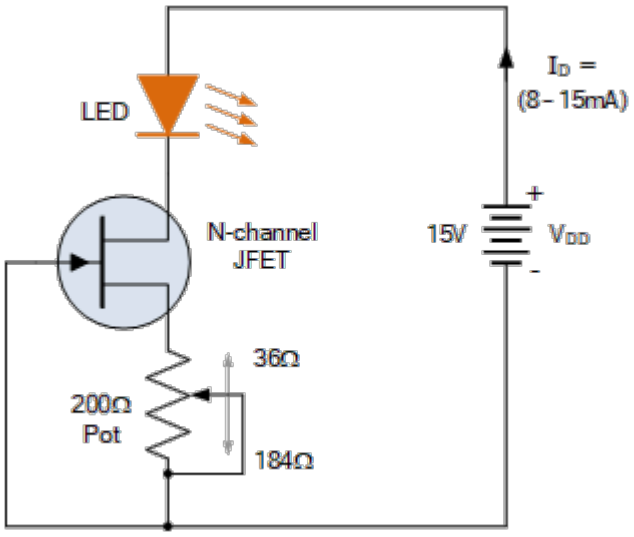
$$V_{GS} = -4\left[1 - \sqrt{\frac{15mA}{20mA}}\right] = -4(1 - 0.866)$$

$$V_{GS}(15mA) = -4 \times 0.134 = -0.536\,volts$$

$$\therefore R_{DS(15mA)} = \frac{V_{GS}}{I_D} = \frac{0.536V}{15mA} = \frac{0.536}{0.015} = 36\Omega$$

Then we would need an external potentiometer capable of varying its resistance between 36Ω and 184Ω. The nearest preferred potentiometer value would be 200Ω.

Adjustable JFET Constant Current Source



A potentiometer or trimmer used instead of a fixed value source resistance, R_S would allow us to vary or fine-tune the current flowing through JFET's conductive channel.

However, in order to ensure a good current regulation through the FET device, and therefore a more stable current flow, it would be better to limit the maximum channel current flowing through the LED (15mA in this example) to between 10% and 50% of the JFETs I_{DSS} value.

Creating constant current sources using MOSFET's allows for much greater channel currents and better current regulation, and unlike JFET's which are only available as normally-on depletion mode devices, MOSFET's are available in both depletion-mode (normally-on) and enhancement-mode (normally-off) devices as either P-channel or N-channel types allowing for a greater range of current source options.

FET Constant Current Source Summary

We have seen in this tutorial about the **FET Constant Current Source** that due to their channel resistance characteristics, field effect transistors can be used to supply a constant current to a load and find numerous applications in electronics circuits where it is required to supply a fixed current to a connected load.

Constant current circuits can be built using depletion mode FET's but also using BJT's (*bipolar junction transistors*), or a combination of these two devices. Remembering that the JFET is a voltage-controlled device, not a current-controlled device like the bipolar junction transistor.

One of the main characteristics of a Junction Field Effect Transistor, or JFET, is that because it is a depletion device, its conductive channel is always open so it requires a gate-to-source voltage, V_{GS} to turn it "OFF".

The $V_{GS(off)}$ voltage required for an N-channel JFET ranges from 0 volts, for full conduction of the channel, to some negative value, usually several volts, required to turn the JFET fully-OFF, thus closing the channel. So by biasing the JFET's gate terminal at some fixed value between zero and $V_{GS(off)}$, we can control the channels depletion layers width and therefore its resistive value, passing a fixed and constant amount of current. For a P-channel JFET, its $V_{GS(off)}$ value ranges from 0 volt for full channel conduction to some positive value of several volts for a particular V_{DS} value.

The regulation and tolerance of the constant current for a given JFET device is related to the amount of drain current, I_D passing through the channel. The lower the drain current through a particular devive, the better the regulation. Biasing a JFET at between about 10% to 50% of its maximum I_{DSS} value will improve the devices regulation and performance. This is achieved by connected an external resististance between the source and gate terminals.

A gate-to-source feedback resistor as shown above, provides the necessary self-biasing of the JFET allowing it to operate as a constant current source at any current level well below its saturation current, I_{DSS}. This external source resistance, R_S can of a fixed resistive value or variable using a potentiometer.

https://www.electronics-tutorials.ws/transistor/open-collector-outputs.html

Open Collector Outputs

Open Collector Outputs are very useful for switching incompatable loads but may require a pull-up or pull-down resistor to ensure the correct switching action.

Open Collector Outputs are increasingly common in digital chip design, operational amplifiers and micro-controller (Arduino) type applications, for either interfacing with other circuits or for driving high-current loads such as indicator lamps and relays which maybe incompatible with the electrical characteristics of the control circuit. But what does “open-collector” mean, and how can we use it within our circuit designs.

We know from our previous tutorials that a *bipolar junction transistor*, whether it is an NPN type or a PNP type, is a 3-terminal device. These three terminals are identified as being the *Emitter*, the *Base*, and the *Collector*.

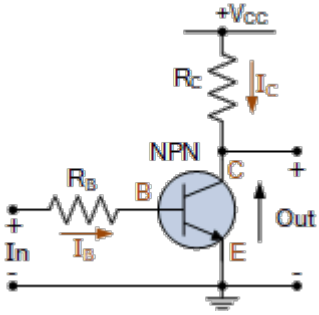
We can use bipolar transistors to operate as either an Amplifier, that is the output signal has a greater amplitude than the input signal, or more commonly, as a solid state “ON/OFF” type electronic switch.

Since the Bipolar Junction Transistor (BJT) is a 3-terminal device, it can be configured and operated in one of three different switching modes. These being *Common Base* (CB), *Common Emitter* (CE), and *Common Collector* (CC).

The “Common Emitter” configuration is by far the most common transistor configuration when used for amplification (active region) or switching (cut-off or saturation regions). So this is the transistor configuration we will look at here in this tutorial about *open collector outputs*.

Consider the standard common emitter amplifier configuration shown below.

Common Emitter Configuration



Here in this single stage common emitter configuraton, a resistance is connected between the collector terminal of the transistor and the positive supply rail, V_{CC}. The input signal is applied between the transistors base and emitter junction, with the emitter’s terminal connected directly to ground. Hence the descriptive term “common emitter”, (CE).

The bias current, IB required to turn “ON” the transistor is fed directly into the base of the NPN transistor via base resistor RB with the output signal, which is 180º-phase inverted relative to the input signal, taken from between the collector and emitter terminals.

This allows the transistors collector current to be controlled between zero (cut-off) and some maximum value (saturation). This is the standard arrangement for the common emitter configuration, either biased to operate as a class-A amplifier or as a logical ON/OFF switch.

The problem here is that both the transistor and its collector load resistance are linked together to one common supply voltage. The collector resistor, R_C is used here to allow the collectors voltage, V_C to change value in response to an input signal applied to the transistors base terminal, thus allowing the transistor to produce an amplified output signal. As without R_C the voltage on the collector terminal would always be equal to supply voltage.

As mentioned earlier, a bipolar junction transistor can be operated between it cut-off and saturation regions when V_{BE} is much less than 0.7 volts (zero base current), or when it is much greater than 0.7 volts (maximum base current) respectively.

In this way the NPN bipolar transistor can be used as an electronic switch performing the operation of inversion, because when the transitor is “OFF”, its collector terminal, and thus V_{CE}, is “HIGH” at VCC level, and when it is “ON”, (conducting) the output taken across V_{CE} will be “LOW”, which is the opposite switching conditions if we want to control a relay, solenoid or lamp, for example.

One way to overcome this inversion of the transistors switching state is to remove the collector resistor, R_C completely and have the transistors collector terminal available to be connected to some external load. This type of set-up produces what is commonly called an open collector output configuration.

NPN Open Collector Output

When an NPN bipolar transistor is operated in an *Open Collector* (OC or o/c) configuration, it is operated between being fully-ON, or fully-OFF, thus acting as an electronic solid-state switch.

That is with no base bias voltage applied, the transistor will be fully-OFF, and when a suitable base bias voltage is applied, the transistor will be fully-ON. So when the transistor is operated between its cut-off (OFF) and saturation regions (ON), it does not operate as an amplifying device as it would do if controlled in its active region.

The switching of the transistor between cut-off and saturation allows for the open collector outputs the capability of driving external connected loads which require higher voltages and/or currents than allowed by the previous common emitter configuration. The only limit is the maximum allowable voltage and/or current values of the actual switching transistor.

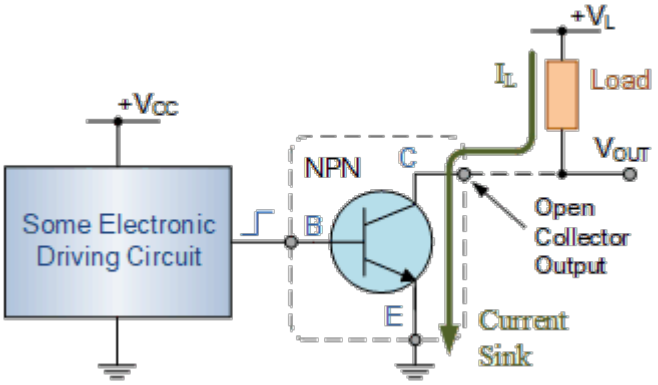
Then the advantage of open collector outputs is that any output switching voltage can be obtained simply by pulling up the collector terminal to the single positive supply as before, or by powering the load from a separate supply rail. For example, you might want to drive a low-current lamp or relay that requires a +12 volt supply from the output of a +5 volt logic gate or Arduino, Raspberry-Pi output pin.

However, the disadvantage is that when using open collector outputs to switch digital signals, gates, or inputs of electronic circuits, an externally connected pull-up resistor is generally required as the collector terminal of the transistor has no output drive capacity. This is because for an NPN transistor, it can only pull the output LOW to ground (0V) when energised, it cannot return or push it back HIGH again when it is in the OFF state.

When de-energised the output must be pulled HIGH again by the use of an external “pull-up resistor” connected between its collector terminal and the supply voltage to stop the open collector terminal from floating about between HIGH (+V) and LOW (0V) when the transistor is OFF.

The value of this pull-up resistor isn’t critical and will depend somewhat on the load current value required at the output, with resistive values ranging from of a few hundred to a few thousand ohms being typical. Thus for an NPN bipolar transistor, its open-collector outputs are *current sinking* outputs only.

Open Collector Transistor Circuit



The above image shows the typical arrangement of an open collector switching circuit which is useful for driving electromechanical type devices as well as many other switching applications. The NPN transistors base driving circuit could be any suitable analogue or digital circuit. The transistor’s collector is connected to the load to be switched, with the transistors emitter terminal connected directly to ground.

For an NPN-type open collector output, when a control signal is applied to the base of the transistor it turns ON, and the output, which is connected to the collector terminal, is pulled down to ground potential through the now conducting transistor junctions energising the connected load and turning it ON. Thus the transistor switches and passes the load current, I_L which is determined using Ohm’s Law as:

Load Current, I_L = Voltage across load / Resistance of load

When the transistors positive base drive is removed (OFF), the NPN transistor stops conducting and the load, which could be a relay coil, solenoid, small dc motor, lamp, etc. is de-energised and also turns OFF. Then the output transistor can be used to control an externally connected load as the current-sink switching action of the NPN transistors open-collector acts as either an open circuit (OFF) or a short circuit (ON).

The advantage here is that the collector load does not need to be connected to the same voltage potential as the transistors driving circuit, as it could use a lower or higher voltage potential, for example 12 volts, or 30 volts DC.

Also the same simple digital or analogue circuit can be used to switch many different loads by simply changing the output transistor. For example, 6 VDC at 10mA (2N3904 transistor), or 40 VDC at 3 amperes (2N3506 transistor), or even use an open collector Darlington transistor.

Open Collector Output Example No1

A +5 volt digital output pin from an Arduino board is required to drive an electromechanical relay as part of a school project. If the relay's coil is rated at 12 VDC, 100Ω and an NPN transistor used in its open collector configuration has a DC current gain (Beta) value of 50, calculate the base resistor required to operate the relay coil.

The current through the coil can be calculated using Ohm's law as: I = V/R

$$I_C = \frac{V_L}{R_L} = \frac{12}{100} = 0.12\,A \text{ or } 120\,mA$$

$$\beta = \frac{I_C}{I_B} \quad \therefore I_B = \frac{I_C}{\beta}$$

$$I_B = \frac{I_C}{\beta} = \frac{0.12}{50} = 2.4\,mA$$

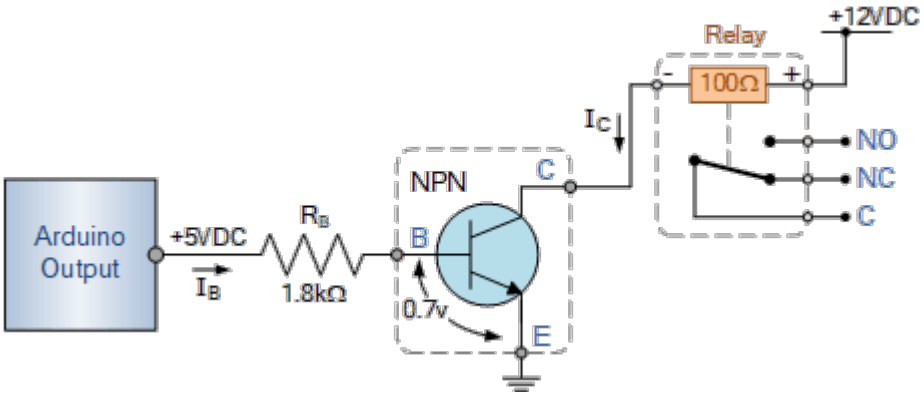
Thus for an NPN transistor with a DC current gain of 50, a base current of 2.4mA is required, ignoring the collector-emitter saturation voltage, ($V_{CE(sat)}$) of about 0.2 volts. Recall that a transistors DC current gain is its specification of how much base current is required to produce the resulting collector current.

The voltage drop across the base-emitter junction (V_{BE}) when the transistor is fully ON will be 0.7 volts. Thus the value of base resistor, R_B required is calculated as:

$$R_B = \frac{V_{RB}}{I_B} = \frac{(5v - 0.7v)}{0.0024} = 1792\Omega \text{ or } 1.8k\Omega$$

Then the open-collector transistor circuit would be:

Open Collector Circuit



While the NPN open collector transistor circuit produces a “current-sinking” output, that is the NPN transistors open collector terminal will sink the current to ground (0V), a PNP-type transistor can also be used in an open collector configuration to produce what is called a “current-sourcing” output.

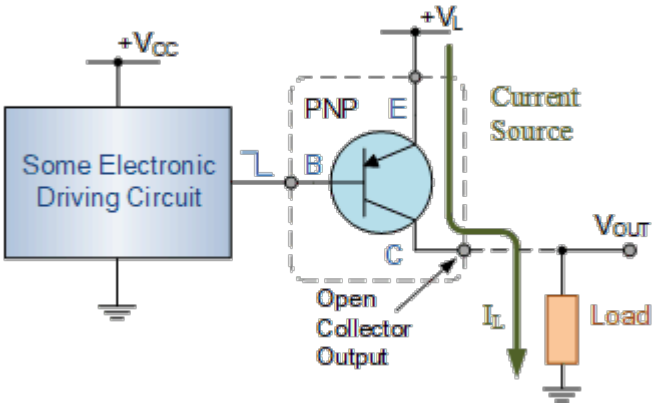
PNP Open Collector Output

We have seen above that the main characteristic of an open-collector output is that the load signal is actively “pulled down” to ground level by the switching action of the NPN bipolar transistor when fully ON, and passively pulled back up again when OFF producing a current sink output.

But we can create the opposite switching condition by using the open collector output of a PNP bipolar transistor to actively switch its output towards a voltage supply rail and use an externally connected “pull-down” resistor to passively pull the output low again when OFF.

For a PNP-type open collector output it is only possible for the transistor to switch the output HIGH to the supply rail, so its output terminal must be passively pulled “LOW” again by an externally connected “pull-down” resistor as shown.

Open Collector PNP Transistor Circuit



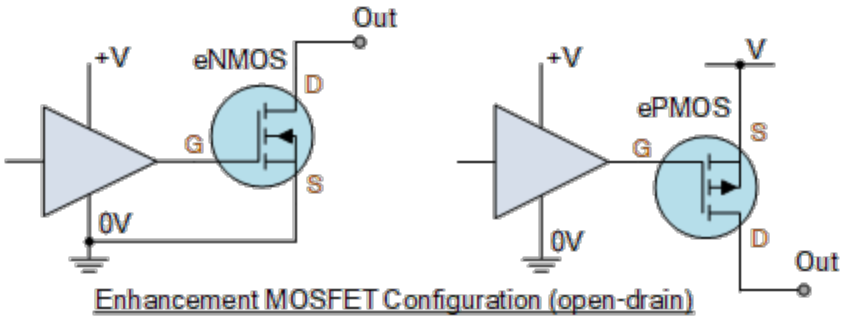
Then we can see that an NPN-type or a PNP-type open collector output configuration can only actively pull its output LOW to ground, or HIGH to a supply rail (depending on transistor type) when ON, but its collector terminal must be pulled up or down passively by the use of a pull-up or pull-down resistor connected to its output terminal if the connected load is not able to do this. The type of output transistor used, and therefore its switching action, produces either a *current sink* or a *current source* condition.

As well as using bipolar transistors in their open collector configuration, it is also possible to use n-channel and p-channel enhancement mode MOSFETs or IGBTs in their **open source** configuration.

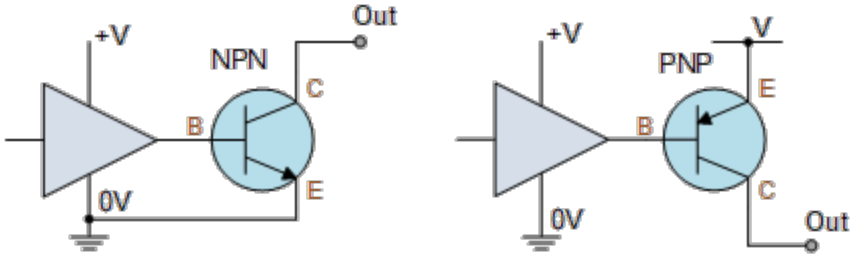
Unlike the bipolar junction transistor (BJT), which requires a base current to drive the transistor into saturation, the normally-open (enhancement) MOSFET requires a suitable voltage applied to its gate (G) terminal. The MOSFET’s source (S) terminal is connected directly to ground or the supply rail, while the open-drain (D) terminal is connected to the external load.

The use of MOSFETs (or IGBTs) as *open-drain*, (OD) devices follow the same requirements as for *open-collector* outputs, (OC) when drivng power loads, or loads connected to a higher voltage supply, in that the use of pull-up or pull-down resistors applies. The only difference being the MOSFETs channel thermal power rating and static voltage protection.

Open Drain Enhancement MOSFET Configuration



Enhancement MOSFET Configuration (open-drain)



Bipolar Transistor Configuration (open-collector)

Tutorial Summary

We have seen here in this tutorial about the **open collector output** that it can provide a current sink or current source output depending on the type of bipolar transistor, NPN-type or PNP-type, used.

When an NPN-type transistor is in its “ON” state, it will provide or “sink” a path to ground. When in the “OFF” state, its output terminal may float unless the open collector output is connected via a pull-up resistor to the positive supply voltage.

The reverse is also true of a PNP-type transistor. When it is in its “ON” state, it will supply or “source” a path from the supply rail. When in the “OFF” state, its output terminal may float unless the open-collector output is connected via a pull-down resistor to ground (0V).

The advantage of open collector outputs, or open drain outputs is that the load to be switched or controlled can be connected to a voltage supply which is independent, and/or different from the supply voltage used by the controlling circuit, and that they can “sink” or “source” an externally-supplied voltage depending upon whether its to ground, or source. The only limit is the maximum allowable voltage and current ratings of the output switching transistor or e-MOSFET.