# BOHAN YANG

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## EDUCATION

**University of Science and Technology of China (USTC)** Sept. 2020 – Current
**School of the Gifted Young (Honor School)** *Hefei, China*

- GPA: 4.07/4.30 Ranking: 1/29 CGPA: 93.19
- Major in physical electronics
- Interested in **Computer Architecture** and **Digital Chip Design**
- Admitted by Yan Jici Talent Class (Honor Class)
- EECS-Related course grades:
  Computer Programming A: 95(A+) Electronic Circuits: 99(A+) Digital Logic Circuits: 97(A+)
  Digital Integrated Circuits Design: 97(A+) Mathematical Analysis B2: 96(A+)
  Electromagnetism A: 100(A+) Probability Theory and Mathematical Statistics: 95(A+)
- English skills:
  TOEFL: 105 (R:30 L:26 S:23 W:26) CET-4: 648 CET-6: 587

## HONOURS AND AWARDS

**National Scholarship (Top 1%)** 2021
**First Prize of the 13th National College Students Mathematics Contest** 2021
**Yan Jici Talent Class Scholarship (Top 1%)** 2022
**Qiangwei Great Ambition Scholarship (Top 1%, the only awarded microelecrionics student)** 2022
**Alumni (Class of 1987) Innovation Scholarship** 2023

## RESEARCH EXPERIENCE

**Research Intern** Oct. 2022 – Current
IIIS, Tsinghua University *Advisor: Prof. Mingyu Gao*

- Explore dataflow optimization methods of the scalable spatial accelerator for dynamic neural networks
- Build a full-stack platform, from operator graph scheduler to chip-based dynamical data shuffling and partition in cluster and block level
- Simulate the design using the Gem5 simulator and build specific simobjects in C++

**Intern** Jul. 2022 – Sept. 2022
Polar Bear Tech

- As a member of the compiling research group, design convolution and transposing logic operators in c++ for the Qiming 940 accelerator
- Verify the logic correctness of operators by generating a large number of sampling cases
- Compose corresponding generation scripts and explore how to speed up the generation and reduce the occupation of disks while ensuring sample coverage level

**Research Intern** Apr. 2022 – Jun. 2022
School of Microelectronics, USTC *Advisor: Prof. Yi Kang*

- Implement operators on the accelerator platform developed by the research group in C++
- Optimize specific AI applications like AI video encoding algorithms for H.265 on this platform

## PROJECTS

**Digital chip design practice** Sept. 2022 – Feb. 2023

- Design an SOC in TSMC 180nm process and explore the whole chain from front-end architecture design to back-end layout generation
- Implement three parts of the SOC: 8-bit MIPS CPU, systolic array co-processor, and SRAM driver
- Manage to quickly iterate the design and simulate it to confirm the correctness of the function using the Synopsys EDAs

**Five-stage-pipelined RISC-V CPU design and SoC design** Apr. 2022 – Jun. 2022

- Manage to implement the design of a RISC-V SOC in verilog RTL level
- The SOC includes a classic five-stage pipeline CPU, UART driver and GPIO (switch and LED light) driver, etc
- Write assembly codes and compile it to do some software tasks like UART communication and LED light array show

## TEACHING

**Teaching Assistant** Sept. 2022 – Feb. 2023
USTC *Lecturer: Xuefei Bai*

- Answer the questions of freshman students in the process of learning C language, prepare corresponding exercises and participate in experiment design
- Review the submitted homework and cooperate with the lecture to complete the student assessment task

## SKILLS

- C++ / C / Python / Linux kernel / Assembly Language (X86 & RISCV & ARM) / Matlab / Gem5 / Verilog / FPGA development / Cadence & Synopsys EDATools / LaTeX / Markdown
- Interests: Go (10 years) / Football (6 years) / Guitar (8 years)
- Languages: Chinese–Mandarin (Native), English (Fluent)

## EXTRACURRICULAR PRACTICES

**Summer Course Outstanding Student (grade: 95 A+)** Peking University, 2022

**The fifth team of the USTC Counter-Strike tactics competition (As Captain)** USTC, 2021

**Team Final Four in USTC Angel Football Cup** USTC, 2020