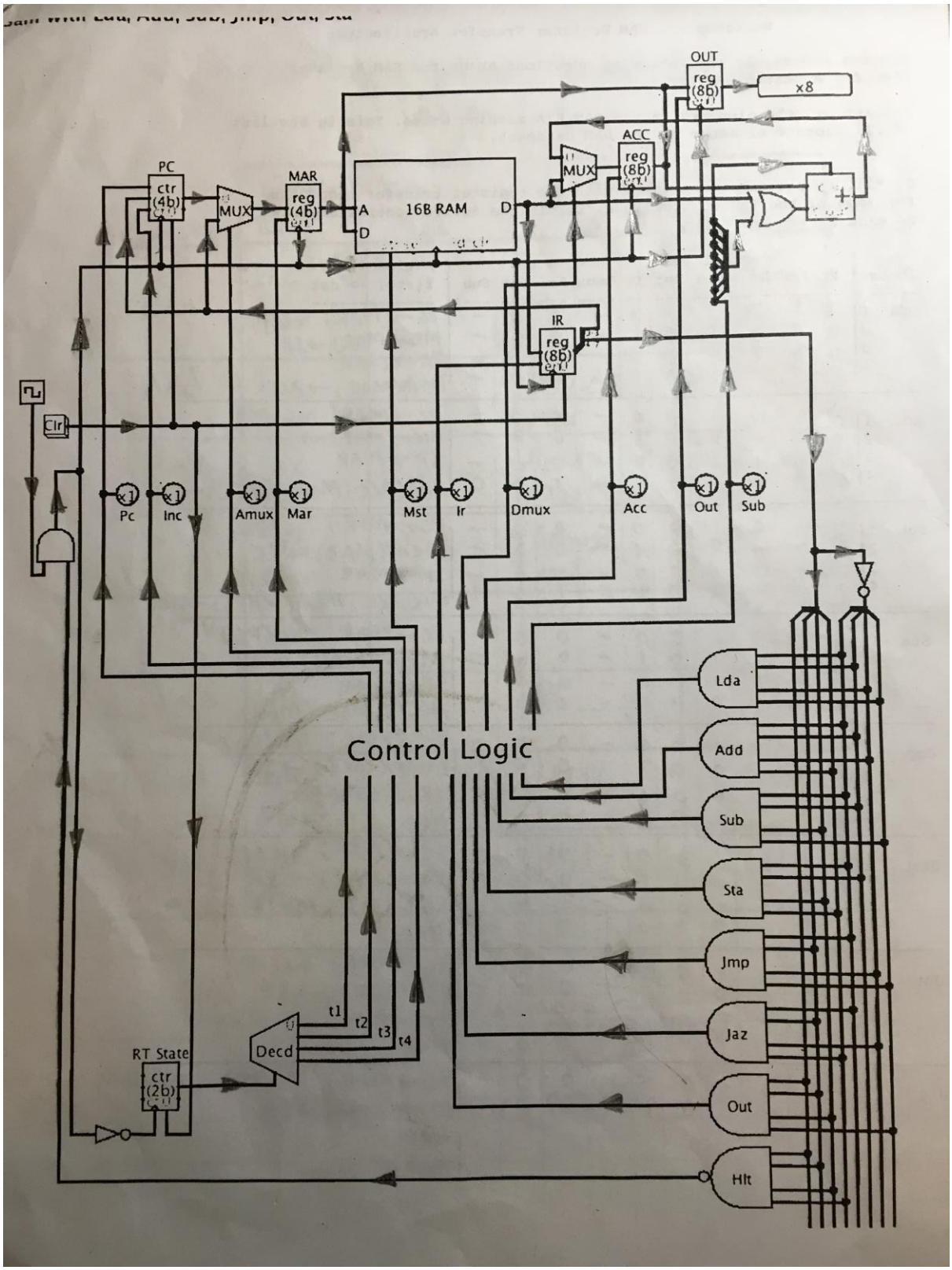
Workshop 2


OUT
reg (8b)
x8
ACC
reg (8b)
MUX
PC
ctr (4b)
MUX
MAR
reg (4b)
A
D
16B RAM
D
IR
reg (8b)
Clr
Pc
Inc
Amux
Mar
Mst
Ir
Dmux
Acc
Out
Sub
Control Logic
Lda
Add
Sub
Sta
Jmp
Jaz
Out
Hlt
t1
t2
t3
t4
Decd
RT State
ctr (2b)

Workshop 2 - SAM Register Transfer Architecture

Discuss and answer the following questions about the SAM Register Transfer Architecture (RTA).

1. List all the elements in the SAM RTA machine state. This is the list of all storage elements in the SAM datapath.

2. Fill in the following table with the register transfer sequences for each of the SAM instructions. Circle the active control signals in each RT action.

Instr		Control Code									Action
		Pc	Inc	Amux	Mar	Mst	Ir	Dmux	Acc	Out	Sub	f(src) -> dst
Lda	1	0	1	0	1	0	0	–	0	0	–	PC → MAR; inc(PC)
	2	0	0	–	0	0	1	–	0	0	–	Mem(MAR) → IR
	3	0	0	1	1	0	0	–	0	0	–	IR → MAR
	4	0	0	–	0	0	0	1	1	0	–	Mem(MAR) → ACC
Add	1	0	1	0	1	0	0	–	0	0	–	PC → MAR; inc(PC)
	2	0	0	–	0	0	1	–	0	0	–	Mem(MAR) → IR
	3	0	0	1	1	0	0	–	0	0	–	IR → MAR
	4	0	0	–	0	0	0	0	1	0	0	Add(ACC, Mem(MAR)) → ACC
Sub	1	0	1	0	1	0	0	–	0	0	–	PC → MAR; inc(PC)
	2	0	0	–	0	0	1	–	0	0	–	Mem(MAR) → IR
	3	0	0	1	1	0	0	–	0	0	–	IR → MAR
	4	0	0	–	0	0	0	0	1	0	1	Sub(ACC, Mem(MAR)) → ACC
Sta	1	0	1	0	1	0	0	–	0	0	–	PC → MAR; inc(PC)
	2	0	0	–	0	0	1	–	0	0	–	Mem(MAR) → IR
	3	0	0	1	1	0	0	–	0	0	–	IR → MAR
	4	0	0	–	0	1	0	–	0	0	–	ACC → Mem(MAR)
Jmp	1	0	1	0	1	0	0	–	0	0	–	PC → MAR; inc(PC)
	2	0	0	–	0	0	1	–	0	0	–	Mem(MAR) → IR
	3	1	0	–	0	0	0	–	0	0	–	IR[3:0] → PC
	4	0	0	–	0	0	0	–	0	0	–	Nop
Jaz	1	0	1	0	1	0	0	–	0	0	–	PC → MAR; inc(PC)
	2	0	0	–	0	0	1	–	0	0	–	Mem(MAR) → IR
	3	1	0	–	0	0	0	–	0	0	–	IR[3:0] → PC, if ACC=0
	4	0	0	–	0	0	0	–	0	0	–	Nop
Out	1	0	1	0	1	0	0	–	0	0	–	PC → MAR; inc(PC)
	2	0	0	–	0	0	1	–	0	0	–	Mem(MAR) → IR
	3	0	0	–	0	0	0	–	0	1	–	ACC → OUT
	4	0	0	–	0	0	0	–	0	0	–	Nop
Hlt	1	0	1	0	1	0	0	–	0	0	–	PC → MAR; inc(PC)
	2	0	0	–	0	0	1	–	0	0	–	Mem(MAR) → IR
	3											NOP
	4											NOP

Sam Logic High Control Signal Table

Instr	Instr Fetch		Instr Exec	
	t_1	t_2	t_3	t_4
Lda	Inc Mar	Ir	Amux Mar	Dmux ACC
Add	Inc Mar	Ir	Amux Mar	ACC
Sub	Inc Mar	Ir	Amux Mar	ACC sub
Sta	Inc Mar	Ir	Amux mar	Mst
Jmp	Inc Mar	Ir	PC	
Jaz	Inc Mar	Ir	PC	
Out	Inc Mar	Ir	Out	
Hlt	Inc Mar	Ir	Hlt	

Fill in Control Signal Names that are logic 1 in the box for each instr & RT state

Control Signal Logic for SAM Control Signals

$Pc = t_3 \wedge (Jmp \vee Jaz)$

$Inc = t_1$

$Amux = t_3 \wedge (Lda \vee Add \vee Sub \vee Sta)$

$Mar = t_1 \vee (t_3 \wedge (Lda \vee Add \vee Sub \vee Sta))$

$Mst = t_4 \wedge (Sta)$

$Ir = t_2$

$Dmux = t_4 \wedge (Lda)$

$Acc = t_4 \wedge (Add \vee Sub)$

$Out = t_3 \wedge (Out)$

$Sub = t_4 \wedge (Sub)$

$Hlt = t_3 \wedge (Hlt)$