DSP Assignment 6

18/03/2021

Q1) The resolution of a 4-bit counting ADC is 0.5 volts. For an analog input of 6.6 volts, what will be the digital output of the ADC?

Q2) An analog voltage in the range 0-8 V is divided in 16 equal intervals for conversion to 4-bit digital output. Find the maximum quantization error?

Q3) Consider an arbitrary digital filer with transfer function:

$$H(z)=\sum_{n=-\infty}^{\infty} h(n)z^{-n}.$$

Perform two-component polyphase decomposition of H(z) by grouping the even numbered samples $h_0(n)=h(2n)$ and odd numbered samples $h_1(n)=h(2n+1)$.

A) Show that $H(z)=H_0(z^2)+z^{-1}H_1(z^2)$.

B) Determine $H_0(z)$ and $H_1(z)$.

Q4) A) Draw the efficient polyphase structure for Interpolation with I=3.

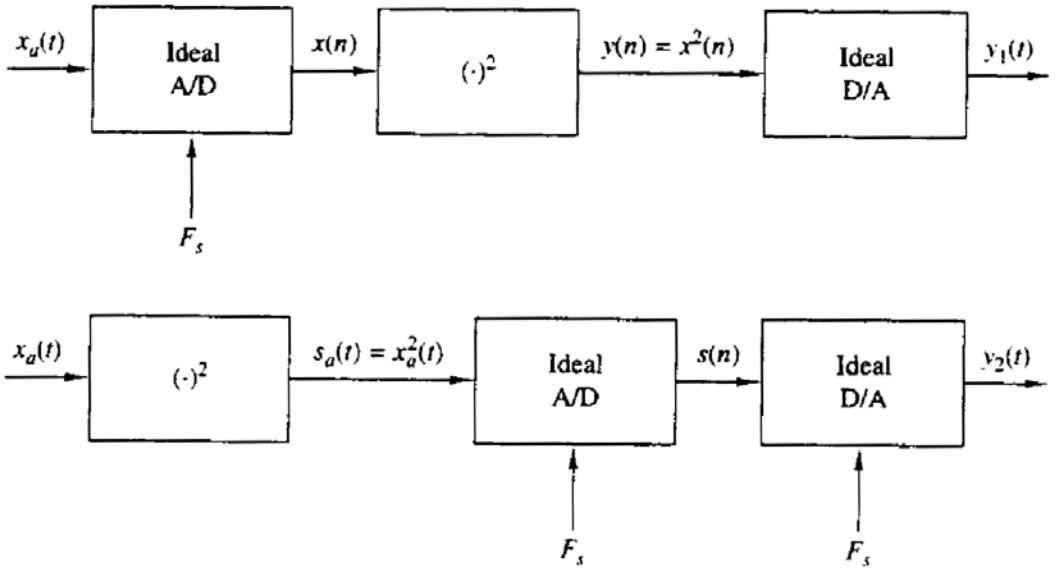
B) What is type II polyphase structure? Derive its relation with type I polyphase structure.

C) Draw the type II polyphase structure for Interpolation with I=3.

Q5) Determine the signal-to-quantization noise ratio(SQNR) of a 8-bit,12-bit ,16-bit and 20-bit quantizer for a full scale sinusoidal signal.

Q6)

Determine $y_1(t)$ and $y_2(t)$ if $x_a(t) = \cos 2\pi F_0 t$, $F_0 = 20$ Hz, and $F_s = 50$ Hz or $F_s = 30$ Hz.



Q7)

Consider a DM coder with input $x(n) = A\cos(2\pi nF/F_s)$. What is the condition for avoiding slope overload? Illustrate this condition graphically.

Q8) Develop a computationally efficient realisation of a factor of 3 interpolator employing a length-15 Type-II FIR filter.