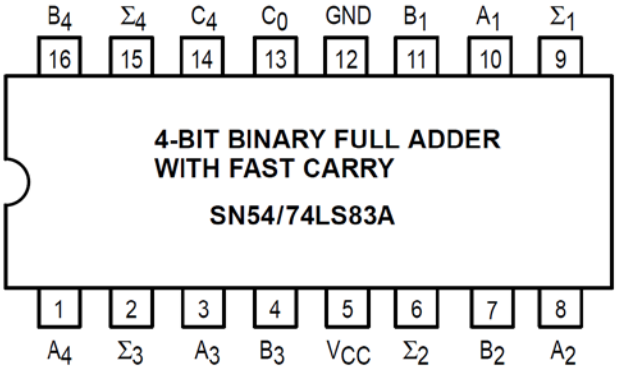
Experiment 4

In this, we shall study and use IC 7483 which performs 4-bit addition / subtraction.

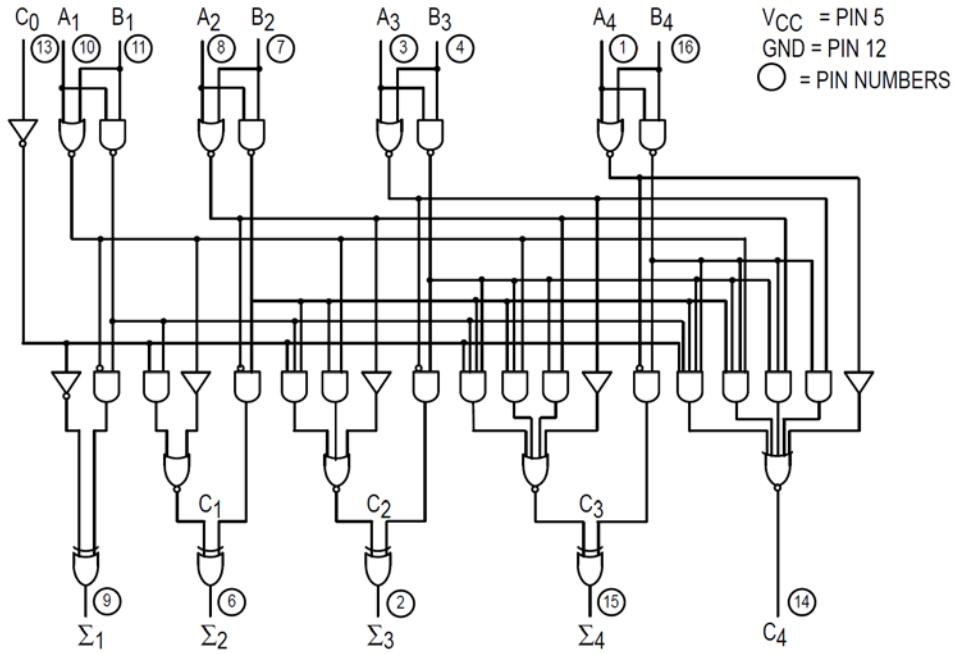


PIN NAMES

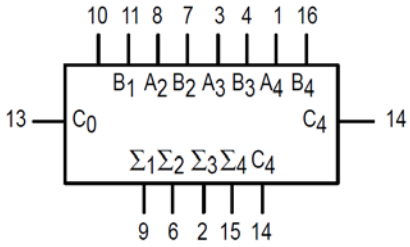
		LOADING (Note a) HIGH	LOADING (Note a) LOW
A_1-A_4	Operand A Inputs	1.0 U.L.	0.5 U.L.
B_1-B_4	Operand B Inputs	1.0 U.L.	0.5 U.L.
C_0	Carry Input	0.5 U.L.	0.25 U.L.
$\Sigma_1-\Sigma_4$	Sum Outputs (Note b)	10 U.L.	5 (2.5) U.L.
C_4	Carry Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



LOGIC SYMBOL



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current C_0 A or B				20 40	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
	C_0 A or B				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current C_0 A or B				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
t_{PLH} t_{PHL}	Propagation Delay, C_0 Input to any Σ Output		16 15	24 24	ns	V_{CC} = 5.0 V C_L = 15 pF Figures 1 and 2
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to Σ Outputs		15 15	24 24	ns	
t_{PLH} t_{PHL}	Propagation Delay, C_0 Input to C_4 Output		11 15	17 22	ns	
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to C_4 Output		11 12	17 17	ns	

AC WAVEFORMS

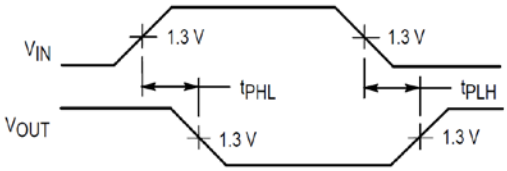


Figure 1

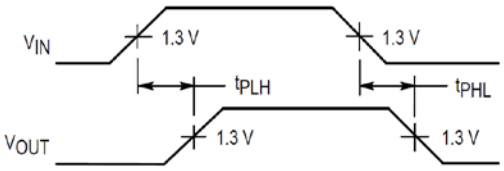


Figure 2

What would have been propagation delay for C_0 input to C_4 output had it not been fast adder?

Task 1: Design a circuit that can perform both 4-bit addition and subtraction in which an input Mode = 0 refers to addition and Mode = 1 refers to subtraction.

Additional: Consider, an additional sign bit is available at the output which if 0, the number is positive and if 1, the number is negative. Show, how a result of subtraction can be read in standard binary form (not 2's complement form in association with sign bit for negative result).

Use LED display of trainer kit to show result and also give input for 4-bit numbers from trainer kit.

Consider the 4 bit addition of Task 1 above where you want to show the result in 7 segment display. If the result is more than 9, say 5 + 7 = 12, then a specific character corresponding to 1100 will appear and not digit 2 in unit's place.

It is interesting to note that whenever a number above 9 is to be displayed, adding 6 to that number will generate appropriate BCD for unit's place. Can you tell why so? For previous example of displaying 12: 1100 + 0110 = 1 0010 or (000)1 0010 i.e. least significant 4 bits 0010 can be used for displaying 2 in unit's place and the carry (generated by another IC 7483 that can be used for addition of 0110) can be sent for displaying BCD of ten's place i.e. 0001 = 1.

Take another example: 9 + 8 = 17 which is 10001. For BCD display, add 6 i.e. 10001 + 0110 = 10111 = (000)1 0111

Note that, 0110 is to be added only when the result of addition is more than 9 and not always.

Task 2: Use two IC 7483 and appropriate combinatorial logic circuit to display result of binary addition of two 4-bit numbers in BCD format through 7-segment display.

Additional: Show how subtraction result can be displayed in BCD format where decimal point of 7 segment can be considered as sign bit.