# Digital Electronics Circuits lab
# Lab Experiment:10

## Name:Harshavardhan Alimi

## Roll No:18EC10021

**AIM**:To implement a 4x4 bit serial parallel multiplier.

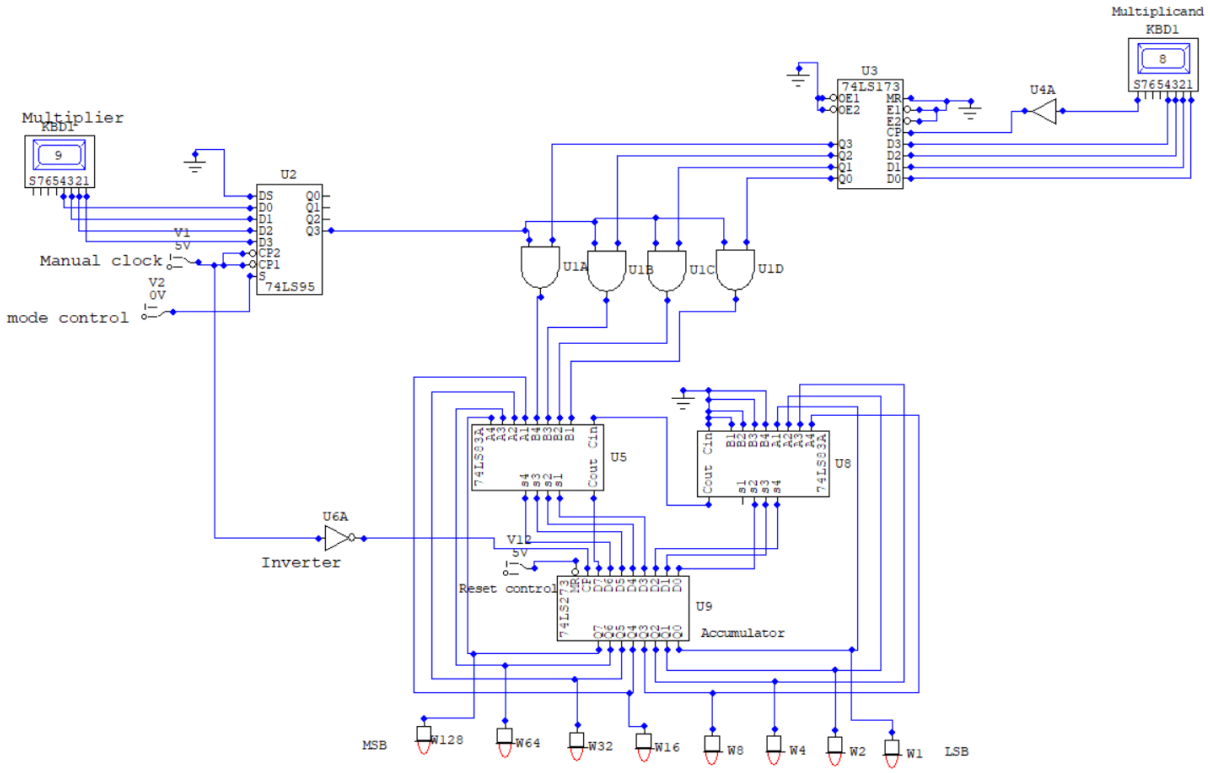
**ICs used:-**

- IC74LS95:-1 quantity
- IC 74LS173:-1 quantity
- IC 74LS273:-1 quantity
- IC 74LS83:-2 quantity
- IC 74LS80:-4 quantity

**Buffer/Driver:-**CD 4050:-1quantity

**Components used:-** ASCII Keypad(2),logic switches(3),logic display(8).

Circuit:Digital circuit to display the product of the multiplier and multiplicand at the 8 logic displays.




product=multiplicand **x** multiplier

## Result:

- The multiplier b3 b2 b1 b0 and the multiplicand a3 a2 a1 a0 ( 4-bit numbers) are multiplied and the number is displayed in binary format using logic displays using a series-parallel adder.

## Discussion:

- The logic used for the implementation is the basic multiplication math.

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | | a3 | a2 | a1 | a0 |
| | | | | b3 | b2 | b1 | b0 |
| | | | | a3b0 | a2b0 | a1b0 | a0b0 |
| | | | a3b1 | a2b1 | a1b1 | a0b1 | x |
| | | a3b2 | a2b2 | a1b2 | a0b2 | x | x |
| | a3b3 | a2b3 | a1b3 | a0b3 | x | x | x |
| R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 |

- The multiplicand is taken as input from the ASCII and gets stored at the register IC74173,where the strobe creates a sufficient delay to store the values at the outputs of the 4D flip-flops in IC74173.
- Writing and storing the multiplier in IC7495:
  - Writing,Input the multiplier from an ASCII into IC7495(shift register)where D3 is to be LSB and D0 is to be MSB.
  - Storing,In IC7495, initially when S = 1, CP2’ is enabled. A high to low transition on enabled CP2’ transfers parallel data from the D3D2D1D0 to Q3Q2Q1Q0. So initially S is kept at 1 and the high to low transition is given using a logic switch to send the data to Q3Q2Q1Q0(b0 b1 b2 b3).
- 8-bit adder is made cascading the 2 4-bit adders where in cout of lower nibble adder is connected to cin of higher nibble adder.
  - So,the output of 8 bit adder adder becomes cout S7 S6 S5 S4 S3 S2 S1 S0.
  - And we neglect the lower bit from adder outputs i.e. S0 and connect the remaining 8 outputs to the accumulator(IC74273) which makes left shift i.e.divide the adder output by 2.

- And we feed this output as input to the 8-bit cascaded adder.

- So here,In 8-bit addition, first a3b0 a2b0 a1b0 a0b0 0 0 0 0 is sent to the register IC74273 and then divided by two. The division by two is done by neglecting the LSB since division by two is nothing but right shifting the binary number by one digit. The new number is 0 a3b0 a2b0 a1b0 a0b0 0 0 0
- And this new number is sent back to the 8-bit adder which is then added to the b1 multiplied with a3a2a1a0 0 0 0 0 and the above step is repeated.
- Pseudo code:-

  for i in range(n) :

  z = z + pow(2,n)*(b)

  z = z/2 (left z by 1 or (z >> 1))

  Where n is number of bits of a (multiplicand) , b is the multiplier and z is the output.
- IC74273 stores the result after each iteration and feeds it back to the 8-bit adder whenever its CP sees a rising edge.(positive edge trigger).
  - PPi=a3 a2 a1 a0 **x** bi
  - So our final product should be FP=8PP3+4PP2+2PP1+PP0
  - Let Y:input from the accumulator, X:other input,Z:adder output=(X+Y)/2
  - 1st clk pulse(rising edge): X=16PP0 ;Y=0 ;Z=8PP0
  - 2nd clk pulse: X=16PP1 ;Y=8PP0 ; Z=8PP1+4PP0
  - 3rd clk pulse: X=16PP2 ; Y=8PP1+4PP0 ;Z=8PP2+4PP1+2PP0
  - 4th clk pulse: X=16PP3 ;Y=8PP2+4PP1+2PP0 ;Z=8PP3+4PP2+2PP1+PP0
- The rising edge is given manually using Logic Switches.
- Care must be taken to reset the IC74273 before starting a new multiplication (MR should be made LOW and then HIGH).(can be controlled by **reset control**)
- IC7495 takes the role of shifting the bit which is to be multiplied with multiplicand:
  - When S = 0,  CP1' is enabled. A high to low transition on enabled CP1' transforms the data from serial input (DS) to Q0, Q0 to Q1, Q1 to Q2, Q2 to Q3. So the transitions are given four times(since the multiplier is four bit) using logic displays.(mode of s can be controlled by **mode control**)
  - Care must be taken to give exactly only four transitions using the logic switches.

- Instead of using the manual clk we can also use the down counter as we had used it in previous experiment(EXP_9).
- The triggering of CP1’ and CP2’ of IC7495 is falling edge whereas CP of IC74273 is triggered by a positive edge. So we can use the same logic switch for triggering CP but with an inverter buffer. Three inverter buffers are used so as to give sufficient time for the input signal to be processed and reach the accumulator.