

### Required ICs:

- (i) IC 74193 - Synchronous 4-bit counter with dual clocks (CPU for upcounting, CPD for downcounting), (ii) IC 7483 (2 are required) 4-bit Parallel adder, (iii) IC 74273 (octal true edge triggered DFF with active low Master Reset)
- (iv) IC 74173 (Quad DFF with input and output enable)  
(v) IC 7432 (Quad 2-in OR gates) (vi) Logic switches  
(vii) Pulser, (viii) LED lamps to read outputs of product register (273)
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Major steps:

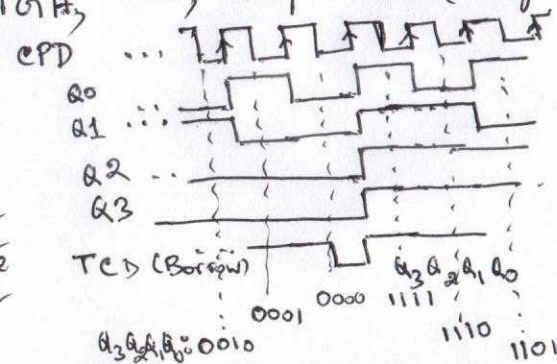
- i) Load 4-bit multiplicand into 74173
- ii) Load 4-bit multiplier into 74193
- iii) Feed manual clock into IC 74193 (as well as IC 74273) for small multiplier values
- iv) Feed auto clock (from pulser) for large multiplier values



➤ **IC 74193 : synchronous 4-bit counter with dual clocks.** :- (a) for our experiment (on multiplication), down-counting is required. So keep CPU (clk for up counting) inactive i.e. HIGH and feed clock pulses in CPD (clock pulse for down counting).  
 (b) while feeding multiplier value into the (down)-counter, place the value in parallel inputs (D3...D0) and make PL (parallel load enable) LOW ("0") for some time by a logic switch. Then make PL HIGH ("1") to enable progressive counting in either direction.

→ Also, keep MR (clear input) inactive (LOW) for all times.  
 (c) based on value of multiplier, multiplicand gets (repeatedly) added to the accumulator (product) register IC 74273. It is advisable to reset (clear) IC 74273 using active low MR input once at the beginning of the experiment. During normal operation, however, keep MR (inactive), i.e. HIGH. So, keep a control (logic) switch for MR of 74273.

(d) During down counting, the TC (Borrow) output which becomes low for small amount of time may be used to inhibit (disable) clock to 74193 (as well as 74273) to freeze the contents of product register. An alternative way to generate clock enable (control) for 74193 and 74273 is  $Q_3 + Q_2 + Q_1 + Q_0$  (logical OR-ing of the outputs of the counter).



2) **IC 74273 - octal +ve edge triggered DFF with MR**

3) **IC 74173 - Quad +ve edge triggered DFF with IF, OF, MR**

4) **IC 7483 - 4-bit parallel adder with Cin, Cout**

5) **Use LED lamps to sense values of 74273** : We need to convert the binary output of product register to BCD format if we wish to view it on 7-segment LEDs.