EC 39003 Digital Ckts Lab

11-11-2020

Experiment on Implementing Binary-to-BCD Conversion.

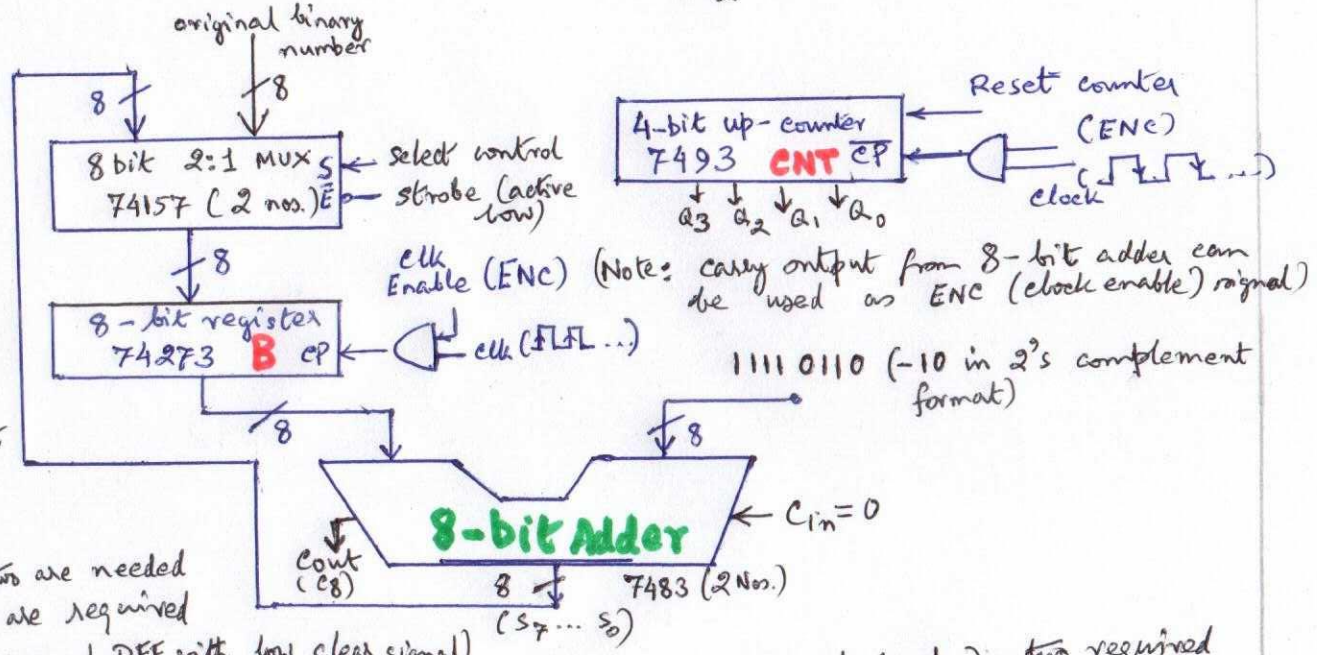
- Assume the given binary number $B \equiv [b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0]_2 < 100_{10}$
- Procedure is:
  (initially, load original binary no. in register B, and clear counter CNT to 0)

```
WHILE (B >= 10) DO
  { B := B - 10;
    CNT := CNT + 1;
  }
/* BD2 = CNT and BD1 = B */
```

```
Cout  0010 0011 (35)
      1111 0110 (-10)
  1   0001 1001 (25)
      1111 0110 (-10)
  1   0000 1111 (15)
      1111 0110 (-10)
  1   0000 0101 (5)
      1111 0110 (-10)
  0   1111 1011 (-5)
```

$[0010\ 0011]_2$ → 35 → $BD_2\ BD_1$

Note: (i) the more significant (BD_2) BCD digit will be displayed as the final content of the up-counter
(ii) the less significant BCD digit (BD_1) will be available as the final content of the lower significant nibble of the 8-bit register



Required components:

i) IC 74157 (quad 2 to 1 MUX) – two are needed
ii) IC 7483 (4-bit adder) – two are required
iii) IC 74273 (octal +ve-edge triggered DFF with low clear signal)
iv) IC 7493 (or 7490) (4-bit up-counter)
v) IC 7447 (BCD-to-7-segment decoder) – two required
vi) 7-segment LED display (common anode) – two required
vii) AND gate, logic switches, pulser

Major steps:

i) **load the given binary number into the register B; reset counter**
ii) **feed manual clock to register B and counter CNT.** Note the intermediate values ('sum' output of the adder and counter state). The 'select' control input of the multiplexer should be adjusted to allow the 'fed back' sum o/p into the register B.
Repeat step ii) until carry output (from adder) becomes '0'

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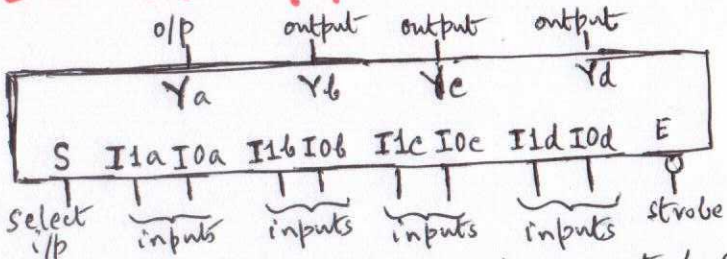
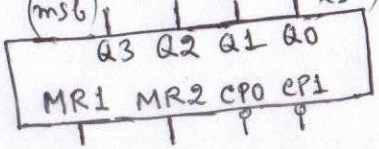
i) IC 74157 (quad 2-to-1 data selectors/multiplexers)



S: select control i/p, $\overline{E}$: strobe (enable) input

Combination of two 74157 chips will constitute a 2-to-1 word multiplexer (word length of eight bits) with S=0, the original 8-bit binary number may be introduced into the 8-bit register 'B', at the beginning. From this point onward, select control S=1 to allow register B to receive the 8-bit output of the 8-bit adder. Note: the strobe i/p $\overline{E}$ is kept '0' throughout.

ii) IC 7493: (mod-16) 4-bit binary counter



— to use the maximum possible count length, apply the primary clock pulses to the $\overline{CP_0}$ input, while the o/p pin Q0 and the other clock i/p pin $\overline{CP_1}$ have to be externally connected by a wire. The 4-bit count value Q_3 (msb) Q_2 Q_1 Q_0 (lsb) can be read via 7-segment common anode (CA) display in the present experiment. Note that reset operation of the counter should be done only once at the beginning by connecting MR1 and MR2 together and momentarily set to '1' (HIGH). At all other times, the reset control must be kept inactive (by setting it to '0' (LOW). One can use IC 7490 (decade or mod-10 counter) instead of IC 7493; however, the MS1 and MS2 (set to nine (1001) input) of '90 must be kept inactive by setting it to LOW.

iii) IC 7483: 4-bit adder

: to use two chips in cascade. The carry output signal of the more significant (4-bit) adder can be used as clock enable signal.

iv) IC 74273: octal positive edge triggered DFFs with active low clear ($\overline{MR}$) input:

for this experiment, one should keep $\overline{MR}$ inactive by connecting it to '1' (HIGH). Note that FFs in 7493 are negative edge triggered while that in 74273 are positive edge triggered. So clk signal fed to 74273 CP i/p can be inverted and fed into $\overline{CP_0}$ input of 7493/7490 counter.

v) ic 7447: BCD to 7-segment display decoder

and common-anode 7-segment LED displays. For this experiment, we require two combinations:- one for displaying the counter contents (higher significant BCD digit, BD2) and the other for displaying the final contents of the lower significant nibble of 74273 (lower significant BCD digit BD1).