

# Digital Electronics Circuits lab

## Lab Experiment:11

**Name:Harshavardhan Alimi**

**Roll No:18EC10021**

**AIM:**To design and implement a binary to BCD converter.

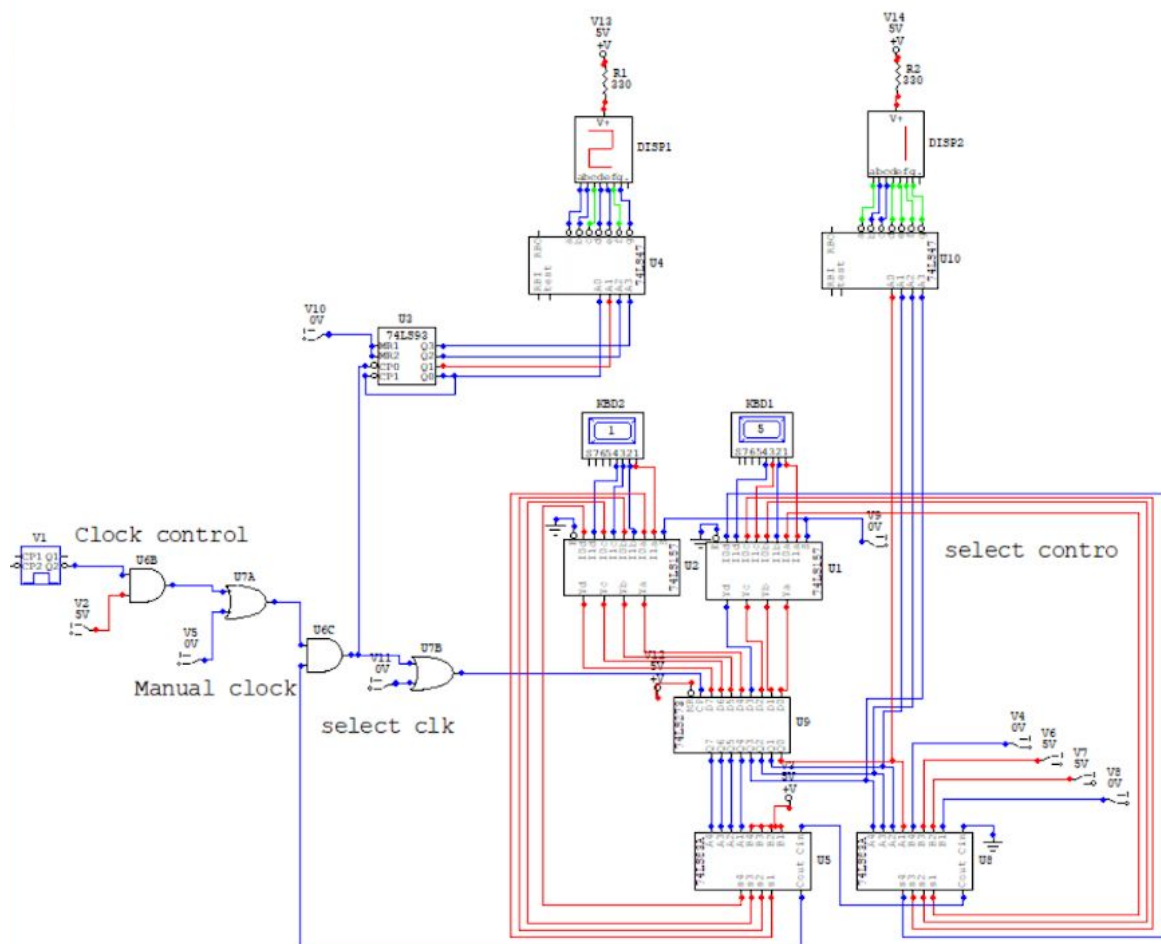
**ICs used:-**

- IC74LS157:-2 quantity
- IC 74LS83:-2 quantity
- IC 74LS273:-1 quantity
- IC 74LS93:-2 quantity
- IC 74LS47:-1 quantity

**Buffer/Driver:-**CD 4050:-1quantity

**Components used:-** ASCII Keypad(2),logic switches,common anode 7-segment display,basic logic gates(AND gates,OR gates).

Circuit:



### Procedure:

- Give input from the 2 ASCII displays: The higher four bit nibble with one ASCII key and the lower nibble with the other. For example, 21 = 0001 0101. The first ASCII key feeds 0001 and the second one feeds 0101..
- Make V2=0(clock control), V5=0(manual clock), V11=0(select clk), V9=1(select control), V10=1(reset control)
- V11: 0->1->0
- V9=0
- V10=0
- V2=1

### Results:-

- The given 8-bit binary number is displayed in BCD format using two displays. (Binary number given upto 99)

### Discussion:-

- The input is a 8-bit number given using two ASCII keys. The higher four bit nibble with one ASCII key and the lower nibble with the other. For example, 21 = 0001 0101. The first ASCII key feeds 0001 and the second one feeds 0101.
- This 8-bit binary number then needs to be stored in some register, this will be done by using two 4-bit nibble multiplexers (IC74157).
- The 8-bit 2:1 multiplexer is implemented by cascading a 4-bit 2:1 multiplexer IC74157 and by connecting the select pins.
- We make the select pin to be 1 to store the initial 8-bit binary number in the register and this pin is controlled by **select control**.
- And we make use of **select clk(U7B)** we make 0->1->0 transition in this select clk such that the initial 8-bit number gets stored in the register IC74273 as, this IC triggers with a positive edge.
- And also this IC74273(accumulator) stores the result after each iteration and feeds it to the 8-bit adder whenever its CP sees a rising edge(positive edge trigger).
- The rising edge is given manually using Logic Switch once(for storing the initial 8bit number) and then using a pulser(while iterations takes place).
- The 8-bit adder feeds it back to the 8-bit multiplexer.
- After the input is given, the select pin of the 8-bit multiplexer is made logic low(using **select control**) allowing the input from the 8-bit adder to reach the register.

- The 8-bit adder is made cascading two 4-bit adders (U5 U8).
- The first adder (U5) has two inputs, one from the upper nibble from IC74273 and the other is 1111. The second adder has two inputs, one from lower nibble from IC74273 and the other is 1001. The second adder's  $C_{out}$  is connected to the first adder's  $C_{in}$ (U8). The second adder's  $C_{in}$  is grounded.
- 11111001 is 2's complement of 10. So we keep subtracting 10 from the given number until  $C_{out}$  of the 8-bit adder becomes 0.(or basically the given number becomes less than 10, ex:- 21->11->1->STOP)
- Initially  $C_{out}$  is 0, so a manual positive edge trigger (**select clk**) is given to IC74273 to store the input given and after that the multiplexer's select pin is changed and the clock is turned on (V2[**clock control**] is turned on). The clock is sent to 2 input AND gate(U6C) with  $C_{out}$  and increments the counter IC7493 till  $C_{out}$  becomes 0. (**select clk**(V11) is left at 0).
- We will make V10 (0->1->1) such that the counter will be in reset position 0000.
- CP0 of IC7493 is connected to the output of U6C to start counting after the input is feeded into the register.
- CP of IC74273 is connected to the U7B so that we can give a manual trigger in the first iteration and later it is governed by  $C_{out}$  and clock pulser.
- The output of IC7493 (counter) is the most significant digit of BCD number and the lowest four bits (lower nibble) of the register IC74273 serve as the least significant digit of the BCD number.
- Each are respectively connected to the common anode 7-segment display through IC7447 (decoder).
- Algorithm used:-
- WHILE( $B \geq 10$ ) DO {
  - B = B-10;
  - CNT+=1;
  - }
  - BD2= CNT, BD1= B;
- B becomes the least significant digit(BD1) of BCD number and CNT represents the most significant digit(BD2) of BCD number.
- Care must be taken to avoid extra counting to the IC7493. Sufficient time must be given for  $C_{out}$  to reach AND gate so as to not count an extra CNT.