

# Digital Electronics Circuits lab

## Lab Experiment:8

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**Roll No:**18EC10021

**AIM:**To design a circuit to store 8 digits(18EC1021) of the roll number in RAM in particular addresses,and display that 8 digits of the roll number in the sequential order using 7-segment display.

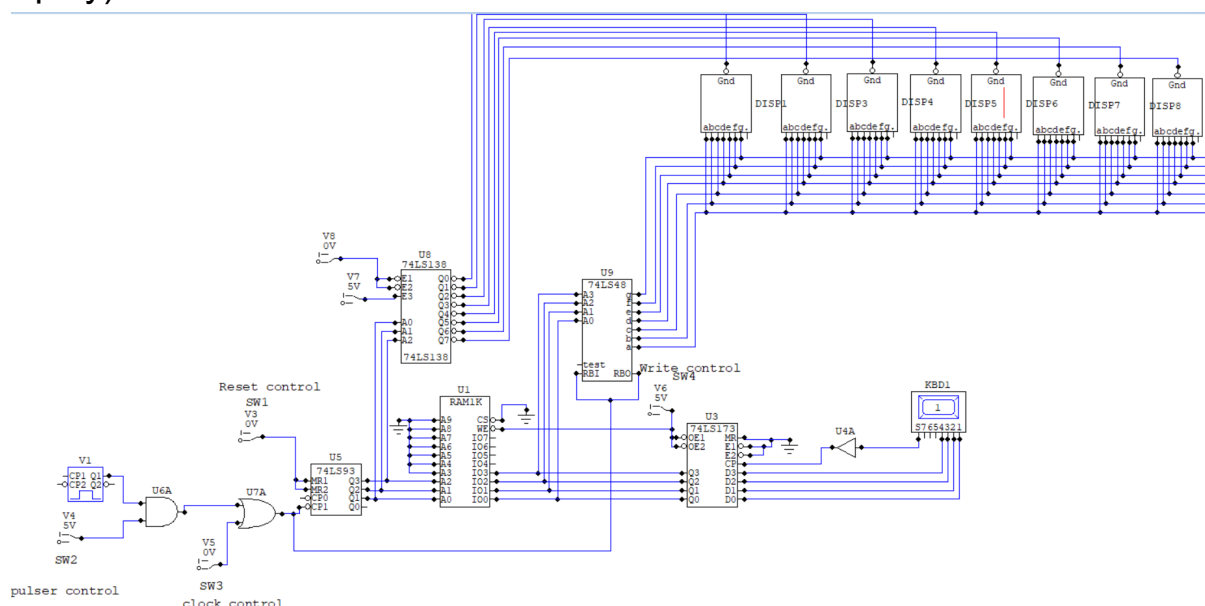
**ICs used:-**

- IC74LS93:-1 quantity
- RAM1K:-1 quantity
- IC 74LS173:-1 quantity
- IC 74LS47:-1 quantity
- IC 74LS138:-1 quantity
- IC 74LS48:-1 quantity

**Buffer/Driver:-**CD 4050:-1quantity

**Components used:-** 7-seg display(quantity:8,common cathode), Logic Gates(and gate;or gate),ASCII Keypad,logic switches(4).

**Circuit:**Digital circuit for writing the 8-digit roll number using a register into the RAM and reading from the RAM and displaying it on the 8 7seg-displays(where each number will be displayed on the separate display).



### Working and Discussion of circuit:

- ❖ We have seen the working of ASCII Keypad in the previous experiment.
  - So to give the input of 18EC1021 we have to type 18nj1021 correspondingly in the ASCII Keypad.
- ❖ IC 74LS173: Quad D-type flip-flops with positive-edge trigger and 3-state outputs.
  - 16-pin DIP: 4D's, 4Q's, OE<sub>1</sub>', OE<sub>2</sub>', IE<sub>1</sub>', IE<sub>2</sub>', CP, MR, V<sub>cc</sub>, GND.
  - When IE<sub>1</sub>', IE<sub>2</sub>'=0, data on D inputs loaded into the register with (0→1 edge) transition on CP input.
  - MR: asynchronous active high clear input.
  - IE<sub>1</sub>', IE<sub>2</sub>': always enabled('0').
  - OE<sub>1</sub>', OE<sub>2</sub>': active low output enable. if either one of them (or both) is high, data at Q outputs is tristated. only if both of them are low, register data is available at Q outputs this is controlled by logic switch **SW4**(write control).
  - CP: it is connected to strobe output of ASCII keypad through non-inverting buffer CD4050, to provide necessary delay of clock pulse after data are presented at D inputs.
- ❖ RAM 1K: it can store 1024 characters, each having 8-bits.
  - For our experiment we will access only 8 characters, each with 4-bits, so we connect 4-IO's (inputs) of this to the 4 outputs Q's (of 74LS173).
  - WE: it decides whether we have to read or write into the RAM, it is controlled by the same switch **SW4**(write control).
- ❖ IC 7493: 4-bit binary ripple counter, we use mod-8 counter (CP<sub>1</sub>', Q<sub>3</sub>, Q<sub>2</sub>, Q<sub>1</sub>), as it is required to get access to the first 8 locations of RAM.
  - MR<sub>1</sub>, MR<sub>2</sub>: asynchronous active high reset inputs, whenever both are high then it gives the output of 000 at outputs, this will be kept low all the time except at beginning, it is controlled by logic switch **SW1**(reset control).
- ❖ Pulser: while writing into RAM, manual clock pulses (negative-edge trigger) are fed to CP<sub>1</sub>' input via logic gate **SW3**(clock control), so that address A<sub>2</sub>A<sub>1</sub>A<sub>0</sub> is increased seven times (manually using the clock switch). While reading contents of RAM, however free-running clock (from pulser) is fed to

CP<sub>1</sub>' of 7493. Logic switch **SW2**(pulser control) selects between manual clock pulses(for writing) and automated(pulser) clock pulses(for reading).

- ❖ IC74138: It is a decoder which has an active low output(only one of the 8 outputs will be low at a time).
  - This IC has 2 active low enable inputs E<sub>1</sub>', E<sub>2</sub>' and one active high enable input E3. The active low outputs of decoder are connected to the ground points of the eight 7-segment display blocks and here the 7-segment displays are common cathode type because the decoder yields active low output. and at a time only one of the eight displays will display.
- ❖ IC7448: BCD to 7-segment decoder with active high outputs. this IC is intended to work with common mode 7-segment display units. The control signals RBI, RBO, To avoid the delays in the logic gates we have connected the RBO and RBI of 7448 to the output of the OR gate which will make sure blinking or glitching in the circuit doesn't happen.
- ❖ The 7(segment) outputs a,b,c,d,e,f,g (IC7448) are connected to the respective segment pins of the display units D1,.....,D8.
- ❖ The value stored at 000 gets displayed at D1 and the value at 001 gets displayed at D2 .....using the decoder and the eight seven segment displays.

### Result:

#### ❑ **Writing:-**(for writing 18EC1021 into RAM)

##### → Initial setup for writing:

- ❑ Reset counter to Q<sub>3</sub>Q<sub>2</sub>Q<sub>1</sub> to 000: connect SW1->'1' and then connect to '1' for the entire writing part.
- ❑ Connect SW2->0 so that we are taking the manual clk pulses, for the entire writing part.
- ❑ Connect SW3->0, SW4->1(not enabling writing into RAM).

##### → Repeating steps for the entire setup: for 8 digits 18nj1021

- ❑ Type the digit from ASCII which gives corresponding 4-bit output, these will be stored in the register.
- ❑ SW4->0 which will make those outputs write in the particular address of RAM.
- ❑ SW4->1, so that the next giving input may not affect the present address.

- ❑ SW3->1 and SW->0 ,this will make 1->0 transition i.e, negative edge trigger which will increment values in the counter(increment address cell).

Storage In RAM :

Address	4-bit value	Digit which will display for corresponding 4-bit input
000	0001	1
001	1000	8
010	1110	E
011	1010	C
100	0001	1
101	0000	0
110	0010	2
111	0001	1

#### ❑ Reading:

- SW1 -> 1 and SW1 ->0 ,so that the address points at the 000.
- SW4 ->1 ,such that no writing takes place from the register.
- SW3 ->0 ,to avoid the manual clk pulses.
- SW2 ->1 ,to select the automated clk pulse over manual clk pulse.
- So,at the counter: for each negative-edge trigger in the clk pulse the address value gets incremented.
- For each value at the counter,the decoder will decide which display to be used and the 7448 will decide which is to be displayed(reading from the particular address of RAM,where address is determined by the counter).
- As the clk keeps on going the above procedure will take place and displays the 8-digit roll number (which is stored in RAM) at the respective display of eight displays.