ii) With the above connection of digital ICs and components in place, and the binary counter clock input being fed with continuous clock pulses (from a pulser), the display can appear to remain steady (for higher clock frequency) or flicker unsteadily (for lower clock frequency). For this simulation \rightarrow Digital Options \rightarrow Simulation speed can be varied from 1 to 30.

Note: as the counter state progresses from agaza = 000 to agaza = 111, at any point of time, only one of the eight 7-segment units will be driven. When Q3Q2Q1 = 000 (for example), only Q0 0/p of IC 74138 will be at logic o' so that only display unit D1 will be glowing. Although the remaining seven units are not powered up at that time, if the clock speed is quite high, they will appear to be emitting light lowing to persistence of vision) at the same time. i) IC 7448 - BCD to 7-segment decoder with active high outputs. This IC is intended to work with common cathode 7-segment display units. The control signals lamp test, RBI and BI/RBO can be kept at inactive (HIGH) level. ii) IC 74138 - 3- to-8 decoder with active low outputs. This IC that two active low enable inputs EI and E2 and one active high enable input E3. The (active low) outputs Q0,..., Qx of the decoder are connected to the ground pins of the eight 7-segment display blocks D1, ..., D8 iii) The seven (segment) outputs a, b, c, d, e, f and g (of IC 7448) are connected to the pespective segment pins of the display units DI,.., D8. That is, the 'a' Gegment output of IC 7448 is connected to only 'a' pin of each of the eight display units D1,..., D8. Likewise, the (6) olp of 7448 should be connected to only "45 pin of each of the eight display blocks D1,..., D8, and so on.