EC 39003 Digital Circuits Lab

Experiment to input one's 8-character Roll No. from ASCII keypad, store it in RAM and display repeatedly on 7-segment display

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(N.B. If a student's Roll No. is 18EC10023 say, then the following keys should be typed in sequence, viz. 1, 8, n, j, 1, 0, 2, 3 for the given Roll No. Thus for displaying 1 (corresponding to E, type the letter "n" and for displaying 1 corresponding to C, type the letter "j".) Also, one needs to take only one of the two consecutive 0s (zeros) in actual Roll No.

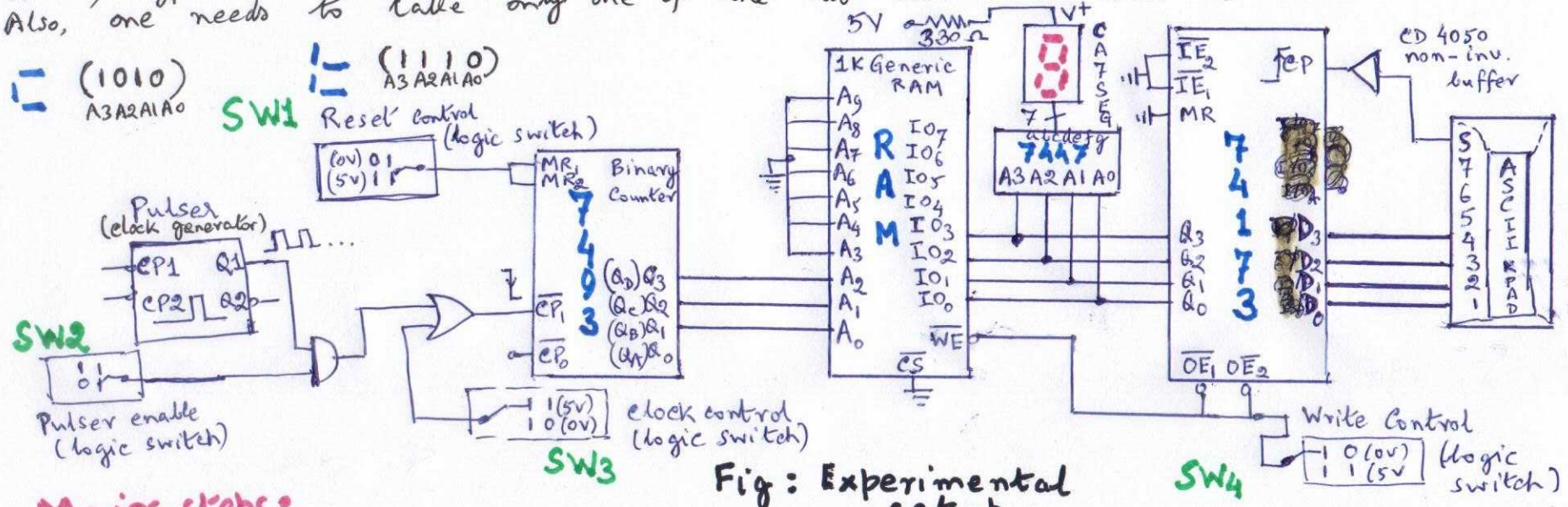

Fig: Experimental setup

Major steps:

1) **Reset counter to $Q_3Q_2Q_1 = 000$** (connect MR_1, MR_2 to '1', trace signal lines ($Q_3Q_2Q_1$) going blue [colour of signal line: red (logic '1') and blue (logic '0')] next set SW1 to '0', i.e. MR ← inactive after this)
Write proper 4-bit word to memory location 0; e.g. type '1' in ASCII Keypad. Data get registered in four FFs of 74173. Now, set SW4 to '0' → data get written to RAM. Now, SW4 ← '1'.

2) **Increment address of counter** – note SW2 must be '0' during writing phase. For changing address, set SW3 to '1' and then to '0' (thereby making $1 \to 0$ transition at $\overline{CP_1}$. Now, location 1 is ready to be written into. Type next data e.g. '8'; next SW4 ← '0' to write '8' to location 1. Next SW4 ← '1'. Go to 'increment address of counter' step. That is, keep (incrementing address) and (writing data in next location) till $A_2A_1A_0 = 111$

3) **Display Roll Number** (one character after another) **repeatedly on CA-7SEG LED** (common anode)

6/N

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1) **IC 74173 :** Quad D-type FFs with positive-edge trigger and 3-state outputs. 16-pin DIP: 4 D's, 4 Q's, $\overline{OE_1}$, $\overline{OE_2}$, $\overline{IE_1}$, $\overline{IE_2}$, CP, MR, V_{cc}, GND
When $\overline{IE_1}$, $\overline{IE_2}$ = '0', data on D i/ps get loaded into register with ⌐ (low-to-high) transition on CP i/p. MR: (asynchronous active high clear input). $\overline{OE_1}$, $\overline{OE_2}$: active low output enable. If either one of $\overline{OE_1}$ or $\overline{OE_2}$ = High, data at Q o/ps: tri-stated. Only if $\overline{OE_1} = \overline{OE_2}$ = '0', register data are available at Q o/ps.

2) **RAM 1K :** $2^{10} = 1024$ locations (words), each having 8 bits. However, for our present experiment, we require least significant four bits (IO_3, IO_2, IO_1, IO_0). So, connect $IO_3 \leftrightarrow Q_3$, $IO_2 \leftrightarrow Q_2$, $IO_1 \leftrightarrow Q_1$, $IO_0 \leftrightarrow Q_0$ of Q o/ps of IC 74173. $\overline{IE_1}$, $\overline{IE_2}$: '0' (always enabled). MR: '0' (always disabled).
CP (clock pulse): connected to strobe(S) i/p of ASCII Keypad through non-inverting buffer CD 4050 (to provide necessary delay of clk pulse after data are presented at Di/ps) of 74174: controlled by $\overline{OE_1}$, $\overline{OE_2}$ (along with active low write enable $\overline{WE}$ of RAM) logic switch SW4.

3) **IC 7493 :** 4-bit binary ripple counter (incorporates independent mod-2 ($\overline{CP_0}$, Q_0) and mod-8 ($\overline{CP_1}$, Q_3, Q_2, Q_1) counters). As it is required to get access to first 8 locations of RAM, we use only the mod-8 counter. MR_1, MR_2: active high asynchronous reset i/ps. They are made active only once at the beginning (and kept low at all other times). They are controlled by logic switch SW1.

4) **Pulser (clock source):** While writing into RAM, manual clk pulses (⌐T) are fed to $\overline{CP_1}$ i/p via logic switch SW3, so that address $A_2A_1A_0$ is incremented seven times. While reading contents of RAM, however free-running clock (from pulser) is fed to $\overline{CP_1}$ i/p of 7493. Logic switch SW2 selects between manual clock pulses and automated (pulser) clk pulses.

6/2