Digital Electronic Circuits Lab.

Experiment: 1

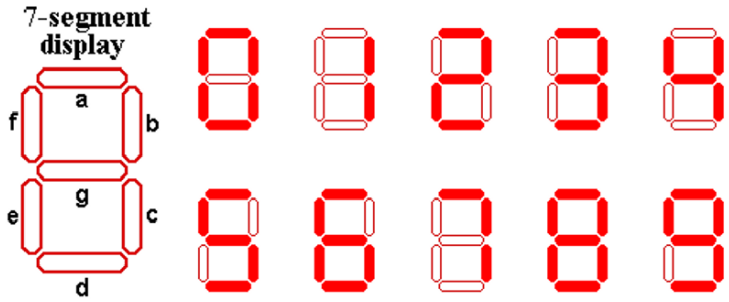
Hello, Everybody! Welcome to Digital Electronic Circuit Lab.

We shall begin the lab. activities with something which may not emerge from the concepts discussed in initial chapters of any Digital Electronics text book. Why so?

In this 3rd year level laboratory, it is expected that we do more than verifying truth table of basic logic gates or their simple combinations. Verifying such truth tables of initial chapters may not seem very inspiring due to its obvious nature, more so due to binary nature of input and output. Therefore, we would try to explore something more non-trivial, in some cases, certain design based solutions. If we need to hop chapters to develop necessary background, we would do so. You may find this and upcoming lab. instruction pages useful in this regard as start-up material. We shall discuss the rest in the lab. as you take up an experiment.

The experiments are designed in such a manner that there would be some happening things in each experiment. How do you want display such an outcome? We shall mostly use 7-segment display that has built-in light emitting diodes. To meet the requirement of the current, such a display should be driven by a display driver.

If we want to display decimal numbers on a 7-segment display as given next,



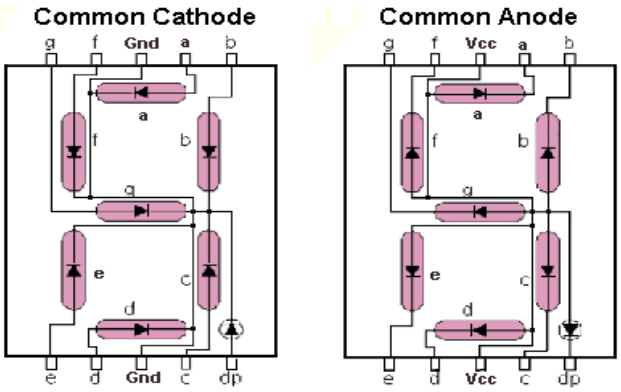
then, we are looking for 4-bit binary input to decode: 0000 representing number ‘0’, 0001 representing number ‘1’, 0010 representing ‘2’, …., 1001 representing ‘9’ in such a way that would generate ‘a’, ‘b’, ‘c’, ‘d’, ‘e’, ‘f’, ‘g’ outputs appropriately where a set of LED conducts to emit light (conducts / does not conduct i.e. ON/OFF i.e. binary 1/0).

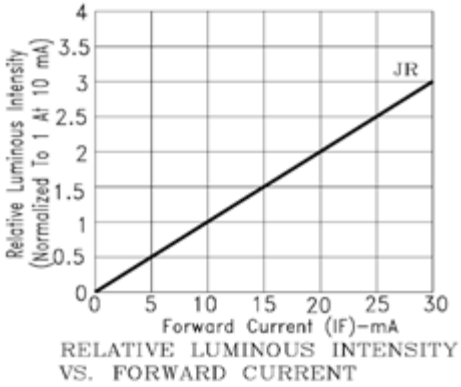
Can the decoder, specially made for such a 7-segment display, be configured in such a manner that it also serves the requirement of providing adequate current to LED i.e. that of a driver? Yes. And, we have 7 segment display driver cum decoder in one block in the form of an Integrated Circuit or IC.

Let us get started with this initial input and the additional material that follows. Let us first understand the various functionalities of 7 segment display driver cum decoder together with a 7-segment display device. In this, we shall give inputs manually to decoder and see corresponding number / pattern getting displayed in the 7-segment display.

Can we improve upon this manual mode of feeding input? We can think of a Counter IC that generates 0000, 0001, 0010, 0011, …. as time progresses and feed this output of the counter to the input of the decoder / driver. We can then sit back, relaxed and find number / pattern changing on its own. We shall learn more about counter soon.

Did you notice that we have quietly introduced ‘pattern’ alongside number in the text description? What is that? We shall find that in the lab. itself.





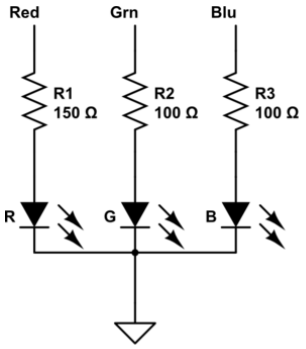
7 segment display: Also, available 9, 14, 16 segment

Common Cathode:

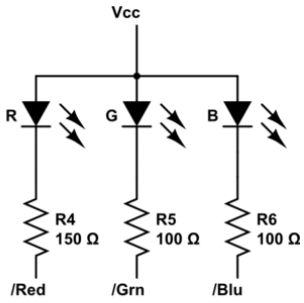
V_{cc} (+ve, power supply, external) → current limiting resistor (external) → input LED pin –internal--> Ground(external)

Common Anode:

V_{cc} (+ve, power supply, external) → input V_{cc} pin – internal --> output LED pin → resistor (external) → Ground(external)



Common Cathode Circuit

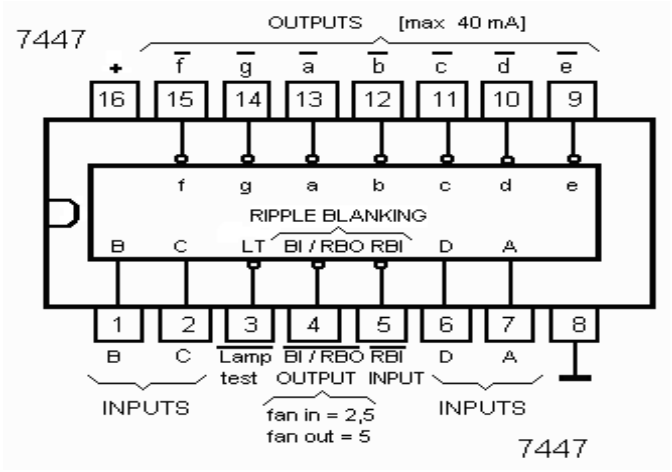


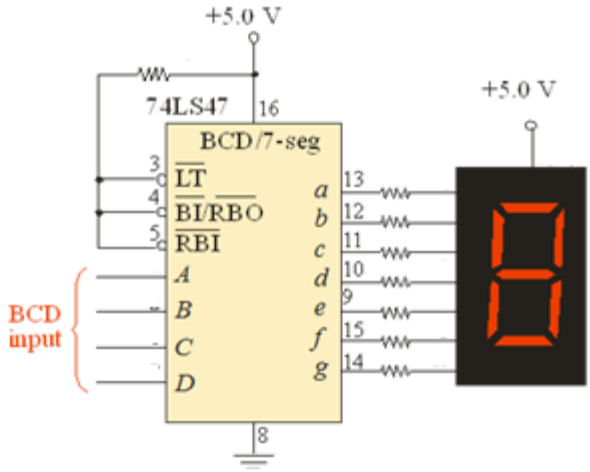
Common Anode Circuit

In the lab.: Common Anode (common resistor after V_{cc}): LT542

DIALIGHT P/N	EMITTED COLOR	MATERIAL	LENS COLOR	LUMINOUS INTENSITY (mcd)			DOMINANT WAVELENGTH (nm)			FORWARD VOLTAGE (V)			VIEWING ANGLE
				If = 20 ma			If = 20 ma			If = 20 ma			° DEGREES
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
598-8010-107F	RED	AlInGaP	Water Clear	30	40	80	630	635	642	1.7	2.2	2.4	140
598-8020-107F	RED-ORANGE	AlInGaP	Water Clear	120	150	200	620	625	630	1.7	2	2.4	140
598-8030-107F	ORANGE	AlInGaP	Water Clear	70	-	150	600	-	610	1.7	2	2.4	140
598-8040-107F	YELLOW	AlInGaP	Water Clear	100	130	160	590	-	595	1.7	2	2.2	140
598-8050-107F	YELLOW	AlInGaP	Water Clear	100	130	160	583	-	590	1.7	2	2.4	140
598-8060-107F	YELLOW-GREEN	AlInGaP	Water Clear	20	40	60	570	-	575	1.8	2	2.4	140
598-8070-107F	GREEN	GaP	Water Clear	10	20	40	562	-	570	1.8	2	2.4	140
598-8081-107F	GREEN	InGaN	Water Clear	220	300	400	520	523	525	3	3.2	3.5	140
598-8091-107F	BLUE	InGaN	Water Clear	90	140	160	470	473	475	2.8	3.2	3.5	140

Luminous intensity, the quantity of visible light that is emitted in unit time per unit solid angle. The unit for the quantity of light flowing from a source in any one second (the luminous power, or luminous flux) is called the lumen. The lumen is evaluated with reference to visual sensation. The sensitivity of the human eye is greatest for light having a wavelength of 555 nanometres (10-9 metre); at this wavelength there are 685 lumens per watt of radiant power, or radiant flux (the luminous efficiency), whereas at other wavelengths the luminous efficiency is less. The unit of luminous intensity is one lumen per steradian, which is the unit of solid angle—there are 4π steradians about a point enclosed by a spherical surface. This unit of luminous intensity is also called the standard candle, or candela, one lumen per steradian.



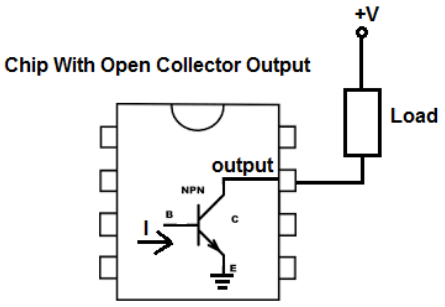


Check from lab. technicians change(s) in above

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS						
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON

Recommended Operating Conditions

Symbol	Parameter	DM5447A			DM7447A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage (a thru g)			15			15	V
I_{OH}	High Level Output Current (BI/RBO)			−0.2			−0.2	μA
I_{OL}	Low Level Output Current (a thru g)			40			40	mA
I_{OL}	Low Level Output Current (BI/RBO)			8			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C



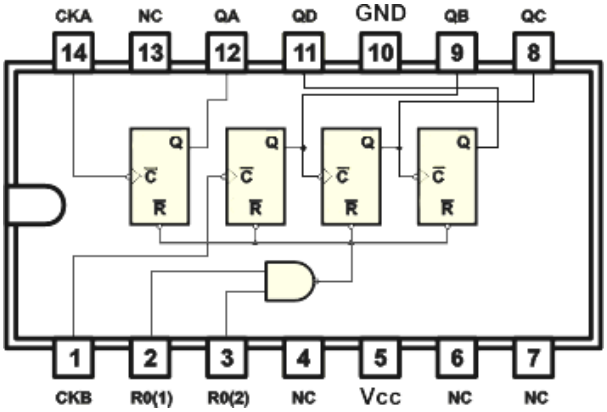
Check which make of 7447 is used in lab. and corresponding data sheet.

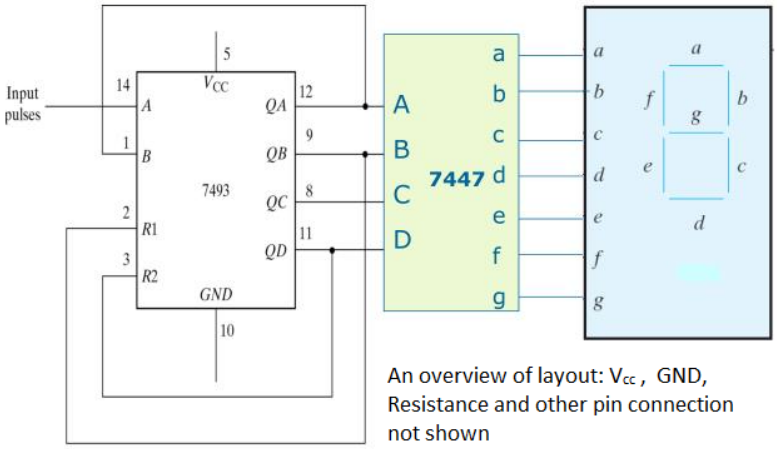
1. BI/RBO is wired-OR logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input must be open or held at a high logic level when output functions 0 through 15 are desired, and ripple-blanking input (RBI) must be open or at a high logic level during the decimal 0 output. X = input may be high or low.

2. When a low logic level is applied to the blanking input (forced condition) all segment outputs go to a low logic level regardless of the state of any other input condition.

3. When ripple-blanking input (RBI) is at a low logic level, lamp test input is at high logic level and A = B = C = D = low logic level, all segment outputs go to a low logic level and the ripple-blanking output goes to a low logic level (response condition).

4. When blanking input/ripple-blanking output is open or held at a high logic level, and a low logic level is applied to lamp test input, all segment outputs go to a high logic level.





An overview of layout: V_{cc} , GND, Resistance and other pin connection not shown

IC 7493: Modulo 2 and 8 Counter (Q_A to CKB: Modulo 16)

93A
Count Sequence
(See Note C)

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
15	H	H	H	H

93A
Reset/Count Function Table

Reset Inputs		Outputs			
R0(1)	R0(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

Note C: Output Q_A is connected to input B.
Note D: H = High Level, L = Low Level, X = Don't Care.

Recommended Operating Conditions

Symbol	Parameter		DM7493A			Units
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.8	mA
I_{OL}	Low Level Output Current				16	mA
f_{CLK}	Clock Frequency (Note 5)	A	0		32	MHz
		B	0		16	
t_W	Pulse Width (Note 5)	A	15			ns
		B	30			
		Reset	15			
t_{REL}	Reset Release Time (Note 5)		25			ns
T_A	Free Air Operating Temperature		0		70	°C

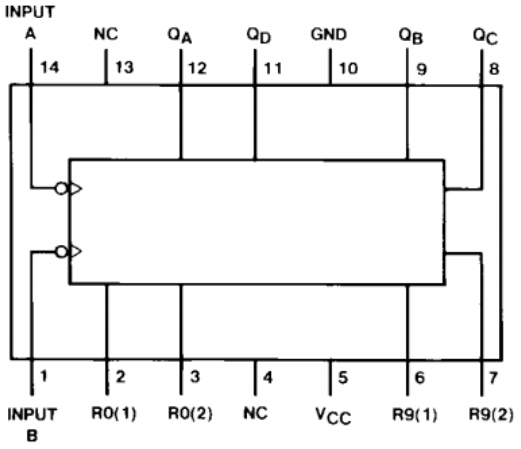
'93A Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency	A to Q_A	32		MHz
		B to Q_B	16		
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_A		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_A		18	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_D		70	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_D		70	ns

IC 7490: Mod 2 and Mod 5 – Together Mod 10 / decade counter

Connection Diagram



Reset/Count Truth Table

Reset Inputs				Output			
R0(1)	R0(2)	R9(1)	R9(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

Function Tables

BCD Count Sequence (Note 1)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Bi-Quinary (5-2) (Note 2)

Count	Output			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

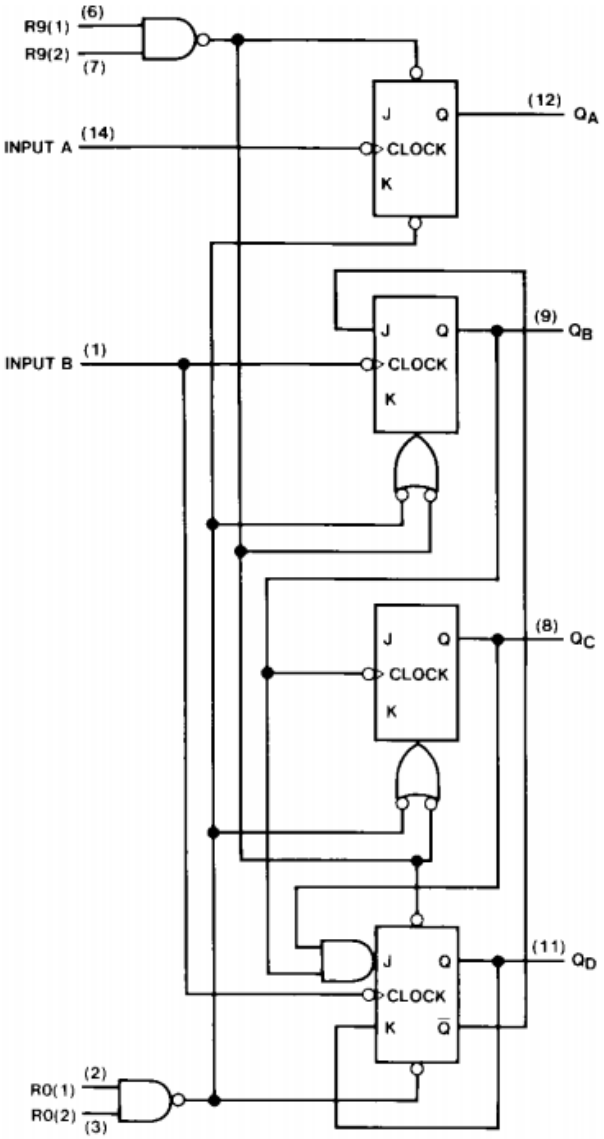
H = HIGH Level
L = LOW Level
X = Don't Care

Note 1: Output Q_A is connected to input B for BCD count.

Note 2: Output Q_D is connected to input A for bi-quinary count.

Note 3: Output Q_A is connected to input B.

Logic Diagram



The J and K inputs shown without connection are for reference only and are functionally at a high level.