Digital Electronics Circuits lab
Lab Experiment:7

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AIM:To design a circuit to store 8 digits(18EC1021) of the roll number in RAM in particular addresses,and display that 8 digits of the roll number in the sequential order using 7-segment display.

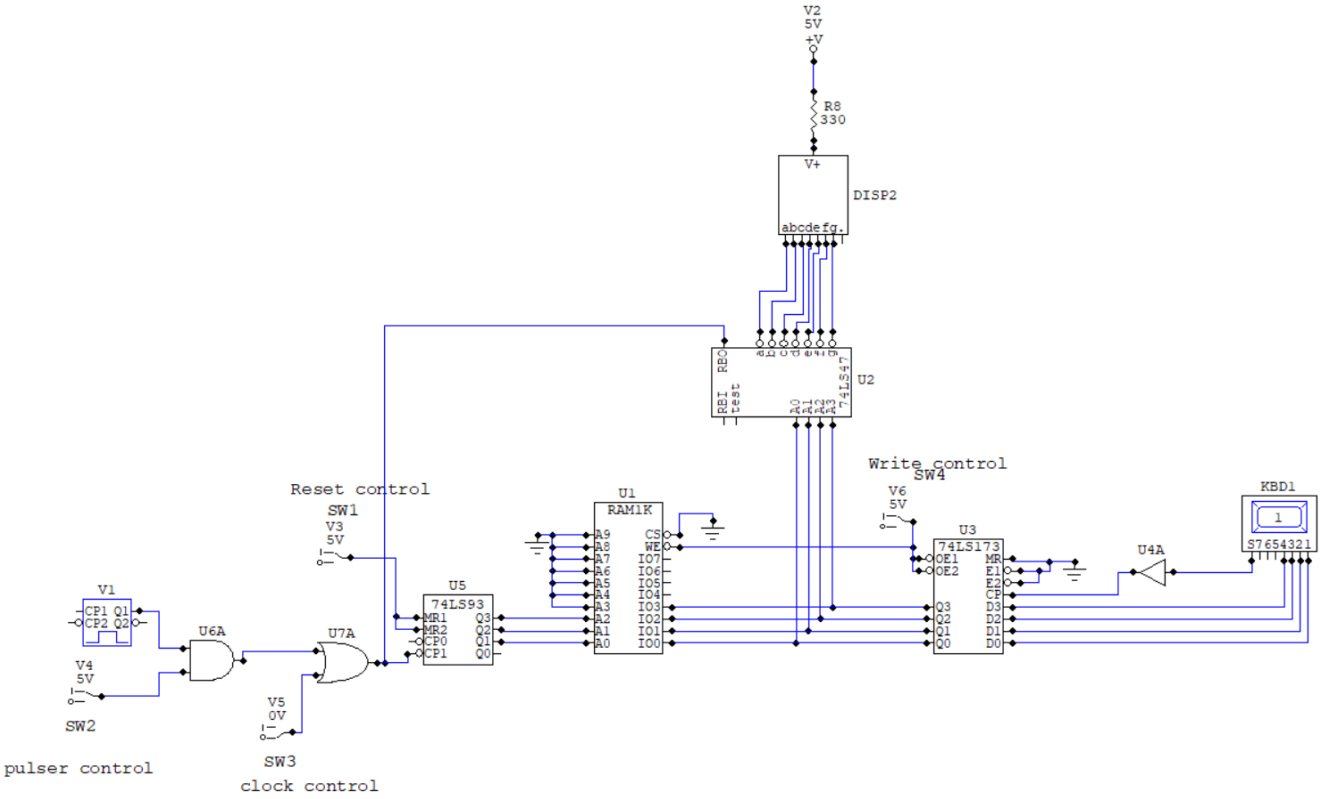
ICs used:-

- IC74LS93:-1 quantity
- RAM1K:-1 quantity
- IC 74LS173:-1 quantity
- IC 74LS47:-1 quantity

Buffer/Driver:-CD 4050:-1quantity

Components used:- 7-seg display, Logic Gates(and gate;or gate),ASCII Keypad,logic switches(4).

Circuit:Digital circuit for writing the 8-digit roll number using a register into the RAM and reading from the RAM.



Working and Discussion of circuit:

- We have seen the working of ASCII Keypad in the previous experiment.
  - So to give the input of 18EC1021 we have to type 18nj1021 correspondingly in the ASCII Keypad.
- IC 74LS173:Quad D-type flip-flops with positive-edge trigger and 3-state outputs.
  - 16-pin DIP: 4D's,4Q's,OE_1',OE_2',IE_1',IE_2',CP,MR,V_{cc},GND.
  - When IE_1',IE_2'=0,data on D inputs loaded into the register with (0->1 edge) transition on CP input.
  - MR:asynchronous active high clear input.
  - IE_1',IE_2':always enabled('0').
  - OE_1',OE_2':active low output enable.if either one of them(or both) is high ,data at Q outputs is tristated.only if both of them are low,register data is available at Q outputs this is controlled by logic switch switch **SW4**(write control).
  - CP:it is connected to strobe output of ASCII keypad through non-inverting buffer CD4050,to provide necessary delay of clock pulse after data are presented at Dinputs.
- RAM 1K: it can store 1024 characters,each having 8-bits.
  - For our experiment we will access only 8 characters,each with 4-bits,so we connect 4-IO's(inputs) of this to the 4 outputs Q's(of 74LS173).
  - WE: it decides whether we have to read or write into the RAM,it is controlled by the same switch **SW4**(write control).
- IC 7493:4-bit binary ripple counter,we use mod-8 counter(CP_1',Q_3,Q_2,Q_1),as it is required to get access to the first 8 locations of RAM.
  - MR_1,MR_2:asynchronous active high reset inputs,whenever both are high then it gives the output of 000 at outputs, this will be kept low all the time except at beginning,it is controlled by logic switch **SW1**(reset control).
- Pulser:while writing into RAM,manual clock pulses(negative-edge trigger) are fed to CP_1' input via logic gate **SW3**(clock control),so that address $A_2A_1A_0$ is increased seven times(manually using the clock switch).While reading contents of RAM,however free-running clock(from pulser) is fed to

CP_1' of 7493.Logic switch **SW2**(pulser control) selects between manual clock pulses(for writing) and automated(pulser) clock pulses(for reading).

Result:

❑ **Writing**:-(for writing 18EC1021 into RAM)

➔ Initial setup for writing:

- ❑ Reset counter to $Q_3Q_2Q_1$ to 000:connect SW1->'1' and then connect to '1' for the entire writing part.
- ❑ Connect SW2->0 so that we are taking the manual clk pulses,for the entire writing part.
- ❑ Connect SW3->0,SW4->1(not enabling writing into RAM).

➔ Repeating steps for the entire setup:for 8 digits 18nj1021

- ❑ Type the digit from ASCII which gives corresponding 4-bit output,these will be stored in the register.
- ❑ SW4->0 which will make those outputs write in the particular address of RAM.
- ❑ SW4->1,so that the next giving input may not affect the present address.
- ❑ SW3->1 and SW->0 ,this will make 1->0 transition i.e, negative edge trigger which will increment values in the counter(increment address cell).

Storage In RAM :

Address	4-bit value	Digit which will display for corresponding 4-bit input
000	0001	1
001	1000	8
010	1110	E
011	1010	C
100	0001	1
101	0000	0
110	0010	2
111	0001	1

❑ Reading:

- ➔ SW1 -> 1 and SW1 ->0 ,so that the address points at the 000.
- ➔ SW4 ->1 ,such that no writing takes place from the register.
- ➔ SW3 ->0 ,to avoid the manual clk pulses.
- ➔ SW2 ->1 ,to select the automated clk pulse over manual clk pulse.
- ➔ So,at the counter: for each negative-edge trigger in the clk pulse the address value gets incremented.
- ➔ This will dynamically display the roll number 18EC1021 in the order.
- ➔ To avoid the delays in the logic gates we have connected the RBO of 7-segment display to the output of the OR gate which will make sure blinking in the circuit doesn’t happens.