VLSI Engineering Laboratory
Experiment 1
CMOS inverter design

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AIM:

To simulate a CMOS inverter in LT-spice and to observe the effect of the parameters like width(W) and length(L) of transistors on the voltage transfer characteristics and to see the effect of it on the charging and discharging time taken for it.

Circuit diagram :-

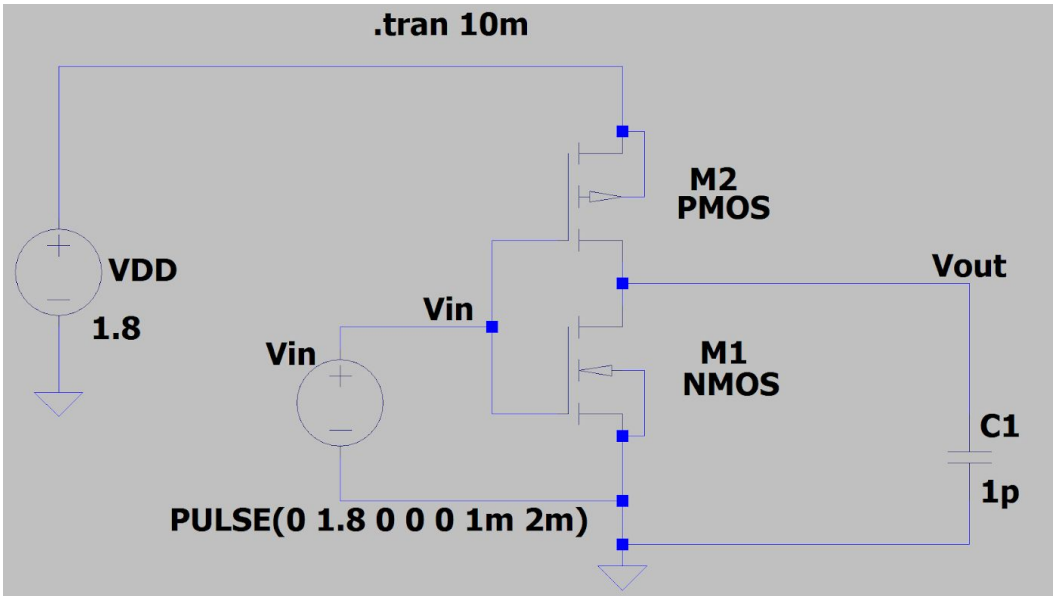
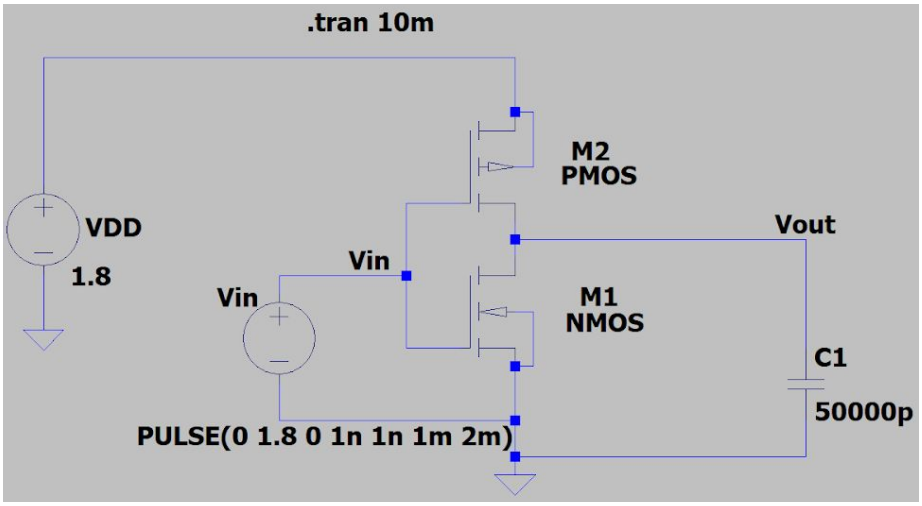


Fig 1:-Circuit diagram of the CMOS inverter design.

Fig 2:- CMOS inverter design to examine the charging and discharging effect.



Description :-

1. CMOS inverter is designed as shown above in the LT-spice software.
2. CMOS inverter contains a PMOS and a NMOS transistors with gate and drain terminals of both connected and the source terminals are connected to supply voltage VDD and ground respectively.
3. In LT-spice we make this connection by taking PMOS4 and NMOS4 from the components section in it(These transistors have the same electron and hole mobility by default in the simulator).
4. The body of PMOS is connected to supply voltage and body of the NMOS is connected to ground (i.e., to their respective sources)to remove the body effect on the threshold voltage of transistors.
5. The load capacitor c1 is connected to the drain terminals across which output is measured,this is the capacitance offered by the subsequent transistors(circuit) in a practical connection.
6. The gate terminals of the both transistors are connected to the input supply which is a square pulse here with 50%duty cycle and a time period of 2msec with maximum value of 1.8V and minimum 0V,to observe the nature of the inverter.
7. The input pulse applied is : PULSE(0 1.8 0 0 0 1m 2m)
8. The inverter is designed in the 180nm technology i.e., minimum length of the transistors channel is 180nm.
9. The w/l ratio of the PMOS should be kept higher than that of NMOS because the mobility of the electrons is double that of holes.so to make the strength of both the transistors similar, we set w/l ratio of PMOS double the NMOS.
10. We set VDD to be 1.8V, standard supply voltage.
11. For different cases of width of the transistors and different load capacitances the output is measured.
12. .tran 10m is used to observe the transient response upto 10msec.
13. Output and input characteristics can be observed by clicking on the Vin for input and Vout for output.
14. After the command simulation.we make x-axis to be V(Vin) to observe the voltage transfer characteristics when y-axis is taken to be V(Vout).
15. In voltage transfer characteristics we observe the switching threshold(Vth),which is the point of intersection of the VTC and Vout=Vin plots,and observe the change of Vth with change in the transistor parameters.
16. Voltage transfer characteristics can also be found by changing the simulation command to .dc Vin 0 1.8 0.0001(DC-Sweep),it will make the Vin change from 0V to 1.8V in the steps of 0.0001V.

Simulation results :-

Transient characteristics V(Vout) and V(Vin) vs t

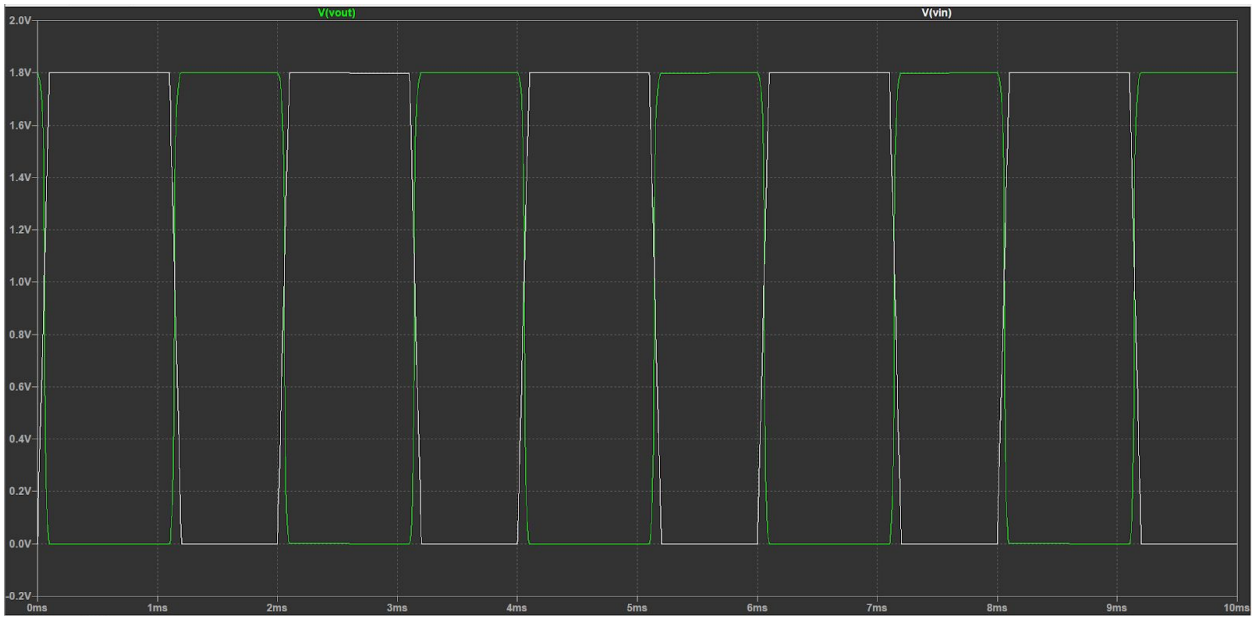


Fig 3:-PMOS width=5u ; NMOS width=2.5u ; C1=1pF

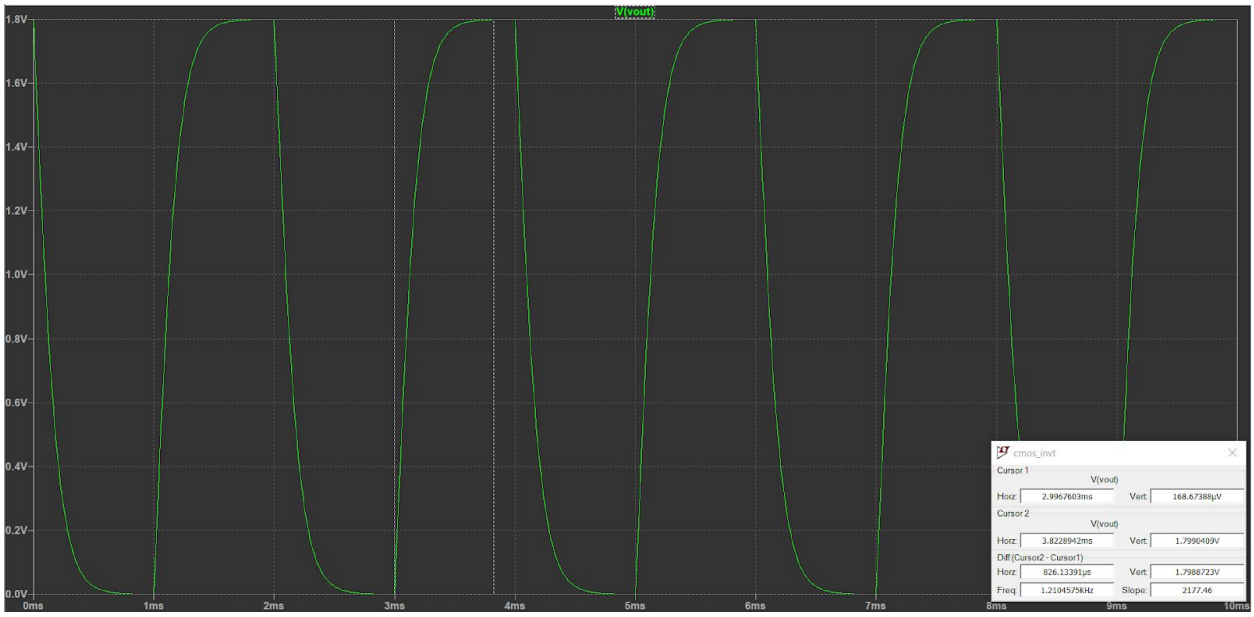


Fig 4:-PMOS width=2.5u ; NMOS width=2.5u ; C1=50000pF
Charging time=826.13 usec

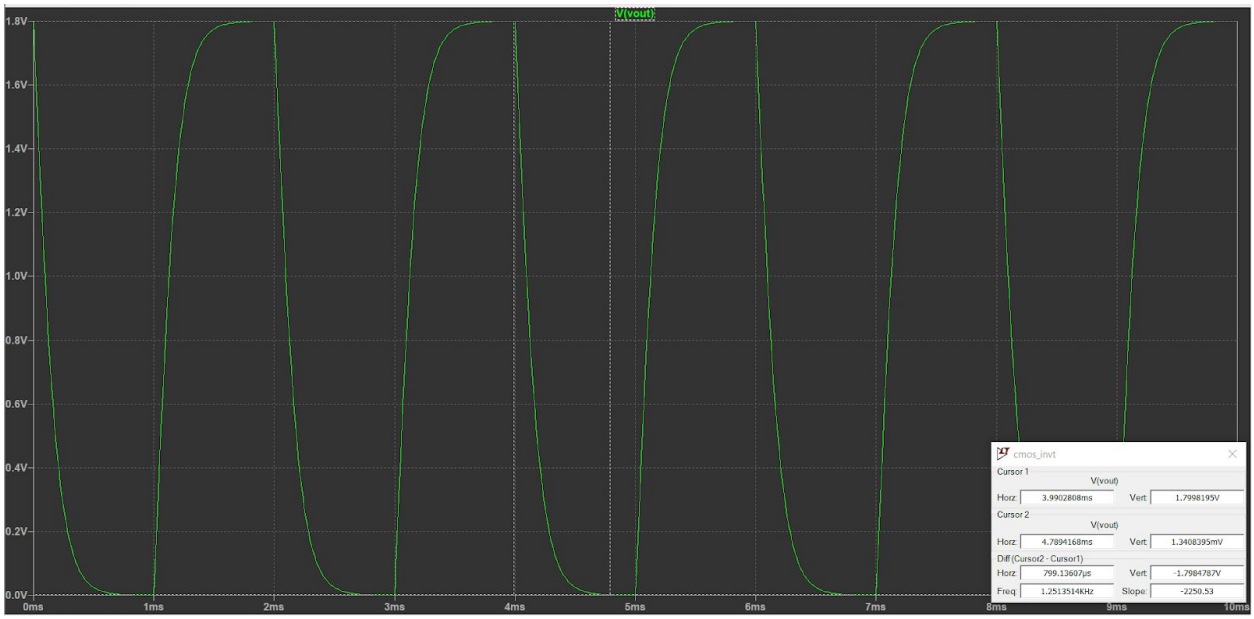


Fig 5:-PMOS width=2.5u ; NMOS width=2.5u ; C1=50000pF
Discharging time=799.13 usec

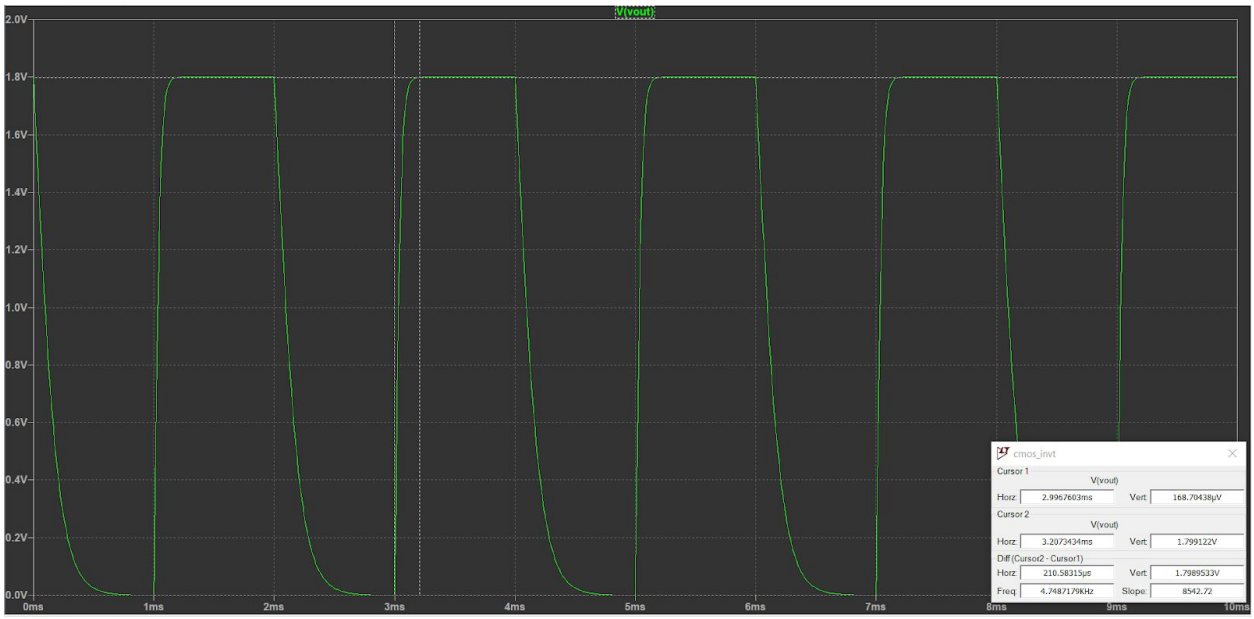


Fig 6:-PMOS width=10u ; NMOS width=2.5u ; C1=50000pF
Charging time=210.583 usec

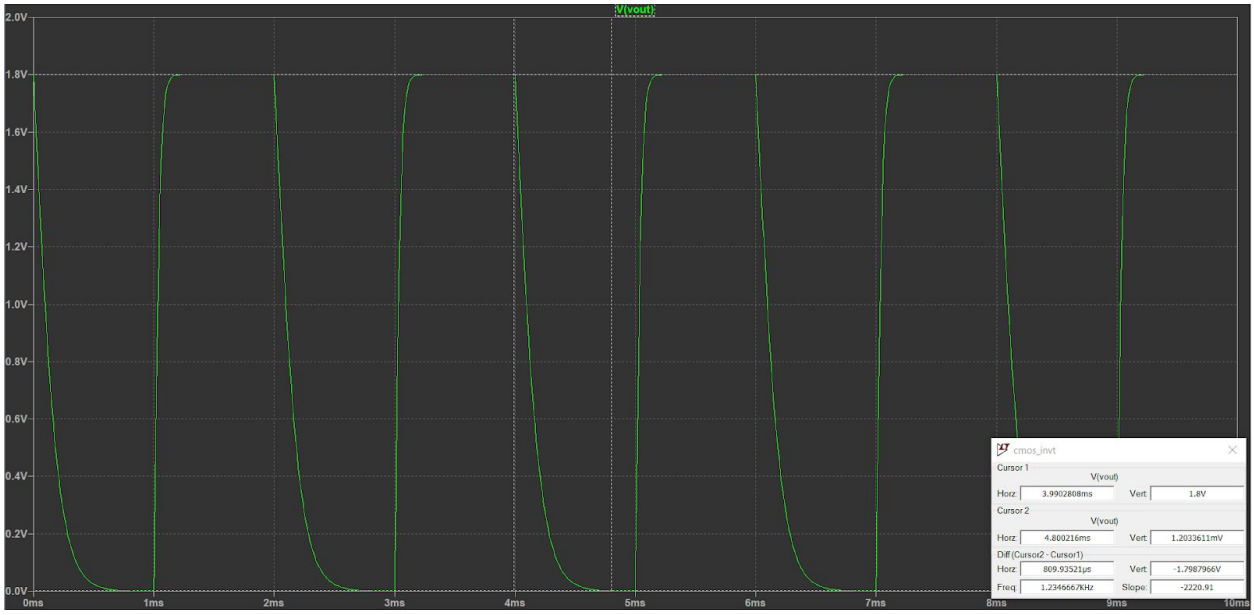


Fig 7:-PMOS width=10u ; NMOS width=2.5u ; C1=50000pF
Discharging time=809.94 usec

Voltage Transfer Characteristics :- V(Vout) vs V(Vin)

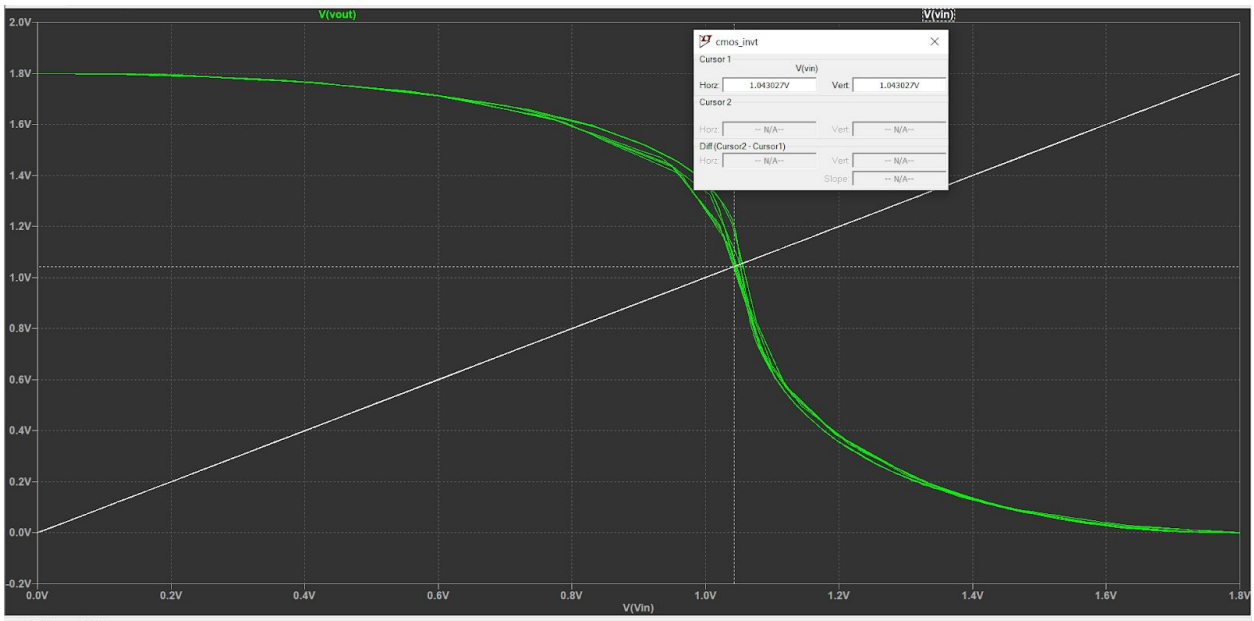


Fig 8:-PMOS width=5u ; NMOS width=2.5u ; C1=1pF
Vth = 1.043 V

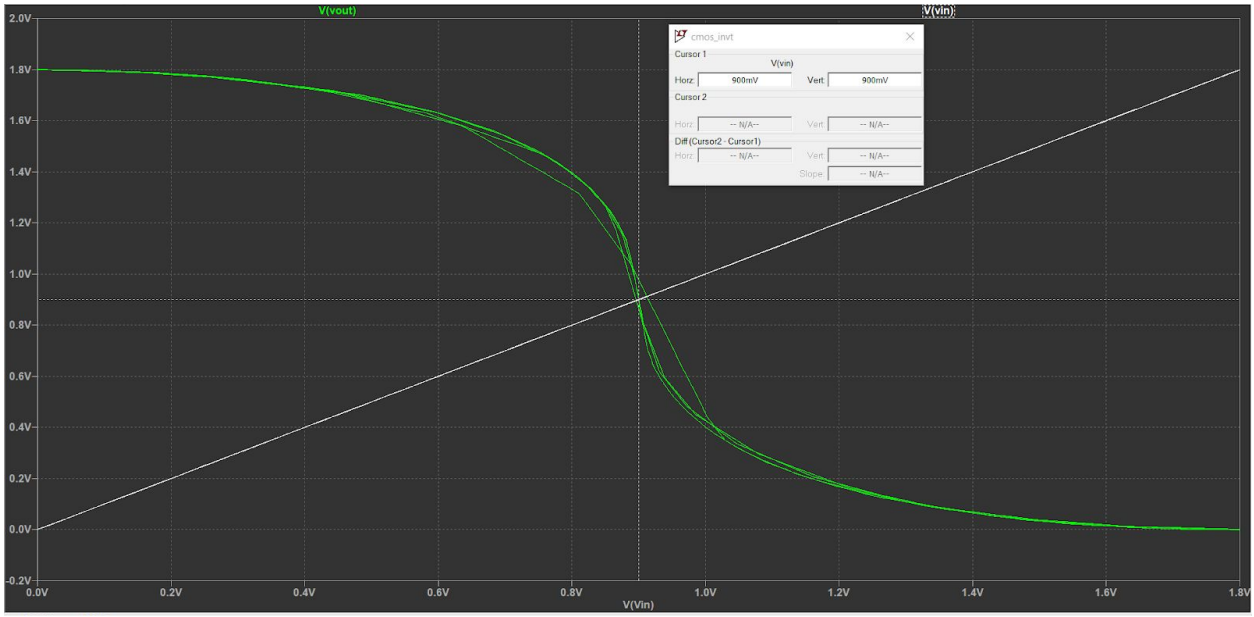


Fig 9:-PMOS width=2.5u ; NMOS width=2.5u ; C1=1pF

Vth = 0.9 V

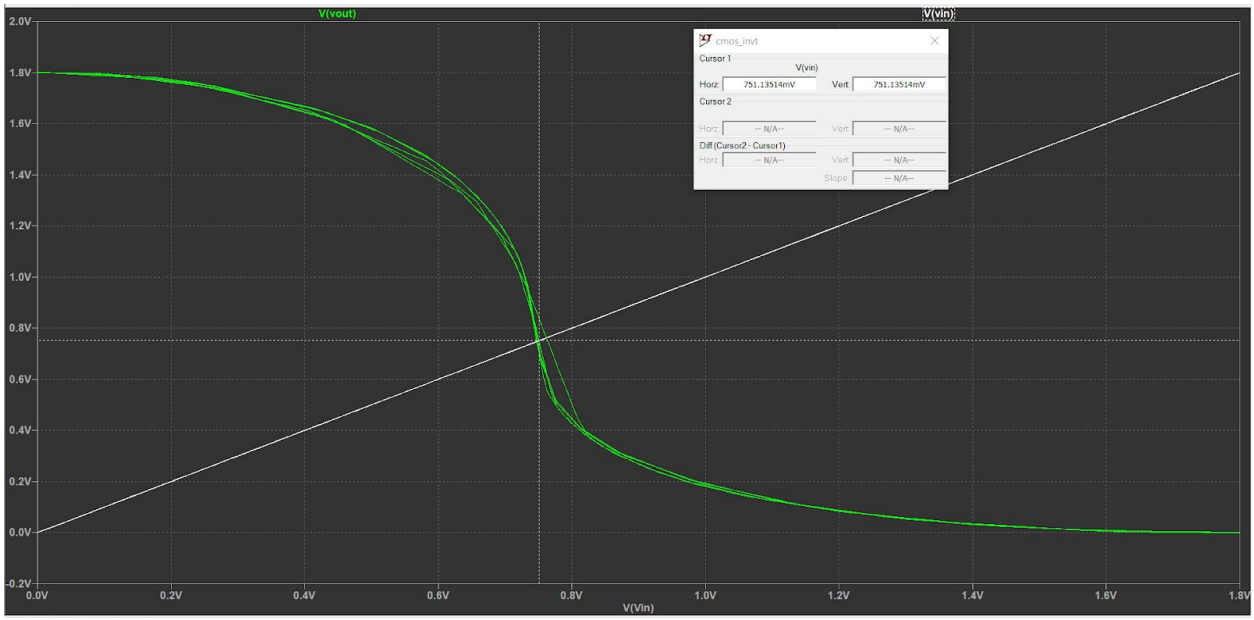


Fig 10:-PMOS width=2.5u ; NMOS width=5u ; C1=1pF

Vth = 0.75114 V

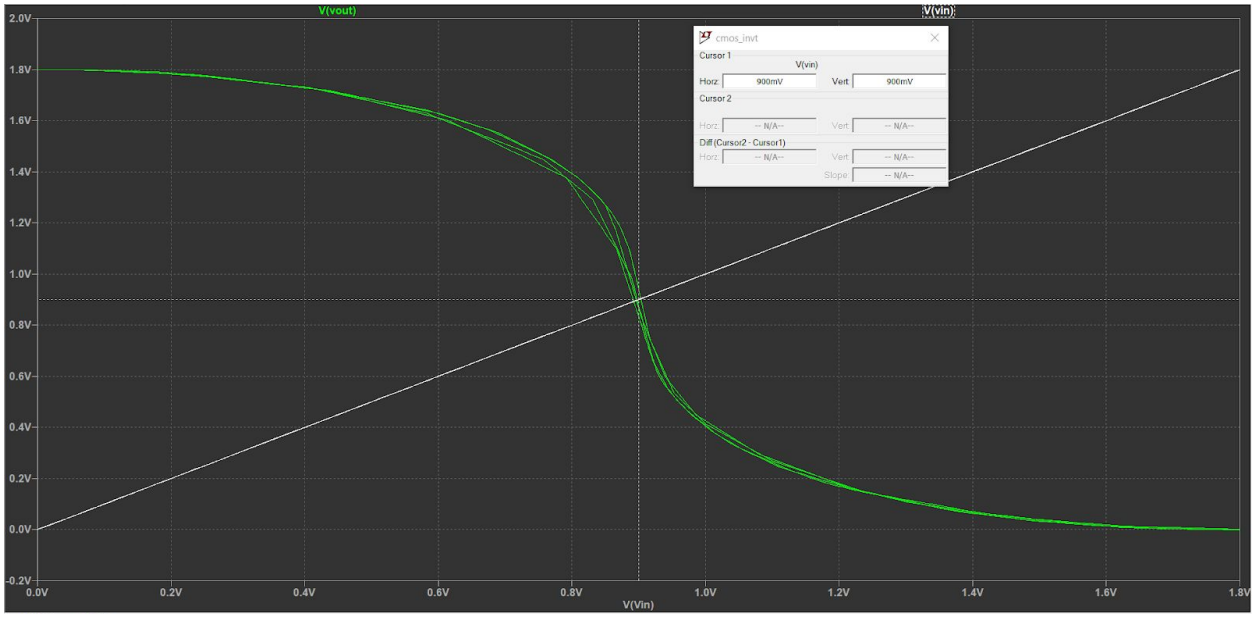


Fig 11:-PMOS width=13u ; NMOS width=13u ; C1=1pF

Vth = 0.9 V

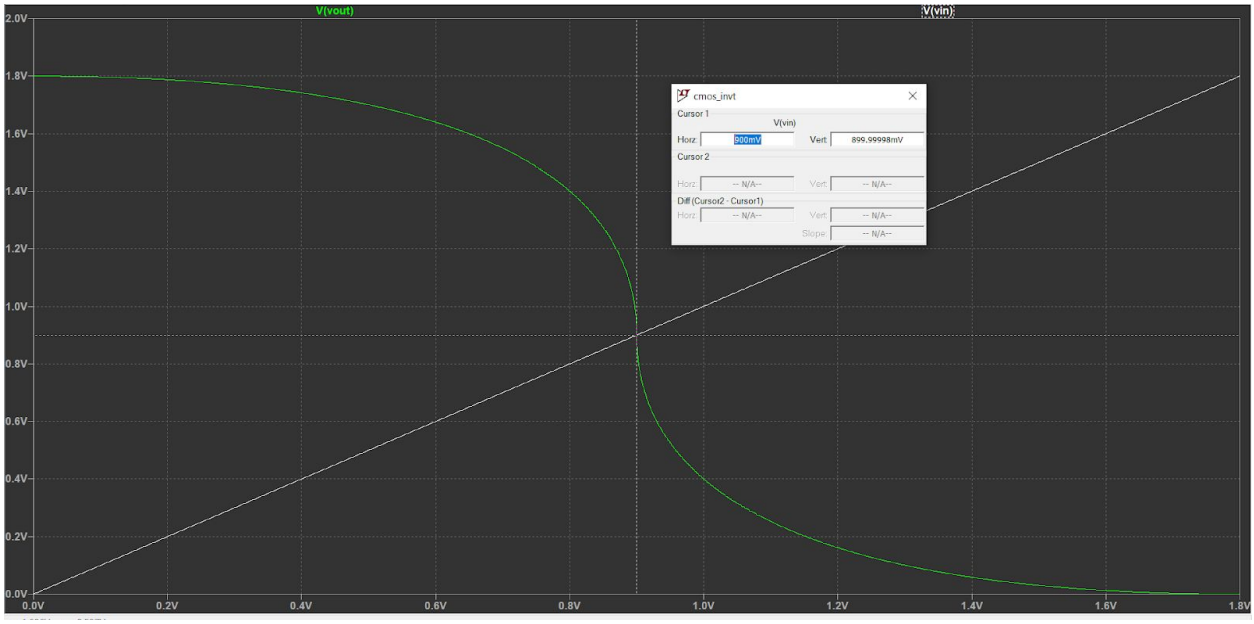


Fig 12:-PMOS width=13u ; NMOS width=13u ; C1=1pF(with different simulation command .dc Vin 0 1.8 0.0001 in place of .tran 10m)

Vth = 0.9 V

Discussion and observations :-

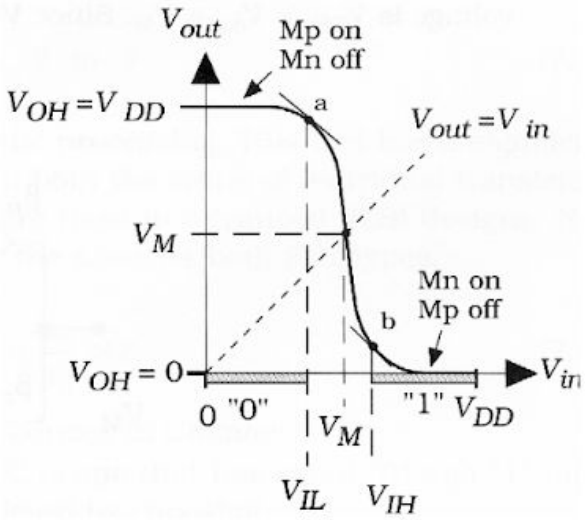
1. In this experiment,we simulated a CMOS inverter in LT-spice and observed its characteristics and dependences on the parameters of the transistors used in the CMOS.
2. The high speed switching characteristics of CMOS was visible in Fig.3 where the rise and fall time of the input signal was very small and the output signal also had small rise and fall times.
3. By changing output capacitance to C1=50000PF in fig.4,there is an exponential rise which is due to RC time constant offered by transistors and output capacitance.
4. From the low-high transition,(logic 0 to logic 1),gate response is determined by the time taken by capacitor C1 to charge through the resistor Rp(resistance offered by the PMOS,which is the resistance looking into drain of it).during this transition the NMOS will be in off stage(as gate voltage is zero the Vgs=0).so,the charging time taken by CMOS depends on the PMOS.
5. From the high-low transition,(logic 1 to logic 0),gate response is determined by the time taken by capacitor C1 tov charge through the resistor Rn(resistance offered by NMOS,which is the resistance looking into the drain of NMOS),during this transition PMOS will be in off stage(as gate voltage is equal to supply voltage then Vsg=0).so,v the discharging time taken by CMOS depends on the NMOS.
6. From Fig 4 and 5 we can see both the times(charging and discharging times) are equal when W/L of both the transistors are equal(in the simulator the NMOS4 and PMOS4 have the same electron and hole mobility built in and with same W/L charge flow will be equal).

$$I_{Dn} = \frac{\mu_n C_{OX}}{2} \frac{W}{L} (V_{GSn} - V_{tn})^2 :$$

7. In Fig 6 and 7, W/L of PMOS is 4 times of the NMOS(charge flow increases by 4 times,evident from the current flow formula for the MOS transistor) due to which the Charging time is 4 times lesser than that of Discharging time.
8. From Fig 5 and 7 we can verify that discharge time of the CMOS depends only on the W/L of the NMOS and not that of PMOS(since,it is in cutoff).
9. It is observed from Fig 8,Fig 9. When the W/L of PMOS is increased,keeping the W/L of NMOS constant the transfer characteristics curve shifts to the right and as W/L of PMOS decreases then the curve shifts to the left.

10. In Fig 9,Fig 10,it is observed that if the W/L of NMOS increases,keeping the W/L of PMOS constant the transfer characteristics curve shifts to the left and as W/L of NMOS decreases then the curve shifts to the right.
11. It is observed from Fig 9 and Fig 11,when we increase or decrease the W/L of NMOS and PMOS by keeping them equal, then the transfer characteristics will not be sifted.Above three results can be evident from the below formulae.

Voltage transfer characteristics of a CMOS inverter



a,b are points where the magnitude of the slopes=1

12. Analytically we can obtain the formulae for the Vm which is switching threshold and it is:

$$V_M = \frac{VDD - |V_{tp}| + V_{tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1+\sqrt{\frac{\beta_n}{\beta_p}}}$$

where, $\beta_n = k'_n \frac{W}{L}$

13. In our simulator $k_n=k_p$ (by default for NMOS4 and PMOS4,in simulator the electron and hole mobility will be equal),with the same W/L for NMOS and PMOS V_M = VDD/2 = 0.9 V .
14. In plots,there were multiple lines seen instead of a single smooth curve due to the multiple iterations taking place in Ltspice.We made the DC-sweep to yield a single smooth curve(Fig 12)

Summary:-

The CMOS inverter is an important circuit device which provides fast switching and low power dissipation,which are desired qualities in inverters for most circuit design.