VLSI Engineering Laboratory
Experiment 2
Common Source Amplifier

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AIM:

To study the transient response and frequency response of the common source amplifier with resistive load using LT-spice software.

Circuit diagram :-

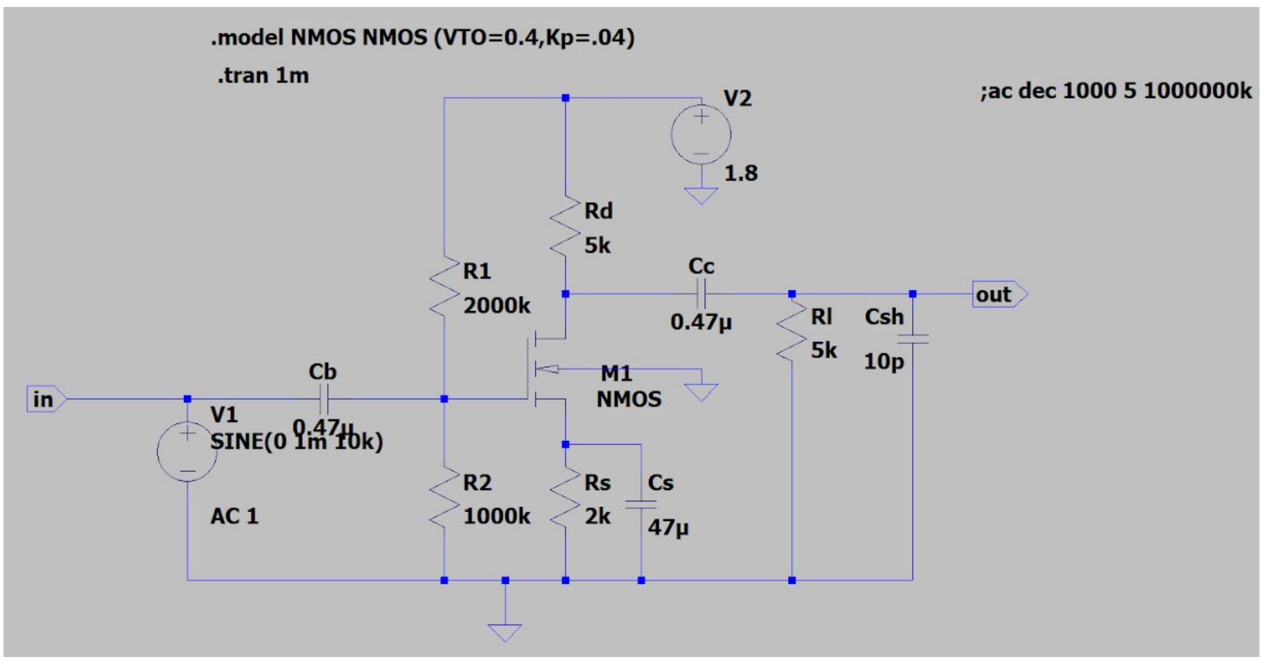

Fig.1:Circuit diagram of common source amplifier with the resistive load

Description:-

1. Common source amplifier with resistive load is designed as shown above in the LT-spice simulator.
2. The first step of designing an amplifier circuit involves designing the biasing network of the transistor.
3. To get the linear amplification of the signal,it is necessary that the transistor operates in the saturation region i.e., $V_{ds} > V_{gs}$-V_{Th}.

4. Resistive divider biasing with source degenerator is the best biasing to obtain a maximum stabilised amplification.
5. We have taken NMOS4 for the NMOS from the components which has built in values for the parameters of transistor,so to set the VTO and the KP for the transistor,we can write some code in the spice like **.include NMOS NMOS (VTO=0.4 KP=0.04),** this will do the need.
6. R1,R2 resistors are used to set the DC voltage of the gate
7. The resistor divider should consume as low power as possible so we have to make the resistances of R1 and R2 as high as practically possible.
8. To observe the transient response of the transistor we have to make sure the Q-point of the transistor lies in the mid-point of the saturation region so as to get the maximum swing in the output.
9. The source resistor in the biasing scheme used will ensure to stabilise the Q-point of the transistor from
10. The changes in the parameters of the transistor,resistance with 2K will be used to ensure that the voltage across it lies between 180mV to 200mV.
11. The value of R_d should be taken in such a way that the transistor gives maximum swing possible i.e.The Q-point lies at the mid-point of saturation region.
12. Sinusoidal signal with amplitude of 1m and frequency of 10KHz is taken to observe the amplification of the signal at the output.
13. The source resistor used to stabilise the Q-point reduces the gain of the amplifier, therefore to reduce this effect a bypass capacitor C_s is used in parallel to the source resistor
14. The capacitor C_b is used to avoid any DC voltages which are coming up from the voltage source which gives the sinusoidal signal.
15. The capacitor C_c is used to DC-offset the signal at the output.
16. The capacitors mentioned above are kept as high as possible to make the lower 3dB cutoff frequency to zero.
17. Transient response of the circuit can be obtained by changing the simulation command to .tran 10m, this will examine the response of the signal for 10msec..
18. Frequency response of the signal can be obtained by the simulation command to .ac dec 1000 5 1000000k,this will make the ac analysis of the signal input and takes 1000 points per decade and simulate from 5Hz to 1000000KHz frequency.

Results :-
a.transient response:-

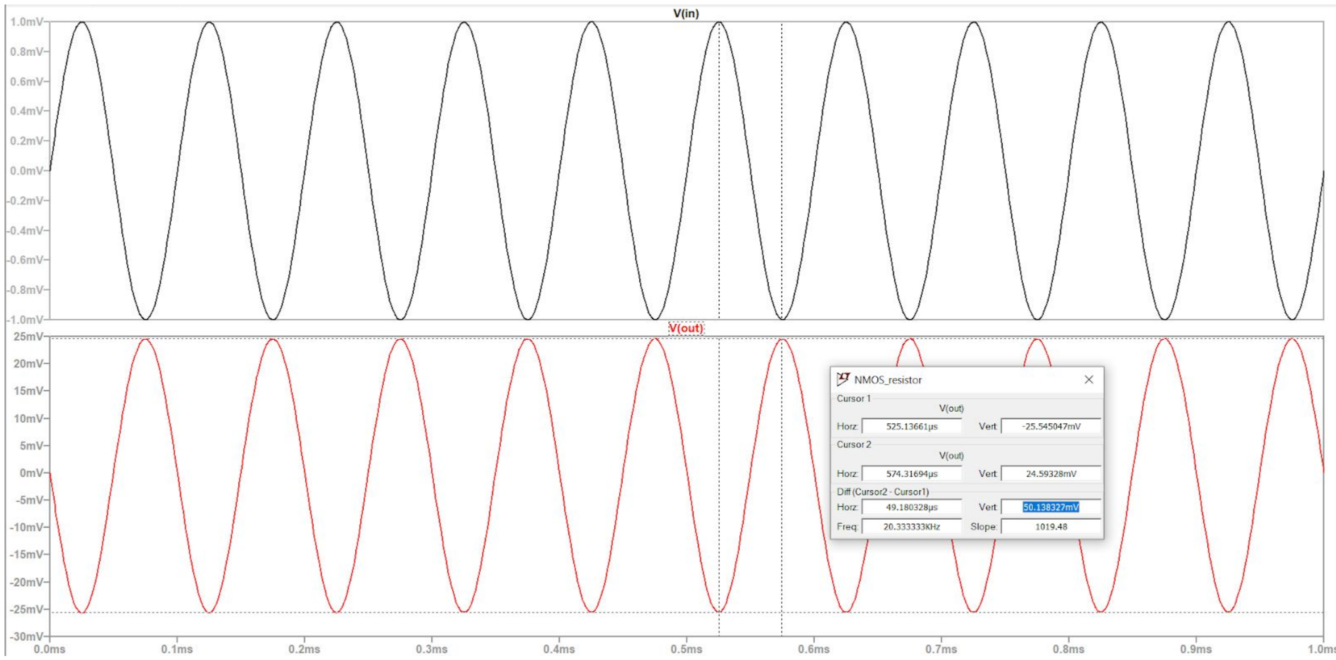

Fig.2:-transient response of the Fig.1
Gain = 50.138/2 = 25.069

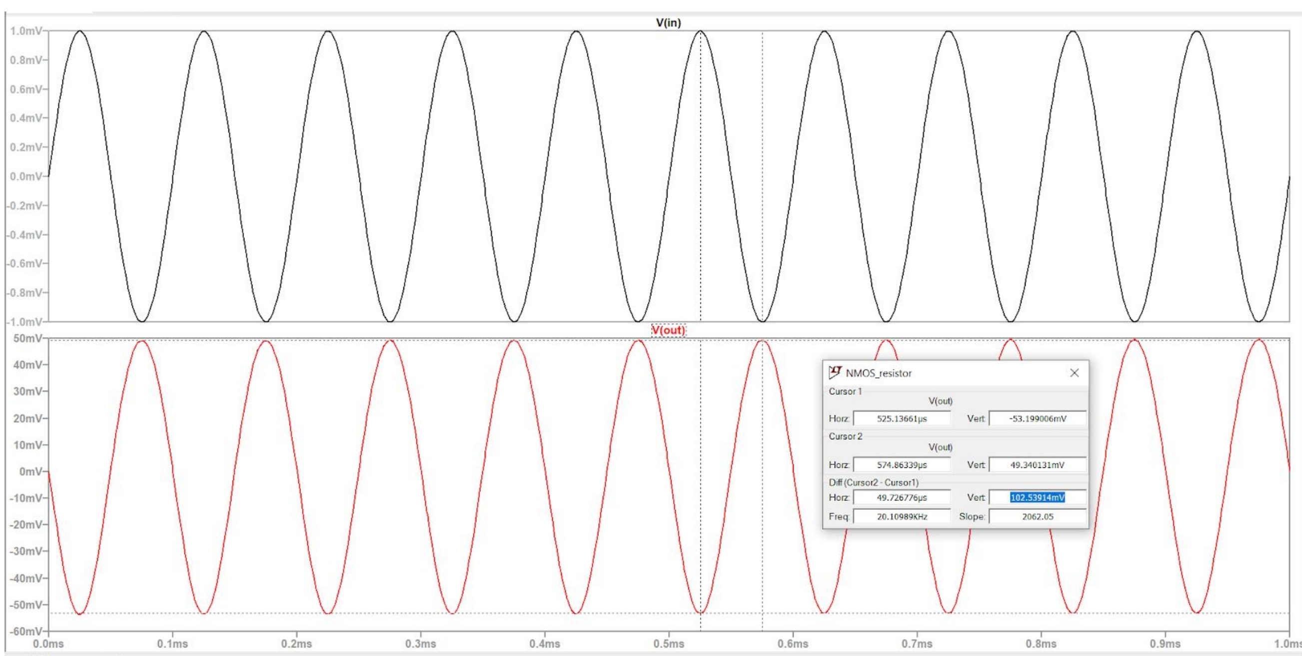

Fig.3:-Circuit with W=10 ; KP=0.04 ; R_s=2Kohm ; Rd &Rl =5Kohm ; C_s=47uF
Gain = 102.539/2 = 51.269

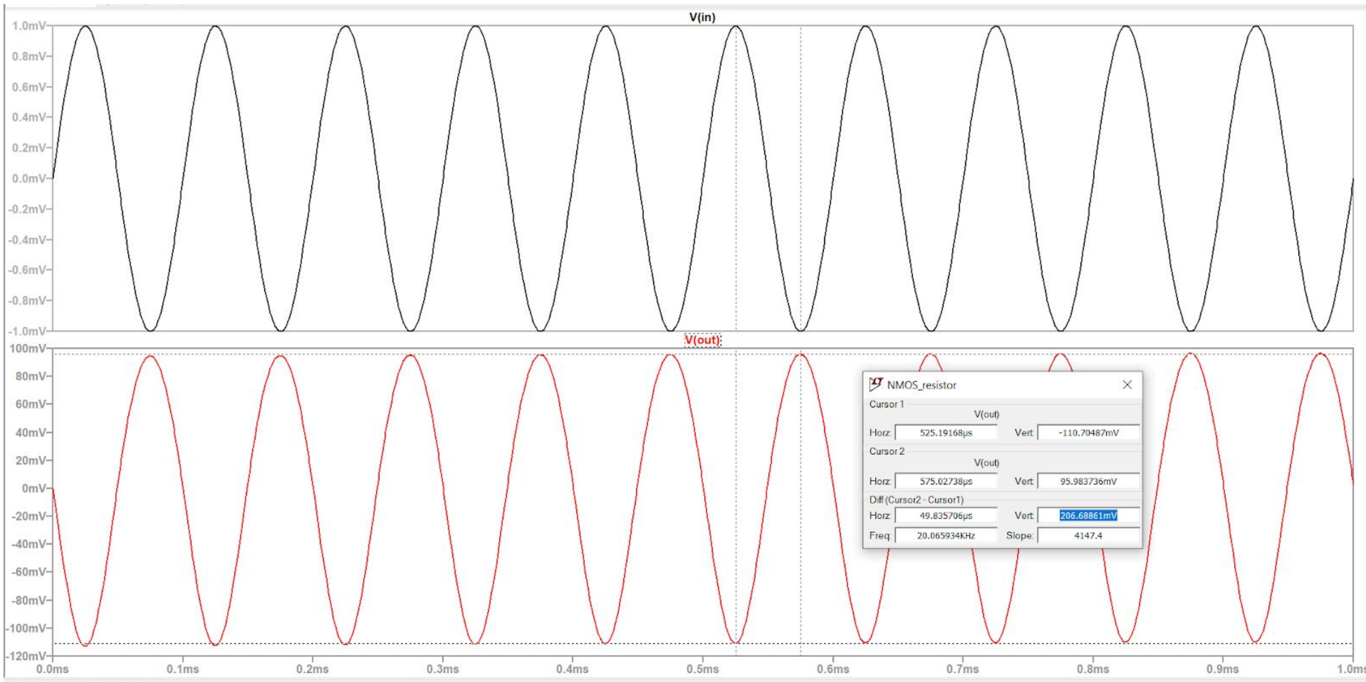

Fig.4:-Circuit with W=10 ; KP=0.16 ; R_s=2Kohm ; Rd &Rl =5Kohm ; C_s=47uF
Gain = 206.689/2 = 103.3445

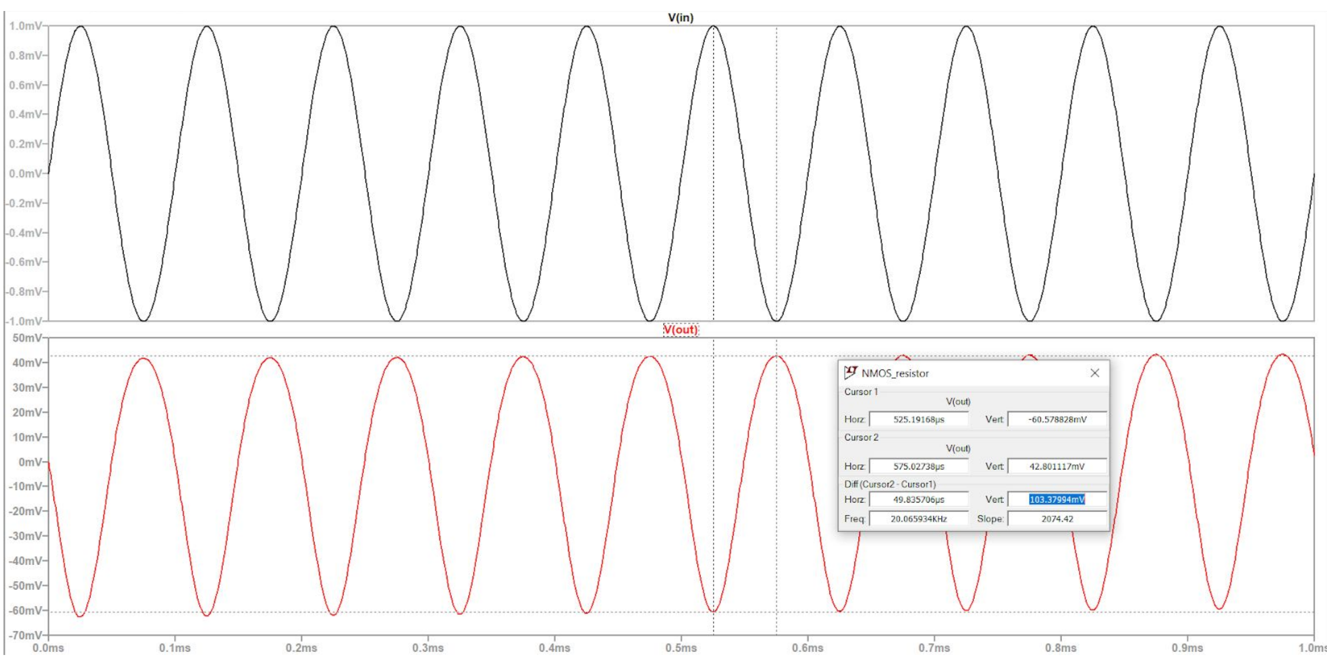

Fig.5:-Circuit with W=10 ; KP=0.16 ; R_s=8Kohm ; Rd &Rl =5Kohm ; C_s=47uF
Gain = 103.38/2 = 51.69

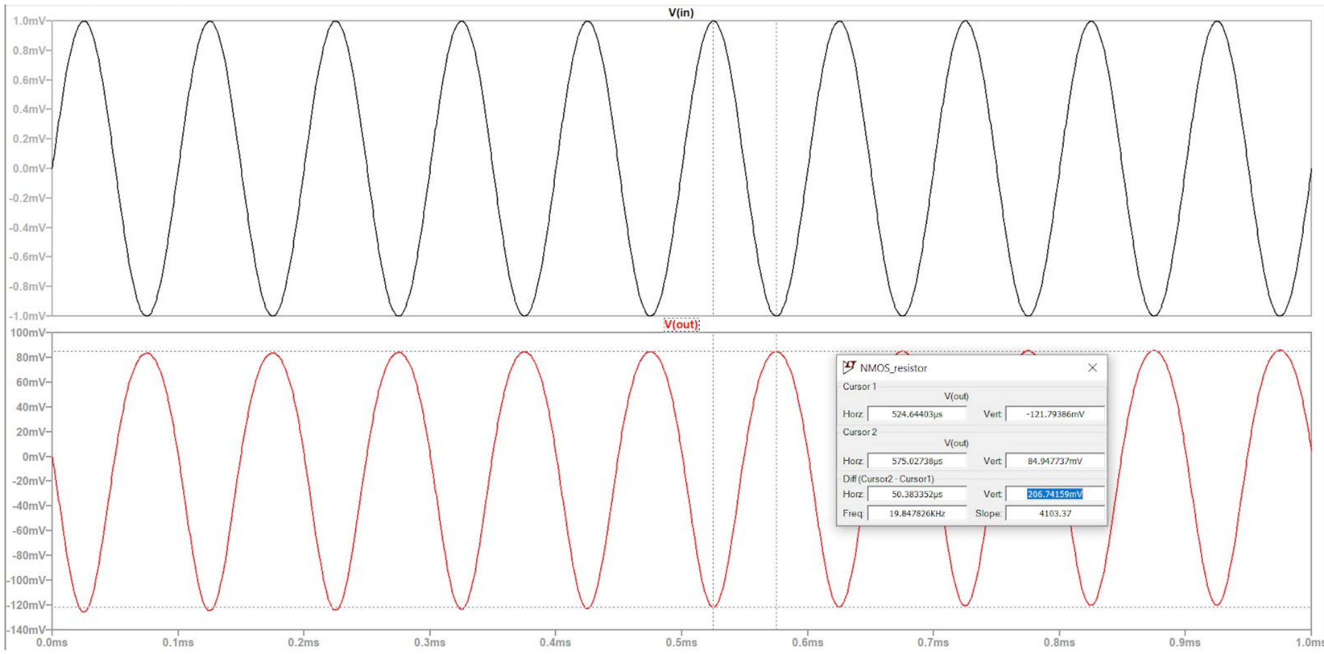

Fig.6:-Circuit with W=10 ; KP=0.16 ; R_s=8Kohm ; Rd &Rl =10Kohm ; C_s=47uF
Gain = 206.741/2 = 103.37

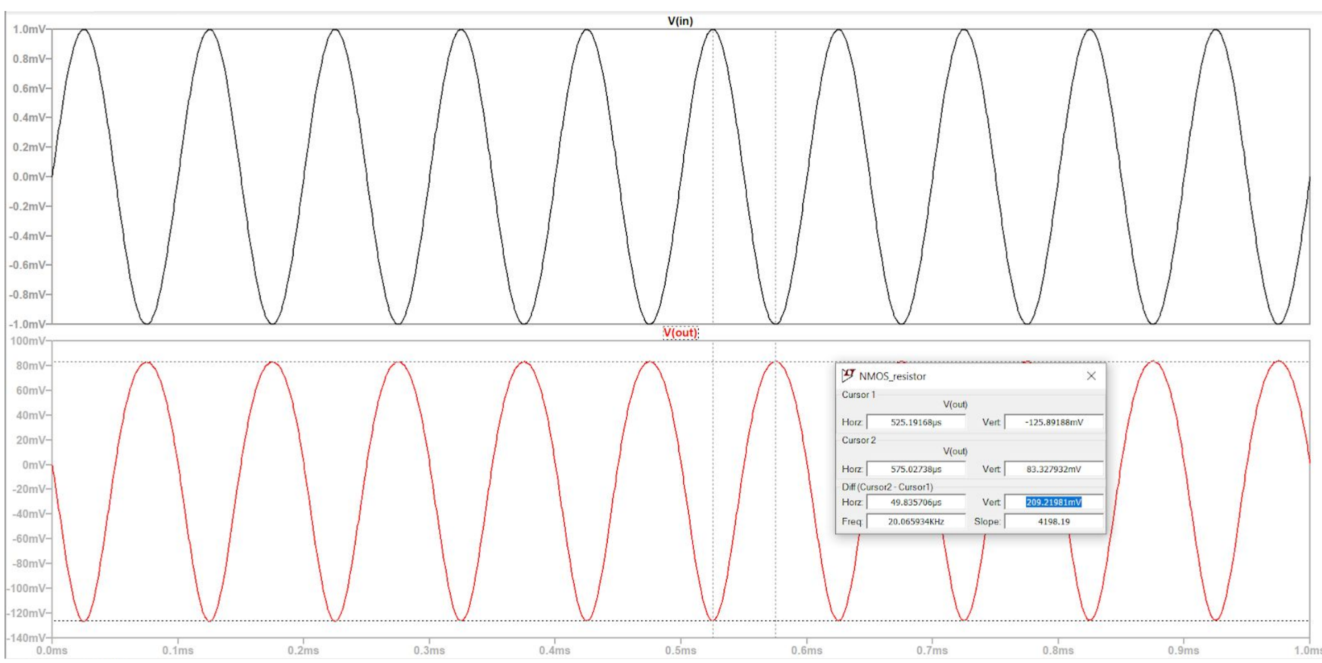

Fig.7:-Circuit with W=10 ; KP=0.16 ; R_s=8Kohm ; Rd &Rl =10Kohm ; C_s=4700uF
Gain = 209.22/2 = 104.61

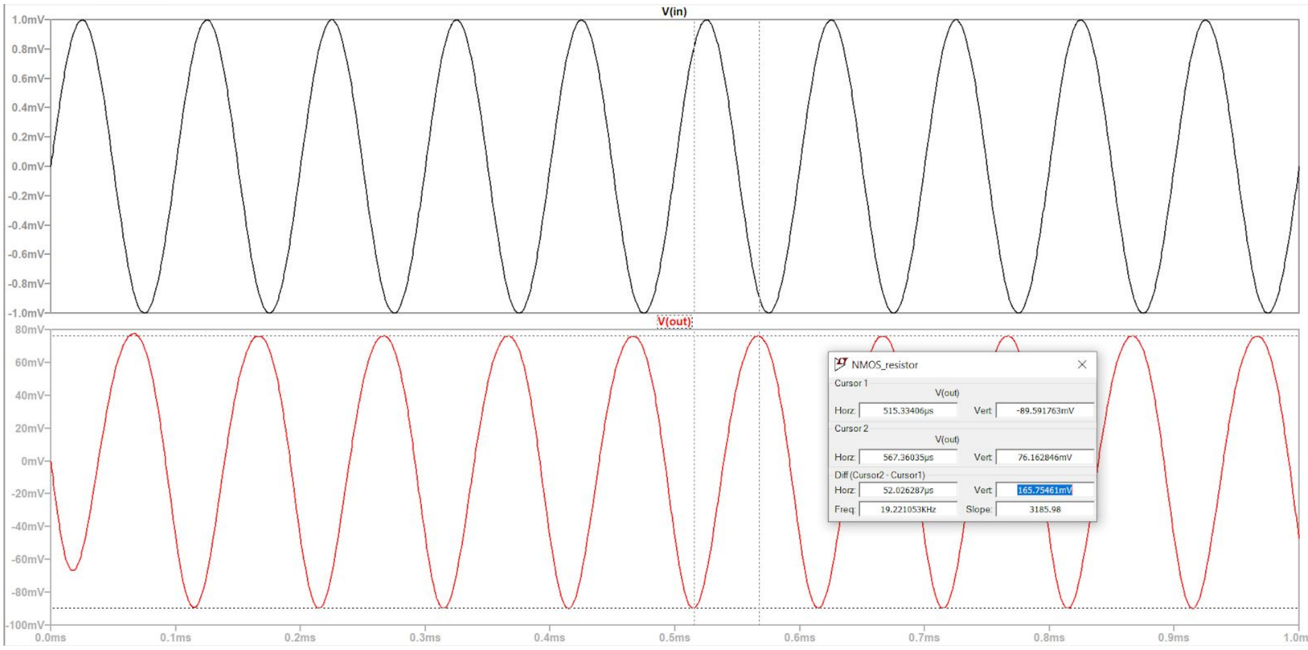

Fig.8:-Circuit with W=10 ; KP=0.16 ; R_s=8Kohm ; Rd &Rl =10Kohm ; C_s=0.47uF
Gain = 165.75/2 = 82.875

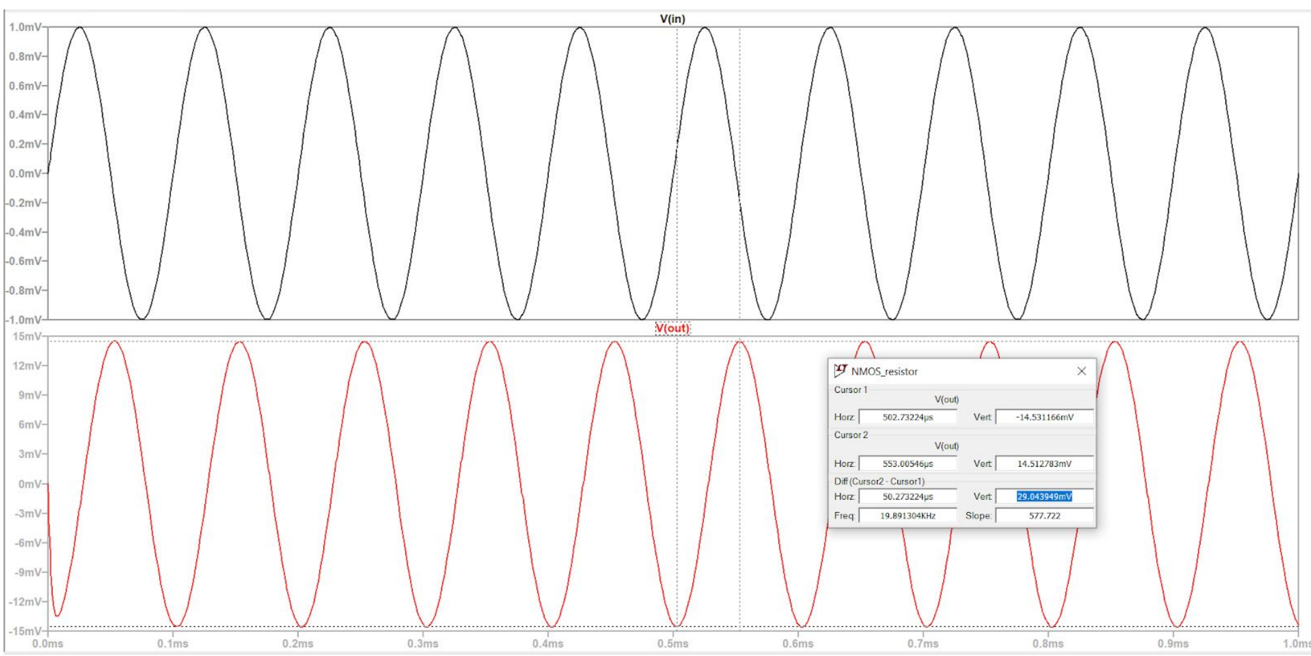

Fig.9:-Circuit with W=10 ; KP=0.16 ; R_s=8Kohm ; Rd &Rl =10Kohm ; C_s=0.047uF
Gain = 29.044/2 = 14.522

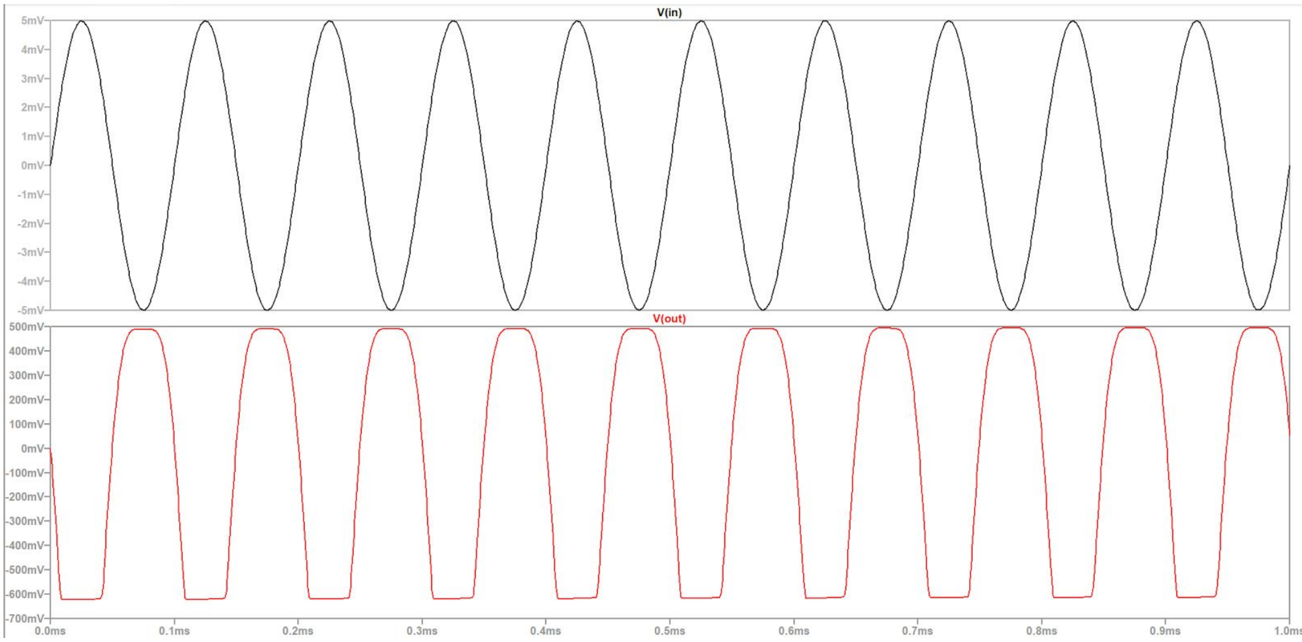

Fig.10:-Circuit with W=10 ; KP=0.16 ; R_s=2Kohm ; Rd &Rl =10Kohm ; C_s=47uF
Clipping of the output

b.Frequency response:-

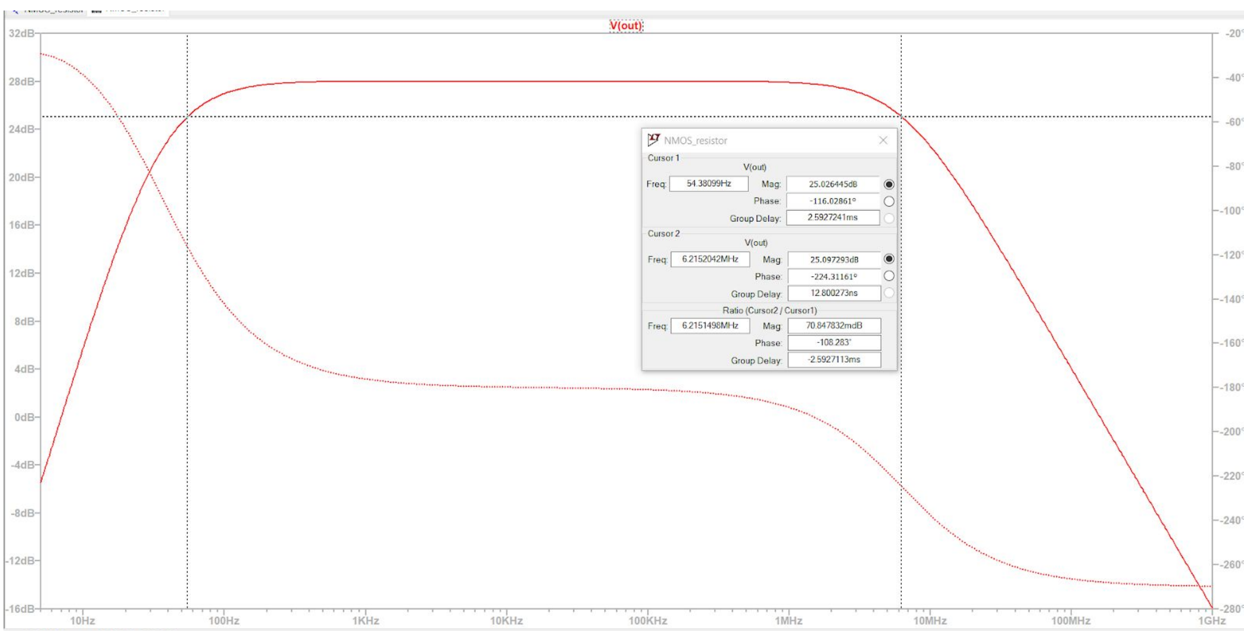

Fig.11 :- Frequency response of the circuit shown(Fig.1)
Gain =28 dB ; Fh=6.21 MHz ; Fl=54.38Hz

Effect of C_b on lower cutoff frequency

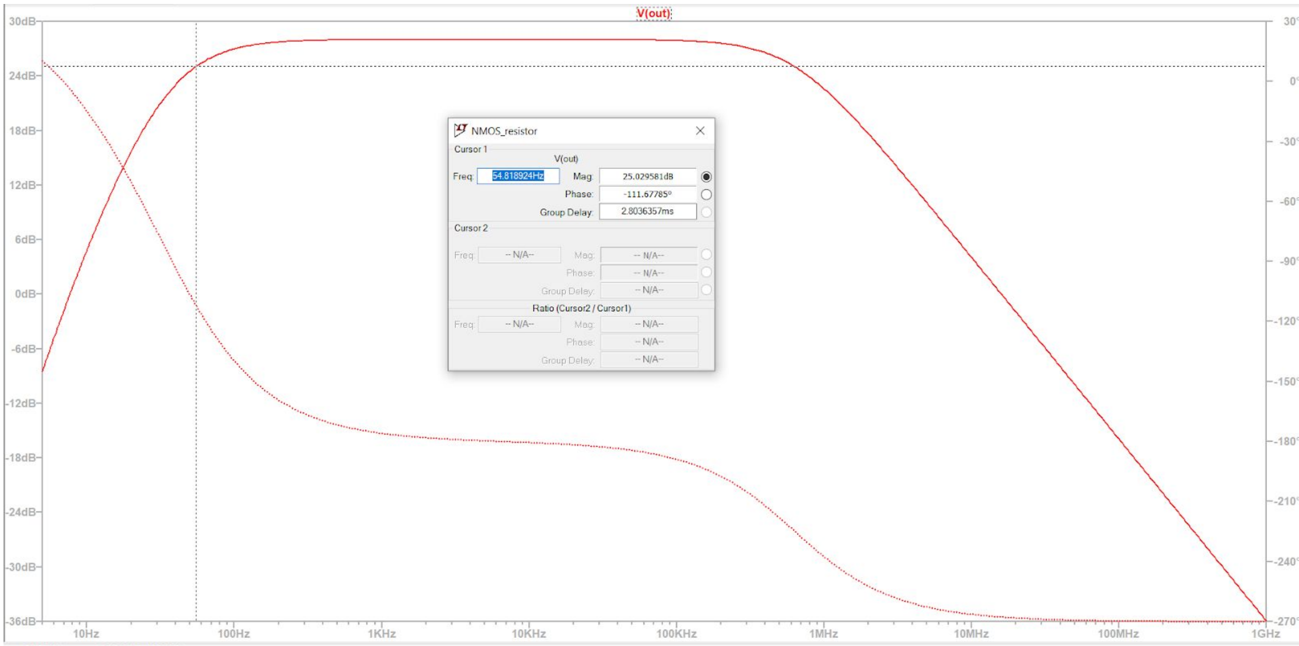

Fig.12 :- circuit(Fig.1) with C_b=0.047 uF
Gain =28 dB ; Fl=54.818 Hz

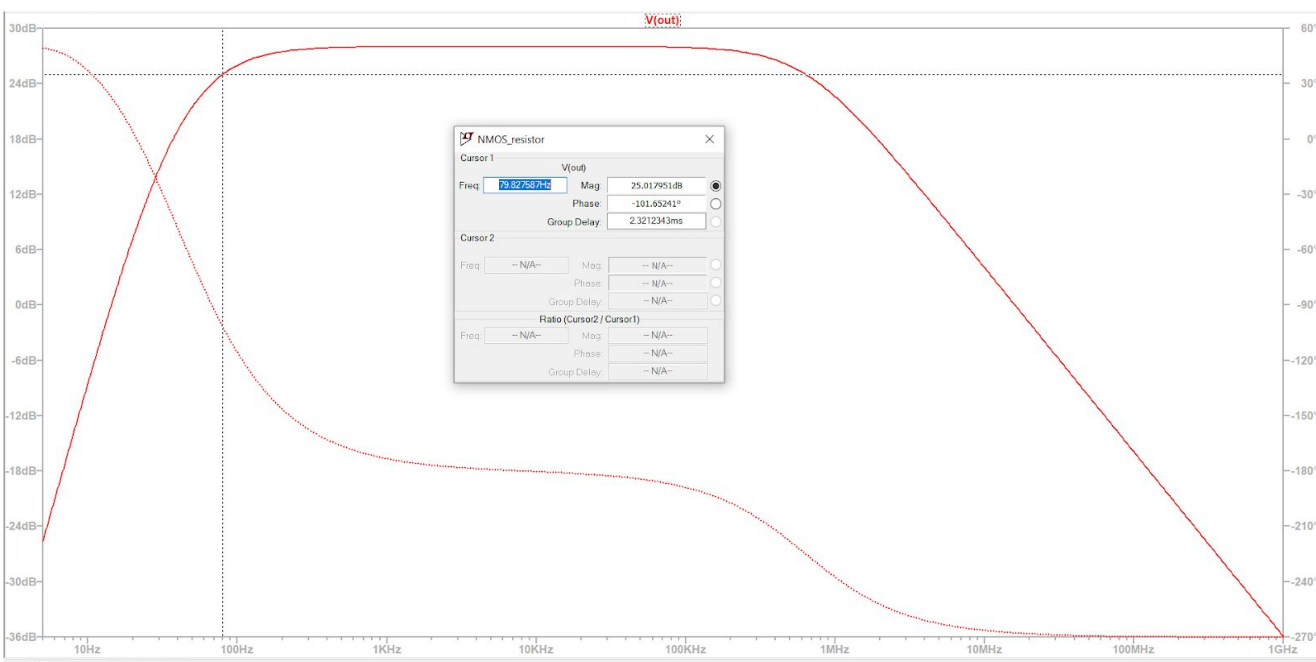

Fig.13 :- circuit(Fig.1) with C_b=0.0047 uF
Gain =28 dB ; Fl=79.825 Hz

Effect of C_c on lower cutoff frequency

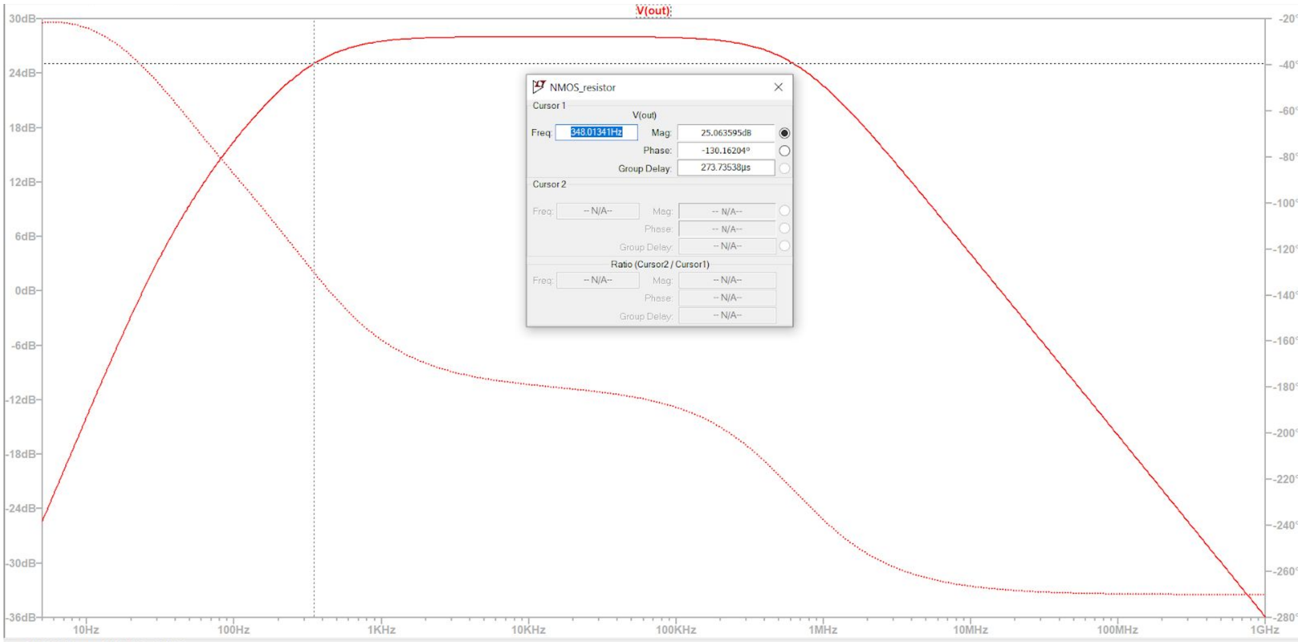

Fig.14 :- circuit(Fig.1) with C_c=0.047 uF
Gain =28 dB ; Fl=348.01 Hz

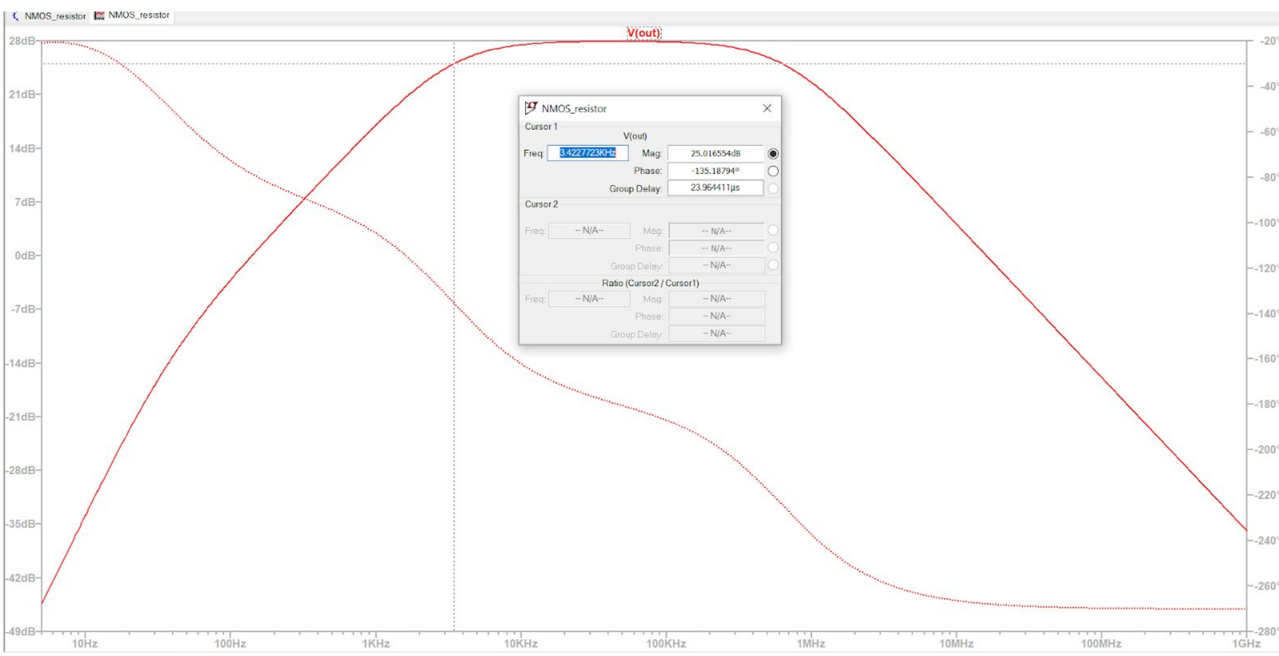

Fig.15 :- circuit(Fig.1) with C_c=0.0047 uF
Gain =28 dB ; Fl=3422.77 Hz

Effect of C_s on lower cutoff frequency

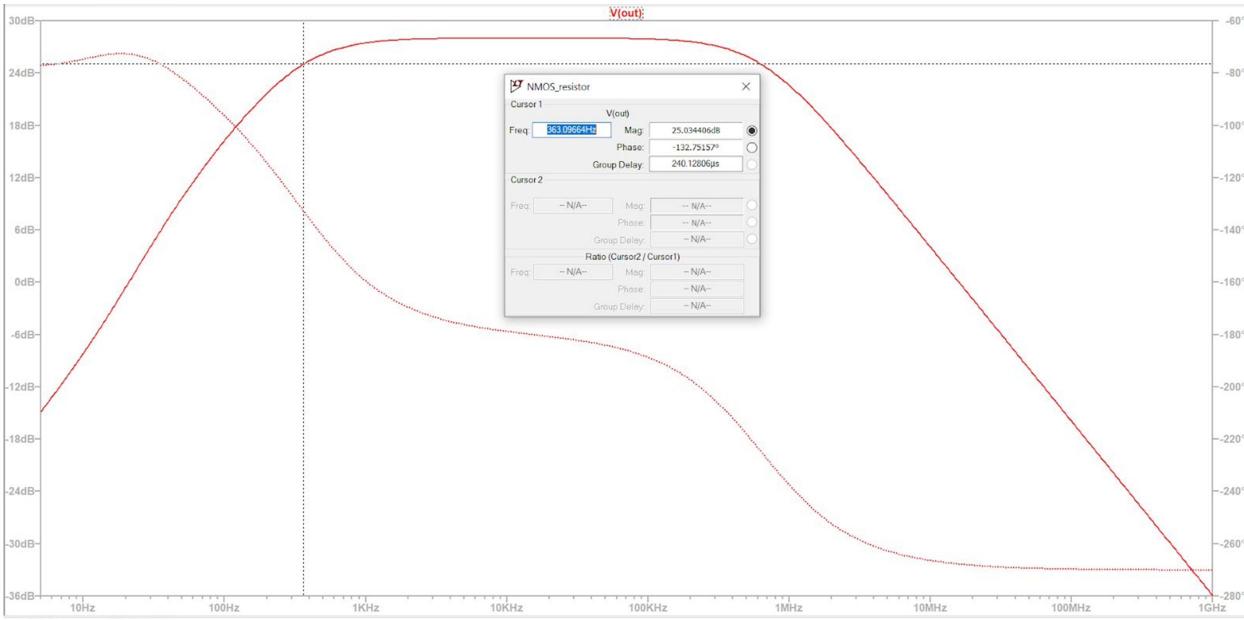

Fig.16 :- circuit(Fig.1) with C_s=4.7 uF

Gain =28 dB ; Fl=363.09 Hz

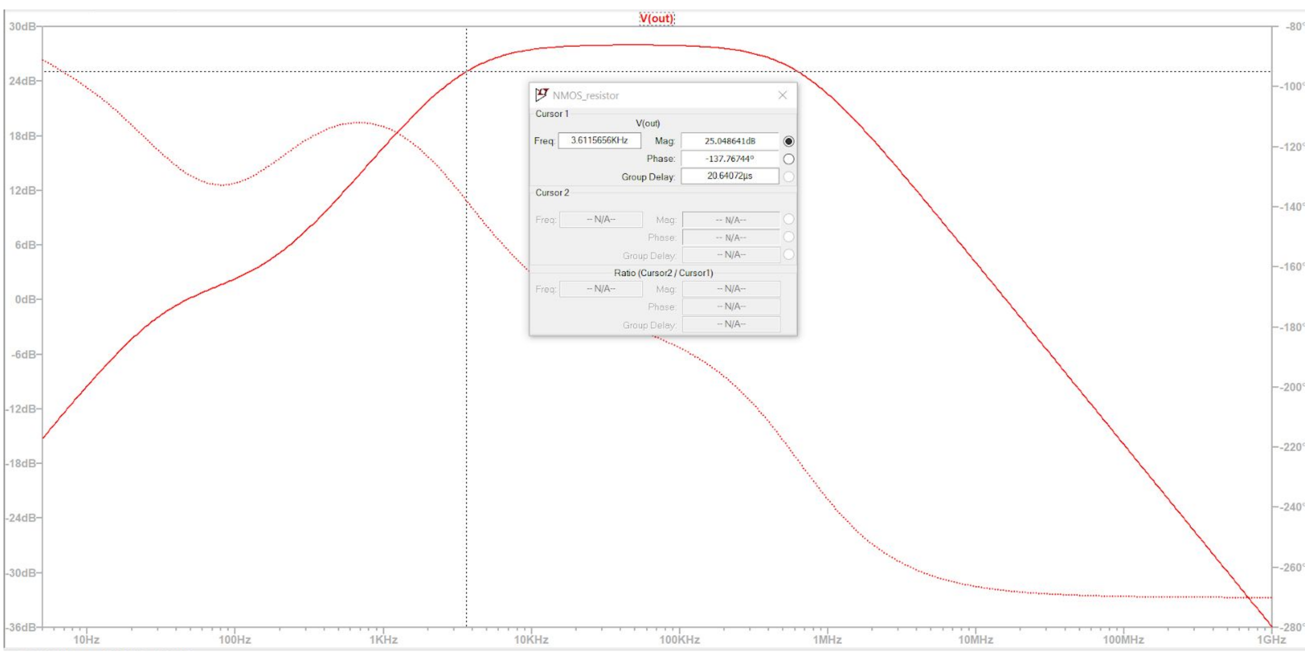

Fig.17 :- circuit(Fig.1) with C_s=0.47 uF

Gain =28 dB ; Fl=3611.56 Hz

Effect of C_{sh} and Rd on upper cutoff frequency

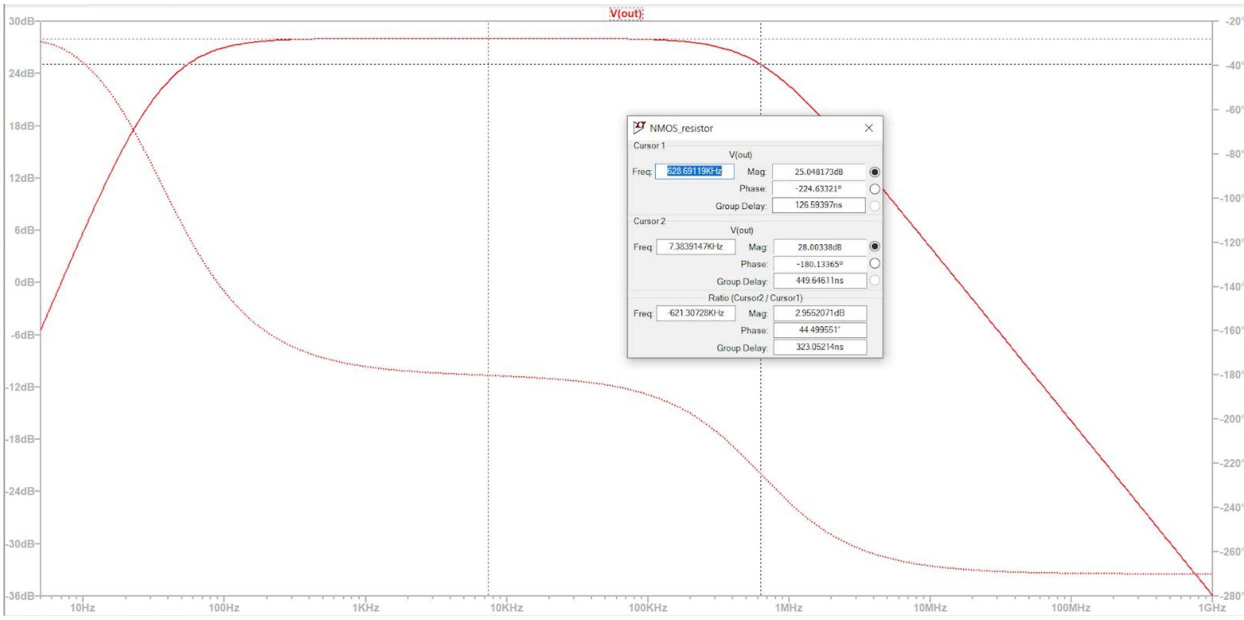

Fig.18 :- circuit(Fig.1) with C_{sh}=100 pF

Gain =28 dB ; Fh=628.69 KHz

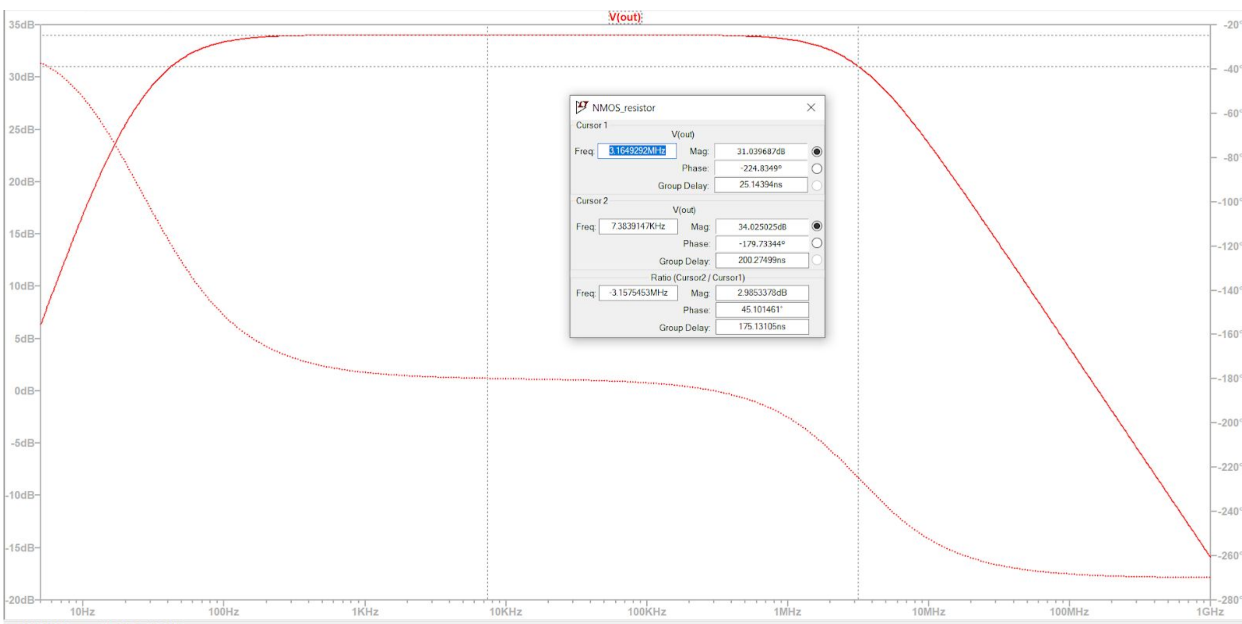

Fig.19 :- circuit(Fig.1) with Rd & Rl=10 Kohm

Gain =34 dB ; Fh=3.149 MHz

Gain increase =34-28(gain with Rd & Rl=5 Kohm)=6 dB which is 2 times

Bandwidth reduced by 2 times.

I.e., gain,bandwidth product is constant.

Observation and discussion:-

1. In this experiment, we simulated a common source MOS amplifier and observed the effect of various circuit parameters and device parameters on the output signal,the gain of the amplifier and the bandwidth of the amplifier.
2. We increased the width of the transistor by 4 times from Fig.2 to Fig.3 and the gain of the amplifier increased by 2 times which shows the gain of the amplifier is proportional to the square root of width of the transistor.
3. We increased the KP of the transistor by 4 times from Fig.3 to Fig.4 and the gain of the amplifier increased by 2 times which shows the gain of the amplifier is proportional to the square root of kp of the transistor.
4. We increased the source resistance of the transistor by 4 times from Fig.4 to Fig.5 and the gain of the amplifier decreased by 2 times which shows the gain of the amplifier is inversely proportional to the square root of source resistance of the transistor.
5. We increased the value of Rd||Rl by 2 times from Fig.5 to Fig.6 and the gain of the amplifier increased by 2 times which shows the gain of the amplifier is proportional to the value of Rd||Rl.
6. By all the above results we can state that gain of the amplifier is:

   Gain = c *square_root(W*KP/Rs)*(Rd || Rl)
   Where c is a constant.

   We have the gain formulae from derivations by assuming Rs >> 1/(KP*W/L)
   Gain = square_root(2*KP*W*(V_g-V_{Th})/(R_s*L)) * (Rd || Rl)

7. Increasing the value of C_s will not be having any effect on gain seen from Fig.6 and Fig.7
8. Decreasing the value of C_s will be having a wide effect of gain because as we increase the capacitance value it loses its bypass character which makes Rs coming into the gain formulae seen from Fig.6,Fig.8,Fig.9.
9. The value of the output signal cant go behind some value which is due to its clipping effect of the signal,here the input signal goes to the triode region or the cutoff region where the signal does not have linear amplification property seen from the Fig.10,.
10. Low frequency response of the above signal will be having 3 poles which are due to 3 capacitors Cb,Cc,Cs.
11. The lower cutoff frequency in the frequency response of the transistor depends on the Cb,Cc,Cs.and the upper cutoff depends on the Csh.
12. The dominating pole among those will decide the lower cutoff frequency of the frequency response.
13. Pole corresponding to Cb: 1/(Cb*(R1 || R2)).

14. Pole corresponding to Cc: 1/(Cc *(Rd+Rl)).
15. Pole corresponding to Cs: 1/(Cs*Rs).
16. From Fig.11 and 12 we can say that the pole corresponding to cb is not the dominating as it shows no effect on the lower cutoff frequency.
17. From Fig.12 and 13 we say that as we keep on decreasing the capacitance of Cb then that will become dominating the pole.
18. From Fig11 , 14 and 15 we can say that Cc is becoming the dominating pole as we decrease its capacitance and from fig 14 to 15 we made capacitance value decrease by 10 times then the lower cutoff frequency increased by 10 times.
19. From Fig11 , 16 and 17 we can say that Cs is becoming the dominating pole as we decrease its capacitance and from fig 16 to 17 we made capacitance value decrease by 10 times then the lower cutoff frequency increased by 10 times.
20. We increased the capacitance value of Csh by 10 times then the upper cutoff frequency gots dropped by 10 times which is seen from Fig.11 and Fig.18,it can be evident from the formulae for the upper cutoff frequency.

    fh=1/(Csh* (Rd || Rl))
21. If we increase the Rd || Rl value by 2 times then the upper cutoff drops by 2 times but here gain * bandwidth product remained constant from Fig11 and Fig19.

$$G_V \cdot BW = \frac{g_m \cdot (R_L \parallel R_D \parallel r_0)}{2 \cdot \pi \cdot C_L \cdot (R_L \parallel R_D \parallel r_0)} = \frac{g_m}{2 \cdot \pi \cdot C_L}.$$

Conclusion:-

The common source MOSFET amplifier which has passive load is a very important electronic system which can be used for amplifying the strength of weak signals.The gain of the MOSFET amplifier is directly proportional to its width.The load resistance also determines the gain and the bandwidth of the amplifier system but gain bandwidth product does not depends on the load resistance.