VLSI Engineering Laboratory
Experiment 4
Operational amplifier

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AIM:

To simulate an operational amplifier in inverting , non-inverting , voltage follower and open-loop configuration and to observe the effect of various parameters on the performance of the amplifier.

Circuit diagram :-

a.Inverter configuration :-

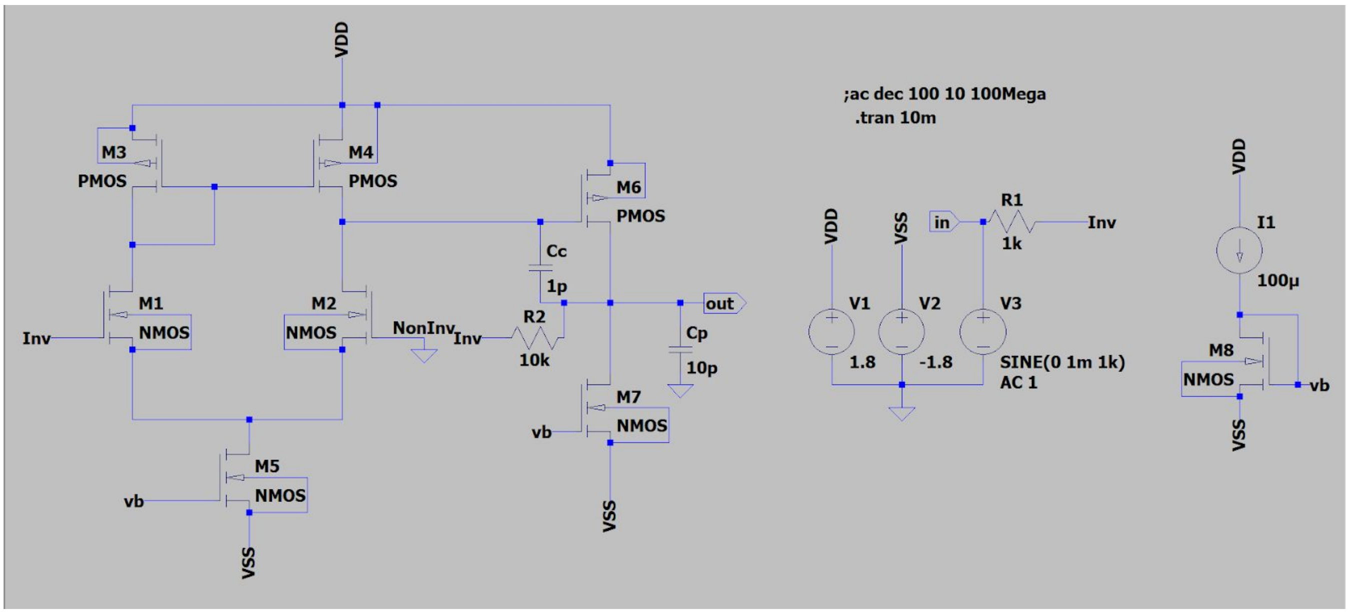

Fig.1

b.Non-inverter configuration :-

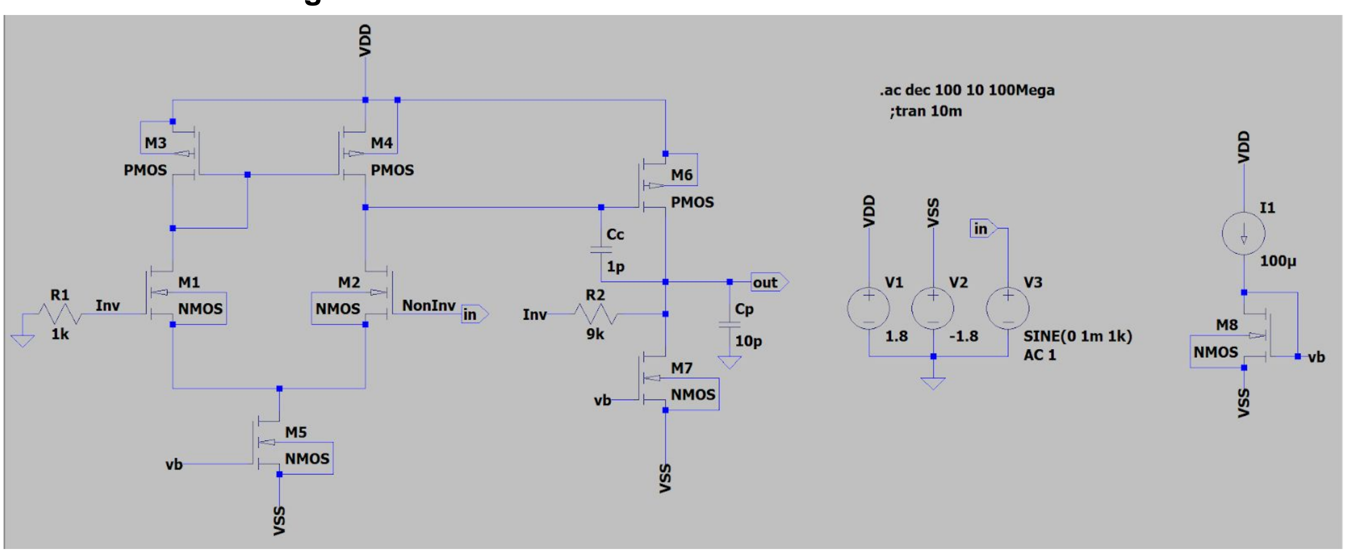

Fig.2

c.Voltage Follower :-

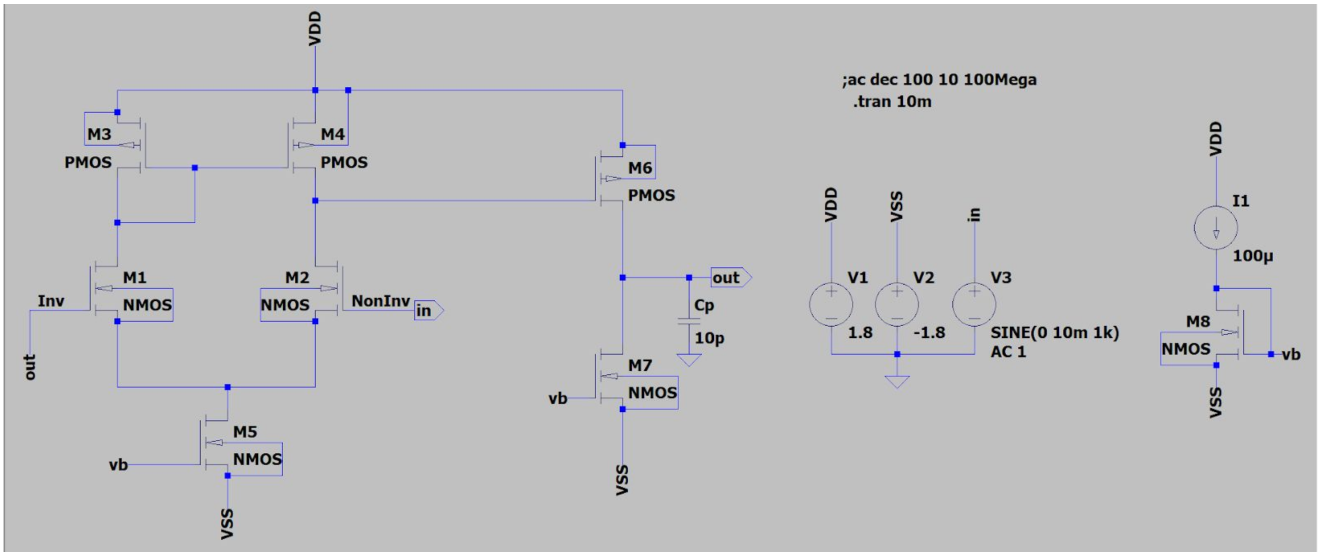

Fig.3

d.open-loop configuration :-

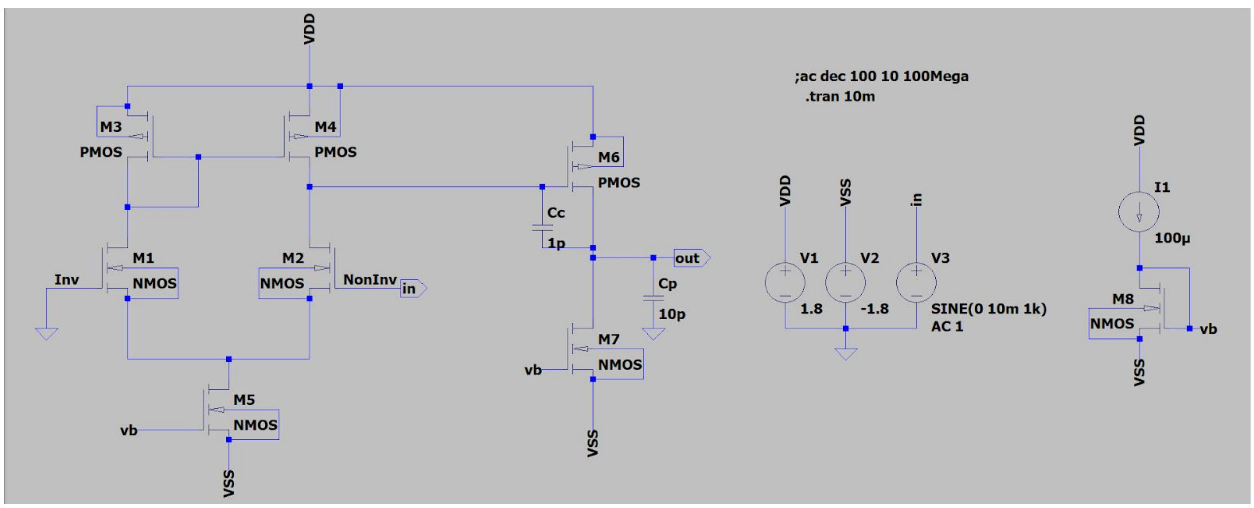

Fig.4

Description :-

1. Block diagram of an operational amplifier consists of a two-stage amplifier which consists of a differential amplifier, a gain stage and level shifter and a source follower.
2. The differential amplifier acts as a differential amplifier to make the opamp consist of two input terminals i.e., inverting terminal and non-inverting terminal and an output terminal.
3. The gain stage is implemented by using a common source PMOS amplifier with NMOS acting as an active load.
4. The level shifter eliminates the DC output coming from previous stages.This DC output value may saturate the output of the amplifier therefore it must be removed.
5. In the circuit diagram the terminal labeled a “NonInv” acts as a non-inverting terminal for the differential stage.

6. If we apply an input at a non-inv terminal keeping the other terminal grounded, then the output of the differential stage will be 180 deg out-off phase with input, and is again shifted by 180 deg by the common source stage, thus giving an overall phase shift of 360 deg. Thus we verify that the non-inv terminal is indeed an non-inverting terminal.
7. Similarly we can verify the terminal with the label "Inv" is the inverting terminal of the Opamp.
8. The tail current for the first stage:differential amplifier circuit is generated by the current mirror which is made by using bias current source I1 and mosfets M8,M5.
9. In the current mirror we have to set the W/L ratio of M5,M8 same so as to maintain same current through both of them as they have same gate-source voltage,so we set W=4um and L=180nm
10. In the differential stage as the current passing through the MOSFET's M1,M2,M3,M4 are all the same so we have to set the w/L ratio of all the above mentioned mosfets to be the same.
11. As the current passing through M5 is double that of M1/M2/M3/M4 so we have to set W/L ratio of all the above to be half of that of M5 i.e., we set W=2um L=180nm(M1,M2,M3,M4).
12. As the gain stage is connected with the current mirror so W/L ratio for M6 and M7 should be equal to that of M8 to maintain the same current flow in the gainstage mosfet.
13. We have used biasing voltages of -1.8V and 1.8V which ensures that no additional biasing network is required.
14. A compensating capacitance Cc is used in the common source amplifier stage, which is connected between the gate and the terminal of the driver PMOS.
15. Capacitance Cp is connected at the output terminal to denote the effective capacitance from the next stage.
16. Operational amplifier is connected with different variations to make different configurations as below :-
17. Inverting configuration is achieved when we apply an AC source(here we use sine signal) through a resistor R1 at the inverting terminal and making R2 as a negative feedback circuit by connecting R2 between the output terminal and inverting terminal of the differential stage and Non-inverting terminal is grounded.
18. For non-inverting configuration the circuit will be the same as that of inverting terminal but the AC input is not fed into the inverting terminal through R1 instead it will be fed directly into the non-inverting terminal and The other terminal of R1 is grounded.
19. For voltage follower circuits,The output of the op-amp is connected to the inverting terminal(which acts like a negative feedback network here) and input is fed through the non-inverting terminal.
20. Open-loop configuration,the input is fed through the non-inverting terminal and inverting terminal is made ground i.e., there is no feedback network.

Results :-

A.Inverting configuration :-

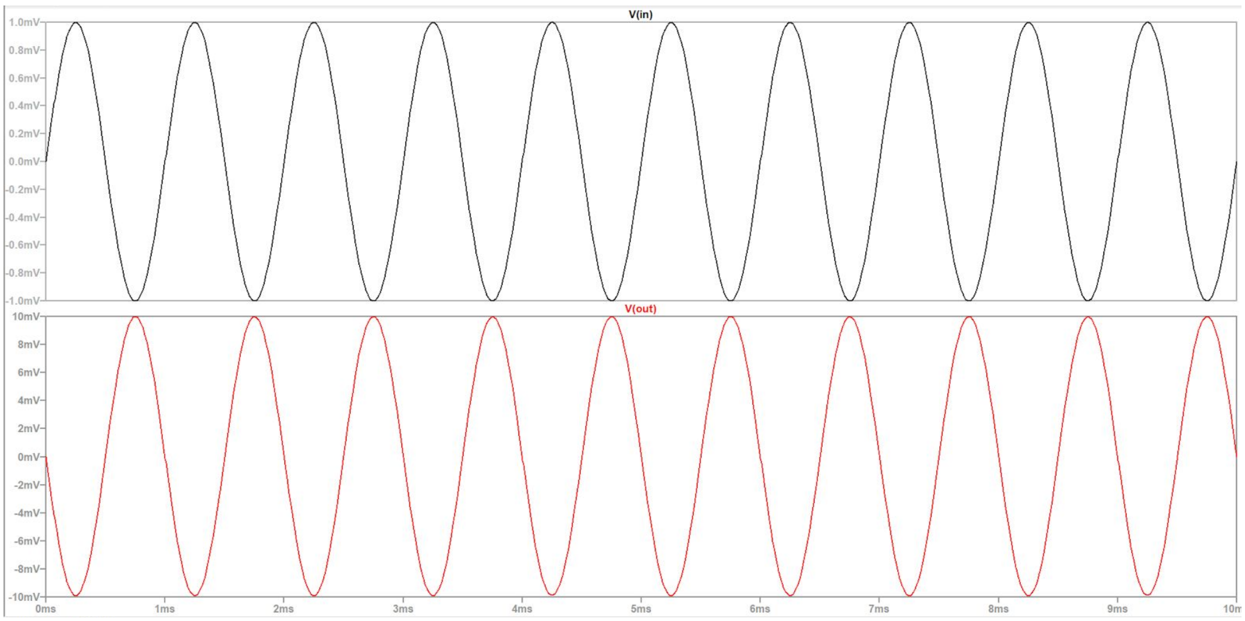

Fig.5:transient response of inverting configuration with R2=10 k and R1=1K

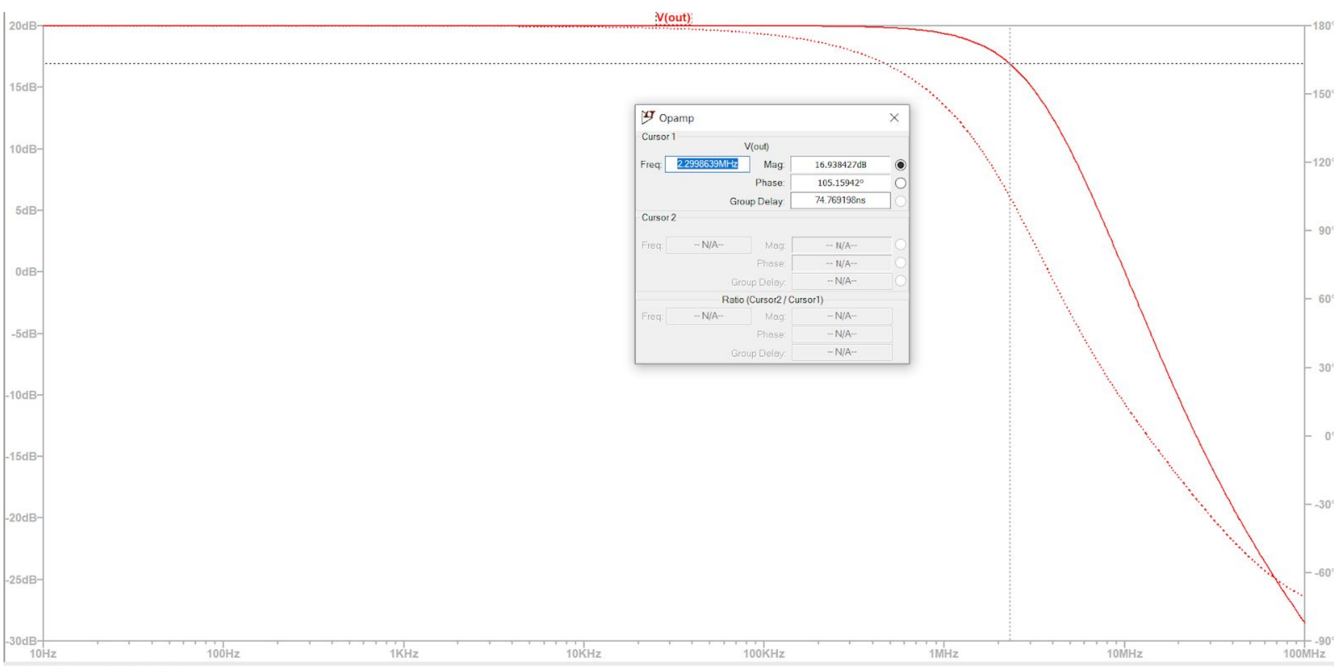

Fig.6:frequency response of inverting configuration with R2=10 k and R1=1K
Bandwidth = 2.29 MHz

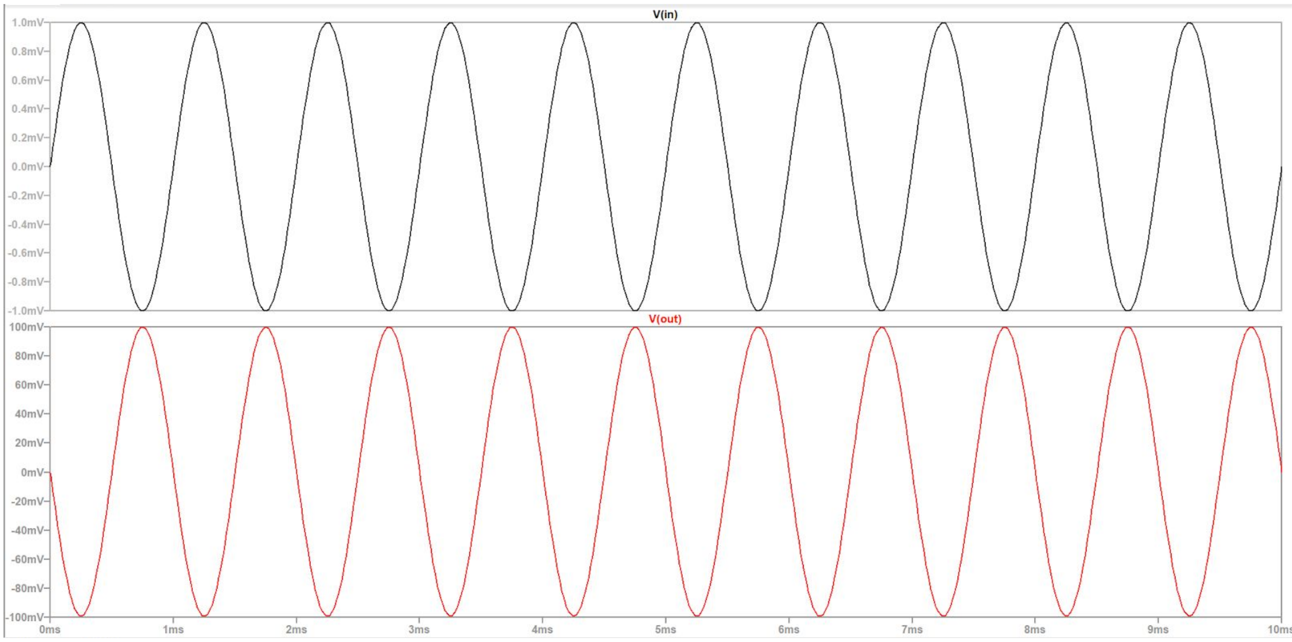

Fig.7:transient response of inverting configuration with R2=100 k and R1=1K

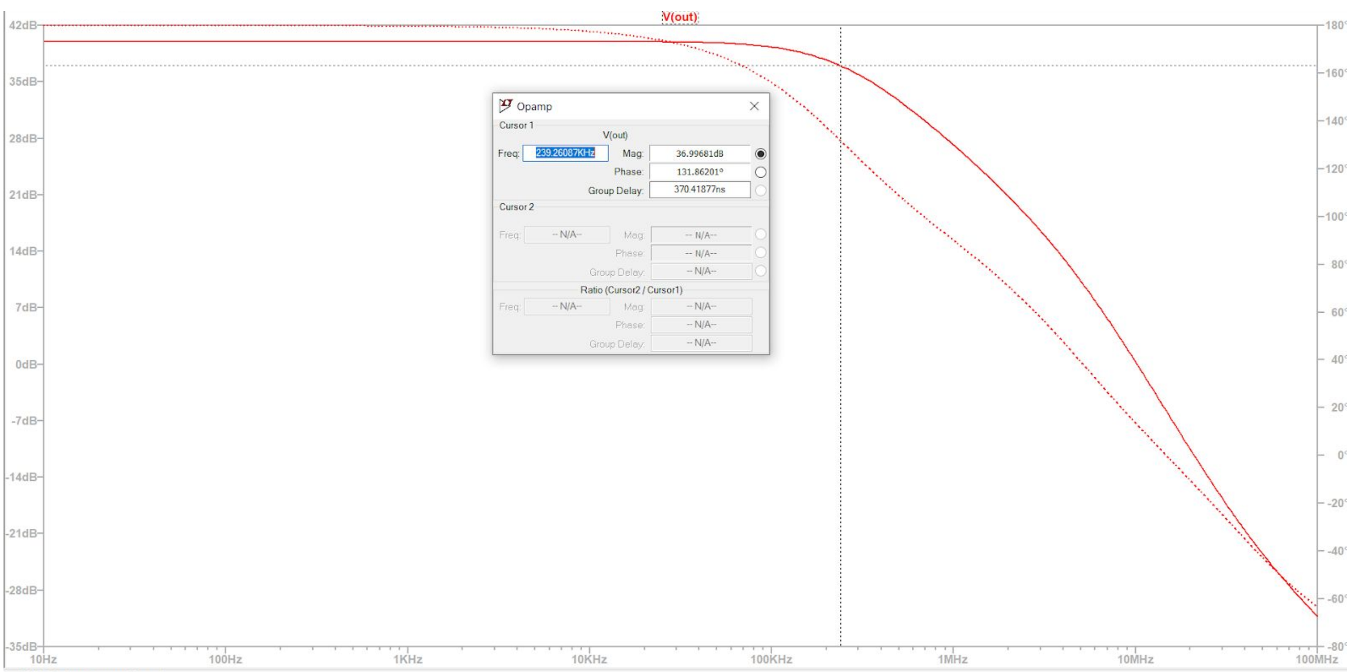

Fig.8:frequency response of inverting configuration with R2=100 k and R1=1K
Bandwidth = 239 KHz

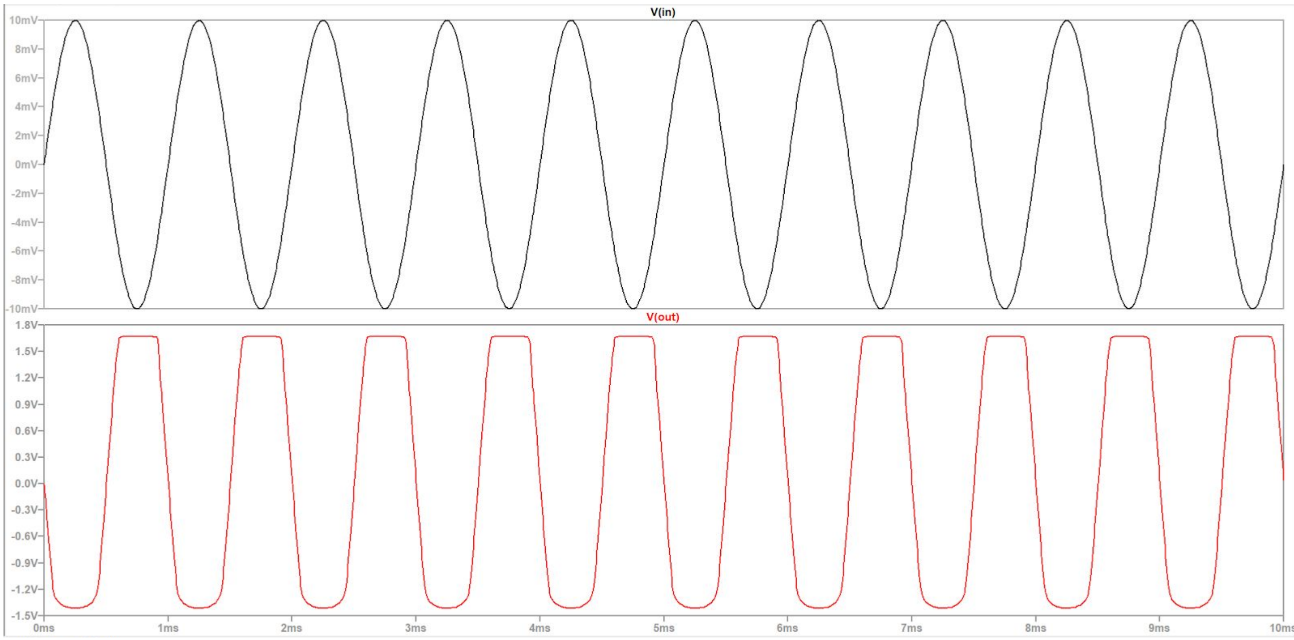

Fig.9:transient response of inverting configuration with R2=300 k and R1=1K And input signal amplitude = 10 mV

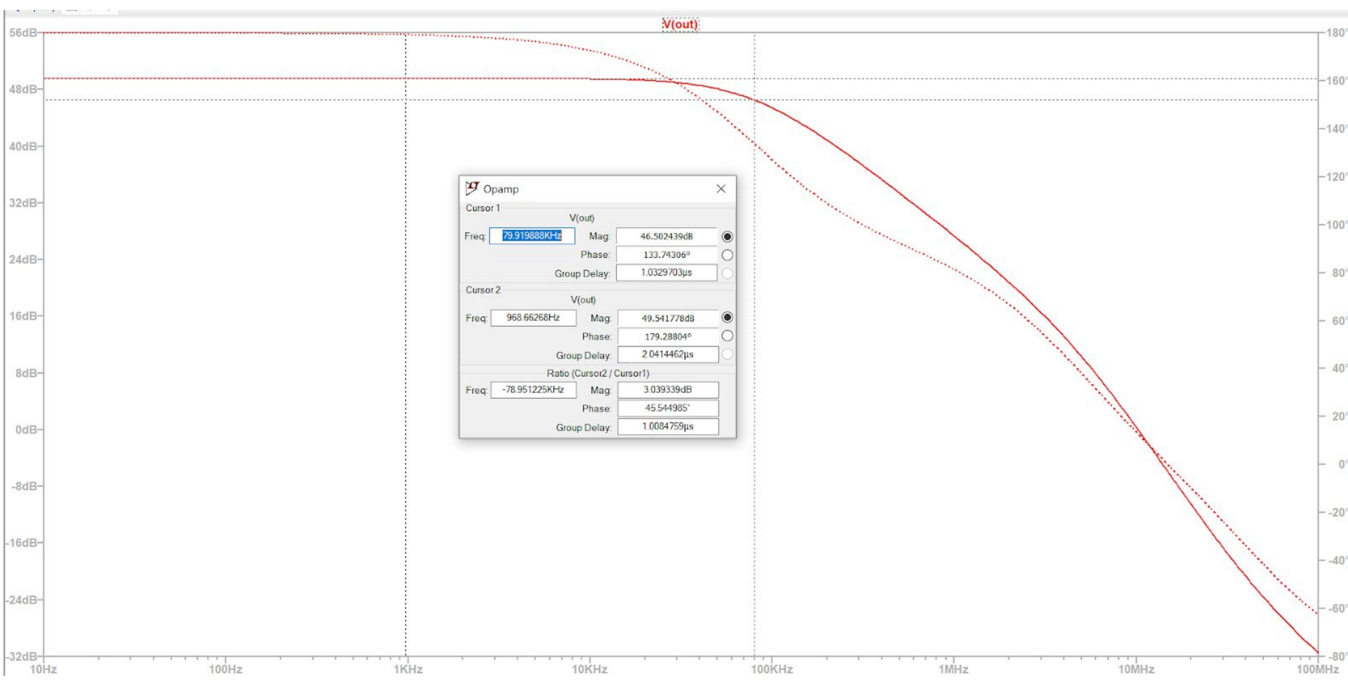

Fig.10:frequency response of inverting configuration with R2=300 k and R1=1K And input signal amplitude = 10 mV

B.Non-inverting configuration :-

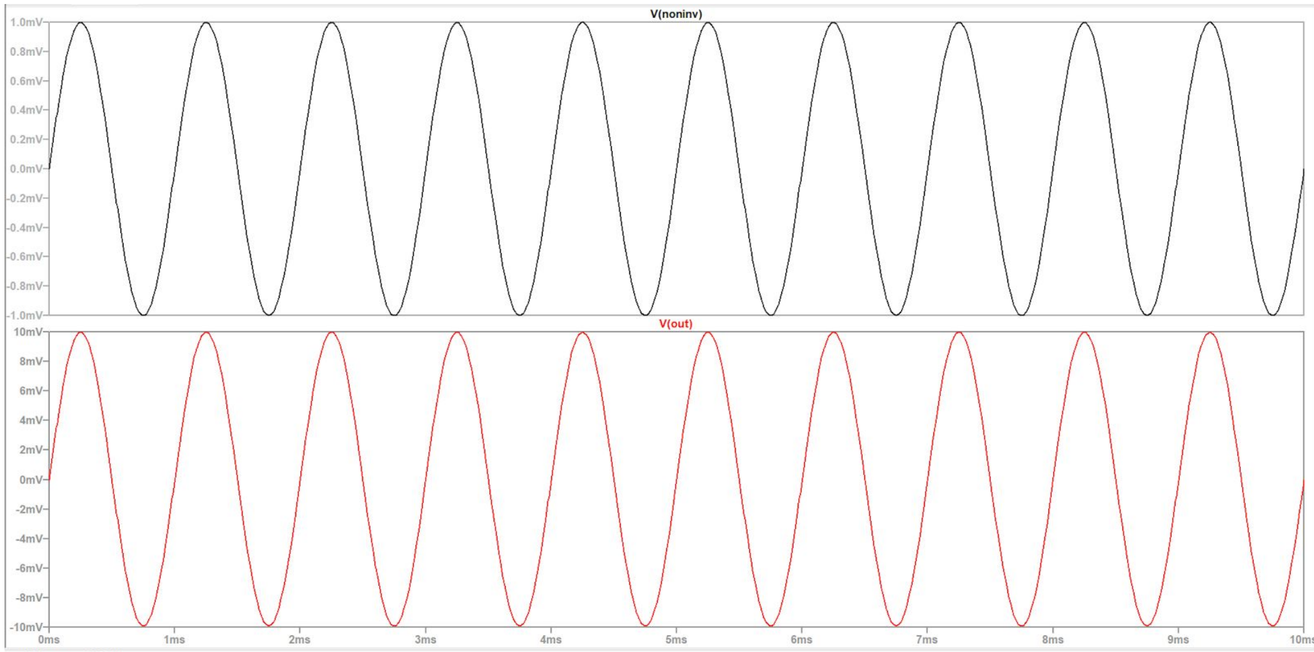

Fig.11:transient response of Non-inverting configuration with R2=9 k and R1=1K

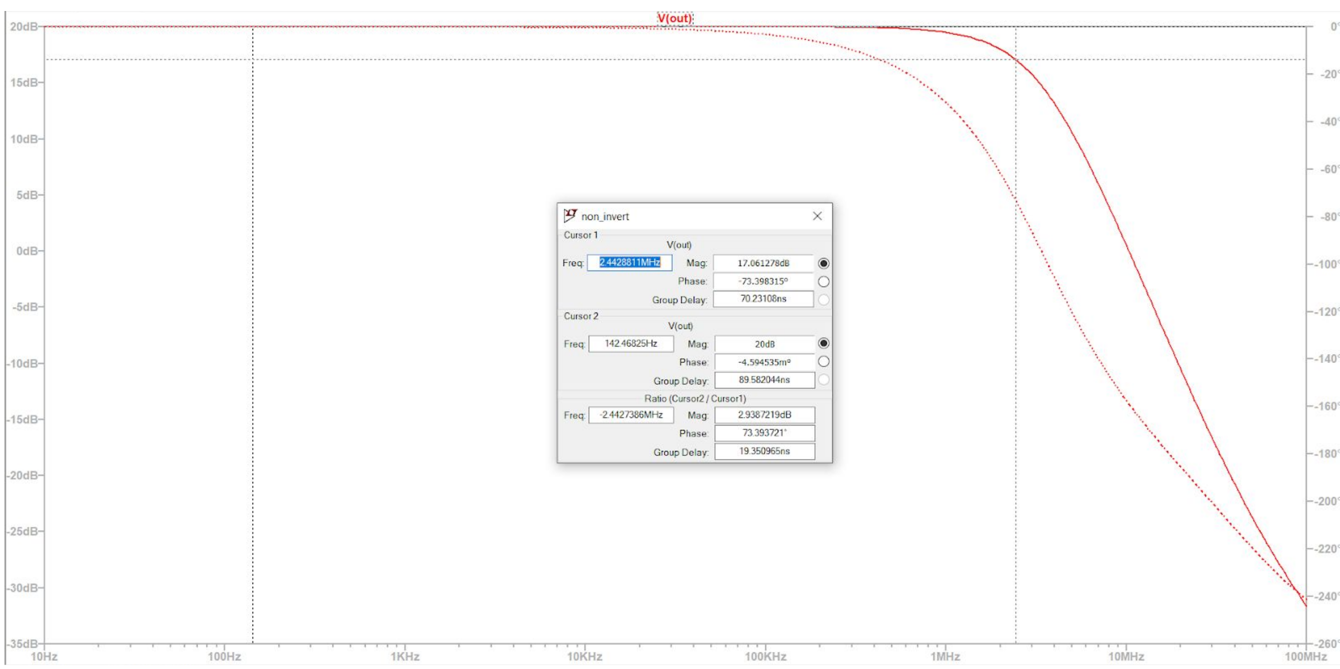

Fig.12:frequency response of Non-inverting configuration with R2=9 k and R1=1K

Bandwidth = 2.443 MHz

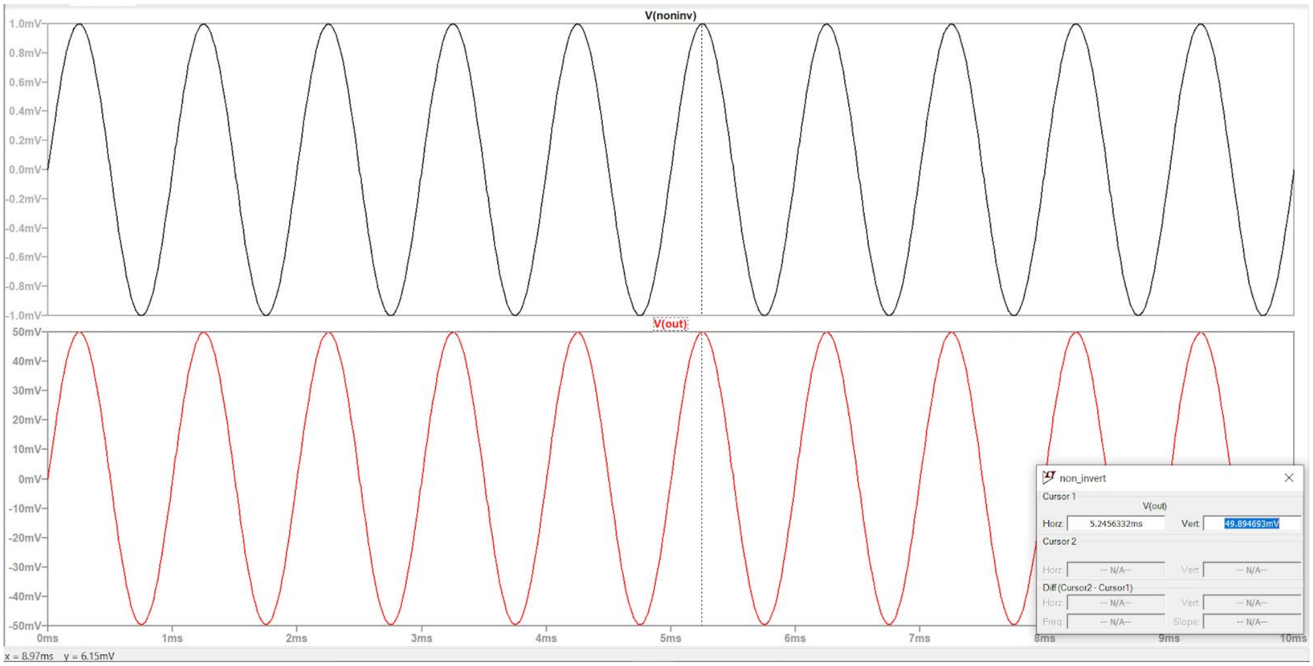

Fig.13:transient response of Non-inverting configuration with R2=49 k and R1=1K

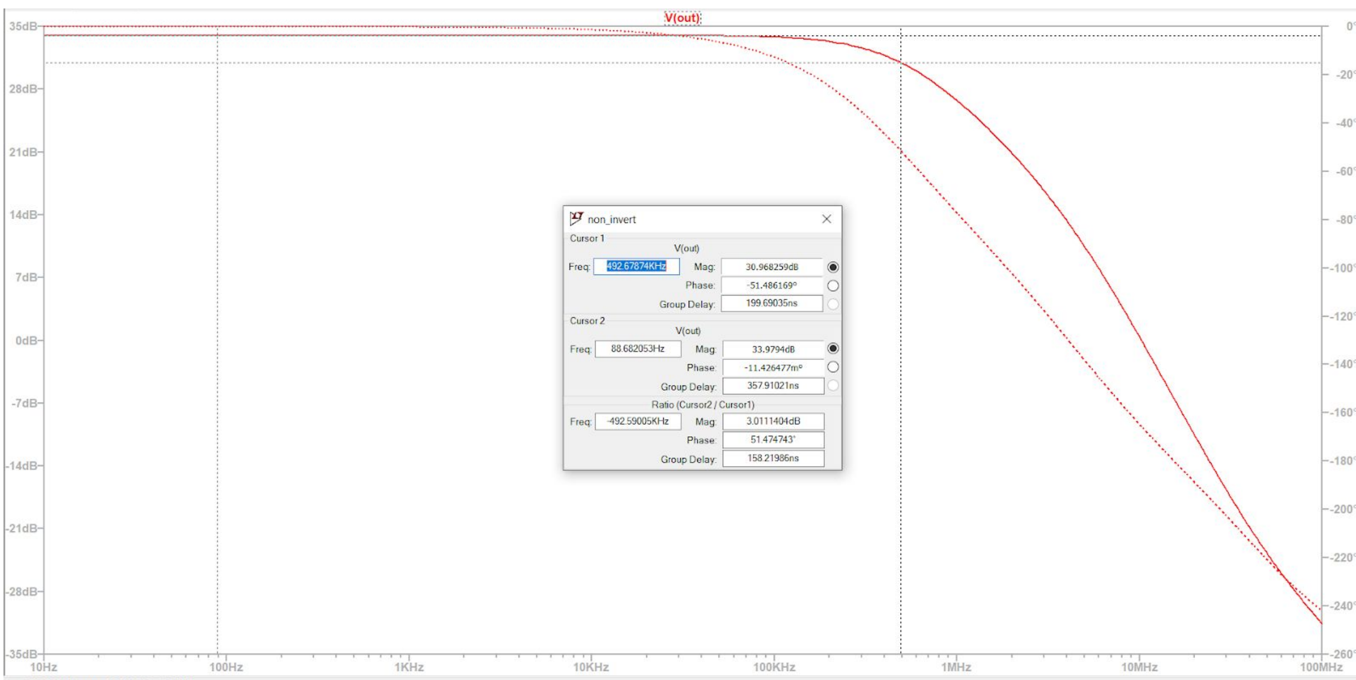

Fig.14:frequency response of Non-inverting configuration with R2=49 k and R1=1K

Bandwidth = 492.678 kHz

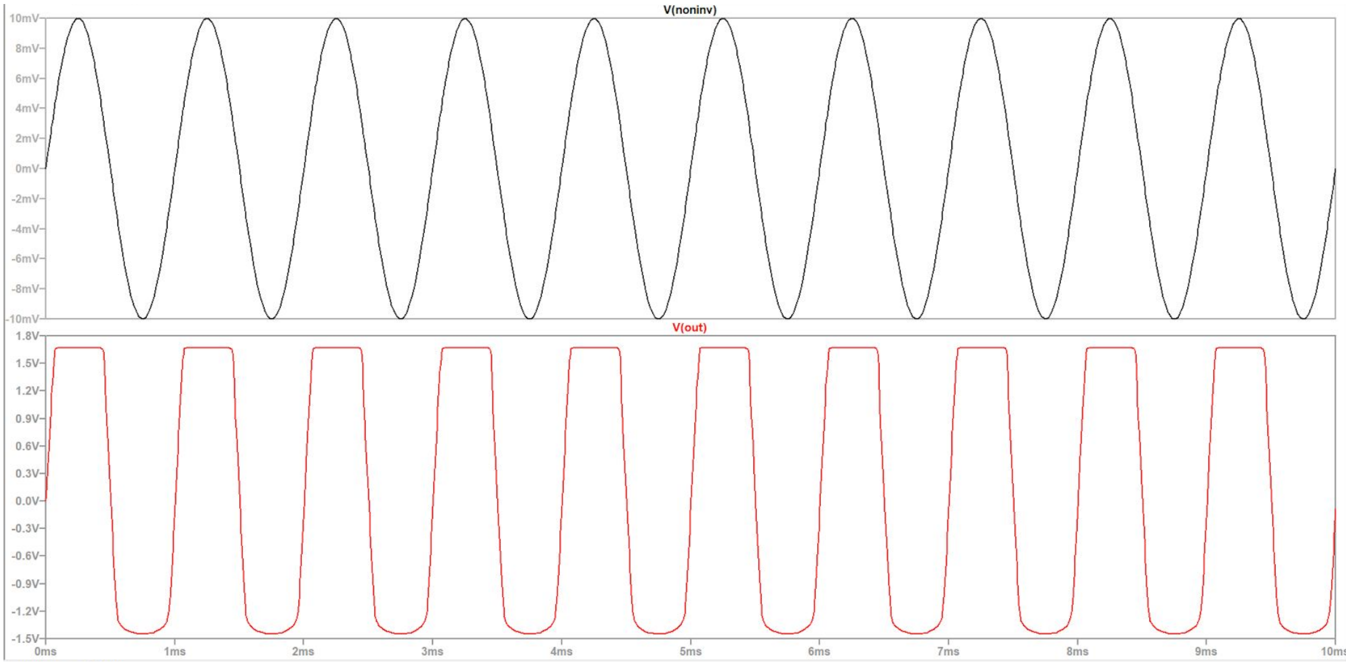

Fig.15:transient response of Non-inverting configuration with R2=449 k and R1=1K And input signal amplitude = 10 mV

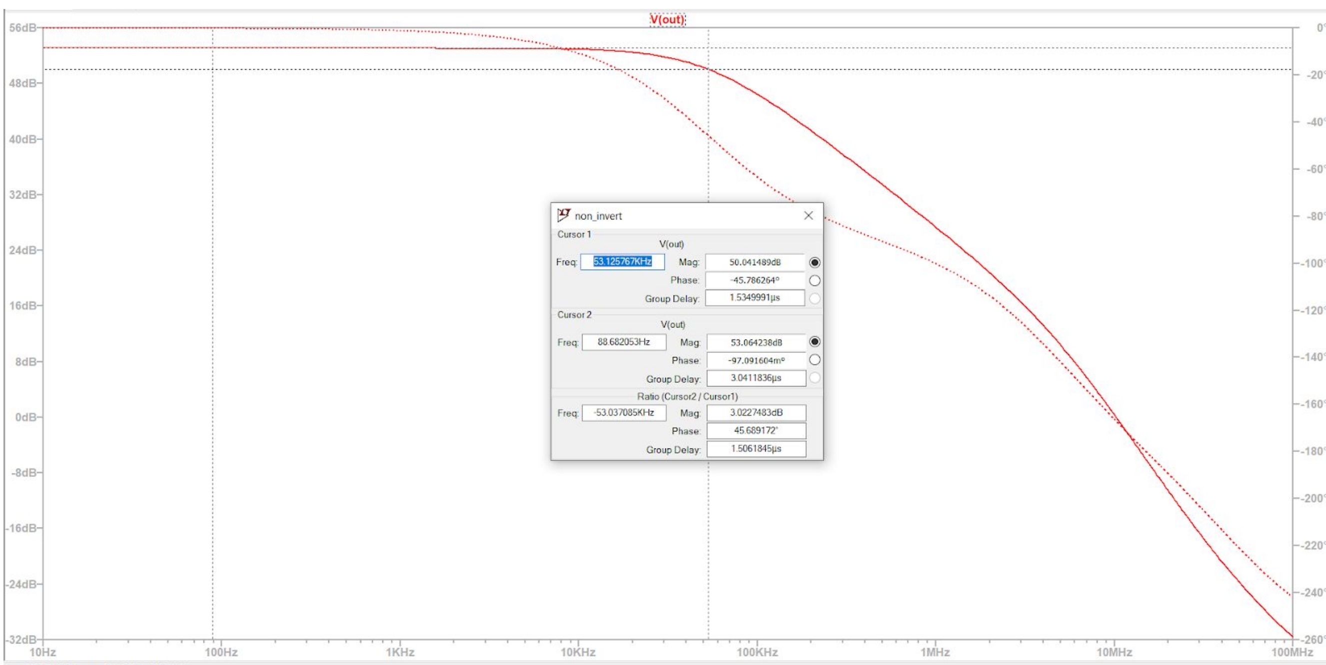

Fig.16:frequency response of Non-inverting configuration with R2=449 k and R1=1K And input signal amplitude = 10 mV

C.Voltage follower :-

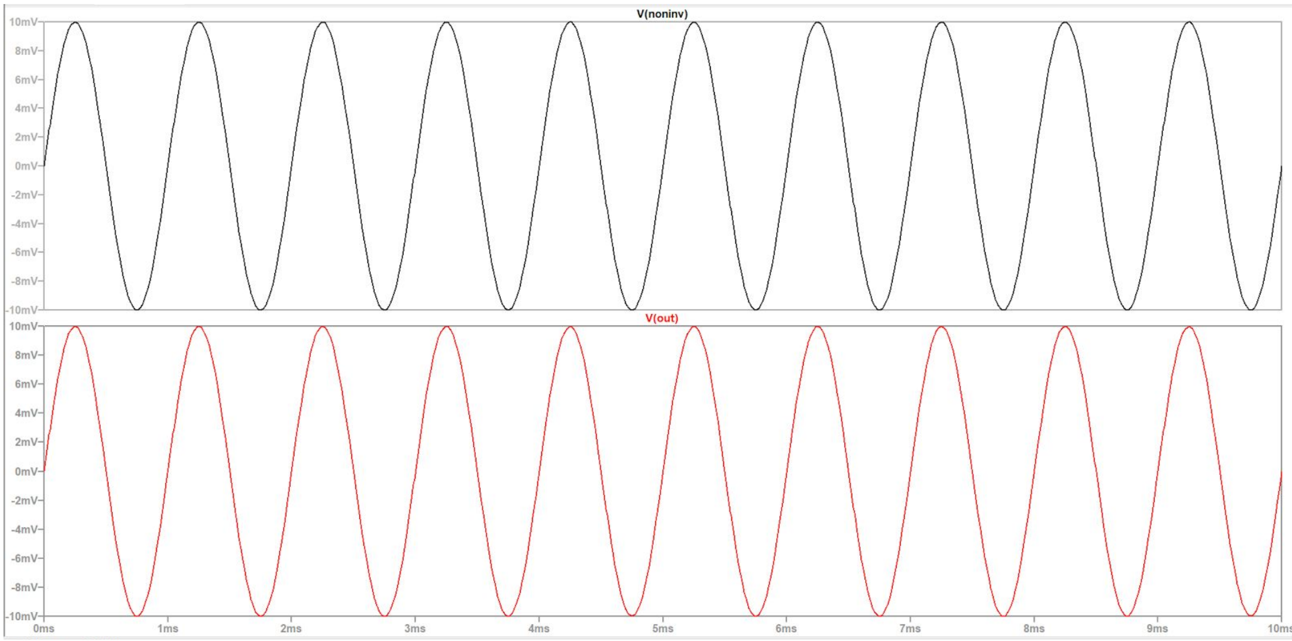

Fig.17:transient response of the voltage follower circuit

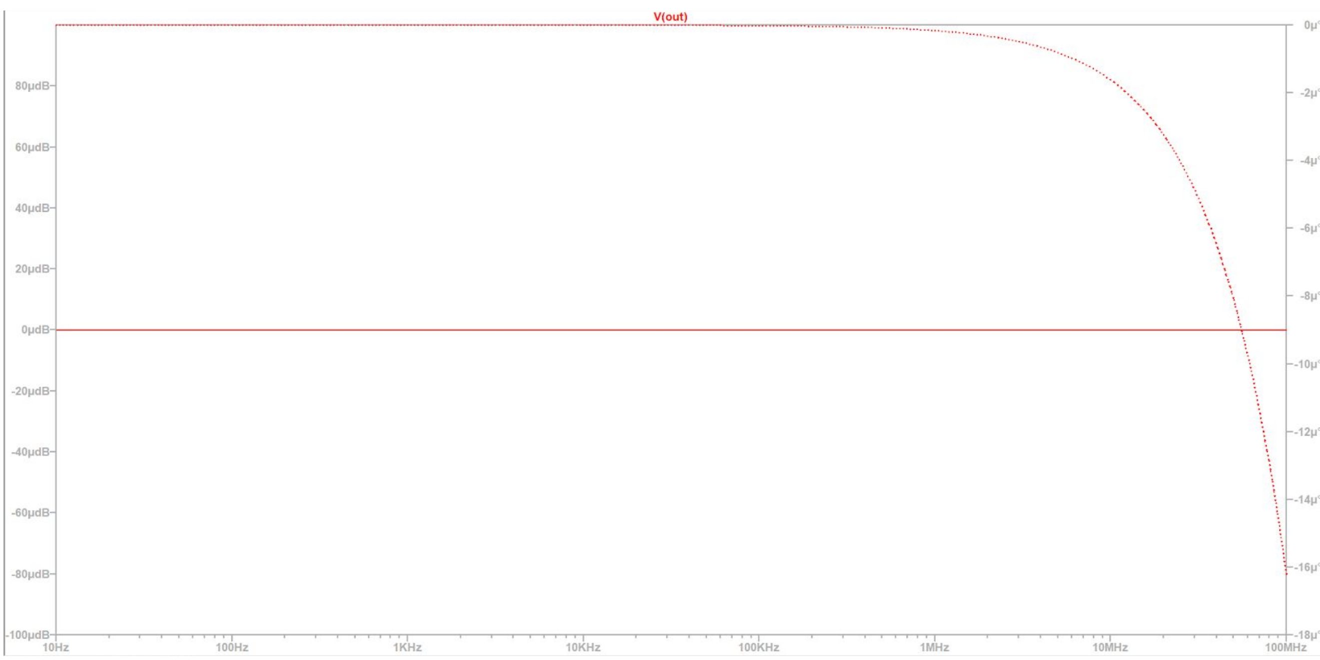

Fig.18:frequency response of the voltage follower circuit without capacitor Cc

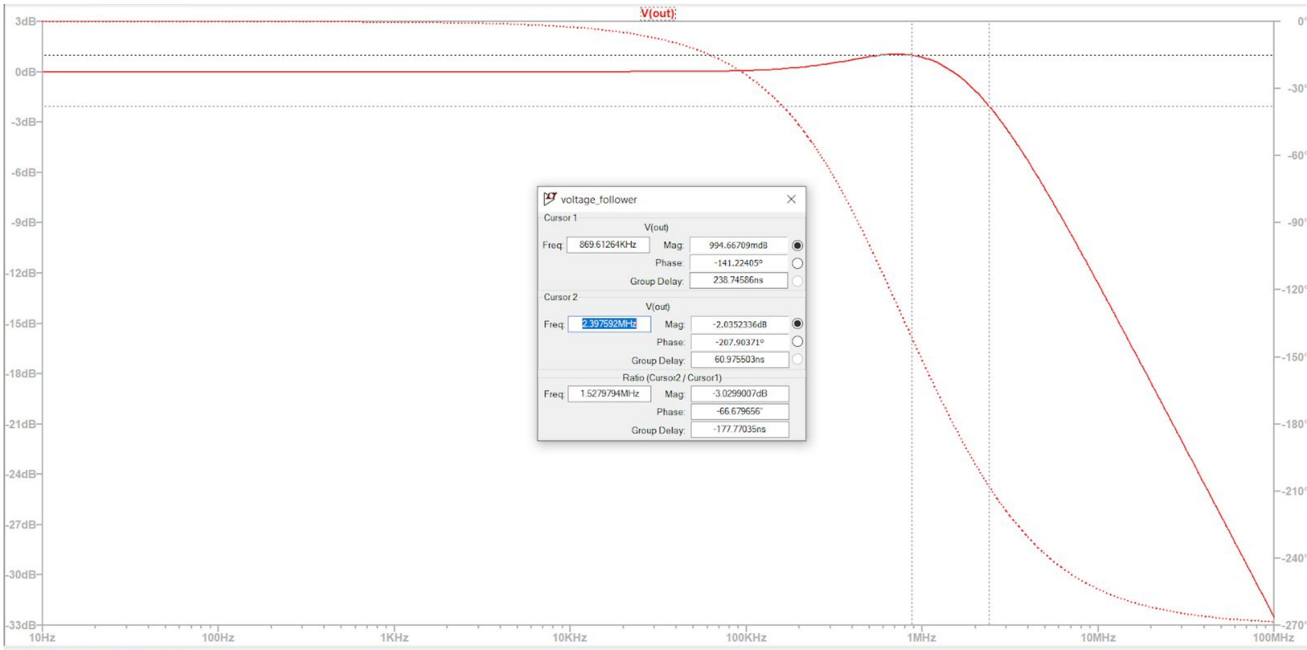

Fig.19:frequency response of the voltage follower circuit with capacitor Cc

D.<u>Open loop configuration</u> :-

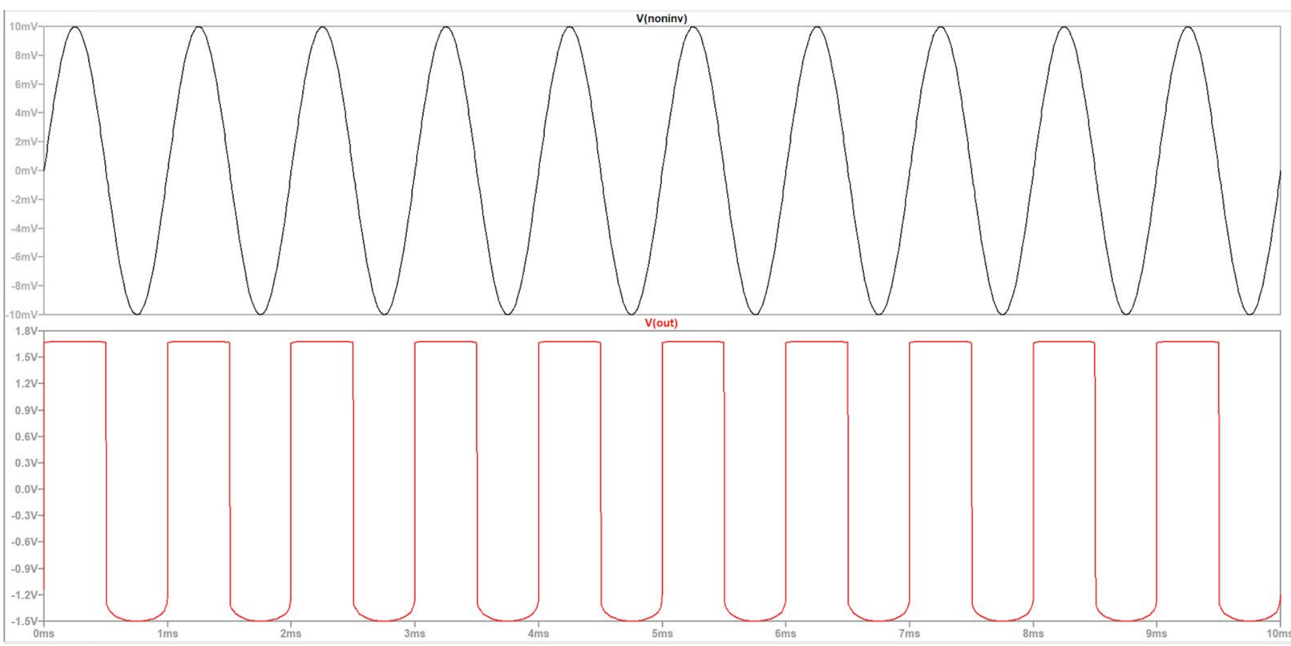

Fig.20:transient response of open loop configuration without Cc

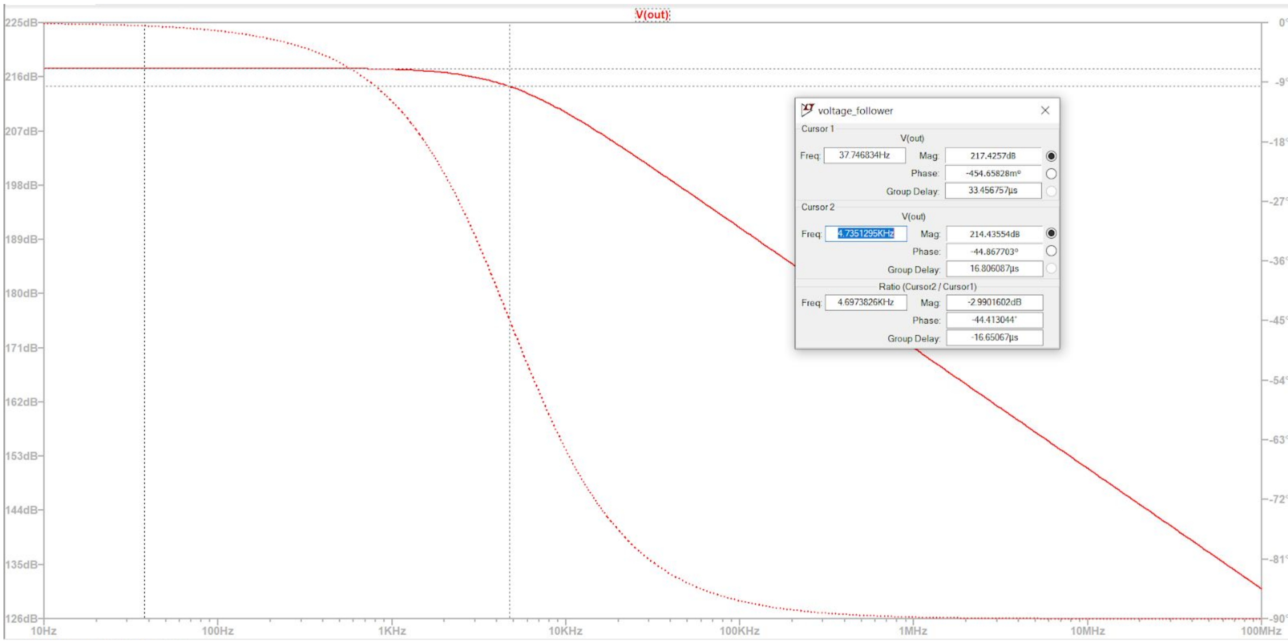

Fig.21:Frequency response of open loop configuration without Cc

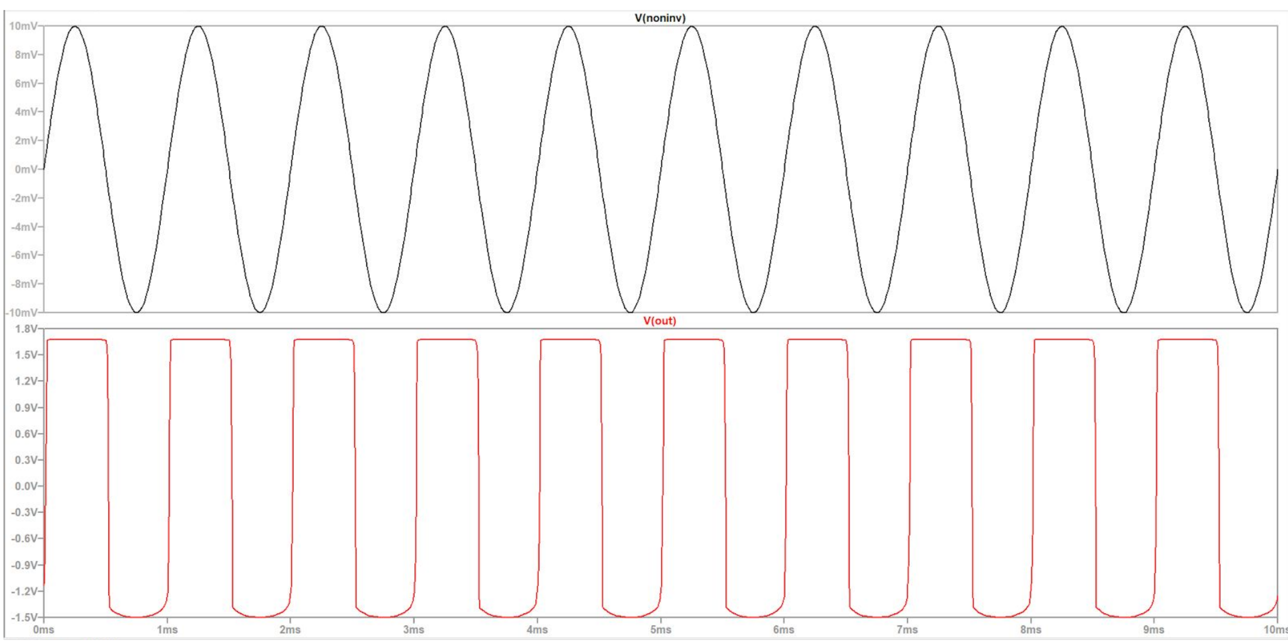

Fig.22:transient response of open loop configuration with Cc=1pF

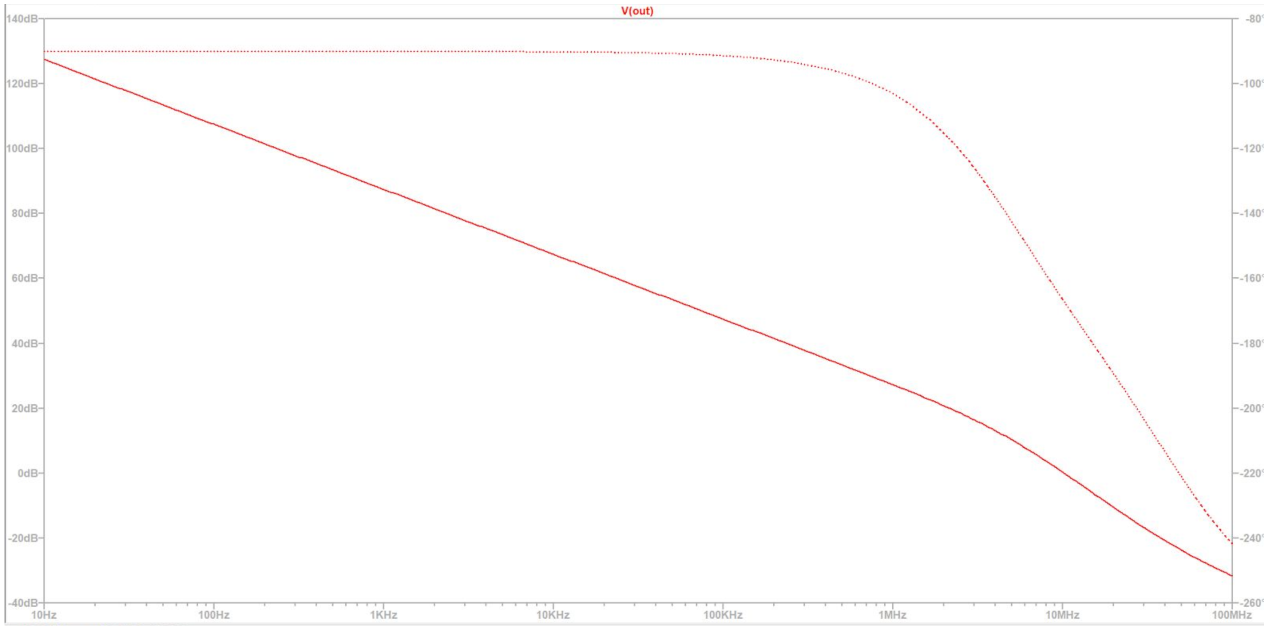

Fig.23:Frequency response of open loop configuration with Cc=1pF

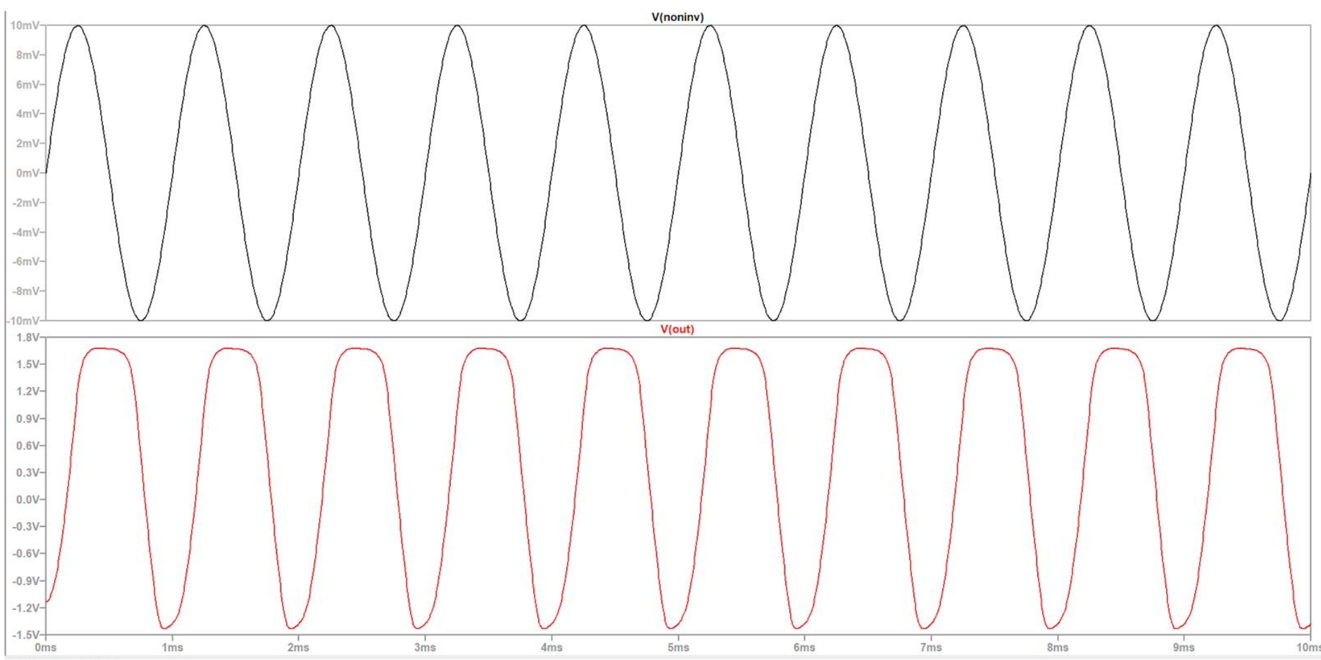

Fig.24:transient response of open loop configuration with Cc=100pF

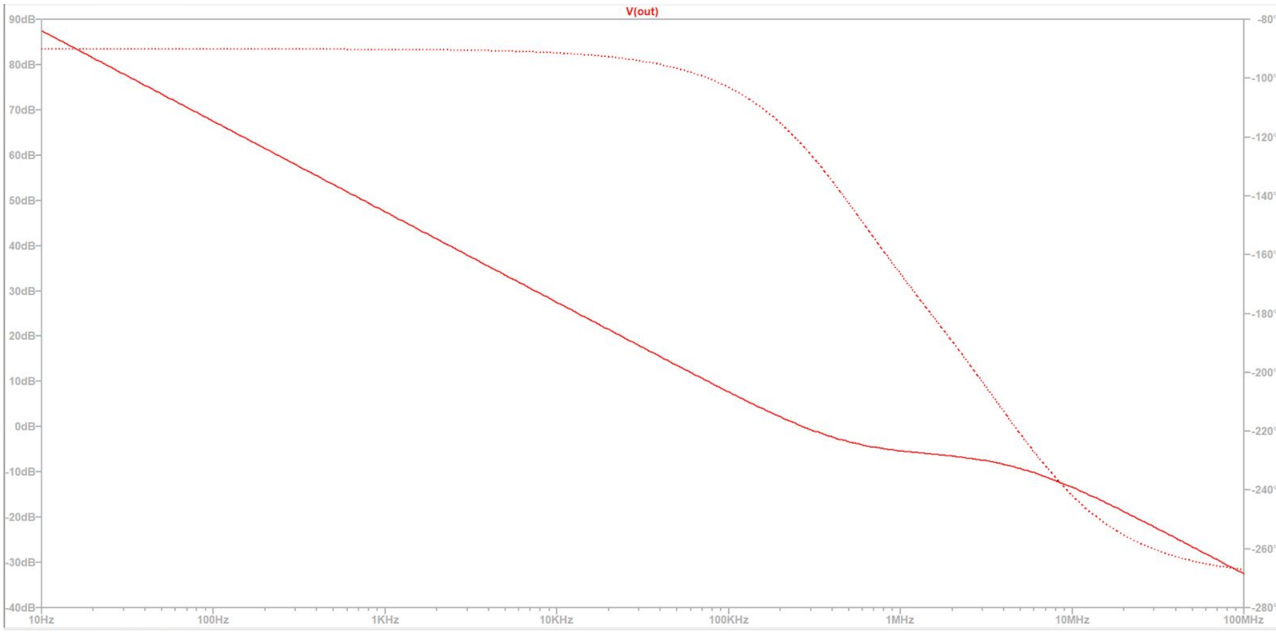

Fig.25:Frequency response of open loop configuration with Cc=100pF

Observations and Discussion :-

1. In this experiment we designed and simulated an operational amplifier in different configurations and observed the effect of various circuit and device parameters on the response of the system.
2. First we simulated the inverting configuration in op-amp,all the transient responses show that the output is phase shifted by 180^o with input as by the definition of the inverting configuration, as the input is connected to the inverted terminal so the output got shifted in phase by 180^o.
3. A sinusoidal input of amplitude 1 mV gave output sinusoidal waveform
   a. of amplitude of 10 mV with a 180 deg phase shift, thus giving a gain of 10 when R2/R1 = 10.(Fig.5)
   b. Of amplitude of 100 mV with a 180 deg phase shift, thus giving a gain of 100 when R2/R1 = 100.(Fig.7)
   c. With clipping when R2/R1=300 and input signal with amplitude 10mV(Fig.9)
4. Theoretically the gain of inverting op-amp should be equal to R2 /R1 , which is verified in the simulation.
5. Gain bandwidth product of the operational amplifier will be constant which can be seen from the fig.6 and Fig.8 from fig.6 to fig.8 we increased the gain by 10 times,The bandwidth got changed from 2.29 MHz to 239 KHz which is almost dropped by 10 times.i.eGain bandwidth remains constant.
6. Fig.10 shows the maximum gain achievable for the circuit as the output got clipped.
7. Fig.2 is the non-inverting configuration in op-amp,all the transient responses show that the outputs are in phase with input as by the definition of the non-inverting configuration, as the input is connected to the Non-inverted terminal so the output got shifted in phase by 360^o (i.e., inphase).

8. A sinusoidal input of amplitude 1 mV gave output sinusoidal waveform
    a. of amplitude of 10 mV with No phase shift, thus giving a gain of 10 when 1+R2/R1 = 10.(Fig.11)
    b. of amplitude of 100 mV with No phase shift, thus giving a gain of 50 when 1+R2/R1 = 50.(Fig.13)
    c. With clipping when 1+R2/R1=500 and input signal with amplitude 10mV(Fig.15)
9. Theoretically the gain of non-inverting op-amp should be equal to 1+R2 /R1 , which is verified in the simulation.
10. Gain bandwidth product of the operational amplifier will be constant which can be seen from the fig.12 and Fig.14 from fig.12 to fig.14 we increased the gain by 5 times,The bandwidth got changed from 2.443 MHz to 492.678 KHz which is almost dropped by 5 times.i.e., Gain bandwidth remains constant.
11. Fig.16 shows the maximum gain achievable for the circuit as the output got clipped.
12. In fig. 17 we observed the transient response of op-amp in voltage follower mode,it shows input is exactly the same as output.
13. In fig. 18 we observed the frequency response of op-amp in voltage follower mode when capacitor Cc is not used.
14. In fig.19 We can observe that the gain is 0dB upto 1 MHz frequency after which it rises to give a peak and then falls down.
15. Thus we can only use the voltage follower upto 1MHz frequency.
16. The op-amp has an upper limit on the amount of gain it can provide,which we call its saturation point.
17. In fig. 20,22,24 we observe the saturation effect of the opamp by running it in open loop configuration.
18. Ideally an op-amp in open loop should have an infinite gain but practically it is not possible and the output gets saturated to a maximum voltage approximately equal to the Vcc voltage supply.
19. In fig.21,23,25 we can see the effect of the capacitor Cc which is generally used to increase the phase margin of the amplifier.

Conclusion :-

The Operational amplifier is a very important electronic system which can be used for amplifying the strength of weak signals and can be used in various configurations according to our needs.