Validation Report

for

Application Protocol 210:

Electronic assembly, interconnect and packaging design

ISO/IS 10303-210:2009

ISO TC/184 SC/4 WG/3 N 2606
Supersedes
ISO TC/184 SC/4 WG/3 N 1892

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March 31, 1994 -- ISO CD Release
June 3, 2005 – Update for ISO CD/NWI Release of 2nd Edition
July 17, 2009 – Update for ISO/IS Release of 2nd Edition

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1.0 VALIDATION PLAN

1.1 Prologue

The objective of the STandard for the Exchange of Product model data (STEP) is to provide a complete, unambiguous, computer-interpretable definition of the physical and functional characteristics of a product throughout its life cycle. The STEP standard is a collection of Parts grouped into several classes which include Integrated Resources (IRs) and Application Protocols (APs). An AP provides a scope and a context for the general-purpose constructs defined in the IRs.

The entire set of STEP standards is called ISO 10303 Industrial Automation Systems: STEP. It is a draft international standard under the development of the International Organization for Standardization (ISO) technical committee 184 (TC184) sub-committee 4 (SC4). Specifically, the STEP Application Protocol 210 (**AP 210**) **Electronic assembly, interconnect and packaging design**, ISO 10303-210, specifies the requirements for the exchange of electrical printed circuit assembly (PCA) design information. It is developed by the **PDES, Inc. PIEE** project team. Recently the PIEE project was renamed the EMPilot project but in the context of this document references to PIEE will not be replaced.

1.2 Validation Approaches

AP 210 has been subjected to validation testing in each development phase to ensure that the scope and requirements are sufficiently covered within the AP. The AP 210 validation uses the following approaches:

1. In-process validation. Validation goes hand in hand with the model development process. It therefore serves as a built-in check to the model under development.

2. Validation with related parties. Periodic status updates, model walk-through's, workshops, and demonstrations are made for PIEE member companies, International Organization for Standardization (ISO) which sponsors the STEP standard, International Electrotechnical Commission (IEC), and IGES/PDES Organization (IPO) which coordinates Initial Graphics Exchange Specification (IGES) and Product Data Exchange using STEP (PDES) standard-making activities.

3. Validation with external parties. Existing EE-standard organizations and EE/computer-aided-design (CAD) vendors are encouraged to provide input to AP 210 during its development. Examples are American National Standards Institute (ANSI) Harmonization Workshops, Electronics Industries Association (EIA), etc.

4. Validation through production implementation. The protocol has been implemented in industrial organizations, including The Boeing Company, Rockwell Collins, Georgia

Institute of Technology, University of Illinois at Urbana-Champaign, NASA Goddard Space Flight Center, LKSoft Gmbh, SFM Technology, Prometheus Computing, and Theorem Solutions.

1.3 Validation Categories

The validation activities and results are documented following their completion. At this writing, the first two AP validation categories are substantially complete while others are partially done:

1. **Scope and requirements evaluation**. The purpose is to determine the proper context, scope, and information requirements by validating the **Application Activity Model (AAM)** and **Data Planning Model (DPM)**.

2. **Application Reference Model (ARM)** validation. The purpose is to determine the completeness and correctness of the information requirements of the ARM which should correspond to the scope defined in AAM and DPM.

3. **Integrated Resources (IR)** interpretation. The purpose is to determine how existing Integrated Resources among STEP APs are applied to meet specific information requirements of AP 210.

4. **Application Interpreted Model (AIM)** validation. The purpose is to verify that each information requirement in the ARM is correlated and represented in the AIM.

5. **Conformance requirements & test guidance evaluation**. The purpose is to verify that each substantial requirement defined in the ARM has at least one abstract test suite developed against it and that valid data can meet conformance requirements and classes within specified constraints. Abstract test suites were replaced with test cases and EXPRESS model based validation

6. **AP validation with prototype implementation**. The prototype is used to demonstrate how printed circuit assembly (PCA) design information can actually be exchanged through AP 210 among electronic computer-aided design (ECAD) systems for design and manufacturing purposes. The standard has been used to demonstrate integrating ECAD and mechanical computer-aided design (MCAD) systems for design and manufacturing.

7. **AP validation through production implementation**. The production software implementation is used for design and manufacturing purposes. Results from the production environment are fed back to the standards development community in the form of issues and enhancement requests.

2.0 SCOPE AND REQUIREMENTS EVALUATION (AAM & DPM)

The first phase of AP 210 includes the development of the **Application Activity Model (AAM)** followed by the **Data Planning Model (DPM)**. The AAM is used to document the printed circuit assembly (PCA) process to identify which activities and associated input, control, output and mechanism (ICOMs) should be within the scope of AP 210. A DPM is then formed by grouping these ICOMs into major categories according to domain information requirements and by denoting their correlation to each other.

2.1 In-Process Validation of AAM

In the AAM the entire process of functional decomposition, printed circuit physical design, and printed circuit assembly (PCA) manufacturing was synthesized into a perspective of information and activity flow. The portion of the process that falls within the scope of AP 210 was further decomposed and analyzed. The ICOMs required for each level of activities were identified and defined. To gain early industry participation and acceptance the validation process frequently occurred in parallel with the development process as follows:

1. Adoption of Institute for Interconnecting and Packaging Electronics Circuits (IPC) Terminology. Instead of redefining those terms that are widely used in the industry, whenever possible AP 210 adopts comparable terms and definitions from IPC-T-50E Terms and Definitions for Interconnecting and Packaging Electronic Circuits, which is published by the (IPC) and already has industry-wide acceptance. This was done with full knowledge and support of the IPC technical director.

2. Liaison with PDES Application Protocol for Electronics (PAP-E) project. The AAM was presented to the PAP-E project team. The design process described in the AAM was deemed to be compatible with theirs. Periodic joint meetings were held to share information on each other's development.

3. Collaboration with the PreAmp project. AP 210 focuses on the exchange of PCA design data between engineering and manufacturing. AP 220 focuses on the exchange of process planning information between manufacturing and production. The goal of the PreAmp project team is to generate PCA process planning and manufacturing information from AP 210 and AP 220. AP 210 and AP 220 are validated by PreAmp's successful prototype implementation in an actual PCA manufacturing environment.

2.2 Application Expert Workshops (AEW)

A series of AEWs were held at the following PIEE member companies for AAM validation:

Hughes Aircraft Co.	Fullerton, CA	910427
Rockwell International	Anaheim, CA Cedar Rapids, IA	920428 920818

Naval Air Warfare Center	Indianapolis, IN	920715
Digital Equipment Corp.	Marlboro, MA	920428
Sandia National Lab.	Albuquerque, NM	920511
Boeing	Seattle, WA	920519
Hewlett-Packard	Palo Alto, CA	920520

In-depth discussions of the Electrical Engineering (EE) design and manufacturing process were conducted in these workshops. PCA design, the scope of AP 210, was targeted, decomposed, and examined in detail. The ICOMs were studied and suggestions were incorporated into the AAM.

2.3 Validation of DPM

The ICOMs were identified and grouped through the AAM. From them, the scope, major information categories, and their correlations were derived and expressed in terms of the **Data Planning Model (DPM)**. The development and validation of the DPM was an iterative process. As the subsequent ARM was developed based on the DPM and the AAM-to-ARM mapping table (see Appendix), the DPM was further reviewed and refined to correspond with the **units of functionality (UoF)** of the ARM. The DPM was validated by the synchronization of the AAM and ARM.

The DPM and the units of functionality in the ARM were used to present a high level view of AP 210 to outside parties interested in developing vendor-specific ECAD-to-AP 210 translators for standardized PCA data exchange. Specific examples are:

1. Meeting with Application Specific Electronics Module Computer Aided (ASEM CAx) Alliance in Austin, Texas on December 16-17, 1993. The ASEM CAx Alliance is a program funded by the DoD Advanced Research Projects Agency (ARPA). It is led by Microelectronics & Computer Technology Corporation (MCC). Organizations participating include U.S. Air Force, Texas Instruments, Harris Corporation (owner of Scicards), Racal-Redac Systems Ltd., Cadence, IBM Corporation, and Motorola.

2. Meeting with two representatives from Cadence and sixteen representatives from Digital Equipment in Marlboro, Massachusetts on February 18, 1994.

3. Meeting with IBM, a PDES, Inc. member, in Austin, TX on 17 March 1994.

In all cases, the DPM was used to represent the kind of information that would be incorporated in the AP 210 ARM. Detailed questions were discussed and answered. Suggestions were incorporated into the model development. All of these served as a check that the information categories included will satisfy the initial expectations of the potential users.

4. Meetings with IPC Representatives during 1994 and 1995. Further detailed technical reviews were held during the 1994 and 1995 time frame with Dieter Bergman, Chief Technology Officer of the IPC to address specifically issues related to reliability determination of high density interconnect. Several significant model changes were incorporated to address these issues, resulting in a robust model suitable for analysis of high density interconnect.

5. Requirements refinement from industry continued to occur as production implementations were rolled out. Interactions with German FED consortium led to the stackup model creation for the use case of PWB fabricators to OEM design teams.

3.0 ARM VALIDATION

3.1 In-Process Collaboration with Other Standards

The PIEE team has incorporated input and feedback from various standards-making organizations during the development phase of AP 210. The information collected from external sources has validated the development of AP 210. This includes the following:

1. Reference to Electronic Design Interchange Format (EDIF) standard. EDIF is a design data exchange standard used extensively in the electronic design automation (EDA) industry for the exchange of data between computer aided engineering and design systems (CAE/CAD). It is a product of international joint development between the EDA industry and universities under the sponsorship of the Electronic Industries Association (EIA). The goal is to combine the extensive descriptive capabilities of EDIF in electronic design data and STEP in product life-cycle data.

a. Reference to EDIF Conceptual Model of a PCB (EDIF PCB) version 9. In the beginning of ARM development the EDIF PCB model was used as a reference to articulate requirements for two units of functionality, namely printed circuit board and printed circuit assembly. They were evolved to the present form through other deliberations.

b. EDIF-PIEE Joint Agreement. During the Design Automation Conference (DAC) held in June 1992 in Anaheim, California, USA, PIEE and EDIF announced a joint agreement to work together on PCA design and manufacturing standards based on the EDIF Information Models.

c. Critique from EDIF. Key EDIF personnel are on the distribution list for major AP 210 releases for their critique. On 7-8 October 1993 members of IEC/TC93/WG1 who were also representatives from EDIF, PAP-E, and PIEE convened at University of Manchester, England which is the major EDIF development centre. Suggestions from this meeting were incorporated into AP 210 models.

2. Adoption of IPC terminology. From the beginning of ARM development IPC terms were used whenever possible. The intention is to adopt those terms and associated concepts that have wide industry acceptance and unambiguous meanings. An IPC technical representative has frequently participated in the ARM development sessions during the development stage.

3. Reference to Cal-Poly Layered Electrical Product (LEP). The LEP model has some degree of acceptance among the IGES community and meets the MIL-D-28000 Class III (electrical) standard. Two members of the ARM development team were members of the Cal-Poly LEP team. Some LEP concepts such as stratum were used in the draft ARM.

4. Critique from Racal-Redac Systems Ltd. A technical representative from Racal-Redac Systems, Ltd. who has in-depth knowledge of Racal-Redac Systems Ltd's and EDIF's information models frequently participates in the AP 210 model development sessions and provided critique.

5. Co-development with Pre-competitive Advanced manufacturing program (PreAmp). The PreAmp project focuses on the PCA product information to be shared between process planning and manufacturing operations. The product data passed to PreAmp originates from an ECAD system which translates to AP 210 and then to AP 220. PreAmp serves as a check and validation of the AP 210 ARM.

6. Cooperation with PAP-E (AP 211).

7. Cooperation with AP 212 (Electrotechnical plants).

8. Cooperation with Cad Framework Initiative Component Information Representation project (CFI CIR).

9. Cooperation with IEC TC3 & ISO TC184/SC4/WG2.

3.2 Review with Other Parties

1. Model walk-through with ISO. PIEE representatives have been attending the International Standard Organization (ISO) quarterly meetings to provide updated ARM model walk-through's to international EE domain experts. These include:

ISO Location	Torino, Italy
Period	17/Feb/1993-26/Feb/1993
Audience	ISO TC184/SC4 -- JWG9, WG2
Organizations represented	* Institute for Machine Tools & Mfg, Swiss Fed Inst of Technology, Zurich * ATG of EDS, MI, USA * Institut fur Maschinenwesen der Technischen Univeritat Clausthal, Clausthal-Zellerfeld, Germany * Nippon Computer Graphics Asso., Japan * Pentel, Soka city, Japan * Newport News Shipbuilding, USA * Ecole Nationale Superieure de Mecanique et d'Aerotechnique, Poiters, France * VW-GEDAS, Berlin, Germany * Aerospatiale, Paris, France * Tanatsugu Co., Osaka, Japan * Tokyo Inst. of Tech., Yokohama, Japan

ISO Location	Oslo, Norway
Period	1/Jan/1992-8/Feb/1992
Audience	ISO/TC184/SC4/WG4/JWG9
Organizations represented	* Microelectronics & Computer Technology Corporation, Texas, USA * Norwegian Electric Power Research Inst. * Siemens, Erlangen, Germany * NIST, Maryland, USA * Fraunhofer Institut fur Graphische Datenverarbeitung, Darmstadt, Germany * Normenausschuss Maschinenbau, im DIN, Frankfurt, Germany * Institutet for Verkstadsteknisk Forskning, Gothenburg, Sweden * Kyushu Institute of Technology, Fukuoka, Japan * Institut de Recherche en Productique et Logistique, Arcueil, France * U. of Manchester, Comp. Sci. Dept, UK * Westinghouse, Maryland, USA * AT&T Network Systems, Hilversum, the Netherlands * GOSET, Nanterre, France

2. Model walk-through with IPO. Through the invitation of the IPO Electrical Application Committee (EAC), PIEE representatives have been attending the IPO quarterly meetings since 1991 to provide updated ARM model walk-through's to EE domain experts in the EAC sessions. The latest meetings include:

IPO Location	Mesa, Arizona, USA
Period	January 1994
Audience	IPO EAC attendees
Organizations represented	* Siemens AG, Erlangen, Germany * Logic Modeling, CA, USA * Raytheon, MA, USA * Allied-Signal Aerospace Co., MO, USA * Intermetrics, VA, USA * IBM Corporation, NY, USA * International TechneGroup Inc., OH, USA * Sandia National Lab., NM, USA * National Research Council, Ontario, Canada * National Semiconductor, ME, USA * INFO Enterprises, Inc., AZ, USA * Fraunhofer, Darmstadt, Germany * Institute of Machine Tools and Manufacturing, Swiss Institute of Technology, Eth Zurich, Switzerland * Grumman Data Systems, SC, USA * Daimler Benz, Ulm, Germany * NASA, MD, USA * Raytheon, MA, USA * South Carolina Research Authority, USA

IPO Location	Novi, Michigan, USA
Period	September 1993
Audience	IPO EAC attendees
Organizations represented	* South Carolina Research Authority, SC, USA * NIST, MD, USA * Sandia National Lab., NM, USA * CALS, Air Force, USA * JEH Consulting, CO, USA

IPO Location	Atlanta, Georgia, USA
Period	June 1993
Audience	IPO EAC attendees
Organizations represented	* Intermetrics, VA, USA * Grumman Data Systems, USA * Institute of Electrical and Electronics Engineers * NIST, MD, USA * National Research Council, Ontario, Canada * South Carolina Research Authority, SC, USA * Sandia National Lab., NM, USA

IPO Location	Nashville, Tennessee, USA
Period	April 1993
Audience	IPO EAC attendees
Organizations represented	* JEH Consulting, Inc. * Naval Air Warfare Center, CA, USA * South Carolina Research Authority, USA * NIST, MD, USA * NASA, MD, USA * Sandia National Lab., NM, USA * CALS, Air Force, USA * IBM Corporation, NY, USA * International TechneGroup Inc., OH, USA * General Dynamics, CN, USA * IPC, IL, USA

IPO Location	Costa Mesa, California, USA
Period	January 1993
Audience	IPO EAC attendees
Organizations represented	* South Carolina Research Authority, USA * Sandia National Lab., NM, USA * International TechneGroup Inc., OH USA * Raytheon, MA, USA * NASA, MD, USA * Air Force, USA

Earlier IPO meetings with PIEE's participation included the following:
October 1992 at Dallas/Fort Worth, TX;
July 1992 at Providence, RI;
April 1992 at Seattle, WA;
January 1992 at Salt Lake City, UT;
October 1991 at Houston, TX; and
July 1991 at Pittsburgh, PA.

3. American National Standards Institute (ANSI) Harmonization Workshops. The purpose of the workshops was to encourage those organizations responsible for making EE standards to:

- o discuss their data models,
- o map terms of one standard to others, and
- o trace the origins and evolution of terms.

AP 210 ARM was presented in the workshops in different stages of development. Suggestions received were incorporated into AP 210 ARM. Suspected areas of overlap with and among the four ANSI standards being harmonized were based on an evaluation report entitled **Harmonizing CALS Product Data Description Standards** published by the Electronic Industries Association (EIA) Ad Hoc CALS Study Group in February 1989. The four ANSI standards involved are EDIF, IPC, IGES, and Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL). In 1993, the workshop became the International Electrotechnical Commission (IEC) Technical Committee 93 (TC93) Working Group 1 (WG1).

Some of the dates and locations of the previous workshops were:
10-13-DEC-91 Albuquerque, NM, USA
13-15-MAY-92 Albuquerque, NM, USA
04-06-AUG-92 Tukwila, WA, USA
11-13-AUG-93 Albuquerque, NM, USA

4. Product Data Information Technology, Inc. (PDIT) Consulting. A STEP modeling consultant from PDIT, Inc. who is also the convener of ISO TC184/SC4/WG4, provided periodic reviews of the domain requirements from a modeling perspective in preparation of the ARM's interpretation and mapping to the STEP Integrated Resources. These meetings have included the following:

November 1992 at Hewlett-Packard in Palo Alto, CA;
February 1993 at SCRA, North Charleston, SC; and
September 1993 at PDES, Inc. off-site meeting in Tucson, AZ.

5. External Communications. Suggestions from the following activities were also incorporated into AP 210:

a. ProSTEP Workshop in Berlin, Germany. The AP 210 ARM was presented to the German STEP specialists in February 1993.

b. Workshop at Microelectronics and Computer Technology Corporation (MCC) in Austin, TX. A detail model walk-through and training on the ARM was presented to MCC domain experts by a PIEE representative on January 27-28, 1994.

c. ASEM CAx Alliance Meeting. On 18 February 1994 the units of functionality and associated key concepts were presented to ASEM members by an MCC expert in Marina Del Rey, CA. A preliminary mapping of the ASEM requirements to AP 210 and EDIF PCB was attempted. ASEM is a DoD ARPA-funded program. Acceptance by ASEM could mean the endorsement of AP 210 as a viable standard.

d. Detailed ARM walk-through given to Cadence and Digital Equipment Corporation representatives in Marlboro, MA on 25 February 1994.

6. During the period of 1994-2004 several additional undocumented walkthroughs and training sessions were held at ISO TC184/SC4 meetings, at PDES Inc offsite conferences, and at university venues such as Georgia Institute of Technology(GIT) and at NIST.

3.3 Data Population

The standard has proven to be a robust model. Production implementations have exercised approximately 60% of the model to date. More than 2000 ECAD models have been converted using the model.

3.4 Issues Log and Resolutions

AP 210 is supported with an internal bug tracking system at http://locke.dcnicn.com/bugzilla/iso10303/. Interested parties may access the issues upon request of the ISO TC 184/SC 4 Secretariat: http://www.tc184-sc4.org. Note that many issues are internal and not of general interest because they relate to internal working drafts. The issues log supporting the 2nd edition DIS to IS transition is ISO TC 184/SC 4/WG 3 N 2607, available at http://www.tc184-sc4.org.

4.0 INTEGRATED RESOURCES INTERPRETATION

4.1 Integrated Resources in Use

The following standards form the **Integrated Resources (IR)** from which information are interpreted to meet the specific information requirements of AP 210 ARM:

1. ISO 10303-41 Industrial automation systems and integration -- Product data representation and exchange -- Part 41: Integrated resources: Fundamentals of product description and support.

2. ISO 10303-42 Industrial automation systems and integration -- Product data representation and exchange -- Part 42: Integrated resources: Geometric and topological representation.

3. ISO 10303-43 Industrial automation systems and integration -- Product data representation and exchange -- Part 43: Integrated resources: Representation structures.

4. ISO 10303-44 Industrial automation systems and integration -- Product data representation and exchange -- Part 44: Integrated resources: Product structure configuration.

5. ISO 10303-45 Industrial automation systems and integration -- Product data representation and exchange -- Part 45: Integrated resources: Material.

6. ISO 10303-46 Industrial automation systems and integration -- Product data representation and exchange -- Part 46: Integrated resources: Visual presentation.

7. ISO 10303-47 Industrial automation systems and integration -- Product data representation and exchange -- Part 47: Integrated resources: Shape variation tolerances.

4.2 Interpretation Workshops

One STEP-modeling consultant from PDIT, Inc. and one from Grumman Data Systems Inc. assisted PIEE in constructing the ARM-to-AIM mapping tables with reference to the Integrated Resources. The workshops for this purpose were held in:
November 1993 at South Carolina Research Authority (SCRA) in N. Charleston, SC;
December 1993 at PDIT, Inc. in Long Beach, CA; and
February 1993 at PDIT, Inc. in Long Beach, CA.
The team assumed responsibility for interpretation after 1993.

4.3 Application Integrated Constructs (AIC)

AP 210 AIC's have been developed in conjunction with WG12.

5.0 AIM VALIDATION

AP 210 AIM validation was included in implementations at The Boeing Company and at Rockwell Collins in 1994-2008 of the CD, DIS, IS version of the first and second editions of the standard. AIM validations were accomplished through round robin testing at LKSoft GmbH. The IDF->210 converter and the PDES Inc. Board Viewer are AIM based implementations. The AP 210 project has developed a public domain Eclipse (www.eclipse.org) based validator (http://www.jsdai.net) as part of JSDAI V 4 and above. InterCAX (www.intercax.com) has performed extensive independent validation using JSDAI. JSDAI converts the AIM files to XIM files, which are based on an EXPRESS schema that is an implementable extension of the ARM and thus includes the ARM rules. The converted files are ISO 10303-21 compliant and may be checked with any model checker. The project uses the following validators:

- JSDAI (http://www.jsdai.net)
- Express Engine (http://sourceforge.net/projects/exp-engine)
- ECCO (http://www.pdtec.de)
- EDMS model checker (http://www.epmtech.jotne.com/)

6.0 CONFORMANCE REQUIREMENTS & TEST GUIDANCE EVALUATION

6.1 Conformance Requirements and Options

Conformance Classes that have been tested extensively include CC1, CC8, CC9, and more recently CC40. For edition 2 of the standard, the project has started migrating to a more granular approach and introduced the concept of Conformance Options. The intent is to enable an implementer to more easily match the capability of their application with a subset of the standard for certification purposes. This methodology has proven useful in a number of cases but is still not ideal. Implementers need to decide which AP 210 product definitions and relationships are essential to their application and work with the project to determine course of action for successful implementation. Practical implementations currently focus on the specific views that are to be exchanged and any associated management and requirements data is dependent on the enterprise engineering computing environment.

There are currently over 180 conformance options with more work to go to distinguish levels of detail in the layout model to support the widely variant levels of complexity from the Eagle™ free EDA tool to e.g., Zuken CR5000™ tool suite.

Views in AP 210 are classified as definitional, document related, occurrence related, or requirement related views. Occurrence related views help to compose definitional related views and are usually instances of a definitional view. The view hierarchical relationship is represented by indenting one name from it's supertype.

6.2 Product definitional views

Product definitional views that may be supported include:

- product_view_definition
- substance_view_definition

- information_definition
- functional_unit_definition
- functional_unit_usage_view
- functional_unit_network_definition
- electrical_network_definition
- thermal_network_definition
- functional_specification_definition
- analytical_model_definition
- software_definition
- rule_software_definition
- rule_definition
- back_chaining_rule
- forward_chaining_rule
- rule_set
- rule_set_group
- evaluation_view_definition
- design_constraint_definition
- part_view_definition
- collection_definition
- stock_material
- anisotropic_material
- braided_assembly
- discontinuous_fiber_assembly
- filament_assembly
- isotropic_material
- stock_core
- woven_assembly
- physical_unit_interconnect_definition
- assembly_definition
- sequential_laminate_stackup_definition
- effectivity_controlled_assembly_definition
- interconnect_module_design_view
- layered_interconnect_module_design_view
- layout_macro_definition
- layered_interconnect_panel_design_view
- assembly_module_design_view
- layered_assembly_panel_design_view
- layered_assembly_module_design_view
- part_design_view
- interconnect_module_design_view
- layered_interconnect_module_design_view
- layout_macro_definition

- layered_interconnect_panel_design_view
- assembly_module_design_view
- layered_assembly_panel_design_view
- layered_assembly_module_design_view
- physical_unit_network_definition
- part_usage_view
- cable_usage_view
- package
- altered_package
- packaged_part
- altered_packaged_part
- minimally_defined_connector
- packaged_connector
- assembly_module_usage_view
- layered_assembly_module_usage_view
- bare_die
- interconnect_module_usage_view
- layered_interconnect_module_usage_view
- breakdown_element_definition
- physical_element_definition
- functional_element_definition
- mating_connector_usage
- functional_unit_network_node_definition
- thermal_functional_unit_network_node_definition
- equivalent_stackup_model_definition
- equivalent_sub_stack_definition
- externally_defined_view_definition
- library_view_definition
- template_definition
- non_conductive_cross_section_template
- printed_part_template
- layout_macro_floor_plan_template
- basic_multi_stratum_printed_part_template
- printed_connector_template
- printed_part_cross_section_template
- structured_printed_part_template
- multi_stratum_printed_part_template
- printed_tiebar_template
- single_stratum_printed_part_template
- parametric_template
- fill_area_template
- hatch_area_template

- tile_area_template
- teardrop_template
- snowball_template
- teardrop_by_angle_template
- teardrop_by_length_template
- trace_template
- default_trace_template
- part_string_template
- part_text_template
- single_stratum_template
- single_stratum_continuous_template
- material_removal_feature_template
- electrical_isolation_removal_template
- dependent_electrical_isolation_removal_template
- stratum_feature_template
- land_physical_template
- default_attachment_size_based_land_physical_template
- default_passage_based_land_physical_template
- default_plated_passage_based_land_physical_template
- default_unsupported_passage_based_land_physical_template
- teardrop_template
- snowball_template
- teardrop_by_angle_template
- teardrop_by_length_template
- single_stratum_structured_template
- single_stratum_printed_part_template
- material_removal_structured_template
- thermal_isolation_removal_template
- dependent_thermal_isolation_removal_template
- single_stratum_special_symbol_template
- special_symbol_template
- multi_stratum_special_symbol_template
- single_stratum_special_symbol_template
- stratum_stack_model
- library_stack_model
- design_stack_model
- stratum_sub_stack
- local_linear_stack
- passage_technology_allocation_to_stack_model
- geometric_template
- continuous_template
- component_termination_passage_template

- single_stratum_continuous_template
- material_removal_feature_template
- electrical_isolation_removal_template
- dependent_electrical_isolation_removal_template
- stratum_feature_template
- land_physical_template
- default_attachment_size_based_land_physical_template
- default_passage_based_land_physical_template
- default_plated_passage_based_land_physical_template
- default_unsupported_passage_based_land_physical_template
- unsupported_passage_template
- blind_passage_template
- counterbore_passage_template
- countersunk_passage_template
- via_template
- inter_stratum_feature_template
- component_termination_passage_template
- inter_stratum_feature_edge_segment_template
- inter_stratum_feature_edge_segment_template_with_cross_section
- inter_stratum_feature_edge_template
- unsupported_passage_template
- blind_passage_template
- counterbore_passage_template
- countersunk_passage_template
- via_template
- structured_inter_stratum_feature_template
- structured_template
- structured_printed_part_template
- multi_stratum_printed_part_template
- printed_tiebar_template
- single_stratum_printed_part_template
- multi_stratum_structured_template
- multi_stratum_printed_part_template
- multi_stratum_special_symbol_template
- padstack_definition
- passage_padstack_definition
- complex_passage_padstack_definition
- stratum_stack_dependent_template
- complex_passage_padstack_definition
- structured_inter_stratum_feature_template
- generic_footprint_definition
- breakout_footprint_definition

- footprint_definition
- single_stratum_structured_template
- single_stratum_printed_part_template
- material_removal_structured_template
- thermal_isolation_removal_template
- dependent_thermal_isolation_removal_template
- single_stratum_special_symbol_template

6.3 Product document views

Product document views that may be supported include:

- document_definition
- specification_definition
- design_specification
- interface_specification_document_definition
- language_reference_manual
- material_specification
- surface_finish_specification
- process_specification
- fabrication_technology_specification
- assembly_technology_specification
- test_specification
- digital_document_definition
- physical_document_definition

6.4 Product occurrence views

Product occurrence views that may be supported include:

- product_occurrence
- part_occurrence
- definition_based_part_occurrence
- physical_component
- assembly_module_macro_component
- sequential_laminate_stackup_component
- cable_component
- interconnect_module_macro_component
- assembly_module_component
- physical_shield
- routed_physical_shield
- interconnect_module_component
- bare_die_component
- packaged_component
- packaged_connector_component

- routed_interconnect_component
- routed_physical_component
- routed_physical_shield
- interface_component
- packaged_connector_component
- specification_based_part_occurrence
- definition_based_product_occurrence
- definition_based_function_occurrence
- functional_unit
- assembly_component
- laminate_component
- fiducial
- inter_stratum_feature
- cutout
- partially_plated_cutout
- physical_connectivity_interrupting_cutout
- plated_cutout
- cutout_edge_segment
- plated_cutout_edge_segment
- unplated_cutout_edge_segment
- dielectric_material_passage
- interconnect_module_edge
- partially_plated_interconnect_module_edge
- plated_interconnect_module_edge
- interconnect_module_edge_segment
- plated_interconnect_module_edge_segment
- unplated_interconnect_module_edge_segment
- plated_inter_stratum_feature
- plated_cutout
- plated_cutout_edge_segment
- plated_interconnect_module_edge
- plated_interconnect_module_edge_segment
- plated_passage
- component_termination_passage
- via
- blind_via
- non_conductive_base_blind_via
- plated_conductive_base_blind_via
- buried_via
- interfacial_connection
- indirect_stratum_component_join_implementation
- physical_network_supporting_inter_stratum_feature

- unsupported_passage
- generic_laminate_text_component
- material_removal_laminate_text_component
- additive_laminate_text_component
- laminate_text_string_component
- material_removal_laminate_component
- electrical_isolation_laminate_component
- interface_access_material_removal_laminate_component
- multi_layer_material_removal_laminate_component
- probe_access_area
- internal_probe_access_area
- stratum_feature_template_component
- area_component
- connected_area_component
- conductive_interconnect_element
- conductive_interconnect_element_with_pre_defined_transitions
- unrouted_conductive_interconnect_element
- interface_access_stratum_feature_template_component
- multi_layer_stratum_feature_template_component
- stratum_feature_template_component_with_stratum_feature
- land
- contact_size_dependent_land
- inter_stratum_feature_dependent_land
- plated_passage_dependent_land
- unsupported_passage_dependent_land
- land_with_join_terminal
- integral_shield
- routed_shield
- structured_layout_component_sub_assembly_relationship_with_component
- assembly_group_component
- structured_layout_component
- footprint_occurrence
- breakout_occurrence
- material_removal_structured_component
- dependent_thermal_isolation_removal_component
- multi_stratum_special_symbol_component
- padstack_occurrence
- single_stratum_special_symbol_component
- primary_stratum_indicator_symbol
- tiebar_printed_component
- multi_stratum_printed_component
- single_stratum_printed_component

- array_placement_group
- laminate_text_string_component
- linear_array_placement_group_component
- rectangular_array_placement_group_component
- interfaced_group_component
- printed_component
- layout_macro_component
- basic_multi_stratum_printed_component
- tiebar_printed_component
- multi_stratum_printed_component
- single_stratum_printed_component
- printed_connector_component
- routed_transmission_line
- physical_component
- assembly_module_macro_component
- sequential_laminate_stackup_component
- cable_component
- interconnect_module_macro_component
- assembly_module_component
- physical_shield
- routed_physical_shield
- interconnect_module_component
- bare_die_component
- packaged_component
- packaged_connector_component
- routed_interconnect_component
- routed_physical_component
- routed_physical_shield
- interface_component
- packaged_connector_component
- thermal_component
- definition_based_part_occurrence
- physical_component
- assembly_module_macro_component
- sequential_laminate_stackup_component
- cable_component
- interconnect_module_macro_component
- assembly_module_component
- physical_shield
- routed_physical_shield
- interconnect_module_component
- bare_die_component

- packaged_component
- packaged_connector_component
- routed_interconnect_component
- routed_physical_component
- routed_physical_shield
- interface_component
- packaged_connector_component
- product_occurrence_with_quantity
- quantified_instance
- selected_instance
- single_instance
- assembly_module_macro_component
- sequential_laminate_stackup_component
- specification_based_function_occurrence
- cable_component
- interconnect_module_macro_component
- assembly_module_component
- laminate_component
- fiducial
- inter_stratum_feature
- cutout
- partially_plated_cutout
- physical_connectivity_interrupting_cutout
- plated_cutout
- cutout_edge_segment
- plated_cutout_edge_segment
- unplated_cutout_edge_segment
- dielectric_material_passage
- interconnect_module_edge
- partially_plated_interconnect_module_edge
- plated_interconnect_module_edge
- interconnect_module_edge_segment
- plated_interconnect_module_edge_segment
- unplated_interconnect_module_edge_segment
- plated_inter_stratum_feature
- plated_cutout
- plated_cutout_edge_segment
- plated_interconnect_module_edge
- plated_interconnect_module_edge_segment
- plated_passage
- component_termination_passage
- via

- blind_via
- non_conductive_base_blind_via
- plated_conductive_base_blind_via
- buried_via
- interfacial_connection
- indirect_stratum_component_join_implementation
- physical_network_supporting_inter_stratum_feature
- unsupported_passage
- generic_laminate_text_component
- material_removal_laminate_text_component
- additive_laminate_text_component
- laminate_text_string_component
- material_removal_laminate_component
- electrical_isolation_laminate_component
- interface_access_material_removal_laminate_component
- multi_layer_material_removal_laminate_component
- probe_access_area
- internal_probe_access_area
- stratum_feature_template_component
- area_component
- connected_area_component
- conductive_interconnect_element
- conductive_interconnect_element_with_pre_defined_transitions
- unrouted_conductive_interconnect_element
- interface_access_stratum_feature_template_component
- multi_layer_stratum_feature_template_component
- stratum_feature_template_component_with_stratum_feature
- land
- contact_size_dependent_land
- inter_stratum_feature_dependent_land
- plated_passage_dependent_land
- unsupported_passage_dependent_land
- land_with_join_terminal
- integral_shield
- routed_shield
- interconnect_module_component
- bare_die_component
- packaged_component
- packaged_connector_component
- interface_component
- packaged_connector_component
- assembly_group_component

- structured_layout_component
- footprint_occurrence
- breakout_occurrence
- material_removal_structured_component
- dependent_thermal_isolation_removal_component
- multi_stratum_special_symbol_component
- padstack_occurrence
- single_stratum_special_symbol_component
- primary_stratum_indicator_symbol
- tiebar_printed_component
- multi_stratum_printed_component
- single_stratum_printed_component
- array_placement_group
- laminate_text_string_component
- linear_array_placement_group_component
- rectangular_array_placement_group_component
- interfaced_group_component
- printed_component
- layout_macro_component
- basic_multi_stratum_printed_component
- tiebar_printed_component
- multi_stratum_printed_component
- single_stratum_printed_component
- printed_connector_component
- routed_transmission_line
- specification_based_product_occurrence
- specification_based_function_occurrence
- specification_based_part_occurrence
- package_footprint_relationship_definition
- stratum
- derived_stratum
- design_layer_stratum
- documentation_layer_stratum
- part_view_definition
- constituent_part
- composite_assembly
- filament_laminate
- ply
- ply_laminate
- ply_piece
- processed_core
- laminate_table

- part_laminate_table
- composite_assembly_table
- ply_laminate_table
- zone_structural_makeup
- percentage_laminate_table
- smeared_material
- thickness_laminate_table

6.5 Product requirement views

Product requirement views that may be supported include:

- requirement_view_definition
- protocol_physical_layer_definition
- protocol_physical_layer_definition_with_characterization
- predefined_requirement_view_definition
- fabrication_thickness_requirement
- layout_land_width_tolerance_requirement
- layout_line_width_tolerance_requirement
- layout_spacing_requirement
- layer_qualified_layout_spacing_requirement
- area_qualified_layout_spacing_requirement
- interface_requirement
- impedance_measurement_setup_requirement
- impedance_requirement
- physical_connectivity_layout_topology_requirement
- constraint_occurrence
- termination_constraint
- view_based_constraint_occurrence
- shape_and_view_based_constraint_occurrence
- design_characteristic_occurrence
- material_electrical_conductivity_requirement
- assembly_group_spacing_requirement
- assembly_spacing_requirement
- item_restricted_requirement
- electrical_isolation_requirement
- thermal_isolation_requirement
- placement_group_requirement_definition

A specific definitional view may relate to one or more occurrence views to help compose it.
The EMPilot project is currently surveying implementations to determine commonly implemented views and levels of detail currently implemented for each view.
This will serve as a baseline for new implementations as the projects gauge the level of data interoperability desired in their particular use case.

At this point the EMPilot project does not have a formal certification program for AP 210 compliance. A goal is to have Conformance options correspond to occurrence views that are optional for a definitional view. Example: A conformance option of "derived stratum" for an interconnect would specify support for the occurrence view Derived_stratum. A conformance option of "basic interconnect" would not.

6.4 Levels of Detail

Once a view or set of views is selected for implementation, the level of detail to be supported is defined and results in a set of ARM and AIM entities to populate or to retrieve. During development EXPRESS model checkers are used to validate pre-processors and manually created unit test cases for post-processors. There are two levels of EXPRESS model checkers. Level one checking is that all population constraints in the AIM schema are conformed to. Level two checking is an ARM checking using the XIM extensions to the ARM in combination with functions compiled from the mapping tables to convert AIM data to XIM data. Once that conversion is done, EXPRESS validation is accomplished on the XIM data. Level three checking is accomplished using AP 210 interfaces on two applications and verifying that source data is correctly interpreted by the target application. Level three checking may be manual or may be automated depending on the nature of the communicating application and the business case. Level four checking is manual inspection of the results of the conversion, usually in conjunction with an EMPilot team member. Level four checking involves reviewing implementations of special cases such as ECAD-Analysis where the design may be incomplete, or where some population constraints may not be able to be satisfied due to the use case.

Evidence that checking at Levels one through three has been successful are usually required to obtain concurrence from the EMPilot project that an application is compliant to the AP 210 standard. Level four issues require documentation to ensure that downstream applications provide updates to the model as needed for success in the business process. Significant resources have been expended to accelerate development of interfaces compliant to AP 210 and implementation projects are encouraged to contribute to the common body of knowledge with validated test cases for specific applications.

6.5 Test Cases

Appendix B provides historical record of the initial set of test cases and their descriptions.

The EMPilot project maintains a repository of unit test cases to ease initial implementation development. Copies of the repository are available upon request. Both the initial test cases and the unit test cases are for the purposes of manual population by software developer directly or by a simulated end user in the context of a CAD system.

The EMPilot project maintains a repository of functional test cases which are more complex but provide realistic examples for implementation debugging. Copies of the test cases are available

under non-disclosure agreements since they may contain proprietary data.

The EMPilot project maintains a public web site that contains sample files for demonstration and educational purposes. http://www.wikistep.org.

The EMPilot project maintains the AP 210 recommended practices documents on wikistep which includes some unit test cases for initial development testing.

The CAX-IF http://www.cax-if.org maintains a repository of test cases for the AP 203 subset of AP 210.

6.6 Recommended Practices

The EMPilot project maintains recommended practices on a public web site http://www.wikistep.org. In addition to traditional recommended practices, the site contains extensive Java™ code and query diagrams to accelerate initial implementation of commonly used functions such as getting the reference designator of a component. Currently available recommendations include:

- Recommendation for thermal component modeling using industry standard component models.
- Recommendation for modeling electrical component packages based on data extracted from JEDEC™ Publication 95. Included are 400 AP 210 instance models spanning 24 separate JEDEC™ SMT package families.

6.7 AP 210 E2 Validation Project

The AP 210 Verification and Validation (V&V) Testbed project originated to validate models, methods, and tools that implement the standard. In Phase 1 of this project, the InterCAX team[1] finished several tasks towards developing a verification and validation testbed framework for the standard. The team developed a tool for validating both ARM and MIM-based AP210 instance models. This validation tool checks if AP210 instance models conform to the AP210 module-ARM and MIM schemas. The tool is particularly useful as it executes mappings from AIM data to augmented ARM data to enable the ARM rules to be evaluated for the sample data. This allows the AP 210 project to not have duplicate rules in the ARM and AIM. The tool is available for free as part of the JSDAI framework on Sourceforge. The team collected 155 AP 210 instance models and developed a scheme to classify these models. By providing a clear identification of design characteristics in the classification scheme, the properties help present the higher coverage of design concepts in AP 210 as compared to other electronics design standards, and provide a mechanism to search for AP 210 models in a repository. Future plans

[1] InterCAX team = InterCAX (www.intercax.com) + LKSoft (www.lksoft.com)

include: update all models to 2nd edition; find a repository site for the models; determine a supported subset of the 155 models (some are redundant with respect to data coverage); coordinate with cax-if on joint efforts.

6.8 AP 203 E2 Validation Report – ISO TC184/SC4/WG3 N2380

AP 210 is a superset of AP 203 edition 2, Configuration controlled 3D design of mechanical parts and assemblies. The validation report and test case documentation for AP 203 E2 is included herein by reference: **ISO TC184/SC4/WG3 N2380**

7.0 VALIDATION WITH PROTOTYPE AND PRODUCTION IMPLEMENTATION

A realistic validation of AP 210 is performed through demonstrations of prototypes and vendor-specific ECAD-AP 210-CAD; ECAD-AP 210-MCAD; or ECAD-AP 210-Analysis translators. Their successful performance provides a high level of confidence in the utility of the AP, and led to production implementations. Paragraphs 7.1 through 7.5 are included for historical purposes. Current production use case implementations are specified in footnotes and in clause 7.6.

7.1 Demonstration Plan

A set of four demonstrations based on the IGES-EAC flasher signal circuit was used to validate the AP 210 prototype. These demonstrations include:

1. Demo 1 -- Assemble PCA. This demonstration involved the translation of PCA design information from a Mentor Graphics System (MGS) to an AP 210 physical file. The AP 210 information was then fed to the Rapid Access Manufactured Part (RAMP) process planning software to provide manufacturing information for the flasher board.

   a. The demonstration board was fabricated in October 1993 and presented at the Computer Aided Lifecycle Support (CALS) Exposition in November 1993 in Atlanta, GA. The translator used for the demonstration was co-developed by International TechneGroup Incorporated (ITI) and South Carolina Research Authority (SCRA) based on AP 210 release 0.65.

   b. A demonstration for the Design Automation Conference (DAC) in June 1994 was performed using surface mount and through hole technologies, ten-layer board with dual side component mounting, and a PCA design used by the U.S. Navy.

2. Demo 2 -- Bare printed circuit board fabrication. This demonstration will show that AP 210 provides sufficient data structures for exchanging necessary information for the fabrication of a printed circuit board, given that the design and layout of the various circuit paths and components have been identified and approved.

The demonstration was provided at DAC 1994 at which conference printed circuit boards fabricated from AP 210 data were provided to attendees.

3. Demo 3 -- In-circuit test. This demonstration will show that AP 210 provides sufficient data structures for exchanging necessary information for continuity testing of a printed circuit board, given that the design and layout of the various circuit paths and components have been identified and approved. This test will verify that conducting paths and areas meet electrical requirements of the design.[2]

4. Demo 4 -- Functional test. This demonstration will show that AP 210 provides sufficient data structures for exchanging necessary information for verifying that the completed printed circuit assembly performs according to original design specifications and requirements.

This effort is currently on hold because of other higher priority items.

7.2 Data Exchange between AP 210 and AP 220

In August 1994 there was an AP 220 demonstration presented to PreAmp's Industry Review Board. It demonstrated how concurrent engineering will be enabled by data sharing through a common design and manufacturing engineering user interface. The prototype translator was developed to translate Mentor Graphics PCA design data to an AP 210 physical file and then passed it to the RAMP software for process planning. The future realistic objective is to enable a full set of design data to be passed from AP 210 to AP 220 for PCA manufacturing and process planning. A fully functional interface provides a viable validation of AP 210 capability.

7.3 Joint Demonstration by CFI/PIEE/PreAmp/RAMP

In the second quarter of 1993 a joint demonstration project was agreed on by CAD Framework Initiative (CFI), PIEE, PreAmp, and RAMP. The focus of the demonstration is on netlist, timing, EE physical design, PCA manufacturing, and process planning. The demonstration was held at the Design Automation Conference (DAC) in June 1994. DAC was chosen because it is the premiere exhibition center to gain industry acceptance.

The major capabilities to be demonstrated were:
a. data archive;
b. extract physical design data;
c. bi-directional design-to-manufacturing interface;
d. flexibility to use different CAx systems.

[2] This use case is implemented in the commercially available DFXpert software (http://www.sfmtech.com).

The business objectives were to demonstrate:

a. the operational convergence of electrical standards;
b. the support of the industry-wide goal to make electrical product data more usable among the EE/CAD systems;
c. the framework to capture design process and manufacturing information over the PCA product life cycle.

7.4 1994 Vendors Participation

EE/CAD vendors and member companies are encouraged to develop translators to convert the vendor-specific ECAD data to AP 210's compliance data representation. The translators are effective AP validation tools. The 1994 activities include:

1. Mentor Graphics Corporation is funding International TechneGroup Incorporated (ITI) to develop a Mentor-AP 210 translator.
2. Racal-Redac Systems, Ltd. is supporting the National Institute of Standards and Technology (NIST, DoC, USA) to develop a Racal-Redac-AP 210 translator.
3. Digital Equipment Corporation is developing a Cadence-AP 210 translator.
4. Intergraph Corporation is developing an Intergraph-AP 210 translator.
5. Harris Corporation (owner of Scicards) is still in consideration.

7.5 1997 TIGER Program

TIGER Collaborative Engineering Scenario

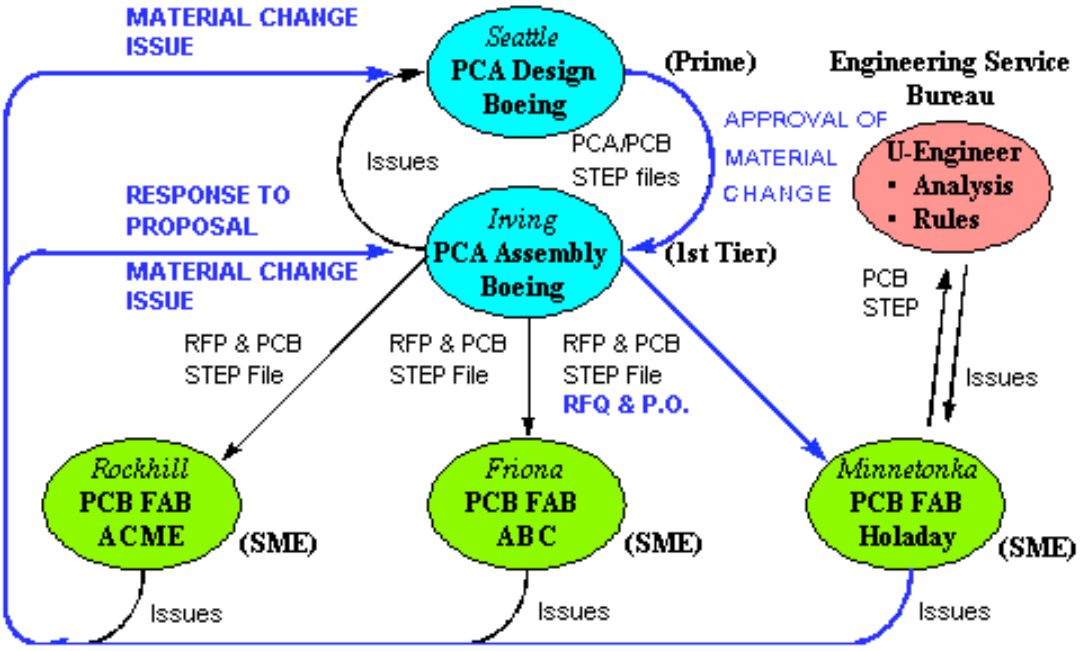


Figure 1 TIGER Collaborative Engineering Scenario

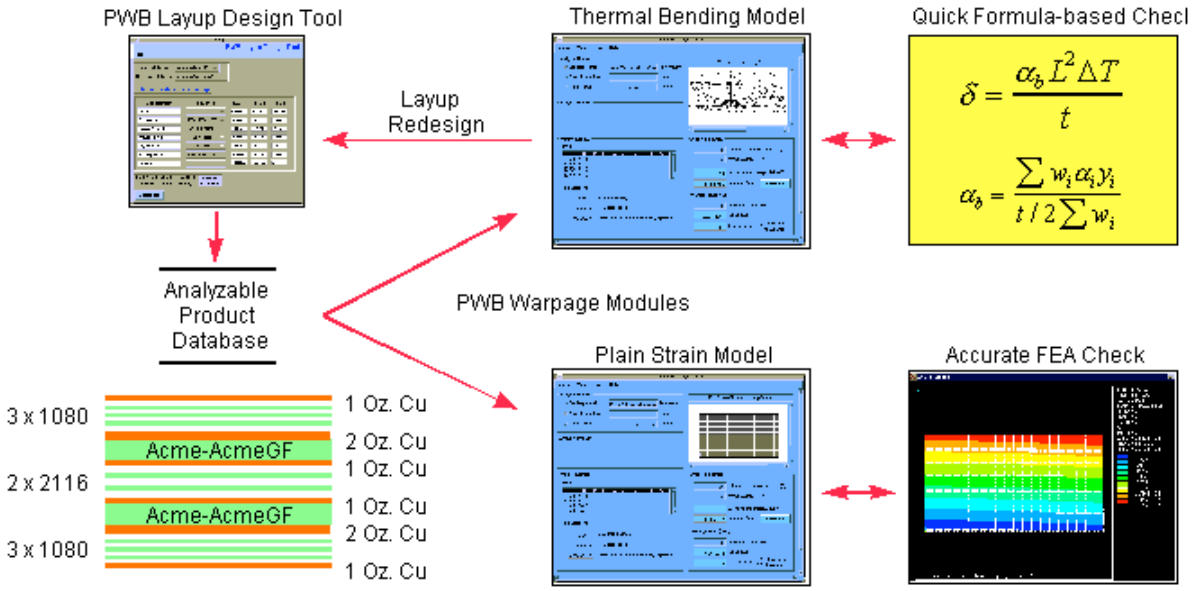


Figure 2 PWB Warpage Modules for Iterative, Multi-Fidelity Design Analysis

Roles

Prime: The Boeing Company This demonstration Prime IntrAnet is hosted at Georgia Tech and includes links to representative suppliers/SMEs like Holaday Circuits.

Small-Medium Enterprise (SME): Holaday Circuits, Inc. This demonstration SME web is hosted at Georgia Tech and supports secure web-based data uploads from Primes. It includes a representative SME IntrAnet with links to representative suppliers used by PWB fabricators, including suppliers of engineering services like U-Engineer.

Engineering Service Bureau (ESB): U-Engineer This demonstration ESB offers highly-automtated, self-service PWA/B analyses driven by STEP product data-driven capabilities built upon Descriptions of analysis modules and instructions for starting TIGER Tools are included. This ESB is a tangible illustration of the above ESB paradigm and DAI techniques.

Premier Demo Highlights from the highly successful demo held Feb. 21, 1997 in Charleston SC

For more details, please visit - http://eislab.gatech.edu/tiger

7.6 1999 ProAm project

One key to obtaining quality parts from Small and Medium-Sized Enterprises (SMEs) is their ability to analyze the physical behavior of parts and manufacturing processes. Through techniques such as

finite element analysis, SMEs can greatly impact products by optimizing their performance, judging design alternatives, and improving manufacturing yields. However, industry often does not benefit from such analysis due to the lack of easy-to-use product-specific capabilities. This situation is exacerbated in SMEs where limited resources typically preclude having in-house analysis tools and staff. Yet SMEs need analysis capabilities as they are often the ones with the precise product and process knowledge required to realize improvements.

The U. S. Department of Defense Joint Electronic Commerce Program Office (JECPO) has sponsored the ProAM effort with the Army Aviation and Missile Command (AMCOM) as primary stakeholder. Under subcontract to Concurrent Technologies Corp. through the Atlanta Electronic Commerce Resource Center (AECRC), ProAM has focused on improving missile electronics through advanced engineering analysis integration and delivery. This Georgia Tech-led effort has addressed barriers to small & medium-sized enterprise (SME) analysis of product physical behavior with the involvement of Circuit Express Inc. and System Studies and Simulation Inc., two SMEs in the AMCOM supply chain (Figure 1).

Tools and technologies resulting from the ProAM project include:

U-Engineer , a self/full-serve Internet-based engineering service bureau (ESB) with highly automated analysis modules for printed wiring board (PWB) fabricators and designers (Figure 2). Some modules, including PWB impedance models and the IPC-D-279 plated-through hole fatigue model, are available for usage via web-based thin clients (Figure 3). Accessing U-Engineer-based solvers as a thick client, *XaiTools PWA-B* provides other tools for PWB layup design and warpage analysis (Figure 4 and Figure 5).

General ESB and analysis integration techniques underlying U-Engineer, including:

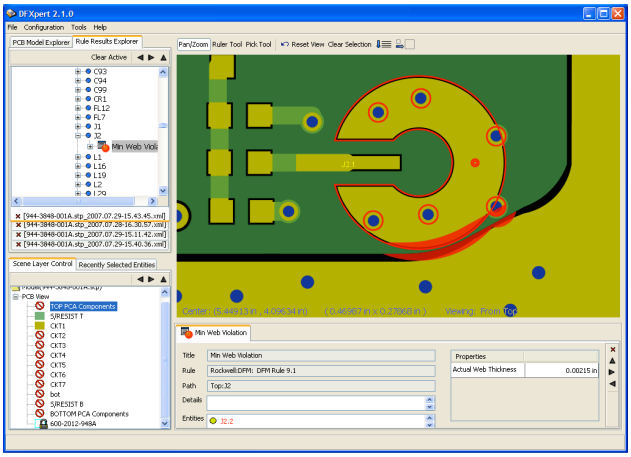
A prototype template to aid establishing other Internet-based ESBs via technologies such as thick and thin client tools, CORBA-wrapped analysis solvers, and Internet security (Figure 6).

Product data-driven analysis techniques to enable highly automated plug-and-play usage via emerging product standards like ISO STEP AP210 and IPC GenCAM/GenX. *XaiTools*, the general-purpose analysis integration toolkit underlying *XaiTools PWA-B*, is highlighted with its integration to commercial CAD/CAE tools and applications to other product domains (Figure 7 and Figure 8).

U-Engineer utilization by SMEs and Primes is highlighted (Figure 3), including solving production problems, evaluating design/process alternatives, and increasing awareness of potential issues. Experience has shown that ProAM technology excels at delivering automated product-specific analysis to places it has never gone before.

While ProAM has focused on tools for the AMCOM PWB supply chain, these same tools and techniques can benefit other industries. Envisioned applications include development of analysis module catalogs for other domains and establishment of company-specific Internet/Intranet-based engineering service bureaus.

7.7 2000-2009 DFXpert : SFM Technology, Inc. (http://www.sfmtech.com)



DFXpert is an integrated environment for multi-disciplinary design-for-X analysis and feedback in the domain of PCB fabrication and assembly. DFXpert embeds domain-specific expertise in the areas of PCB fabrication, automated assembly, and testability, and provides a wide-variety of stakeholders in the product realization process with critical feedback to enables continuous improvements in Producibility, quality, cost, and robustness. DFXpert is the first commercially available DFx tool to be compliant with the AP 210 standard for product data representation. The comprehensive AP 210 data model supports unprecedented fidelity and integration between footprint, board, component, and assembly level product representations, as well as opportunities for interoperability with mechanical data because the 2nd edition of AP 210 is fully harmonized with IS AP 203 2nd edition. DFXpert has been updated to and validated against the IS of AP 210 2nd edition.

DFXpert embeds domain-specific expertise that has been developed and validated through a near decade-long research collaboration between University of Illinois at Urbana-Champaign and Rockwell Collins, a leading provider of communication and aviation electronic solutions to the aerospace and defense industries. The embedded rule-sets have been vetted with domain experts and validated on hundreds of advanced production designs. The DFXpert model and result browsers offer direct visualization of reports, warnings, and violations for rapid review by process stakeholders, incorporated within a full-featured user interface that supports manual PCA/PCB review, rule configuration and execution, and browsing.

During the development of the 2nd edition Of AP 210, DFXpert was used extensively to debug and understand exchange issues arising from model problems or mis-understandings, accelerating the acceptance of the 2nd edition of AP 210.

AP 210 Conformance: Implements the following product definitions:

- Assembly_module_design_view,
- Assembly_module_usage_view,
- Footprint definition,
- Layered_interconnect_module_design_view,

- Layered_interconnect_module_usage_view,
- Layered_interconnect_panel_design_view,
- Package,
- Packaged_part.

7.8 2005 Vendors Participation

Translators have been created for:

- Zuken Visula™,
- Mentor Board Station™,
- Theorem AP 210-> AP 203,
- Theorem AP 203->AP 210,
- IDF->AP 210,
- Mentor PADS™,
- Orcad™,
- Eagle™,
- CircuitCam™,
- VHDL->AP 210,
- AP 210->VHDL.

The following native interfaces were implemented:

- UIUC Board Viewer (IS ed 1 version),
- PDES Inc. Board Viewer (DIS ed 1 version),
- UIUC Design Rule engine (IS ed 1 version prototype),
- Boeing Design Rule engine (DIS ed 1 version),
- InterCAX warpage analysis engine (DIS ed2, IS ed2),
- LKSoft board stackup tool (DIS ed2, IS ed2),
- Boeing Durability analysis system (DIS ed1).

7.9 2007-2009 Prometheus Computing, LLC

Translator: Bidirectional AP210 to IPC 2581 Offspring
AP 210 Conformance: Implements the following product definitions:

- Assembly_module_design_view
- Assembly_module_usage_view
- Component_termination_passage_template
- Default_attachment_size_based_land_physical_template
- Design_stack_model

- Electrical_network_definition
- Footprint_definition
- Interconnect_module_design_view
- Interconnect_module_usage_view
- Package
- Packaged_part
- Trace_template
- Unsupported_passage_template

Currently it uses a developmental AP 210 schema. After edition 2 is released it will be updated to use the edition 2 schema.
Description:
This is a proof of concept translator that uses a Rule engine to perform the translation. Large data sets would have very long run times.

It currently translates:

- Assembly: assembly to component relationships
- AVL: parts and suppliers
- Gerber: traces, lands
- History: engineering change notices
- LandPattern: footprint, but only for surface mount parts
- Logistics: people and organizations
- Netlist: logical connections between component pins
- Stackup: stratum and their order

List of AIM entities used by the AP 210 to Offspring translator.

Assembly

```
(LENGTH_MEASURE_WITH_UNIT & MEASURE_REPRESENTATION_ITEM &
MEASURE_WITH_UNIT & REPRESENTATION_ITEM)
(LENGTH_UNIT & NAMED_UNIT & SI_UNIT)
APPLICATION_CONTEXT
APPLICATION_PROTOCOL_DEFINITION
DIMENSIONAL_CHARACTERISTIC_REPRESENTATION
DIMENSIONAL_SIZE
MATERIAL_DESIGNATION
PRODUCT
PRODUCT_CONTEXT
PRODUCT_DEFINITION
PRODUCT_DEFINITION_CONTEXT
PRODUCT_DEFINITION_FORMATION
PRODUCT_DEFINITION_SHAPE
REPRESENTATION_CONTEXT
```

```
SHAPE_ASPECT
SHAPE_DIMENSION_REPRESENTATION
```

AVL

```
ALTERNATE_PRODUCT_RELATIONSHIP
APPLICATION_CONTEXT
APPLIED_ORGANIZATION_ASSIGNMENT
ORGANIZATION
ORGANIZATIONAL_ADDRESS
ORGANIZATION_ROLE
PRODUCT
PRODUCT_CONTEXT
PRODUCT_RELATED_PRODUCT_CATEGORY
```

Gerber

```
(GEOMETRIC_REPRESENTATION_CONTEXT & GLOBAL_UNCERTAINTY_ASSIGNED_CONTEXT &
GLOBAL_UNIT_ASSIGNED_CONTEXT & REPRESENTATION_CONTEXT)
(LENGTH_MEASURE_WITH_UNIT & MEASURE_REPRESENTATION_ITEM &
MEASURE_WITH_UNIT & REPRESENTATION_ITEM)
(LENGTH_UNIT & NAMED_UNIT & SI_UNIT)
(NAMED_UNIT & PLANE_ANGLE_UNIT & SI_UNIT)
APPLICATION_CONTEXT
ASSEMBLY_COMPONENT_USAGE
CARTESIAN_POINT
COMPOSITE_CURVE
COMPOSITE_CURVE_SEGMENT
CONDUCTIVE_INTERCONNECT_ELEMENT_WITH_PRE_DEFINED_TRANSITIONS
CSG_PRIMITIVE_SOLID_2D
CURVE_STYLE_PARAMETERS_WITH_ENDS
DESCRIPTIVE_REPRESENTATION_ITEM
DESIGN_LAYER_STRATUM
INTERCONNECT_MODULE_DESIGN_VIEW
INTERCONNECT_MODULE_USAGE_VIEW
JOIN_SHAPE_ASPECT
LAMINATE_COMPONENT_FEATURE
LAMINATE_COMPONENT_JOIN_TERMINAL
LAND
LAND_PHYSICAL_TEMPLATE
LAYER_CONNECTION_POINT
NEXT_ASSEMBLY_USAGE_OCCURRENCE_RELATIONSHIP
PATH_AREA_WITH_PARAMETERS
PHYSICAL_NETWORK
PLANAR_PATH_SHAPE_REPRESENTATION_WITH_PARAMETERS
POLYLINE
PRODUCT
PRODUCT_CONTEXT
```

PRODUCT_DEFINITION_CONTEXT
PRODUCT_DEFINITION_FORMATION
PRODUCT_DEFINITION_USAGE
PROPERTY_DEFINITION_REPRESENTATION
REPRESENTATION_CONTEXT
REPRESENTATION_MAP
SHAPE_ASPECT
SHAPE_ASPECT_RELATIONSHIP
SHAPE_DEFINITION_REPRESENTATION
STRATUM_FEATURE
TRACE_TEMPLATE
UNCERTAINTY_MEASURE_WITH_UNIT

History

ACTION_METHOD
APPLICATION_CONTEXT
APPLICATION_PROTOCOL_DEFINITION
APPLIED_APPROVAL_ASSIGNMENT
APPROVAL
APPROVAL_DATE_TIME
APPROVAL_PERSON_ORGANIZATION
APPROVAL_ROLE
APPROVAL_STATUS
CALENDAR_DATE
DESIGN_OBJECT_MANAGEMENT_RELATIONSHIP_ACTION
PERSON

LandPattern

(GEOMETRIC_REPRESENTATION_CONTEXT & GLOBAL_UNCERTAINTY_ASSIGNED_CONTEXT &
GLOBAL_UNIT_ASSIGNED_CONTEXT & REPRESENTATION_CONTEXT)
(LENGTH_UNIT & NAMED_UNIT & SI_UNIT)
(NAMED_UNIT & PLANE_ANGLE_UNIT & SI_UNIT)
APPLICATION_CONTEXT
AXIS2_PLACEMENT_2D
CARTESIAN_POINT
CONTACT_SIZE_DEPENDENT_LAND
DEFAULT_ATTACHMENT_SIZE_BASED_LAND_PHYSICAL_TEMPLATE
FOOTPRINT_DEFINITION
ID_ATTRIBUTE
INTERCONNECT_MODULE_DESIGN_VIEW
INTERCONNECT_MODULE_USAGE_VIEW
INTERCONNECT_MODULE_INTERFACE_TERMINAL
LAMINATE_COMPONENT_INTERFACE_TERMINAL
NAME_ATTRIBUTE
PACKAGE
PRODUCT

PRODUCT_CONTEXT
PRODUCT_DEFINITION_CONTEXT
PRODUCT_DEFINITION_FORMATION
PRODUCT_DEFINITION_RELATIONSHIP
PROPERTY_DEFINITION_RELATIONSHIP
REPRESENTATION_MAP
SHAPE_ASPECT_RELATIONSHIP
SHAPE_DEFINITION_REPRESENTATION
SHAPE_REPRESENTATION
SINGLE_AREA_CSG_2D_SHAPE_REPRESENTATION
STRUCTURED_LAYOUT_COMPONENT_SUB_ASSEMBLY_RELATIONSHIP
UNCERTAINTY_MEASURE_WITH_UNIT
USAGE_CONCEPT_USAGE_RELATIONSHIP

Logistics

APPLICATION_CONTEXT
APPLICATION_PROTOCOL_DEFINITION
ORGANIZATION
PERSON
PERSONAL_ADDRESS
PERSON_AND_ORGANIZATION
PERSON_AND_ORGANIZATION_ADDRESS

Netlist

APPLICATION_CONTEXT
ASSEMBLY_MODULE_DESIGN_VIEW
ASSEMBLY_MODULE_USAGE_VIEW
PACKAGED_COMPONENT
PACKAGED_PART
PHYSICAL_COMPONENT_TERMINAL
PHYSICAL_CONNECTIVITY_DEFINITION
PRODUCT
PRODUCT_CONTEXT
PRODUCT_DEFINITION_CONTEXT
PRODUCT_DEFINITION_FORMATION
SHAPE_ASPECT_RELATIONSHIP

Stackup

(GEOMETRIC_REPRESENTATION_CONTEXT & GLOBAL_UNCERTAINTY_ASSIGNED_CONTEXT &
GLOBAL_UNIT_ASSIGNED_CONTEXT & REPRESENTATION_CONTEXT)
(LENGTH_MEASURE_WITH_UNIT & MEASURE_REPRESENTATION_ITEM &
MEASURE_WITH_UNIT & REPRESENTATION_ITEM)
(LENGTH_UNIT & NAMED_UNIT & SI_UNIT)
APPLICATION_CONTEXT
DESCRIPTION_ATTRIBUTE
MATERIAL_DESIGNATION_WITH_CONDUCTIVITY_CLASSIFICATION

```
PRODUCT
PRODUCT_CONTEXT
PRODUCT_DEFINITION_CONTEXT
PRODUCT_DEFINITION_FORMATION
PROPERTY_DEFINITION
PROPERTY_DEFINITION_RELATIONSHIP
PROPERTY_DEFINITION_REPRESENTATION
REPRESENTATION
SHAPE_ASPECT_RELATIONSHIP
STRATUM
STRATUM_SURFACE
STRATUM_TECHNOLOGY
STRATUM_TECHNOLOGY_OCCURRENCE
UNCERTAINTY_MEASURE_WITH_UNIT
```

7.10 2000-2009 LKSoft CADIF -> AP 210 converters

Translator: CADIF to AP 210
AP 210 Conformance: Implements the following product definitions:

default_attachment_size_based_land_physical_template

default_plated_passage_based_land_physical_template

design_stack_model

document

electrical_isolation_removal_template

fill_area_template

footprint_definition+stratum_stack_dependent_template

functional_unit

inter_stratum_feature_template

layered_assembly_module_design_view+physical_unit_network_definition

layered_assembly_module_usage_view

layered_interconnect_module_design_view

layered_interconnect_module_usage_view

library_stack_model

material_removal_feature_template

multi_stratum_special_symbol_template+stratum_stack_dependent_template

package

packaged_connector

packaged_part

padstack_definition

part_connected_terminals_definition

part_feature_template_definition

part_string_template

part_text_template

passage_padstack_definition

physical_unit

predefined_requirement_view_definition

product_definition

snowball_template

stratum_feature_template

thermal_isolation_removal_template

trace_template

unsupported_passage_template

via_template

List of AIM entities used by the CADIF -> AP 210 translator

Entity name	Module schema name(_MIM) or Integrated Resource schema name(_SCHEMA)
additive_laminate_text_component	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM
application_context	APPLICATION_CONTEXT_SCHEMA
applied_classification_assignment	CLASSIFICATION_ASSIGNMENT_MIM
applied_document_reference	DOCUMENT_ASSIGNMENT_MIM
applied_identification_assignment	IDENTIFICATION_ASSIGNMENT_MIM
area_component	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM
area_component+ stratum_feature_template_component_with_stratum_feature	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM
area_with_outer_boundary	CONSTRUCTIVE_SOLID_GEOMETRY_2D_MIM
area_with_outer_boundary+primitive_2d_with_inner_boundary	CONSTRUCTIVE_SOLID_GEOMETRY_2D_MIM
assembly_component_usage	PRODUCT_STRUCTURE_SCHEMA
assembly_item_number	PHYSICAL_UNIT_DESIGN_VIEW_MIM
assembly_joint	ASSEMBLY_TECHNOLOGY_MIM
assembly_module_interface_terminal	ASSEMBLY_MODULE_USAGE_VIEW_MIM
assigned_requirement	REQUIREMENT_ASSIGNMENT_MIM
axis2_placement_2d	GEOMETRY_SCHEMA
boolean_result_2d	CONSTRUCTIVE_SOLID_GEOMETRY_2D_MIM
cartesian_point	GEOMETRY_SCHEMA
cartesian_transformation_operator_2d	GEOMETRY_SCHEMA
character_glyph_font_usage	PRESENTATION_RESOURCE_SCHEMA
character_glyph_symbol+solid_character_glyph_2d_symbol	MIXED_COMPLEX_TYPES
characterized_object	PRODUCT_PROPERTY_DEFINITION_SCHEMA
circle	GEOMETRY_SCHEMA
circular_area	GEOMETRIC_MODEL_SCHEMA
circular_area+primitive_2d_with_inner_boundary	MIXED_COMPLEX_TYPES
class	CLASSIFICATION_SCHEMA
classification_role	MANAGEMENT_RESOURCES_SCHEMA
closed_curve_style_parameters	CONSTRUCTIVE_SOLID_GEOMETRY_2D_MIM
component_2d_location	PHYSICAL_UNIT_2D_DESIGN_VIEW_MIM
component_termination_passage	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM
component_termination_passage_template	LAYERED_INTERCONNECT_SIMPLE_TEMPLATE_MIM
composite_curve	GEOMETRY_SCHEMA
composite_curve_segment	GEOMETRY_SCHEMA
conductive_interconnect_element_terminal_link	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM
conductive_interconnect_element_with_pre_defined_transitions	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM
connected_area_component	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM
contact_size_dependent_land+land_with_join_terminal	LAND_MIM

context_dependent_unit	MEASURE_SCHEMA
conversion_based_unit+length_unit	MEASURE_SCHEMA
conversion_based_unit+plane_angle_unit	MEASURE_SCHEMA
csg_primitive_solid_2d	CONSTRUCTIVE_SOLID_GEOMETRY_2D_MIM
csg_solid_2d	CONSTRUCTIVE_SOLID_GEOMETRY_2D_MIM
curve_style_parameters_with_ends	CONSTRUCTIVE_SOLID_GEOMETRY_2D_MIM
default_attachment_size_based_land_physical_template	LAYERED_INTERCONNECT_SIMPLE_TEMPLATE_MIM
default_plated_passage_based_land_physical_template	LAYERED_INTERCONNECT_SIMPLE_TEMPLATE_MIM
dependent_electrical_isolation_removal_component	LAND_MIM
dependent_thermal_isolation_removal_component	LAND_MIM
description_attribute	BASIC_ATTRIBUTE_SCHEMA
descriptive_representation_item	QUALIFIED_MEASURE_SCHEMA
design_layer_stratum	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM
design_stack_model	FABRICATION_TECHNOLOGY_MIM
dimensional_exponents	MEASURE_SCHEMA
direction	GEOMETRY_SCHEMA
document	DOCUMENT_SCHEMA
document_product_equivalence	DOCUMENT_ASSIGNMENT_MIM
document_type	DOCUMENT_SCHEMA
documentation_layer_stratum	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM
electrical_isolation_removal_template	LAYERED_INTERCONNECT_SIMPLE_TEMPLATE_MIM
fabrication_joint	FABRICATION_JOINT_MIM
fiducial+stratum_feature_template_component	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM
fiducial_part_feature	PART_FEATURE_FUNCTION_MIM
fiducial_stratum_feature	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM
fill_area_template	LAYERED_INTERCONNECT_SIMPLE_TEMPLATE_MIM
footprint_definition+stratum_stack_dependent_template	MIXED_COMPLEX_TYPES
footprint_occurrence	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM
functional_unit	FUNCTIONAL_USAGE_VIEW_MIM
geometric_curve_set	GEOMETRIC_MODEL_SCHEMA
geometric_representation_context	GEOMETRY_SCHEMA
geometric_representation_context+global_uncertainty_assigned_context+global_unit_assigned_context	MIXED_COMPLEX_TYPES
geometrically_bounded_2d_wireframe_representation	AIC_GEOMETRICALLY_BOUNDED_2D_WIREFRAME
global_uncertainty_assigned_context+parametric_representation_context	REPRESENTATION_SCHEMA
id_attribute	BASIC_ATTRIBUTE_SCHEMA
identification_role	MANAGEMENT_RESOURCES_SCHEMA
inter_stratum_feature_template	LAYERED_INTERCONNECT_SIMPLE_TEMPLATE_MIM
interconnect_module_component	ASSEMBLY_MODULE_WITH_INTERCONNECT_COMPONENT_MIM
interconnect_module_component_surface_feature	ASSEMBLY_MODULE_WITH_INTERCONNECT_COMPONENT_MIM
interconnect_module_edge	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM

interconnect_module_interface_terminal	INTERCONNECT_MODULE_USAGE_VIEW_MIM
interconnect_module_terminal+test_point_part_feature	MIXED_COMPLEX_TYPES
interfacial_connection	VIA_COMPONENT_MIM
internal_probe_access_area+land_with_join_terminal+plated_passage_dependent_land	MIXED_COMPLEX_TYPES
item_defined_transformation	REPRESENTATION_SCHEMA
join_shape_aspect	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM
keepout_design_object_category	SHAPE_PARAMETERS_MIM
laminate_component_feature	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM
laminate_component_interface_terminal	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM
laminate_component_join_terminal	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM
laminate_text_string_component	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM
land_template_terminal	LAYERED_INTERCONNECT_SIMPLE_TEMPLATE_MIM
land_with_join_terminal+plated_passage_dependent_land	LAND_MIM
layer_connection_point	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM
layered_assembly_module_design_view+physical_unit_network_definition	MIXED_COMPLEX_TYPES
layered_assembly_module_usage_view	ASSEMBLY_MODULE_USAGE_VIEW_MIM
layered_interconnect_module_design_view	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM
layered_interconnect_module_usage_view	INTERCONNECT_MODULE_USAGE_VIEW_MIM
layout_spacing_requirement	INTERCONNECT_PLACEMENT_REQUIREMENTS_MIM
length_measure_with_unit	MEASURE_SCHEMA
length_measure_with_unit+measure_representation_item	MIXED_COMPLEX_TYPES
length_measure_with_unit+measure_representation_item+qualified_representation_item	MIXED_COMPLEX_TYPES
length_measure_with_unit+uncertainty_measure_with_unit	MIXED_COMPLEX_TYPES
length_unit+si_unit	MEASURE_SCHEMA
library_stack_model	LAYERED_INTERCONNECT_COMPLEX_TEMPLATE_MIM
library_to_design_stack_model_mapping	LAYERED_INTERCONNECT_COMPLEX_TEMPLATE_MIM
mapped_item	REPRESENTATION_SCHEMA
material_designation_with_conductivity_classification	CONDUCTIVITY_MATERIAL_ASPECTS_MIM
material_designation_with_conductivity_classification+passage_deposition_material_identification	MIXED_COMPLEX_TYPES
material_removal_feature_template	LAYERED_INTERCONNECT_SIMPLE_TEMPLATE_MIM
material_removal_laminate_component	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM
measure_representation_item	QUALIFIED_MEASURE_SCHEMA
multi_stratum_special_symbol_component	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM
multi_stratum_special_symbol_template+stratum_stack_dependent_template	LAYERED_INTERCONNECT_COMPLEX_TEMPLATE_MIM
name_attribute	BASIC_ATTRIBUTE_SCHEMA

next_assembly_usage_occurrence_relationship	PHYSICAL_UNIT_DESIGN_VIEW_MIM
object_role	BASIC_ATTRIBUTE_SCHEMA
package	PACKAGE_MIM
package_terminal	PACKAGE_MIM
package_terminal_template_definition	PACKAGE_MIM
packaged_component	ASSEMBLY_MODULE_DESIGN_MIM
packaged_connector	PACKAGED_CONNECTOR_MODEL_MIM
packaged_connector_component	ASSEMBLY_MODULE_WITH_PACKAGED_CONNECTOR_COMPONENT_MI
packaged_connector_terminal_relationship	PACKAGED_CONNECTOR_MODEL_MIM
packaged_part	PACKAGED_PART_BLACK_BOX_MODEL_MIM
packaged_part_terminal	PACKAGED_PART_BLACK_BOX_MODEL_MIM
padstack_definition	LAYERED_INTERCONNECT_COMPLEX_TEMPLATE_MIM
padstack_occurrence	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM
part_connected_terminals_definition	FUNCTIONAL_ASSIGNMENT_TO_PART_MIM
part_feature_template_definition	PHYSICAL_UNIT_USAGE_VIEW_MIM
part_string_template	LAYERED_INTERCONNECT_SIMPLE_TEMPLATE_MIM
part_template_keepout_shape_allocation_to_stratum_stack	LAYERED_INTERCONNECT_COMPLEX_TEMPLATE_MIM
part_text_template	LAYERED_INTERCONNECT_SIMPLE_TEMPLATE_MIM
part_tooling_feature	PART_FEATURE_FUNCTION_MIM
passage_padstack_definition	LAYERED_INTERCONNECT_COMPLEX_TEMPLATE_MIM
passage_technology	FABRICATION_TECHNOLOGY_MIM
passage_technology_allocation_to_stack_model	FABRICATION_TECHNOLOGY_MIM
path_area_with_parameters	CONSTRUCTIVE_SOLID_GEOMETRY_2D_MIM
physical_component	PHYSICAL_UNIT_DESIGN_VIEW_MIM
physical_component_feature	PHYSICAL_COMPONENT_FEATURE_MIM
physical_component_interface_terminal	INTERFACE_COMPONENT_MIM
physical_component_terminal	PHYSICAL_COMPONENT_FEATURE_MIM
physical_connectivity_definition	PHYSICAL_CONNECTIVITY_DEFINITION_MIM
physical_network	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM
physical_unit	PHYSICAL_UNIT_USAGE_VIEW_MIM
physical_unit_keepout_shape_allocation_to_stratum_stack	LAYERED_INTERCONNECT_COMPLEX_TEMPLATE_MIM
placed_feature	SHAPE_FEATURE_MIM
planar_box	PRESENTATION_RESOURCE_SCHEMA
planar_extent	PRESENTATION_RESOURCE_SCHEMA
plane_angle_measure_with_unit	MEASURE_SCHEMA
plane_angle_unit+si_unit	MEASURE_SCHEMA
polygonal_area	GEOMETRIC_MODEL_SCHEMA
polygonal_area+primitive_2d_with_inner_boundary	MIXED_COMPLEX_TYPES
polyline	GEOMETRY_SCHEMA
predefined_requirement_view_definition	REQUIREMENT_DECOMPOSITION_MIM
primitive_2d_with_inner_boundary+rectangular_area	MIXED_COMPLEX_TYPES
product	PRODUCT_DEFINITION_SCHEMA
product_context	APPLICATION_CONTEXT_SCHEMA

product_definition	PRODUCT_DEFINITION_SCHEMA
product_definition_context	APPLICATION_CONTEXT_SCHEMA
product_definition_context_association	PRODUCT_DEFINITION_SCHEMA
product_definition_context_role	PRODUCT_DEFINITION_SCHEMA
product_definition_formation	PRODUCT_DEFINITION_SCHEMA
product_definition_relationship	PRODUCT_DEFINITION_SCHEMA
product_definition_shape	PRODUCT_PROPERTY_DEFINITION_SCHEMA
product_definition_usage	PRODUCT_STRUCTURE_SCHEMA
product_related_product_category	PRODUCT_DEFINITION_SCHEMA
property_definition	PRODUCT_PROPERTY_DEFINITION_SCHEMA
property_definition_relationship	MATERIAL_PROPERTY_DEFINITION_SCHEMA
property_definition_representation	PRODUCT_PROPERTY_REPRESENTATION_SCHEMA
rectangular_area	GEOMETRIC_MODEL_SCHEMA
representation	REPRESENTATION_SCHEMA
representation_context	REPRESENTATION_SCHEMA
representation_item	REPRESENTATION_SCHEMA
representation_map	REPRESENTATION_SCHEMA
representation_relationship	REPRESENTATION_SCHEMA
representation_relationship_with_transformation+shape_representation_relationship	MIXED_COMPLEX_TYPES
requirement_assigned_object	REQUIREMENT_ASSIGNMENT_MIM
requirement_assignment	REQUIREMENT_ASSIGNMENT_MIM
requirement_view_definition_relationship	REQUIREMENT_VIEW_DEFINITION_RELATIONSHIP_MIM
role_association	BASIC_ATTRIBUTE_SCHEMA
seating_plane	NON_FEATURE_SHAPE_ELEMENT_MIM
shape_aspect	PRODUCT_PROPERTY_DEFINITION_SCHEMA
shape_aspect_relationship	PRODUCT_PROPERTY_DEFINITION_SCHEMA
shape_definition_representation	PRODUCT_PROPERTY_REPRESENTATION_SCHEMA
shape_representation	PRODUCT_PROPERTY_REPRESENTATION_SCHEMA
single_area_csg_2d_shape_representation	CONSTRUCTIVE_SOLID_GEOMETRY_2D_MIM
single_boundary_csg_2d_shape_representation	CONSTRUCTIVE_SOLID_GEOMETRY_2D_MIM
single_stratum_special_symbol_component	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM
single_stratum_special_symbol_template	LAYERED_INTERCONNECT_COMPLEX_TEMPLATE_MIM
snowball_template	LAYERED_INTERCONNECT_SIMPLE_TEMPLATE_MIM
stratum	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM
stratum_feature	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM
stratum_feature_template	LAYERED_INTERCONNECT_SIMPLE_TEMPLATE_MIM
stratum_feature_template_component	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM
stratum_feature_template_component_with_stratum_feature	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM
stratum_specific_template_location	LAYERED_INTERCONNECT_COMPLEX_TEMPLATE_MIM
stratum_technology	FABRICATION_TECHNOLOGY_MIM
stratum_technology_occurrence	FABRICATION_TECHNOLOGY_MIM
stratum_technology_occurrence_link	FABRICATION_TECHNOLOGY_MIM
stratum_technology_occurrence_swap_relationship	FABRICATION_TECHNOLOGY_MIM

structured_layout_component_sub_assembly_relationship	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM
text_font	PRESENTATION_RESOURCE_SCHEMA
text_literal_with_extent	PRESENTATION_DEFINITION_SCHEMA
thermal_isolation_removal_template	LAYERED_INTERCONNECT_COMPLEX_TEMPLATE_MIM
trace_template	LAYERED_INTERCONNECT_SIMPLE_TEMPLATE_MIM
trimmed_curve	GEOMETRY_SCHEMA
type_qualifier	QUALIFIED_MEASURE_SCHEMA
uncertainty_measure_with_unit	REPRESENTATION_SCHEMA
unsupported_passage	LAYERED_INTERCONNECT_MODULE_DESIGN_MIM
unsupported_passage_template	LAYERED_INTERCONNECT_SIMPLE_TEMPLATE_MIM
usage_concept_usage_relationship	PART_FEATURE_LOCATION_MIM
via_template	LAYERED_INTERCONNECT_SIMPLE_TEMPLATE_MIM

7.11 2009 Vendors Production Participation

This is a partial listing of production implementations of the second edition of the standard. Translator status is available at PDES Inc., http://pdesinc.aticorp.org

The following native interfaces are available for the second edition of AP 210:

LKSoft ecad converters;
SFM Technology DFXPert DFx analysis software;
InterCAX PCA/PCB Warpage simulation system;
LKSoft IDA-STEP Electronics;
LKSoft PCB stackup editor;
LKSoft IDA-STEP Center PDM system.

APPENDIX A

ARM-TO-AAM MAPPING TABLE

The mapping table is available at http://www.tc184-sc4.org in the file:
ISO TC184/SC4/WG3 N1892.

APPENDIX B

TEST CASES & DATA POPULATION PHYSICAL FILES

These test cases are obsolete since modular APs do not have UoFs but are retained for historical purposes. See http://www.wikistep.org for current publicly available examples.

B.1 Test Cases

1. **Test Case: Allocation UoF**
   a. Populate the model entities which describe the association between "functional" gate and a real part that encapsulates that function. The specific example will be performed on a NAND gate to a SN74xx00 family member.
   b. Populate the model entities which describe the association between a real part and the "functional" gates which are encapsulated by the real part. The specific example will be performed on a SN74xx00 family member and a NAND gate.

2. **Test Case: CMDM UoF**
   a. Populate the model entities required to track an "Engineering Change" to a released product. The specific example will be performed on the FLASHER design. The reason for change is attributed to a customer complaint, the flash rate of the LEDs is to fast. The change effects the values of R2, C1 and C2 but, not the package styles.
   b. Populate the model entities for the above case but, allowing both versions to exist a separate products, have as a released product a fast rate flasher and a slow rate flasher.

3. **Test Case: Functional UoF**
   a. Populate the model entities which show how a Programmable Array Logic device (PAL) can be decomposed into constituent logical units, discrete gate types, (NAND, NOR, XOR, etc) to implement a specific function.

4. **Test Case: Geometry UoF**
   a. Populate the model entities which will describe the physical shape of a conductor as it would appear on a PCB.
   b. Populate the model entities which will describe the physical shape of an eight lead flat pack's layout pattern as it would appear on a PCB.

5. **Test Case: Part UoF**
   a. Populate the model entities which shows how a ferrite bead can be associated to a specific resistor of a given PCA design.
   b. Populate the model entities which will describe the different possible mounting styles of a specific axial component. The specific example will be performed on a resistor showing different mountings like horizontal, vertical, surface.
   c. Populate the model entities which will describe how a printed capacitor would be implemented on a PCA/PCB design.
   d. Populate the model entities which shows how an IC would be mounted into a compatible socket.

6. **Test Case: PCA UoF**
   a. Populate the model entities which will describe the relationship between an IC and its socket; such that both will be positioned and may be moved together.

7. **Test Case: PCB UoF**
   a. Populate the model entities which describe the situation when a net can not be fully implemented within the confines of the PCB outline and layer structure, a incomplete route. For this occurrence a jumper/"green wire" is to be used to realize the conduction path in order to get the circuit to function as designed, complete the route of the given net.

8. **Test Case: Requirement UoF**
   a. Populate the model entities which show how a specific specification will get permeated through out the schema. The specific example will use the following specifications:
   i. MIL-P-55110 PCB specification
   ii. MIL-M-38510 IC specification
   b. Populate the model entities which will describe how a requirement to use a specification is permeated through a design. The specific example will be based upon the above case.
   c. Populate the model entities of a specific requirement which will provide information concerning part selection. The specific example will be related to the operational environment that a given design must survive.
   d. Populate the model entities necessary to specify a customer's requirement to have a design "work" within a next higher assembly. The specific example will be limited to the connector and interface_signals are previously defined from the next higher assembly's design.

9. **Test Case: Utility UoF**
   a. Populate the model entities which will show the association of a given design to a mathematical model. The specific example will show the relation of the FLASHER to an analytic_model.
   b. Populate the model entities which will show the association of a given part to a mathematical model. The specific example will show the relation between a 555 timer to an analytic_model. The model will able to be reused for other occurrences of the same part.

c.Populate the model entities which describe how a material specification causes an impact in other areas.

d.Populate the model entities which describe how a tolerance in material composition can alter a given part's characteristic.

10. **Test Case: Complete PCA**

Test population of a complete PCA.

B.2 List of Physical Files

Physical File	Purpose
allo.one	test case 1a
allo.two	test case 1b
cmdm.one	test case 2a
cmdm.two	test case 2a
flasher	test case 10
func.one	test case 3a
geom.one	test case 4a
geom.two	test case 4b
part.four	test case 5d
part.one	test case 5a
part.three	test case 5c
part.two	test case 5b
pca.one	test case 6a
rqmt.four	test case 8d
rqmt.one	test case 8a
rqmt.three	test case 8c
rqmt.two	test case 8b
util.four	test case 9d
util.one	test case 9a
util.three	test case 9c
util.two	test case 9b

B.3 Description of Physical Files

In an effort to keep the size of the files reasonable and not loaded with extraneous entities, some "short cuts" were taken. The specifics for each file are as follows:

1.Allo.one shows the association between a functional gate and it's physical equivalent. Attributes and entities which describe any geometry of the part or sections of the part were omitted. Characteristics and numeric parameters were omitted. Also any detailed information on materials were omitted.

2.Allo.two shows the association between a physical gate and it's functional equivalent. The same omissions from allo.one were also followed in this example.

3.Cmdm.one shows how an engineering change may be tracked. The detailed product entities were omitted. All the entities shown deal with the tracking of a change; not the data that was changed.

4.Cmdm.two shows how a different version of an established product can be tracked. The same omissions from cmdm.one were also followed in this example.

5.Flasher shows a finished Printed Wiring Assembly. Geometric part and Printed Circuit Board information was omitted. However, the positioning of the components on to the board, as well as, the plated through hole for the components are accurate. Just the shape of parts and conductor shapes are missing but, their position in the file are accurate.

6.Func.one shows how discrete functional gates can be used to construct another functional device. Only a limited number of characteristics and parameters were used in this example.

7.Geom.one shows how a conductor on a Printed Circuit Board can be described. It is not certain that the cartesian points, orientations, and geometric entities used will construct a shape that does look like a conductor. However, the order and manner in which they were used are accurate.

8.Geom.two shows how a land for a surface mounted part can be described. The same disclaimer from geom.one applies to this file as well.

9.Part.one shows how an association between two parts can occur. Attributes and entities which describe any geometry of the part or sections of the part were omitted. Characteristics and numeric parameters were omitted. Also any detailed information on materials were omitted.

10.Part.two shows how an axial component can be mounted in different styles. The same omissions from part.one were also followed in this example.

11.Part.three shows how a printed part can be described. The same omissions from part.one were also followed in this example.

12.Part.four shows how an Integrated Circuit can be associated with a compatible socket. The same omissions from part.one were also followed in this example.

13.Pca.one shows the same association of a socket to an Integrated Circuit but, treats them a an inseparable part. Attributes and entities which describe any geometry of the part or sections

of the part were omitted. Characteristics and numeric parameters were omitted. Also any detailed information on materials were omitted.

14. Rqmt.one shows how specifications get permeated through out a design. Specific information on the Printed Circuit Board were omitted.

15. Rqmt.two shows how a specification becomes a requirement and how it gets imposed through out a design. Geometric and certain part information were omitted.

16. Rqmt.three shows how a requirement to utilize a specification associates certain performance criteria to specific parts. Geomtric information on these parts was omitted. Limited performance information on the parts were provided.

17. Rqmt.four shows how a requirement for a product to work within a higher assembly can be described. Geometric information on the parts was omitted.

18. Util.one shows how a mathematical model can be associated to a given design. Detailed information on the product was omitted.

19. Util.two shows how a mathematical model can be associated to a given part. Limited performance information on the part was provided.

20. Util.three shows how a material specification can get associated to certain parts. Detailed information on the product was omitted.

21. Util.four shows how a tolerance in the material's composition can alter the material's characteristic. Limited material information was provided.

B.4 CONTENT OF PHYSICAL FILES

The physical file representations are available at http://www.tc184-sc4.org in the file:
ISO TC184/SC4/WG3 N1892.