Open-Q™ 820 µSOM Development Kit based on the Snapdragon™ 820 (APQ8096) Processor User Guide

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IDENTIFICATION

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Revision History

REVISION	DATE	DESCRIPTION	PAGES
1.0	Dec 5, 2016	Initial Draft	All
1.1	Jan 10, 2017	Added info on battery charging software Updated figure 16	25, 35
1.2	Feb 1, 2017	Added information on GPS antenna	33
1.3	Feb 14, 2017	Added information on WiFi/ BT certification	16

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1. INTRODUCTION

1.1 Purpose

The purpose of this user guide is to provide primary technical information on the Open-Q™ 820 µSOM Development Kit based on the Snapdragon™ 820 (APQ8096) Processor.

For more background information on this development kit, visit: www.intrinsyc.com

1.2 Scope

This document will cover the following items on the Open-Q 820 µSOM Development Kit:

- Block Diagram and Overview
- Hardware Features
- Configuration
- µSOM
- Carrier Board
- Display Board for LCD (Optional)

1.3 Intended Audience

This document is intended for users who would like to develop custom applications on the Intrinsyc Open-Q 820 µSOM Development Kit.

2. DOCUMENTS

This section lists the supplementary documents for the Open-Q 820 µSOM development kit.

2.1 Applicable Documents

REFERENCE	TITLE
A-1	Intrinsyc Purchase and Software License Agreement for the Open-Q Development Kit

2.2 Reference Documents

REFERENCE	TITLE
R-1	Hardware Document Set for the Snapdragon™ APQ8096 based Open-Q Development Kit
R-2	Open-Q 820 Schematics (µSOM, Carrier)
R-3	Open-Q 820 Dev Kit µSOM Tech Note 19
R-4	ITCNFA324 Module Certification OEM Integrator Instructions

2.3 Terms and Acronyms

Term and acronyms	Definition
AMIC	Analog Microphone
ANC	Audio Noise Cancellation
B2B	Board to Board
BLSP	Bus access manager Low Speed Peripheral (Serial interfaces like UART / SPI / I2C/ UIM)
BT LE	Bluetooth Low Energy
CSI	Camera Serial Interface
DSI	MIPI Display Serial Interface
EEPROM	Electrically Erasable Programmable Read only memory
eMMC	Embedded Multimedia Card
FCC	US Federal Communications Commission
FWVGA	Full Wide Video Graphics Array
GPS	Global Positioning system
HDMI	High Definition Media Interface
HSIC	High Speed Inter Connect Bus
JTAG	Joint Test Action Group
LNA	Low Noise Amplifier
MIPI	Mobile Industry processor interface
MPP	Multi-Purpose Pin
NFC	Near Field Communication

RF	Radio Frequency
SATA	Serial ATA
SLIMBUS	Serial Low-power Inter-chip Media Bus
µSOM	micro System On Module
SPMI	System Power Management Interface (Qualcomm® PMIC / baseband proprietary protocol)
SSBI	Single wire serial bus interface (Qualcomm® proprietary mostly PMIC / Companion chip and baseband processor protocol)
UART	Universal Asynchronous Receiver Transmitter
UFS	Universal Flash Storage
UIM	User Identity module
USB	Universal Serial Bus
USB HS	USB High Speed
USB SS	USB Super Speed

2.4 List of Figures

2.5 List of Tables

3. OPEN-Q 820 µSOM DEVELOPMENT KIT

3.1 Introduction

The Open-Q 820 µSOM provides a quick reference or evaluation platform for Qualcomm's latest 820 series - Snapdragon™ 820 processor. This kit is suited for Android / Linux application developers, OEMs, consumer manufacturers, hardware component vendors, video surveillance, robotics, camera vendors, and flash chip vendors to evaluate, optimize, test and deploy applications that can utilize the Qualcomm® Snapdragon™ 820 series technology.

3.2 Development Platform Notice

This development platform contains RF/digital hardware and software intended for engineering development, engineering evaluation, or demonstration purposes only and is meant for use in a controlled environment. This device is not being placed on the market, leased or sold for use in a residential environment or for use by the general public as an end user device.

This development platform is not intended to meet the requirements of a commercially available consumer device including those requirements specified in the European Union directives applicable for Radio devices being placed on the market, FCC equipment authorization rules or other regulations pertaining to consumer devices being placed on the market for use by the general public.

This development platform may only be used in a controlled user environment where operators have obtained the necessary regulatory approvals for experimentation using a radio device and have appropriate technical training. The device may not be used by members of the general population or other individuals that have not been instructed on methods for conducting controlled experiments and taking necessary precautions for preventing harmful interference and minimizing RF exposure risks. Additional RF exposure information can be found on the FCC website at http://www.fcc.gov/oet/rfsafety/

3.3 Anti-Static Handling Procedures

The Open-Q 820 µSOM Development Kit has exposed electronics and chipsets. Proper anti-static precautions should be employed when handling the kit, including but not limited to:

- Using a grounded anti-static mat
- Using a grounded wrist or foot strap

3.4 Kit Contents

The Open-Q 820 µSOM Development Kit includes the following:

- Open-Q 820 µSOM with the Snapdragon™ 820 (APQ8096) processor or main CPU board

- Mini-ITX form-factor carrier board
- 4.5” FWVGA (480x854) 16.7 M LCD (Additional Accessory)
- AC power adapter and HDMI cable

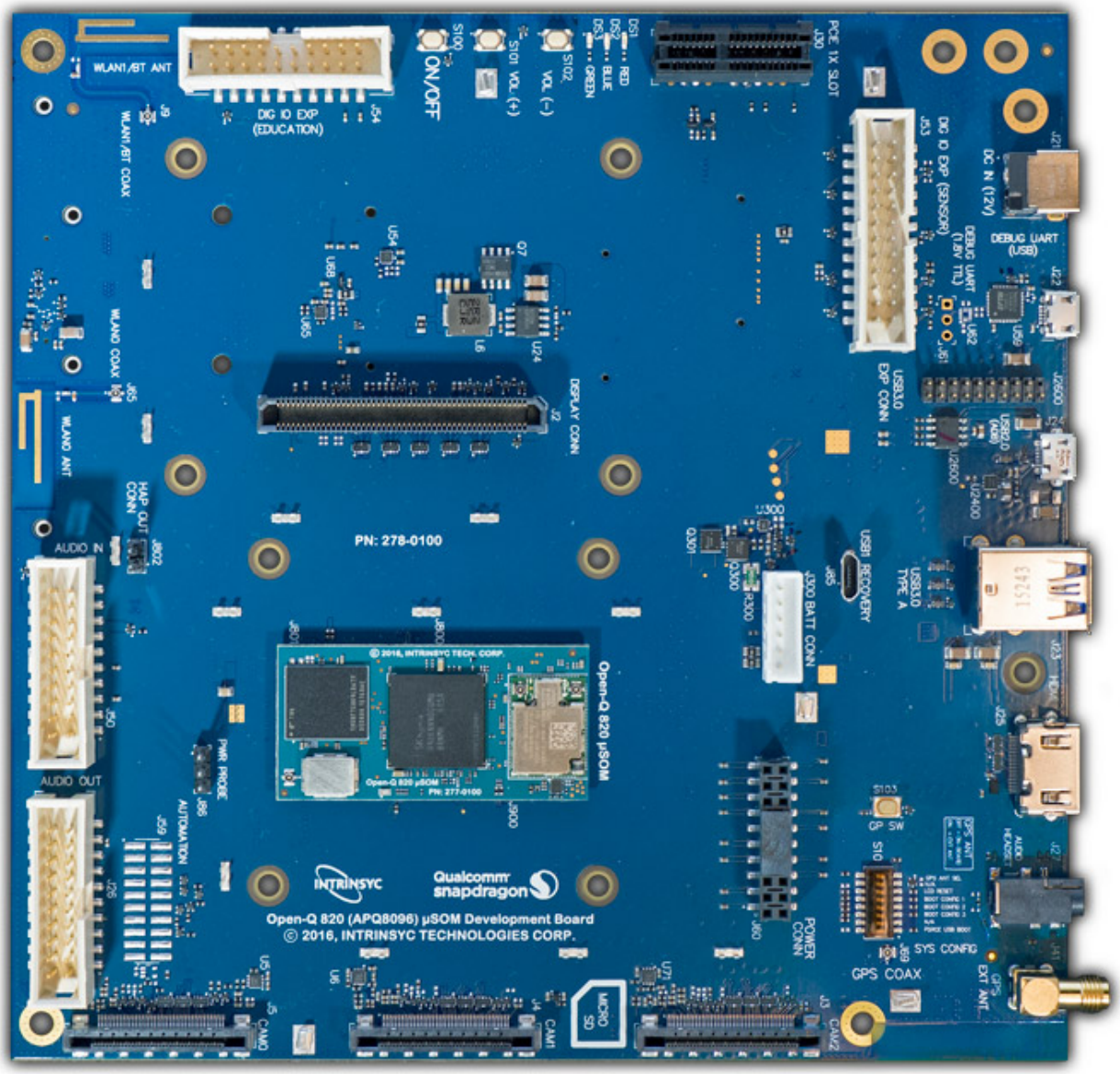

Figure 1 Assembled Open-Q 820 µSOM Development Kit

The development kit comes with Android 6.0 (Marshmallow) software pre-programmed on the CPU board (µSOM). Please contact Intrinsyc for availability of camera modules, sensor boards, and other accessories: sales@intrinsyc.com

3.5 Hardware Identification Label

Labels are present on the CPU board and the mini-ITX form-factor carrier board. The following information is conveyed on these two boards:

CPU board (µSOM).:

- Serial Number
- WIFI MAC address

Refer to http://support.intrinsyc.com/account/serialnumber for more details about locating the serial number, as this will be needed to register the development kit. To register a development kit, please visit: http://support.intrinsyc.com/account/register

Mini-ITX form-factor carrier board:

- Serial Number

Note: Please retain the µSOM and carrier board serial number for warranty purposes.

3.6 System Block Diagram

The Open-Q 820 µSOM development platform consists of three major components

- Open-Q 820 µSOM
- Carrier board for I/O and connecting with external peripherals
- Display Adapter Board (additional accessory)

The following diagram explains the interconnectivity and peripherals on the development kit.

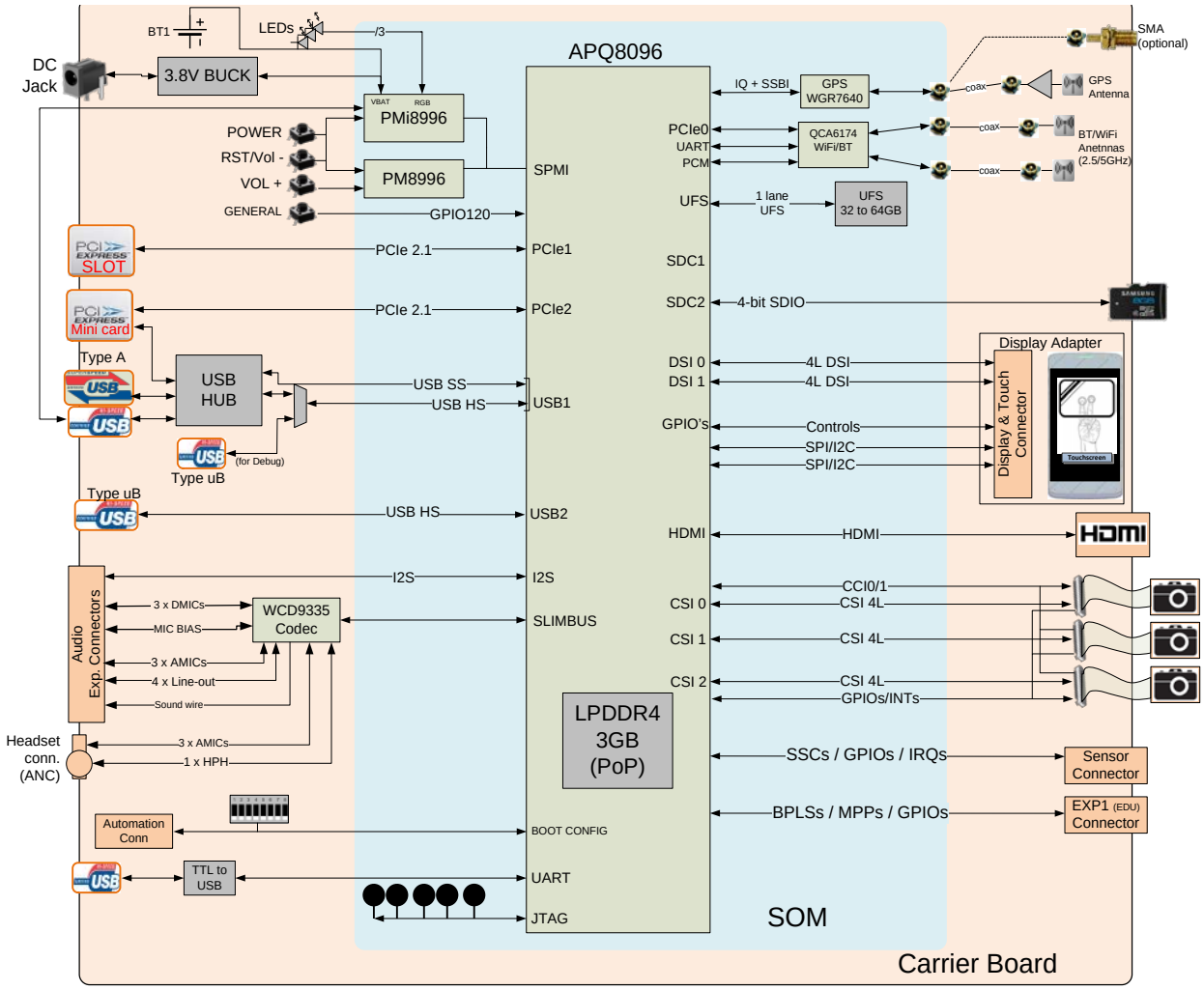

Figure 2 Open-Q 820 µSOM + Carrier Board Block Diagram

3.7 Open-Q 820 µSOM

The µSOM provides the basic common set of features with minimal integration efforts for end users.

It contains the following:

- Snapdragon™ 820 (APQ8096) main application processor
- LPDDR4 up to 1866MHz 3GB RAM (POP)
- PMi8996 + PM8996 – PMIC for Peripheral LDOs, Boost Regulators
- QCA6174 Atheros Wi-Fi + BT combo chip over PCIe, UART, PCM
- 32 GB UFS 2.0.
- WGR7640 RF Front End

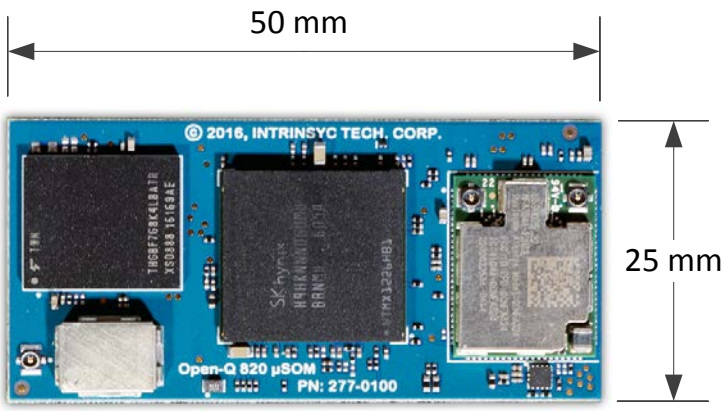

Figure 3 Open-Q 820 µSOM

3.7.1 µSOM Mechanical Properties

Area	12.5 cm^2(25 mm x 50 mm)
Interface	3 x 100-pins Hirose DF40 connectors (B2B Connector).
Thermal	A top side heat sink is installed by default.
Shielding	A top side shield can for the GPS front end is installed by default.

3.7.2 µSOM Block Diagram

The Open-Q 820 µSOM measuring 25mm x 50mm is where all the processing occurs. It is connected to the carrier via three 100 pin Hirose DF40 connectors. The purpose of these connectors is to bring out essential signals such that other peripherals can be connected to the platform.

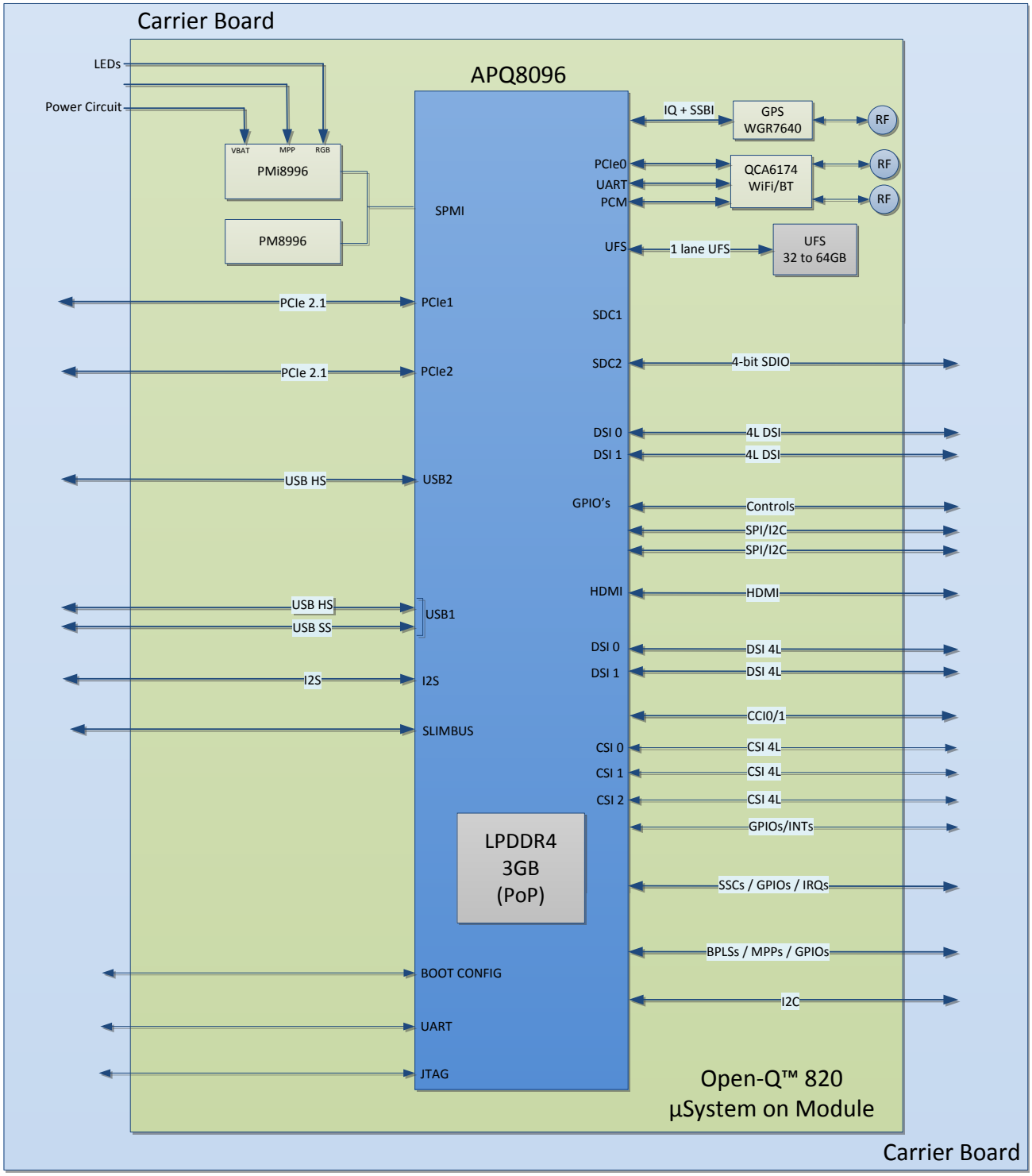

Figure 4 µSOM Block Diagram

3.7.3 Hardware Specification

The Open-Q 820 µSOM platform encompasses the following hardware features:

Table 3.7-1 Open-Q 820 µSOM Hardware Features

Subsystem / Connectors	Feature Set	Description	Specification
Chipset	APQ8096	Qualcomm® Snapdragon™ 820 Processor	Qualcomm® Kyro CPU, quad core, 64-bit ARM V8 compliant processor, 2.2GHz
	PMIC (PM8996 & PMI8996)	Qualcomm® PMIC, Companion PMIC for APQ8096 processor	NA
Memory	3GB LPDDR4	Memory POP	Up to 1866MHz LPDDR4 POP on CPU BGA chip. Supports via 4x16bit channels
	32 GB UFS	Primary Storage for platform. Mainly used for storing SW applications and user data etc.	Toshiba UFS on board. Can support up to 256GB
Connectivity	Wi-Fi 2.4 GHz/ 5GHz via QCA6174 – SDIO	Wi-Fi Atheros QCA6174 Wi-Fi + BT Combo Chip	802.11a/b/g/n/ac 2.4/5.0 GHz via QCA6174 over PCIe0. Full 2x2 antenna configuration
	BT 2.4 GHz via QCA6174 – UART / PCM	Wi-Fi Atheros 6174 Wi-Fi + BT Combo Chip	Support BT 4.1 + HS and backward compatible with BT 1.x, 2.x + EDR
	GPS via WGR7640 – SSBI Qualcomm® Proprietary Protocol	GPS Frontend	GPS, GLONASS, COMPASS
RF Interfaces	2xWLAN / BT	Connect to antenna on carrier board via coax cable	2.4/ 5 GHz
	1x GPS	Connect to antenna on carrier board via coax cable	GPS/GLONASS/COMPASS
Interfaces	3 x MIPI CSI	Camera Connectors CSI0, CSI1, CSI2	MIPI Alliance Specification v1.0
	2 x USB HS & 1 x USB SS	1 x USB3.1 header, 1 x dual stack type A USB3.0 via USB HUB for front USB (from USB1 line), 1 x USB 2.0 via switch (from USB1 line), 1 x micro AB USB 2.0 (from USB2 line)	USB3.1 & USB2.0
	1 x MIPI DSI (DSI0 & DSI1) + Touch 100-pin display Connector	100- pin display connector. Interfaces with Intrinsyc Display Adapter Board	MIPI Alliance Specification v1.01. MIPI D-PHY Specification v0.65,v0.81, v0.90, v1.01
	3 X PCIe	PCIe 0 PCIe signal to Wi-Fi module. PCIe 1, 2 routed out of µSOM	PCI Express Specification, Rev 2.1

Subsystem / Connectors	Feature Set	Description	Specification
Connector	3 x board to board connector	Connectors to interface with carrier board	Hirose DF40C series 100pin connector

3.7.4 µSOM RF Specification for WIFI, BT, GPS

The µSOM includes the following radio interfaces:

- Wi-Fi + BT: ANT1
- Wi-Fi only: ANT2
- WGR7640: For GPS RF Front end

Antenna 1: Antenna 1 is used for providing Wi-Fi and Bluetooth connectivity to QCA6174. This antenna is meant to be connected to the carrier board via a coaxial cable. The function of this connector is for extending the dual band capabilities of the Wi-Fi chip; therefore, enabling this antenna to be used simultaneously with Antenna 2. For example, Antenna 2 can be connected to 2.4GHz while Antenna 1 can be connected to 5.1 GHz. To turn on Bluetooth, only Antenna 1 can be used.

Antenna 2: Antenna 2 provides Wi-Fi connectivity for QCA6174. This antenna connector is meant to be connected to the carrier board PCB antenna via a coaxial cable. ANT2 is a standard dual band antenna from 2.4 GHz to 5.1 GHz.

The µSOM WiFi/BT module has received regulatory certifications (see FCC ID: 2AFDI-ITCNFA324 for details). Please note that the on-board PCB antennas were not the antennas used for the µSOM WiFi/BT module certification. Refer to the certification documents for the WiFi/ BT module (see R-4) for information regarding the test configurations used for certification. Deviating from the documented configuration may trigger the need for re-certification.

For details on connecting the WiFi module to the on-board PCB antennas on the carrier board, refer to section 3.8.13 below.

WGR7640: GPS Front End WGR7640 is the primary GPS radio interface used on the Open-Q 820 µSOM development kit. This provides the RF capabilities for GNSS functions. It has both digital and RF interfaces. Digital interface is required for configuration and status of the APQ8096 baseband processor.

The following are the operating frequencies for WGR7640

GPS: 1574.42 MHz – 1576.42 MHz
GLONASS: 1598 MHz to 1606 MHz

3.8 Open-Q 820 µSOM Carrier Board

The Open-Q 820 µSOM Carrier board is a Mini-ITX form factor board with various connectors used for connecting different peripherals. The following are the mechanical properties of the carrier board:

Dimensions	289 cm^2 (170mm x 170mm)
Form Factor	Mini-ITX
Major Interfaces	See section 3.9 for details regarding carrier board interfaces

3.8.1 Dip switch S10 Configuration Options

There is a DIP switch S10 on the top side of the Open-Q 820 µSOM carrier board. The 8-bit switch allows the user to control the system configuration and boot options. Table 3.8-1 below outlines the pin outs and connections of this DIP switches.

Table 3.8-1 Dip Switch HW / SW configuration

Function	DIP Switch	Description	Notes
FORCED_USB_BOOT	S10-1	Toggles between FORCE USB boot and EDL mode. Enables FORCE USB (GPIO 57) when DIP switch turned on	Default out of the box configuration is OFF which is the EDL mode **Note:** FORCE USB boot option not supported by Intrinsyc
NC	S10-2	N/A	N/A
BOOT_CONFIG[3]	S10-3	Enables APQ boot configuration 3 when DIP switch turned on. Controlled by APQ GPIO104 See schematic for boot configuration options. NOTE: µSOMe boot configurations are not supported on the development kit.	Default out of the box configuration is ON
BOOT_CONFIG[2]	S10-4	Enables APQ boot configuration 2 when DIP switch turned on. Controlled by APQ-GPIO103	Default out of the box configuration is OFF
BOOT_CONFIG[1]	S10-5	Enables APQ boot configuration 1 when DIP switch turned on. Controlled by APQ-GPIO 102	Default out of the box configuration is OFF
WATCHDOG_DISABLE	S10-6	Enables WATCHDOG_DISABLE when DIP switch turned on. Controlled by APQ-GPIO 101	Default out of the box configuration is OFF
N/C	S10-7	NA	NA
GPS_ANT_SEL	S10-8	Option to select which antenna to use for GPS. When DIP switch ON GPS external antenna is being used (SMA connector). When OFF, GPS printed antenna is being used (on-board)	Default out of the box configuration is OFF

Warning! : Before making any changes to the dip switch, make sure to note down the previous configuration. The default switch settings are above.

3.8.2 Carrier Board Expansion Connectors

The following table lists the connectors, expansions and their usages on the carrier board:

Table 3.8-2 Carrier Board Expansion Options and Usage

Domain	Description	Specification	Usage
Power	AC / Barrel charger	12 V DC Power Supply 5 A	Power Supply
	Power connector	20 pin header	For providing extra current to camera connectors when needed (ie: when high performance cameras used)
	Battery Connector	6 pin header	For Battery operation and charging development
Debug Serial via USB	Debug Serial UART console over USB for development	Vertical USB Micro B connector	Development Serial Connector for debug output via USB
Buttons	General Purpose SW button	SMD Button	Additional button for general purpose (connected to APQ_GPIO120)
	Power Button	SMD Button	Power Button for Suspend / Resume and Power off
Zoom / Volume Keys	Volume + key	SMD Button	Volume +Key
	Volume – key	SMD Button	Volume – Key
Sensor IO Connector	24 pin Sensor Expansion Connectors	Support any user sensor card, Standard 24-pin ST Micro PLCC support via optional daughter card	Available via Intrinsyc optional accessories kit
GPIO / Education connector Header	20-pin general purpose IO for SPI / I2C / GPIOs/ UIM/ UART functions and other unused GPIOs from PMIC and APQ education header.	Full BLSP1 (SPI/ UART/ I2C/ GPIO) APQ GPIOs MPPs Power	Useful when user wants to use UART GPIOs pins as BLSP other functions (GPIO/ I2C/ UIM/ SPI).
Micro SD (on bottom)	Micro SD card	4bit Micro SD card support	External Storage
ANC Audio Jack	Audio Jack supported using WCD9335	ANC audio jack providing 2lineout and 1 headset drivers (with Qualcomm® ANC technology)	Audio support
3-Digital Microphone via audio input expansion header	Audio expansion Supported using WCD9335	Digital Audio header	For Digital audio input for Digital MIC, I2S codec, Slim bus interface.

Domain	Description	Specification	Usage
3-Analog Microphone via audio input expansion header	Audio expansion Supported using WCD9335	Analog Audio header	For Analog audio input for Analog MIC (differential signal)
2-Loud Speaker via audio output expansion header	Audio expansion Supported using WCD9335	Analog Audio header	For loud speaker output after signal has been processed
Earpiece via audio output expansion header	Audio expansion Supported using WCD9335	Analog Audio header	For earpiece output after signal has been processed
Haptics driver via audio output expansion header	Audio expansion Supported using WCD9335	Analog Audio header	For haptics output (ex: vibrator) after signal has been processed
Ultrasound transducer via audio output expansion header	Audio expansion Supported using WCD9335	Analog Audio header	Ultrasound transducer output
HDMI Port	Extended Display ports	HDMI port supports up to 4K without HDCP 1.4A spec	External Display
USB OTG	USB 2.0 OTG	Micro AB connector	ADB and USB client / host mode
USB 3.1	USB 3.1 via USB1 through USB switch and hub	Dual Type A connector	Host mode transfer data to and from CPU
USB Expansion connector	2 additional USB3.1 ports via USB1 through USB switch and Hub	Samtec TMMH series header	Additional USB ports
USB Recovery	USB 2.0 via USB1 through USB switch	Micro B connector	USB recovery/ debug
WLAN Antenna	2X PCB Antenna	2.4 – 5.1 GHz	Antenna to µSOM WiFi module
GPS Antenna	PCB Antenna	GPS : 1574.42 MHz – 1576.42 MHz GLONASS : 1587 MHz – 1606 MHz	Antenna to µSOM GPS module

Domain	Description	Specification	Usage
GPS External Antenna via SMA Connector	SMA connector for external GPS antenna	Supports active antenna	External GPS antenna
Coin Cell Holder(Optional)	Coin Cell battery(Optional via stuffing)	Coin cell battery for PMIC RTC	RTC
LED	3xLED	Red : PMIC Driven Green: PMIC Driven Blue: PMIC Driven	Blue : General Purpose Red : Charging Green : Charging complete
LCD Display and Touch connector	100 pin for LCD signals via b2b connector to display adapter board	4-lane MIPI DSI0 , DSI1 I2C/SPI/GPIO Backlight MIPI Alliance Specification v1.01 MIPI D-PHY Specification v0.65,v0.81, v0.90, v1.01	Can work as one dual DSI or both independent display
Gen10 connector	Connector for Qualcomm's internal sensor boards	60 pin connector sensor Gen 10	To interface with Qualcomm's internal sensor boards **(for Intrinsyc internal use only – not supported) Can be used for other purposes.**
VIP Extension connector	Connector for interfacing with Qualcomm® legacy automotive VIP boards	60 pin connector	To connect to Qualcomm® legacy automotive VIP boards **(for Intrinsyc internal use only – not supported) Can be used for other purposes.**
Ethernet AVB connector	Connector for interfacing with Ethernet AVB standard	60 pin connector	To connect to automotive peripherals via Ethernet AVB standard **(for Intrinsyc internal use only – not supported) Can be used for other purposes.**
PCI Express Slot	PCI Express for external peripheral connectivity	PCIe1 v2.1 Supports half card only Supports 10W card via power supply Supports 25W card via ATX power supply	To connect an Ethernet PCIe card board to support Ethernet.
Mini PCI Express Connector	Mini PCI Express for external peripheral connectivity	PCIe1 v2.1 Can support half or full size card	For external mini PCIe card

Domain	Description	Specification	Usage
WWAN SIM Card (on bottom)	WWAN SIM card connector (optional)	4bit Mini SIM card support	For WWAN mini PCI express cards
CSI Camera connectors	3 x CSI port connector with CLK, GPIOS, CCI	Supports 3 x Camera interfaces via three separate connectors • 3 x MIPI-CSI each 4 lane • External flash driver control • Support for 3D camera configuration • Separate I2C / CCI control MIPI Alliance Specification v1.00 for Camera Serial Interface	
Power Probe Header	3 pin power probe header	Sense lines connected across 0.005 Ohm resistor	To measure current consumption of µSOM
Haptics Connector	2 pin haptics driver header	Haptics driver output from PMI8996	For connecting a 2 pin vibrating motor

The sections below will provide in depth information on each expansion header and connector on the carrier board. The information listed below is of particular use for those who want to interface other external hardware devices with the Open-Q 820 µSOM. Before connecting anything to the development kit, please ensure the device meets the specific hardware requirements of the processor.

3.8.3 DC Power Input J21

The Open-Q 820 µSOM development kit power source connects to the 12V DC power supply jack J21. Starting from the power jack, the 12V power supply branches off into different voltage rails via step down converters on the carrier board and PMIC on the µSOM. The µSOM is powered by 3.8V via a Texas Instrument step down converter U400 on the carrier board. To ensure the µSOM is getting powered correctly, user can monitor the current going into the µSOM via the power probe header J86 (see section below).

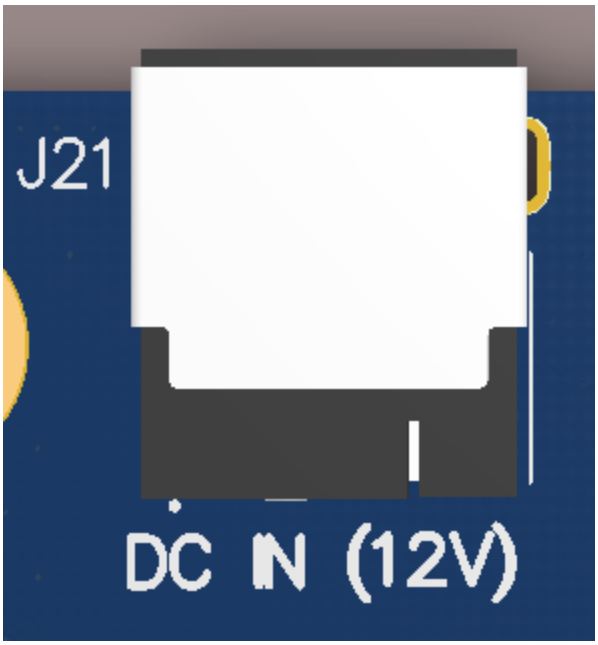

Figure 5 J21 12V DC Power Jack

The µSOM consists of 2 PMIC modules. Functionalities of the 2 modules are outlined below.

PMI8996 PMIC is used for:

- Source various regulated power rails
- Battery charging. Please see section below for additional information on battery support.
- Please note that support for battery charging over external charger is not implemented in the design. Please contact Intrinsyc for such customization.

PM8996 PMIC is used for:

- Source various regulated power rails
- Source system clock

3.8.4 Battery Header J300

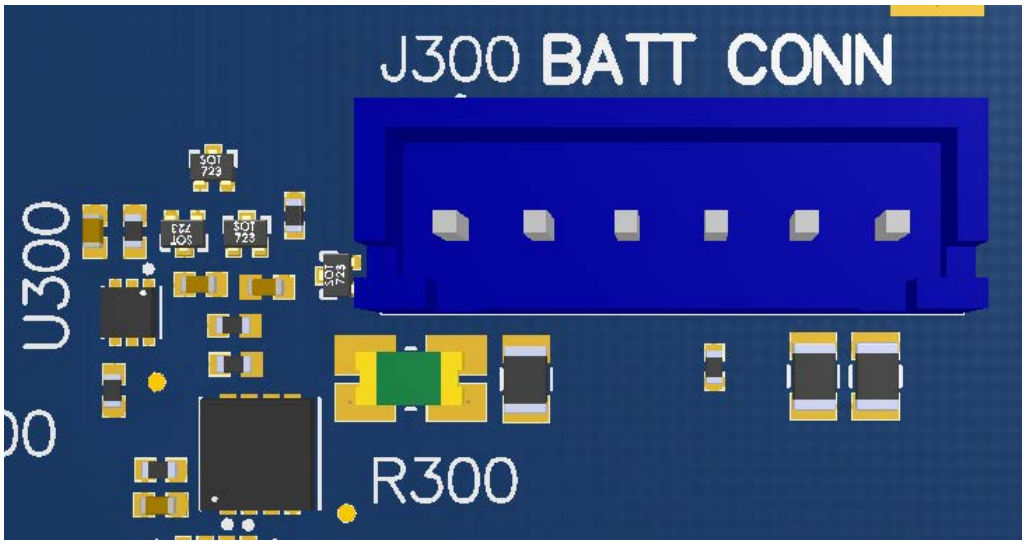

Figure 6 J300 Battery Header

The Open-Q µSOM 820 development platform can also power the µSOM with a single cell Lithium-Ion Polymer (LiPo) battery pack which connects to header J300. The purpose of this header is to be used by the end user to develop a battery charging solution, including battery characterization. Intrinsyc recommends using the AA Portable Power Corp's CU-J479-V2 / 1ICP7/55/85 Lithium ion battery pack. This is a single cell pack with a nominal voltage of 3.8V and a capacity of 3200mAh (11.8 Wh, 5A rate). If user intends to use a different battery, please note the pin outs on this battery header.

Description	Signal	Pin	Note
µSOM Battery positive supply terminal	VBAT Plus (VBAT+)	J300[1]	
µSOM Battery positive supply terminal	VBAT Plus (VBAT+)	J300[2]	
N/C	N/C	J300[3]	
Internal battery pack temperature	BATT_THERM (The recommended battery has a 10K Ohm thermistor)	J300[4]	Depopulate R197 if battery selected has a 10K ohm thermistor
µSOM Battery negative supply terminal	VBAT Minus(VBAT-)	J300[5]	
µSOM Battery negative supply terminal	VBAT Minus(VBAT-)	J300[6]	

Please note that the battery only powers the µSOM. To ensure proper functionality of the development kit, the 12V power supply must be attached at J21. When a battery is not in use, the TI step down converter U400 is used to power the µSOM.

Note that the software that is shipped with the development kit does NOT support battery charging. Please visit the Intrinsyc support site and follow the instructions for preparing the platform to support battery charging.

3.8.5 Power Probe Header J86

Figure 7 J86 Power Probe Header

The power probe header is used to sense/ monitor the current on the 3.8V power rail going into the µSOM. The table below summarizes the pin outs of header J86.

Description	Signal	Pin
µSOM power positive current sense line	µSOM_PWR_SENSE_P	J86[1]
µSOM power negative current sense line	µSOM_PWR_SENSE_N	J86[2]
GND	GND	J86[3]

3.8.6 Debug Serial UART Header J61

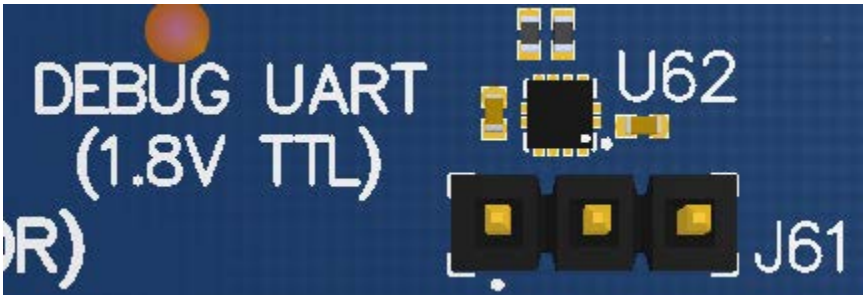

Figure 8 J61 3.3V TTL Debug UART

The UART header and supporting circuitry does not come preinstalled. To have access to the debug UART, a 3-pin header needs to be installed as well as the supporting circuitry. Please see page 17 of the µSOM carrier board schematic for details on what to install for this header to be functional.

The header consists of TX, RX and GND pins. This is a 3.3V TTL UART header. To get the serial terminal working with a PC, the following cable (or similar) is needed
http://www.digikey.ca/product-detail/en/TTL-232R-RPI/768-1204-ND/4382044

Description	Signal	Pin	FTDI RPI cable connection
APQ UART RX (GPIO5)	BLSP8_UART_RX	J61[1]	Orange
APQ UART TX (GPIO4)	BLSP8_UART_TX	J61[2]	Yellow
GND	GND	J61[3]	Black

3.8.7 Debug Serial UART over USB J22

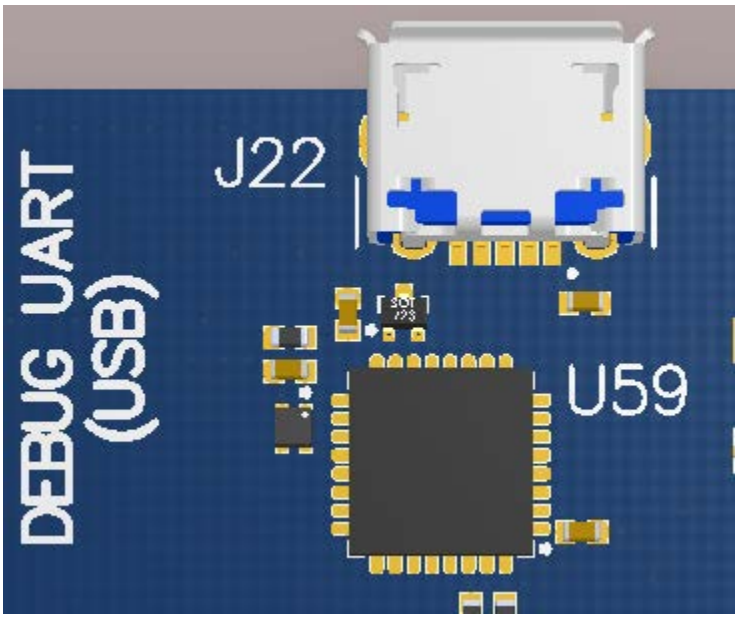

Figure 9 J22 Debug UART over USB

The UART connection used on the Open-Q 820 µSOM is a USB micro B connector (J22). This debug UART is available over USB via the FTDI FT232RQ chip on the carrier board. To get the serial terminal working with a PC, user needs to ensure that the appropriate FTDI drivers are installed.

3.8.8 Sensor IO Expansion Header J53

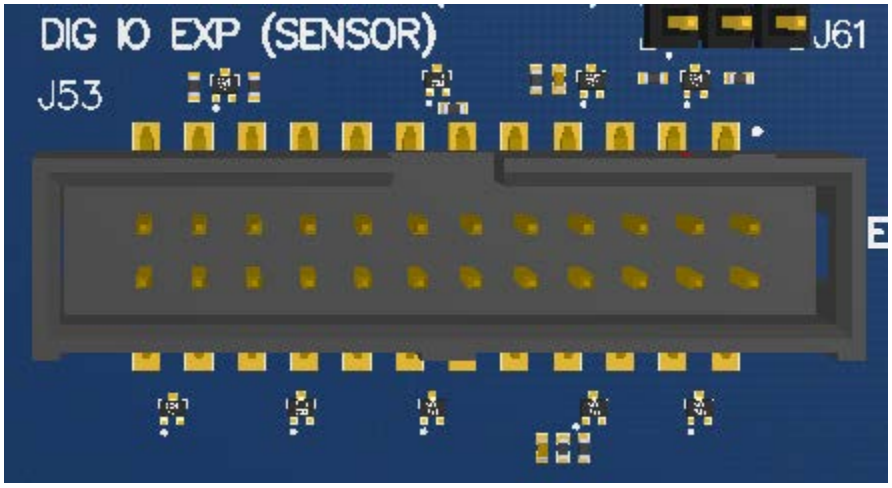

Figure 10 J53 Sensor Expansion Header

The sensor expansion header J53 allows for a 24-pin connection to an optional sensor board. If user application does not require a sensor, then this header can be used for other applications that require I2C or GPIO input and output connections.

Following is the pin breakout for sensor expansion header J53.

Table 3.8-3 Sensor Expansion Header J53 Pin out

Description	Signal	Pin NO	Description	Signal	Pin NO
SSC I2C-3 serial data	SSC_I2C_3_SDA	J53[1]	Accelerometer interrupt input to processor via GPIO117	ACCEL_INT_N	J53[2]
SSC I2C-3 serial clock	SSC_I2C_3_SCL	J53[3]	Cap interrupt input to processor via GPIO123	CAP_INT_N	J53[4]
Sensor reset signal from processor to sensor via GPIO80	MEMS_RESET_N	J53[5]	Gyroscope interrupt input to processor via GPIO118	GYRO_INT	J53[6]
Sensor IO PWR 1.8 V VREG_LVS2A_1P8 power supply regulator (Digital)	SENS_IO_PWR	J53[7]	Sensor Analog power supply from VREG_L19A 2.85V or 3.3V (If R160 populated)	SENS_ANA_PWR	J53[8]
GND	GND	J53[9]	GND	GND	J53[10]
HRM interrupt/ configurable GPIO122	HRM_INT	J53[11]	Touch screen interrupt input from processor via GPIO125	TS_INT0	J53[12]
SSC SPI-1 chip select 2	SSC_SPI_1_CS1_MAG_N	J53[13]	Alternate sensor interrupt input to processor via GPIO120	ALSPG_INT_N	J53[14]
NC	NC	J53[15]	Digital Compass interrupt input to processor via GPIO119	MAG_DRDY_INT	J53[16]
NC	NC	J53[17]	NC	NC	J53[18]
SSC SPI-1 chip select 1	SSC_SPI_1_CS_N	J53[19]	SSC SPI-1 data master out/ slave in	SSC_SPI_1_MOSI	J53[20]
SSC SOI-1 clock	SSC_SPI_1_CLK	J53[21]	SSC SPI-1 data master in/ slave out	SSC_SPI_1_MISO	J53[22]
NC	NC	J53[23]	SSC power enable	SSC_PWR_EN	J53[24]

In sum, if sensor application is not needed, this expansion header can provide two full BLSP7 and BLSP5 for UART/ SPI/ I2C/ UIM. Please refer to the schematic and consider the power before connecting anything to this header.

Note that there is an unpopulated Gen-10 connector header (J55) footprint at the bottom of the carrier board. Install the Samtec (part number: QSH-030-01-L-D-A) connector here if needed.

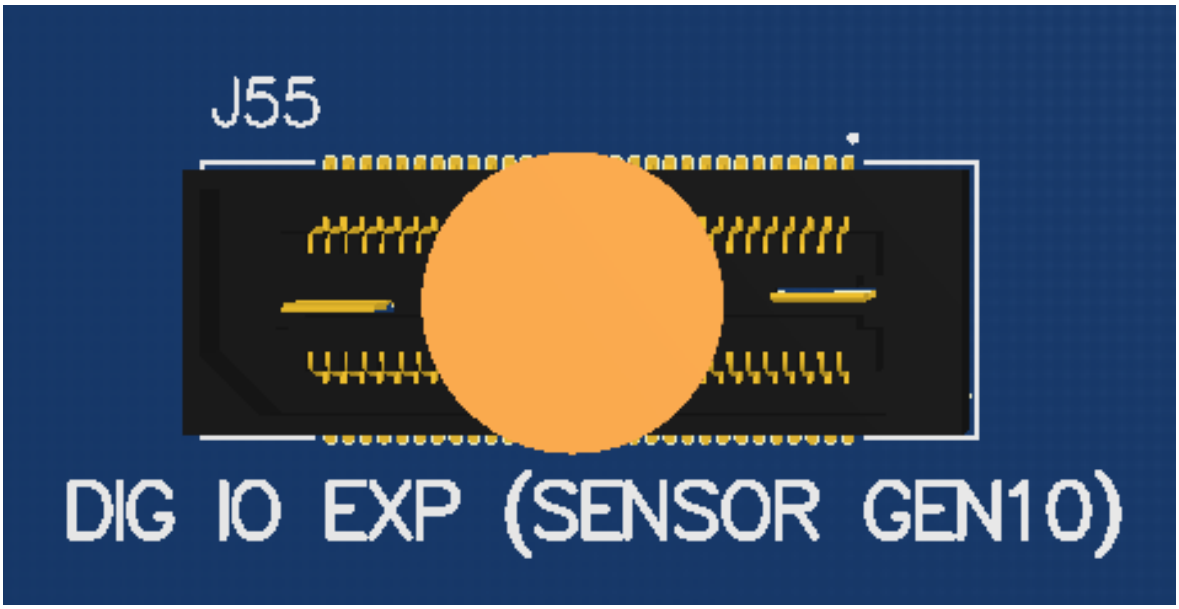

Figure 11 J55 Gen-10 Sensor Connector (Samtec QSH-030 series)

3.8.9 Education / GPIO header J54 (EXP2)

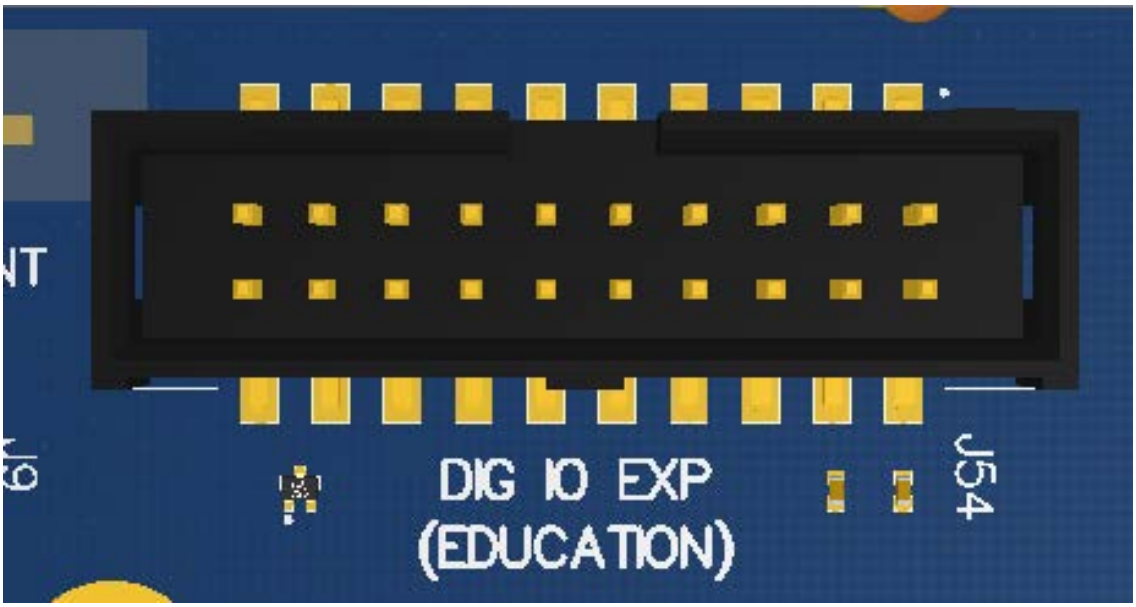

Figure 12 J54 Education / GPIO header

Education/ GPIO header expansion J54 is a 20 pin connector that provides access to BLSP1 signals with level shifters. It is ideally used for connecting external peripherals such as microcontrollers and any other devices that are based on I2C, SPI, UART, UIM and GPIO. Please refer to the µSOM carrier board schematic for the level shifter, target voltage and current rating depending on stuffing option. The education expander also supports multiple voltage ratings. The table below outlines the configurations for these settings:

Voltage Rails	Resistors to Populate (0 Ohm)
MB_VREG_3P3 – 3.3 V	R150 (Default)
VREG_S4A_1P8 – 1.8V	R149
MB_VREG_5P0 – 5.0 V	R151

The following are the detailed pin out information for education header J54.

Table 3.8-4 Education Connector Expansion Header J54 Pin Out

Description	Signal	Pin NO	Description	Signal	Pin NO
NC	NC	J54[1]	VREG_S4A 1.8V voltage regulator max 150mA	VREG_S4A_1P8	J54[2]
BLSP1_3_3P3(3.3V)	BLSP1_SPI_MOSI (APQ-GPIO0)	J54[3]	VDD_EXP2 (Default 3.3V Power Supply) max 300mA	VDD_EXP2	J54[4]
BLSP1_2_3P3(3.3V)	BLSP1_SPI_MISO (APQ-GPIO1)	J54[5]	NC	N/C	J54[6]

Description	Signal	Pin NO	Description	Signal	Pin NO
BLSP1_1_3P3(3.3V)	BLSP1_SPI_CS_N (APQ-GPIO2)	J54[7]	PM8996 MPP GPIO4	PM_MPP04	J54[8]
BLSP1_0_3P3(3.3V)	BLSP1_SPI_CLK (APQ-GPIO3)	J54[9]	NC	N/C	J54[10]
NC	N/C	J54[11]	NC	N/C	J54[12]
NC	N/C	J54[13]	NC	N/C	J54[14]
NC	N/C	J54[15]	NC	N/C	J54[16]
GND	GND	J54[17]	NC	N/C	J54[18]
NC	N/C	J54[19]	5V power supply max 150mA	MB_VREG_5P0	J54[20]

3.8.10 ANC Headset Jack J27

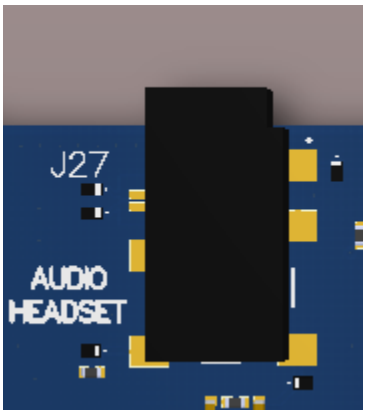

Figure 13 ANC Headphone Jack

The ANC headset jack (J27) is a special 3.5mm TRRS jack with ANC capabilities. It is backwards compatible with standard headset jacks. Please contact Intrinsyc at sales@intrinsyc.comfor compatible ANC headsets.

3.8.11 Audio Inputs Expansion Header J50

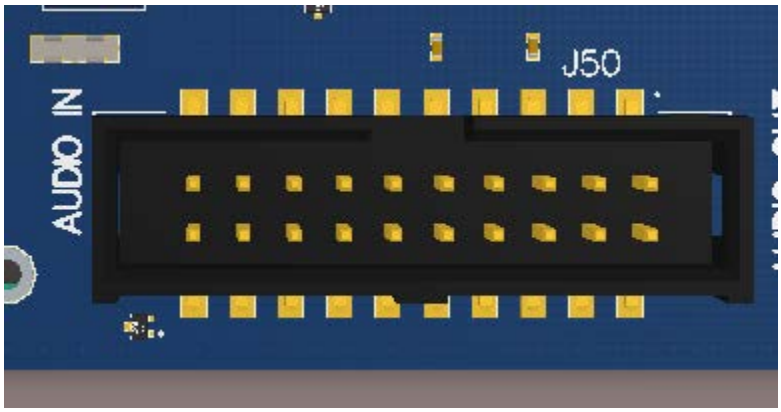

Figure 14 J50 Audio Inputs Expansion Header

This header expansion provides the following audio inputs:

1. 3 digital mic inputs (each can support 2 digital microphones)
2. 3 analog mics
3. Voltage rails to support analog and digital mics

For details on how to connect analog or digital microphones to system, refer to sections 4.1.9 on Open-Q 820 µSOM Development Kit µSOM Technical Note19 (document R-3).

The table below outlines the pin out information of the audio inputs expansion header J50:

Table 3.8-5 Audio Inputs Expansion Header J50 Pin out

Description	Signal	Pin NO	Description	Signal	Pin NO
Analog MIC1 positive differential input	CDC_IN1_P	J50[1]	Analog MIC1 negative differential input	CDC_IN1_N	J50[2]
Analog MIC5 positive differential input	CDC_IN5_P	J50[3]	Analog MIC5 negative differential input	CDC_IN5_N	J50[4]
MIC bias output voltage 1	MIC_BIAS1	J50[5]	MIC bias output voltage 3	MIC_BIAS3	J50[6]
Analog MIC6 positive differential input	CDC_IN6_P	J50[7]	Analog MIC6 negative differential input	CDC_IN6_N	J50[8]
MIC bias output voltage 4	MIC_BIAS4	J50[9]	3.3V power supply max 500mA	MB_VREG_3P3	J50[10]
GND	GND	J50[11]	GND	GND	J50[12]
Clock for digital MIC 1 and 2	CDC_DMIC_CLK0	J50[13]	Clock for digital MIC 3 and 4	CDC_DMIC_CLK1	J50[14]
Digital MIC 1 and 2 data line	CDC_DMIC_DATA0	J50[15]	Digital MIC 3 and 4 data line	CDC_DMIC_DATA1	J50[16]

Description	Signal	Pin NO	Description	Signal	Pin NO
1.8V power supply max 300mA	VREG_S4A_1P8	J50[17]	Clock for digital MIC 5 and 6	CDC_DMIC_CLK2	J50[18]
GND	GND	J50[19]	Digital MIC 5 and 6 data line	CDC_DMIC_DATA2	J50[20]

3.8.12 Audio Outputs Expansion Header J26

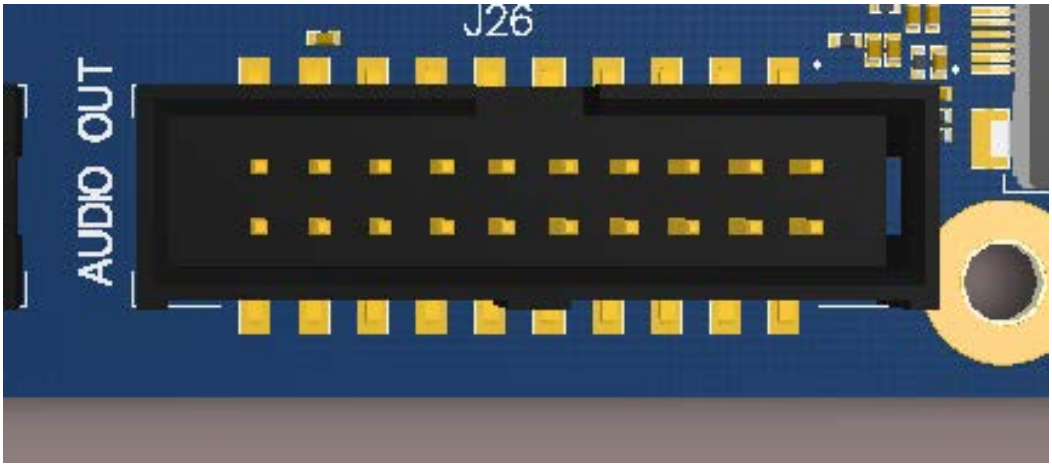

Figure 15 J26 Audio Outputs Expansion Header

This header expansion provides the following audio outputs:

1. 2 differential analog audio line out
2. 2 single ended analog audio line out
3. 1 differential analog earpiece amplifier output (no external amp needed)
4. 2 speaker amplifier enable control
5. Voltage rails to support analog and digital mics

The table below outlines the pin out information of the audio outputs expansion header J26:

Table 3.8-6 Audio Outputs Expansion Header J26 Pin out

Description	Signal	Pin NO	Description	Signal	Pin NO
Analog audio line out 1, positive differential output	CDC_LINE_OUT1_P	J26[1]	Analog audio line out 1, negative differential output	CDC_LINE_OUT1_N	J26[2]
Analog audio line out 2, positive differential output	CDC_LINE_OUT2_P	J26[3]	Analog audio line out 2, negative differential output	CDC_LINE_OUT2_N	J26[4]
Audio line outputs 3 and 4 GND reference	CDC_LINE_REF	J26[5]	3.3V output power supply	MB_VREG_3P3	J26[6]

Description	Signal	Pin NO	Description	Signal	Pin NO
Analog audio line out 3, single ended output	CDC_LINE_OUT3	J26[7]	Analog audio line out 4, single ended output	CDC_LINE_OUT4	J26[8]
Analog earpiece amplifier out, positive differential output	CDC_EAR_P	J26[9]	Analog earpiece amplifier out, negative differential output	CDC_EAR_N	J26[10]
GND	GND	J26[11]	3.8V output power supply	MB_VREG_SOM	J26[12]
Digital soundwire data for WSA8810/ WSA8815 smart speaker amplifier	CDC_SWR_CLK	J26[13]	Digital soundwire data for WSA8810/ WSA8815 smart speaker amplifier	CDC_SWR_DATA	J26[14]
Speaker amplifier enable 1	SPKR_AMP_EN1	J26[15]	Speaker amplifier enable 2	SPKR_AMP_EN2	J26[16]
1.8V output power supply	VREG_S4A_1P8	J26[17]	12V output power supply	DC_IN_12V	J26[18]
5.0V output power supply	MB_VREG_5P0	J26[19]	GND	GND	J26[20]

3.8.13 On Board PCB WLAN Antenna

The Open-Q 820 µSOM carrier board has two on board WLAN PCB antennas that connects to the QCA6174 WiFi module on the µSOM via coaxial cables that attaches to MH4L receptacles. These antennas connect to the µSOM in the following configuration:

- WLAN1 on the carrier board connects to ANT2 on the QCA6174 WiFi module
- WLAN0 on the carrier board connects to ANT1 on the QCA6174 WiFi module

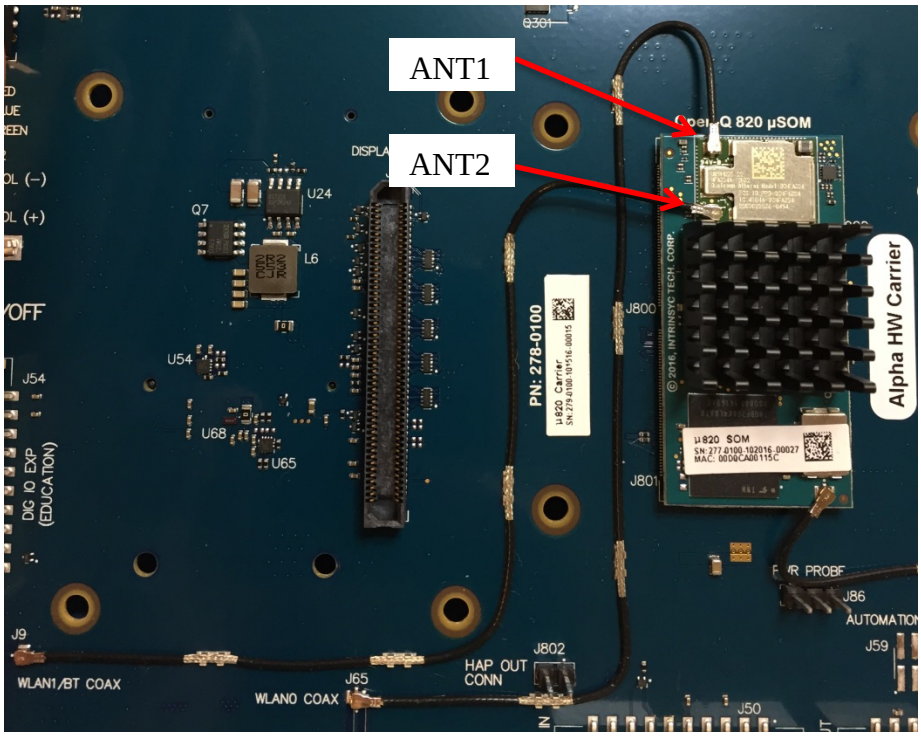

Figure 16 On Board PCB Antennas

3.8.14 External and on-Board PCB GPS Antenna

The Open-Q 820 µSOM carrier board allows user the flexibility of using an external (via SMA connector) or an on-board PCB GPS antenna. Depending on which antenna is used, dip switch S10 needs to be configured (see table below for details).

GPS Antenna Selection	Dip Switch S10 (Position 8) Selection
On Board PCB Antenna	Off Position
External Antenna (Supports Both Active and Passive Antenna)	On Position

If an external GPS antenna is preferred, Intrinsyc recommends the Laird Technologies hepta-band dipole antenna (manufacture part number: MAF94300). It is important to note that GPS should be used or tested near a window or a location where satellites are easily "seen" by the device.

3.8.15 Open-Q Display

The display output options for the Open-Q 820 µSOM Development Kit consists of:

- An HDMI type A connector
  - HDMI 2.0 (4K60) or 4K30 Miracast
- A 100-pin display connector J2 that supports:
  - Dual DSI DPHY 1.2 (up to 3840 x 2400 at 60 fps)
  - Touch screen capacitive panel via I2C or SPI, and interrupts (up to one device)
  - Backlight LED
    - Can support external backlight driver control and power
    - PMI8996 backlight driver supports three LED strings of up to 30mA each with 28V maximum boost voltage

The Open-Q 820 µSOM development platform can support the following display combinations:

MIPI DSI	1 x 4lane DSI0 + 1 x 4lane DSI1 1 x 8 lane combining DIS0 and DSI1 for up to 4K resolution 2 x 4-lane DSI DPHY 1.2 and HDMI (4K60) or 4K30 Miracast Display 3840 x 2400 at 60fps, 2560 buffer width (10 layers blending)
HDMI	V2.0 (4K60)

3.8.16 HDMI Connector J25

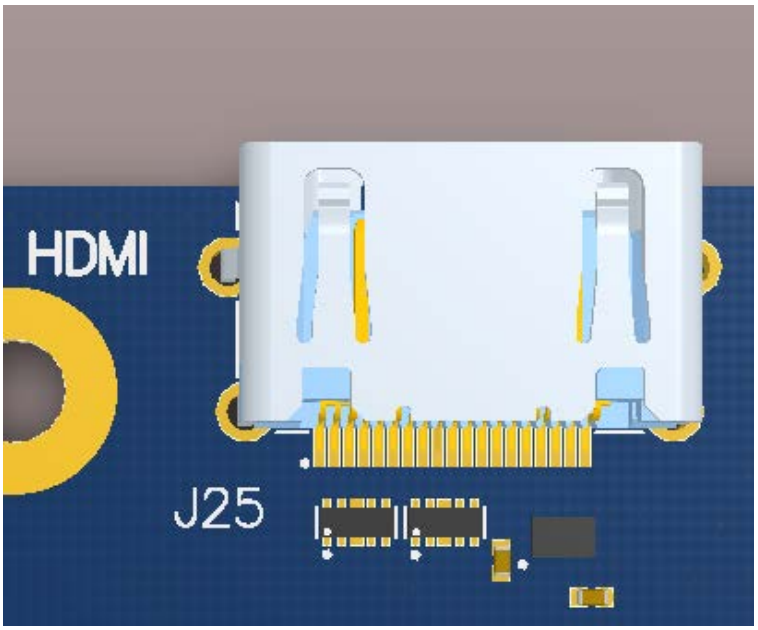

Figure 17 HDMI Type A Connector

The on-board HDMI type A connector enables the Open-Q 820 µSOM development platform to connect to an external HDMI monitor/ television via an HDMI cable. As part of a new feature, the APQ8096 can now support up to 4K UHD (3840 x 2400 at 60fps) and HDMI 2.0 (4K60)/ 4K30 Miracast.

Please note that the Open-Q 820 µSOM Development kit is for evaluation purposes only and may not be HDMI compliant.

3.8.17 Display Connector J2

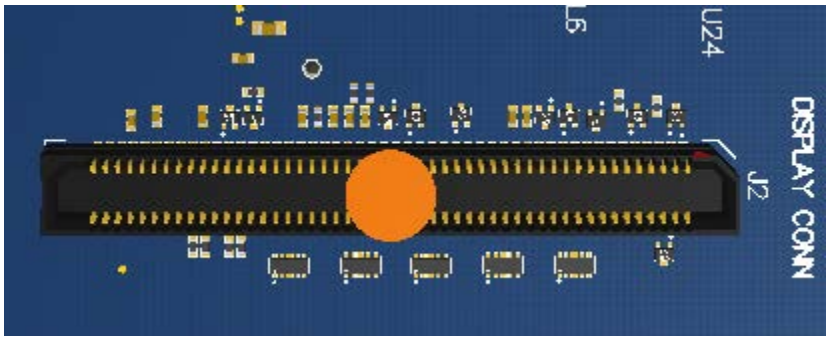

Figure 18 100-Pin Display Connector

The 100-pin display connector provides the following features/ pin-outs that enables the development kit to connect to a MIPI DSI panel/ device:

Note: Please refer to the carrier schematic and display board tech note when designing a custom display board.

- DSI
    - 2 x 4 lane DSI
- Backlight
    - Built-in backlight WLED driver on PMI8996
        - WLED driver supports up to 28.5V output for backlight
    - Primary external backlight (BL0)
        - Backlight control signals
        - External Power
- Display connector – LCD/ AMOLED
    - PMI8996 programmable display bias output voltage:
        - 5V to 6.1V and -1.4V to -6.0V (LCD display)
        - 4.6V to 5V and -1.4V to -5.4V (AMOLED display)
- Additional GPIOs for general purposes available
- VREG_S4A voltage rail from PM8996
    - Required by display for DOVDD
    - 300mA current path
- Touch Panel
    - Supports one touch screen controller
    - Supports I2C or SPI via BLSP12
    - Can chose between I2C or SPI signals in SW U9 via BLSP12

Power specifications

The display connector supports the following power domains:

Display Signal	Power Domain
PM8996 LDO22 (3.3-2.8V)	up to 150 mA
PM8996 LDO14 (1.8V- 2.15V)	up to 150 mA
PM8996 LDO15(1.8V – 2.15V)	up to 300 mA
PM8996 S4A (1.8V)	up to 300 mA
Carrier 3.3V	up to 0.5A
Carrier 5 V	up to 1.5A
Carrier 12 V	up to 0.5A

The Intrinsyc Display Adapter Open-Q 820 board (part number: 280-0100) is an additional PCB that mates with the display connector J2 on the carrier board. This board allows users

to interface with the development kit via the LCD that comes preinstalled on the display board. The following figure illustrates the interfacing connectors on the display board.

Note: The display board comes as an additional add-on to the Open-Q 820 µSOM development kit. To purchase this, please visit http://shop.intrinsyc.com or contact Intrinsyc at sales@intrinsyc.com for details.

Note: Please refer to "Intrinsyc Open-Q 820 (APQ8096) Development Kit Technical Note 15: Display Board Design Guide" for more information on designing a custom display board.

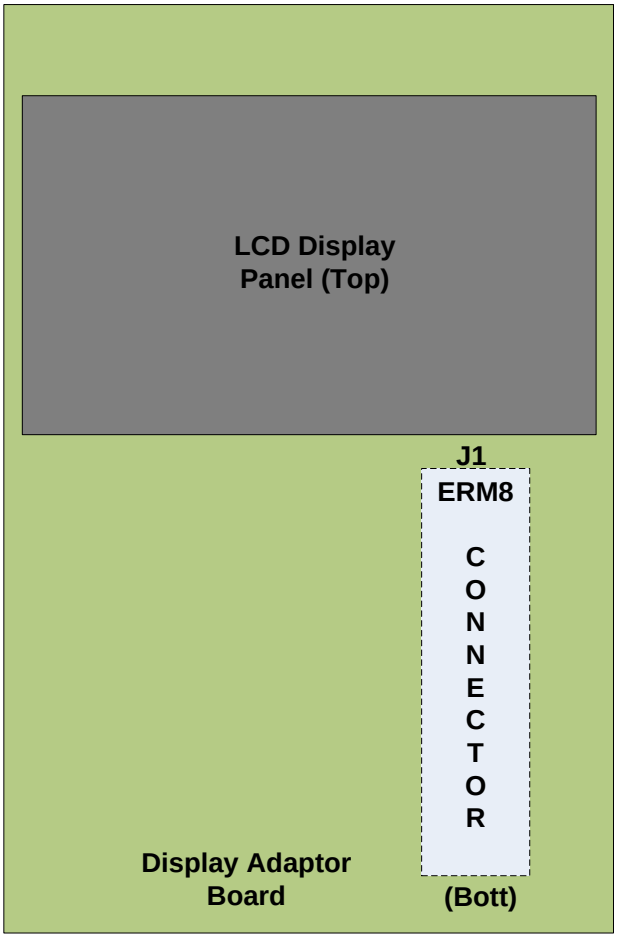

Figure 19 Display Board Block Diagram

Connecting the Display Board to the Development Kit

This configuration allows the user to use the preinstalled LCD display that comes with the display adaptor board. As shown in the block diagram below, the MIPI DSI0 lines, which come from the 100-pin ERM8 connector, directly connects to the LCD panel. See the section below for more details on this LCD panel. It is important to note that connector J1 on the display board needs to connect to J2 on the carrier board for this configuration to work.

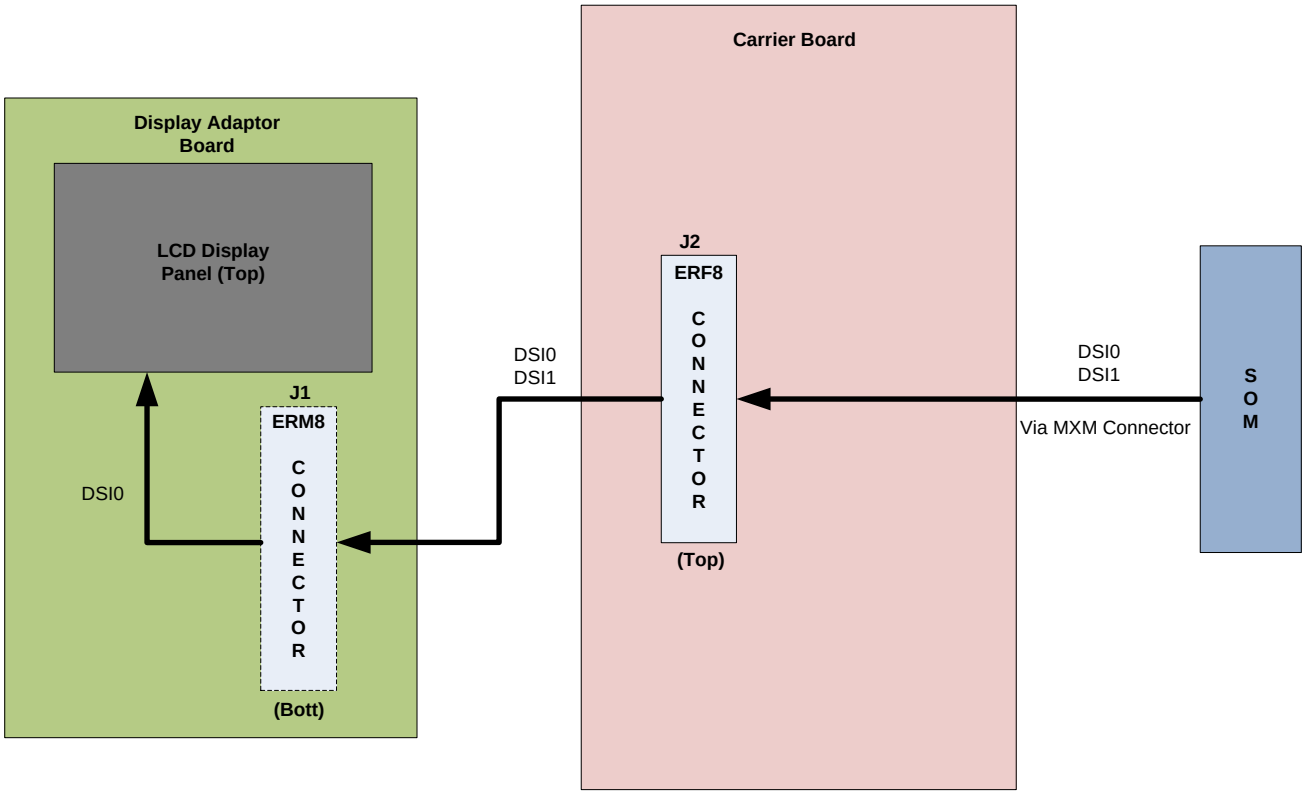

Figure 20 Display Board Default Configuration

3.8.17.1 LCD display panel

The LCD panel comes preinstalled on the Intrinsyc Open-Q 820 display adaptor board (P/N# 280-0100). Below are the Panel specifications:

- **Resolution:** 480x854
- **LCD Type:** IPS
- PCAP touch panel with cover glass
- **No of Lanes:** 1 x 2 lane MIPI DSI interface via Display Board.
- **Diagonal Length**: 4.5”
- Contact sales@intrinsyc.com for more information

Note: **The display above when mounted on the Intrinsyc Open-Q 820 Display Adapter is meant to work with the carrier board. Altering the use of this LCD panel is not recommended.**

3.8.18 PCI Express 1X Slot J30

The PCI Express slot J30 used on the Open-Q 820™ µSOM development kit is a standard PC style half card slot. It allows for external peripheral connectivity such as Gigabit Ethernet, Gigabit Wi-Fi, PCIe based audio / video processors etc. Since there is no native Ethernet connectivity on the Open-Q platform, an off-the shelf PCIe based Ethernet card can be used here. Please check the software compatibility before connecting the PCIe Ethernet card. In addition to being able to establish external connectivity, the connector provides access to the PCIE2 interface which is being routed out from the µSOM.

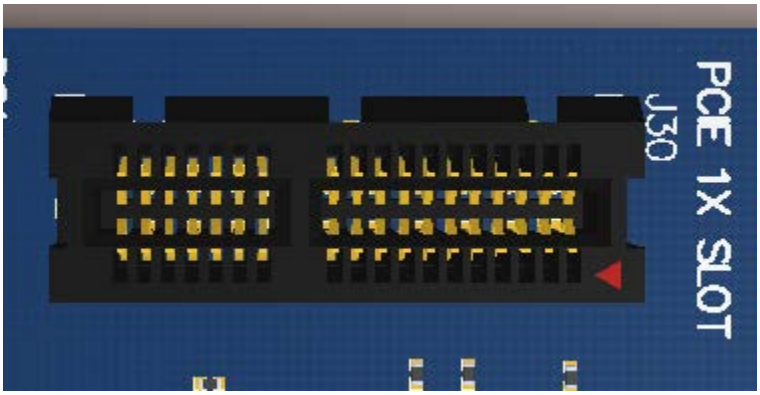

Figure 21 J30 PCIe Connector

- PCI slot power specification
  - Supports half card only
  - Supports 10W card via PSU
  - Supports 25W card via ATX PSU

Power Rail	Low Power	High Power
3.3 V ± 9%	3 A Max	3A Max
12 V ± 8%	0.5 A Max	2.1 A max
3.3 Vaux ± 9%	375mA Max	375mA Max

- PCIe card Mechanical Specifications:
  - Card length:
    - Half card: 6.6” (167.65mm)
    - Full size card: > 7.0” (177.8mm) (This will not support mini ITX)
  - Card height:
    - Standard: 4.2” (106.7mm)
    - Low profile: 2.536” (64.4mm)

3.8.19 Mini PCI Express Connector J72

The Open-Q 820 µSOM development kit also supports the use of a PCI Express mini card. The primary difference between a PCI Express 1X card and a PCI Express mini card is the unique form factor optimized for mobile computing platforms. In addition to that, the mini card is optimized for communication applications. Similarly, the PCI Express mini card allows for external peripheral connectivity such as Ethernet and wireless connectivity as well as acting like a modem.

The Mini PCI Express connector J72 used on the Open-Q 820 µSOM development kit supports both the standard full and half size PCI Express mini card. Depending on the size of card used, user can utilize the 4 mounting holes below connector J72 to secure the card in place. The figure below depicts these mounting holes. Please check the software compatibility before connecting any PCI Express mini cards.

Note: The pin-outs of this connector comply with the PCI Express mini card standards. Please refer to the document in the following link for more information: https://www.pcisig.com/specifications/pciexpress/base/#mini1.2

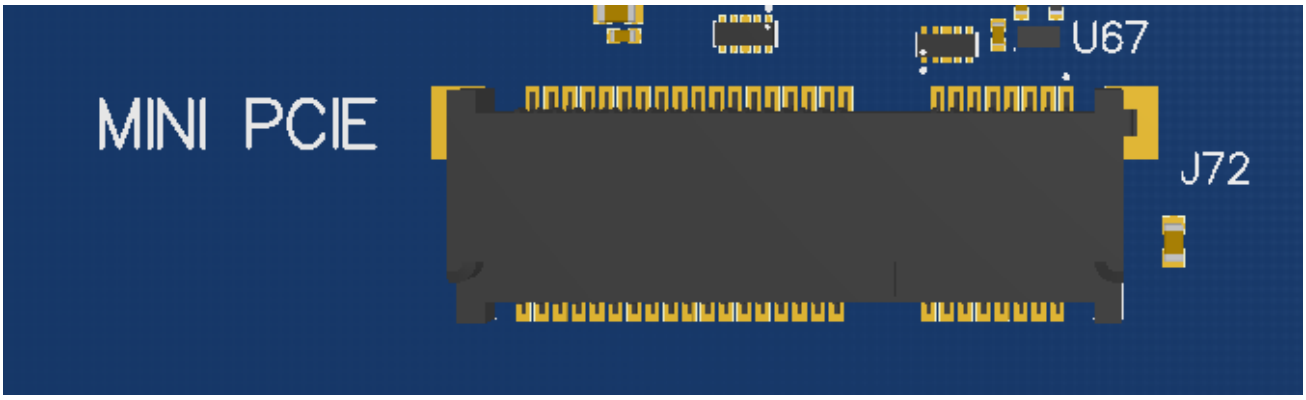

Figure 22 J72 Mini PCIe Connector

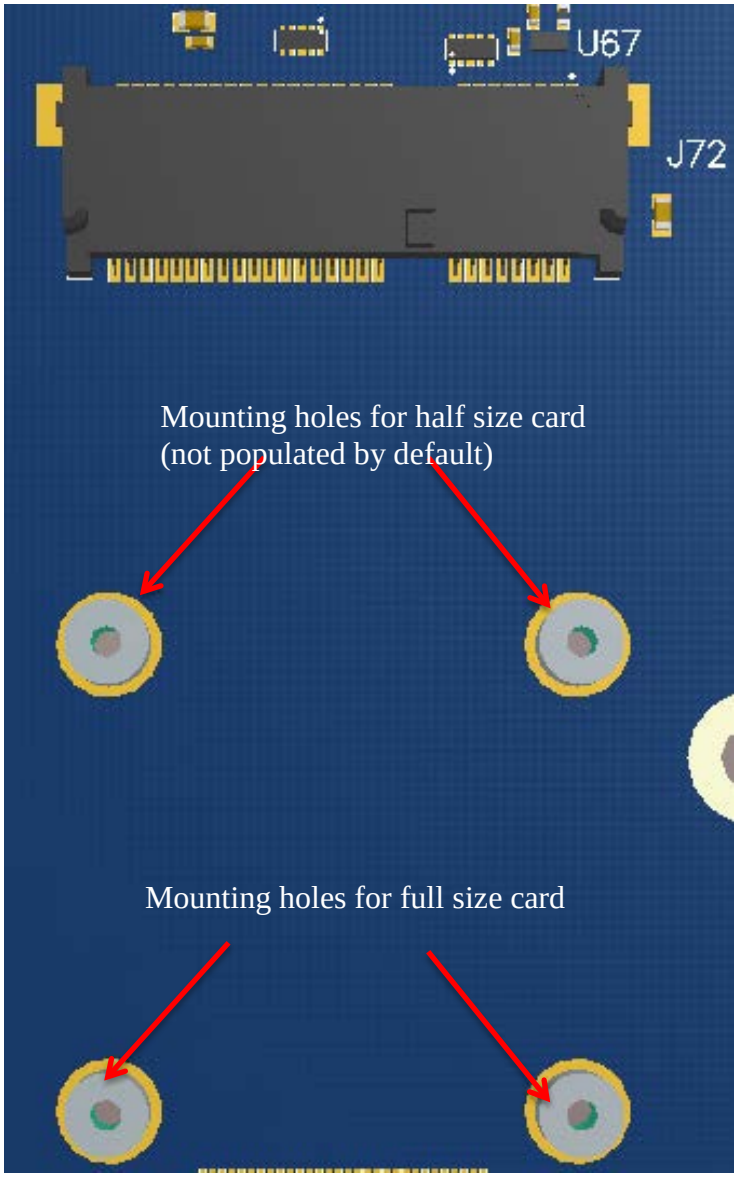

Figure 23 Mounting holes for Mini PCIe Connector

3.8.20 Camera Connectors

The Open-Q 820™ µSOM development kit supports three 4-lane MIPI CSI camera interfaces via three separate JAE 41-pin connectors.

The following are some features of the camera connectors:

- 3 x 4 lane MIPI CSI signals
- No support for integrated flash driver
- Support for 3D camera configuration
- Separate I2C control (CCI0, CCI1)

- Supports all CSI interfaces
- All camera CSI connectors are on the carrier board edge
- Self-regulated camera modules can be powered with 3.3V power (MB_VREG_3P3)
- Uses JAE FI-RE41S-VF connector for exposing MIPI, CLK, GPIOs and Power rails.
- Please use JAE FI-RE41S-HF to mate with the camera connectors on the carrier board

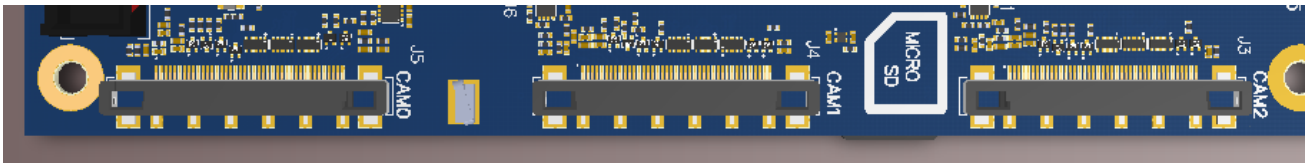

Figure 24 Camera Connectors (J5, J4, J3)

The figure above shows the three MIPI CAM0 (J5), CAM1 (J4) and CAM2 (J3) connectors. The table below outlines the pin outs of these connectors

Table 3.8.20-1. MIPI CSI Camera Connector Pinouts (J5,J4,J3)

Pin#	CAM0 (J5)	CAM1 (J4)	CAM2 (J3)	Description
1, 2, 3	MB_VREG_3P3	MB_VREG_3P3	MB_VREG_3P3	Power output. Connected to main +3.3V MB_VREG_3P3 max current 700mA
4	GND	GND	GND	Ground
5	VREG_L17A_2P8	VREG_L18A_2P8	VREG_L29A_2P8	Power output. Connected to PM8996 VREG_L17A/ L18A/ L29 regulator. Default is +2.8V. Maximum current 300mA
6	MB_ELDO_CAM0_ DVDD	MB_ELDO_CAM1_D VDD	MB_ELDO_CAM2_DV DD	Power output. Connected to U5, U6, and U71 AMS LDO regulator. Default is +1.2V. Maximum current 1A
7, 8	VREG_L23A_2P8	MB_ELDO_CAM1_V CM/ VREG_L23A_2P8 (DNP)	VREG_L23A_2P8	Power output. Connected to PM8996 VREG_L23A regulator. Default is +2.8V. Maximum current 300mA. For CAM1 J4, U10 is used. Default is 2.8V and maximum current is 300mA
9, 10	VREG_LVS1A_1P8	VREG_LVS1A_1P8	VREG_LVS1A_1P8	Power output. Connected to PM8996 VREG_LVS1A switch output. Default is +1.8V. Maximum current 300mA
11	GND	GND	GND	Ground
12	FLASH_STROBE_E N (APQ_GPIO22)	FLASH_STROBE_E N (DNP) (APQ_GPIO22) Install R36 to access signal	FLASH_STROBE_EN (DNP) (APQ_GPIO22) Install R42 to access signal	Output. Connected to APQ8096 Default use is for camera flash strobe enable

Pin#	CAM0 (J5)	CAM1 (J4)	CAM2 (J3)	Description
13	CAM0_RST_N (APQ_GPIO25)	CAM1_RST_N (APQ_GPIO104)	CAM2_RST_N (APQ_GPIO23)	Output. Connected to APQ8096 GPIO25 / GPIO104 / GPIO23. Default use is for camera reset
14	CAM0_STANDBY_N (APQ_GPIO26)	CAM1_STANDBY_N (APQ_GPIO98)	CAM2_STANDBY_N (APQ_GPIO133)	Output. Connected to APQ8096 GPIO26 / GPIO98 / GPIO133. Default use is for camera standby
15	CCI_I2C_SCL0 (APQ_GPIO18)	CCI_I2C_SCL0 (APQ_GPIO18)	CCI_I2C_SCL0 (APQ_GPIO18)	Output. Connected to APQ8096 GPIO18. Default use is for camera CCI0 I2C clock interface
16	CCI_I2C_SDA0 (APQ_GPIO17)	CCI_I2C_SDA0 (APQ_GPIO17)	CCI_I2C_SDA0 (APQ_GPIO17)	Input / output. Connected to APQ8096 GPIO17. Default use is for camera CCI0 I2C data interface
17	CAM_MCLK0_BUF (APQ_GPIO13)	CAM_MCLK1_BUF (APQ_GPIO14)	CAM_MCLK2_BUF (APQ_GPIO15)	Output. Connected to APQ8096 GPIO13 / GPIO14 / GPIO15. Default use is for camera master clock. Maximum 24MHz
18	FLASH_STROBE_TRIG (APQ_GPIO22)	FLASH_STROBE_TRIG (DNP) (APQ_GPIO22) Install R37 to access signal	FLASH_STROBE_TRIG (DNP) (APQ_GPIO22) Install R43 to access signal	Output. Connected to APQ8096 GPIO25. Default use is for camera flash strobe trigger
19	GND	GND	GND	Ground
20	MIPI_CSI0_LANE0_N	MIPI_CSI1_LANE0_N	MIPI_CSI2_LANE0_N	Input. MIPI CSI0 / CSI1 / CSI2 data lane 0
21	MIPI_CSI0_LANE0_P	MIPI_CSI1_LANE0_P	MIPI_CSI2_LANE0_P	Input. MIPI CSI0 / CSI1 / CSI2 data lane 0
22	GND	GND	GND	Ground
23	MIPI_CSI0_CLK_N	MIPI_CSI1_CLK_N	MIPI_CSI2_CLK_N	Input. MIPI CSI0 / CSI1 / CSI2 clock lane
24	MIPI_CSI0_CLK_P	MIPI_CSI1_CLK_P	MIPI_CSI2_CLK_P	Input. MIPI CSI0 / CSI1 / CSI2 clock lane
25	GND	GND	GND	Ground
26	MIPI_CSI0_LANE1_N	MIPI_CSI1_LANE1_N	MIPI_CSI2_LANE1_N	Input. MIPI CSI0 / CSI1 / CSI2 data lane 1
27	MIPI_CSI0_LANE1_P	MIPI_CSI1_LANE1_P	MIPI_CSI2_LANE1_P	Input. MIPI CSI0 / CSI1 / CSI2 data lane 1
28	GND	GND	GND	Ground
29	MIPI_CSI0_LANE2_N	MIPI_CSI1_LANE2_N	MIPI_CSI2_LANE2_N	Input. MIPI CSI0 / CSI1 / CSI2 data lane 2
30	MIPI_CSI0_LANE2_P	MIPI_CSI1_LANE2_P	MIPI_CSI2_LANE2_P	Input. MIPI CSI0 / CSI1 / CSI2 data lane 2
31	GND	GND	GND	Ground
32	MIPI_CSI0_LANE3_P	MIPI_CSI1_LANE3_P	MIPI_CSI2_LANE3_P	Input. MIPI CSI0 / CSI1 / CSI2 data lane 3
33	MIPI_CSI0_LANE3_N	MIPI_CSI1_LANE3_N	MIPI_CSI2_LANE3_N	Input. MIPI CSI0 / CSI1 / CSI2 data lane 3
34	GND	GND	GND	Ground
35	CCI_I2C_SDA1 (APQ_GPIO19)	CCI_I2C_SDA1 (APQ_GPIO19)	CCI_I2C_SDA1 (APQ_GPIO19)	Output / Input. Connected to APQ8096 GPIO19. Default

Pin#	CAM0 (J5)	CAM1 (J4)	CAM2 (J3)	Description
				use is for camera CCI1 I2C data interface
36	CCI_I2C_SCL1 (APQ_GPIO20)	CCI_I2C_SCL1 (APQ_GPIO20)	CCI_I2C_SCL1 (APQ_GPIO20)	Output. Connected to APQ8096 GPIO20. Default use is for camera CCI1 I2C clock interface
37	CAM_IRQ (APQ_GPIO24)	CAM_IRQ (DNP) (APQ_GPIO24) Install R40 to access signal	CAM_IRQ (DNP) (APQ_GPIO24) Install R46 to access signal	Input. Connected to APQ8096 GPIO24. CAM_IRQ signal
38	CAM0_MCLK3 (APQ_GPIO13)	CAM1_MCLK3 (APQ_GPIO13)	CAM2_MCLK3 (APQ_GPIO13)	Output. Connected to APQ8096 GPIO13. Default N/C. Use is for secondary camera master clock. Maximum 24MHz
39	MB_ELDO_CAM0_ DVDD	MB_ELDO_CAM1_D VDD	MB_ELDO_CAM2_DV DD	Power output. Connected to U5, U6, and U71 AMS LDO regulator. Default is +1.2V. Maximum current 500mA
40, 41	MB_VREG_5P0 (DNP) Install R10 to access rail	MB_VREG_5P0 Install R28 to access rail	MB_VREG_5P0 Install R35 to access rail	Power output. 5V Power supply. Maximum 700mA

Note: A connection from the camera connectors on the carrier board to the Intrinsyc camera adapter board is established by a 41-pin cable assembly from JAE Electronics (part number JF08R0R041020MA)

The following table shows the combinations of camera usage for different use cases

Table 3.8.20-2. MIPI CSI Camera Use Cases

CSI PHY	Use case	Comment
CSI0	Up to 4 lane	One Camera of 4 lane or One camera of 3 lane One Camera of 2 lane One Camera of 1 lane
CSI 1	Up to 4 lane	One Camera of 4 lane or One camera of 3 lane One Camera of 2 lane One Camera of 1 lane
CSI 2	Up to 4 lane	One Camera of 4 lane or 2 x Camera of 1 lane each
CSI0 + CSI1	Up to 4 lane 3D	4 lane 3D use case / Dual 4 lane configuration
CSI 2	Up to 1 lane 3D	1 lane 3D use case / Dual 1 lane configuration
CSI0 + CSI1 + CSI2	Up to 4 lane	Three 4-lane CSI (4+4+4 or 4+4+2+1)
CPHY		Three 3-trio CPHY1.0

3.8.21 Power Header via 20 Pin Connector J60

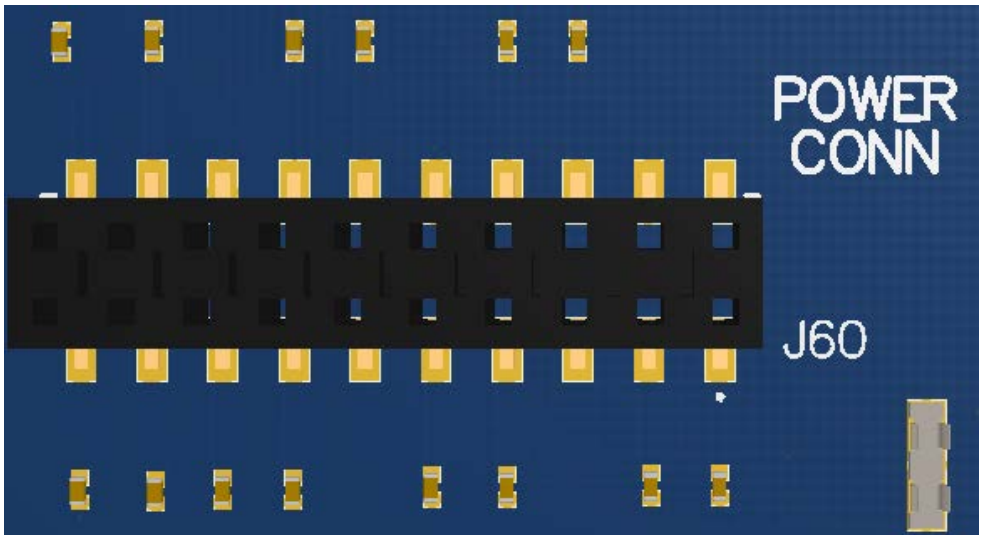

Figure 25 J60 Power Connector

- For providing camera connectors with additional current than what is originally supported by on board regulators. This is to mitigate the effect of high resistance and IR drop on flat cables which can violate camera sensor requirements for high performance cameras
- It is recommended to use this when high performance (high mega pixels) cameras are being used. Usually high-performance cameras require more power
- Can also be used as a general power header if user would like to use voltage rails brought out by connector

Description	Signal	Pin NO	Description	Signal	Pin NO
1.05V power rail for camera 0	MB_ELDO_CAM0_DVDD	J60[1]	2.85V power rail for camera 0 (AVDD)	VREG_L17A_2P8	J60[2]
2.8V power rail for camera 0, 2 (VDD)	VREG_L23A_2P8	J60[3]	GND	GND	J60[4]
GND	GND	J60[5]	3.3V power rail for camera 0, 1, 2	MB_VREG_3P3	J60[6]
1.05V power rail for camera 1	MB_ELDO_CAM1_DVDD	J60[7]	2.85V power rail for camera 1 (AVDD)	VREG_L18A_2P85	J60[8]
2.8V power rail for camera 1	MB_ELDO_CAM1_VCM	J60[9]	GND	GND	J60[10]

Description	Signal	Pin NO	Description	Signal	Pin NO
(VDD)					
GND	GND	J60[11]	3.3V power rail for camera 0, 1, 2	MB_VREG_3P3	J60[12]
1.05V power rail for camera 2	MB_ELDO_CAM2_DVDD	J53[13]	2.85V power rail for camera 2 (AVDD)	VREG_L29A_2P8	J60[14]
2.8V power rail for camera 0, 2 (VDD)	VREG_L23A_2P8	J53[15]	GND	GND	J60[16]
1.8V power rail for camera 0, 1, 2	VREG_LVS1A_1P8	J60[17]	3.3V power rail for camera 0, 1, 2	MB_VREG_3P3	J60[18]
5V power rail for camera 0, 1, 2	MB_VREG_5P0	J60[19]	12V power rail for camera 0, 1, 2	DC_IN_12V	J60[20]

3.8.22 Ethernet AVB Expansion Header J73

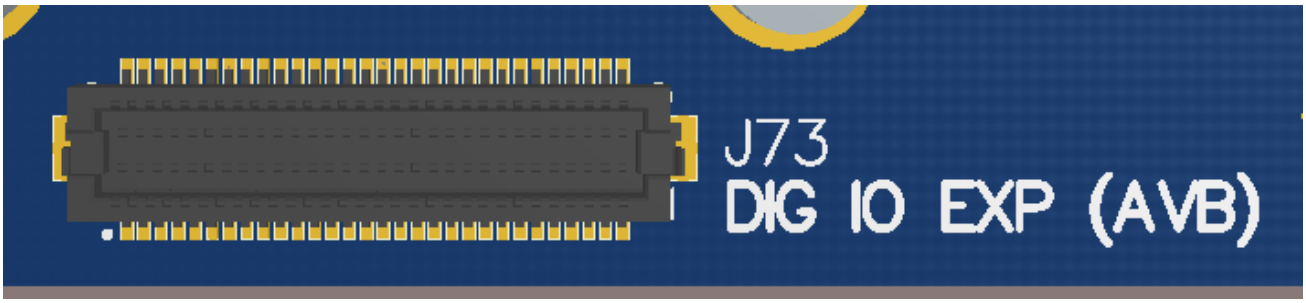

Figure 26 J73 Ethernet AVB Expansion Header

This header is used for interfacing with automotive peripherals via Ethernet AVB standard. Note that this is used for Intrinsyc internal testing and is not supported.

3.8.23 VIP Expansion Header J71

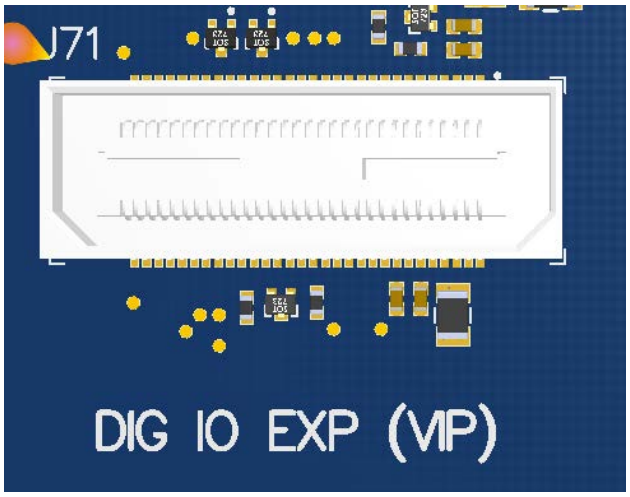

Figure 27 J71 VIP Expansion Header

This header is used for interfacing with Qualcomm® legacy automotive VIP boards. Note that this is for Intrinsyc internal testing and is not supported.

3.8.24 USB 2.0 Client Port Operation

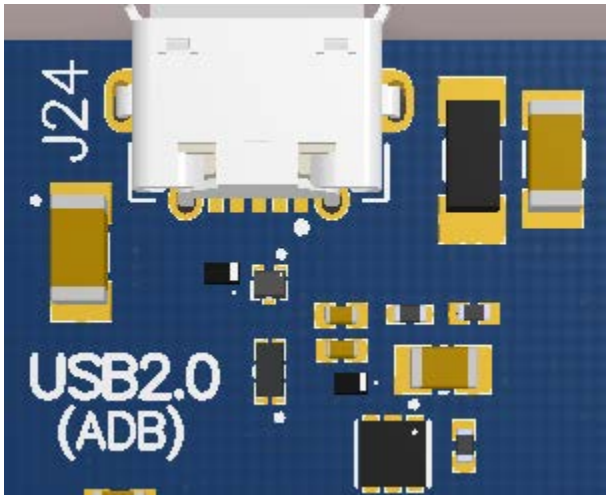

Figure 28 J24 USB2.0 for ADB

J24 allows the development kit to communicate with a host PC using the Android Debug Bridge (ADB). This port is a client mode port only and can be used simultaneously with the USB3.0 SuperSpeed ports.

3.8.25 USB 2.0 Interface Operation

Figure 29 J85 USB1 Connector

J85 allows the development kit to communicate with a host PC using Qualcomm® Flash Image Loader (QFIL) tool set. QFIL is used to download a software image to the development kit.
To access this port, switch S1 position 2 needs to be set to the on position. Switch S1 is in the off position by default.

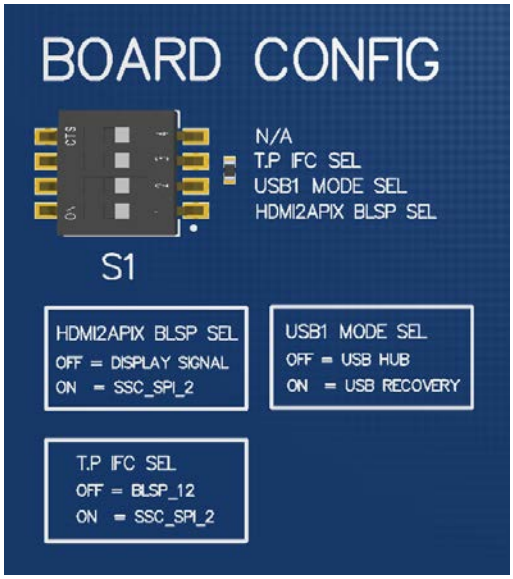

Figure 30 S1 Board Configuration Switch (on Bottom of Development Kit)

3.8.26 USB 3.0 Interface Operation

Figure 31 J23 USB3.0 Host Ports

J23 allows the development kit to communicate as a SuperSpeed host. This is a dual stacked USB3.0 Type-A connector. To access these ports, the switch S1 position 2 needs to be set to the off position.

Two additional USB3.0 SuperSpeed ports are located on header J2600. This header allows an end user to design their own daughter card with additional USB ports. In addition to that, this header can be used with the Akasa dual USB3.0 PCI slow connector with 19-pin connector (P/N# AK-CBUB17-40BK).

Note that this header only consists of 19 pins.

Similar to the connector J23, switch S1 position 2 needs to be set to the off position.

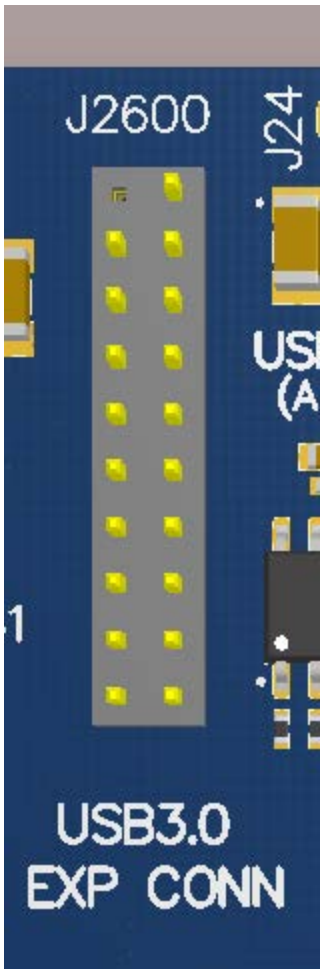

Figure 32 J2600 USB3.0 Expansion Connector