Qualcomm

Qualcomm Technologies, Inc.

WSA8810/WSA8815 Class-D Smart Speaker Amplifier

Device Specification

LM80-P2751-28 Rev. A

February 12, 2018

Questions or comments: https://www.96boards.org/product/dragonboard820c/

Qualcomm Technologies, Inc.
5775 Morehouse Drive
San Diego, CA 92121
U.S.A.

Device description

WSA8810 is a class-D smart speaker amplifier and WSA8815 is a high-output power class-D smart speaker amplifier. They both support multimedia solutions, including the WCD9335 audio codec of the APQ8096 chipset. Their primary operating mode uses a SoundWire digital audio interface, but they also support an analog audio input supplemented by I2C status and control.

One WSA is used for mono speaker configurations; a second is added to support stereo configurations. This flexibility allows cost optimization for both configurations. Standalone speaker amplifiers allows them to be placed near the speakers (potentially far from the codec), providing key performance advantages:

- Better temperature sensor accuracy
- Shorter routing lengths – lower voltage drop and reduced EMI susceptibility

Major functional blocks for WSA8810 and WSA8815:

- Analog core – Class-D smart speaker amplifier
- Digital core – SoundWire for digital audio and I2C for control
- Fully integrated multilevel boost SMPS – high voltage, high power applications, multiple boost output levels. (Smart boost feature is available in the SoundWire mode).
- Support circuits – temperature and battery monitors

This 2.24 × 2.63 mm device is supplemented by an audio codec (such as the WCD9335) to create an audio solution that provides flexibility (output power level, mono or stereo) while reducing part count and PCB area.

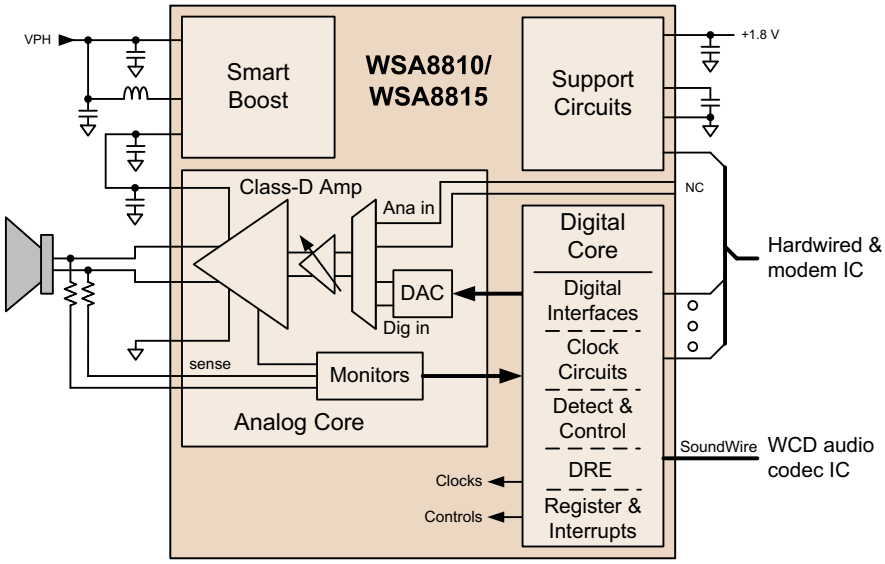
See Chapter 9 for complete functional details.

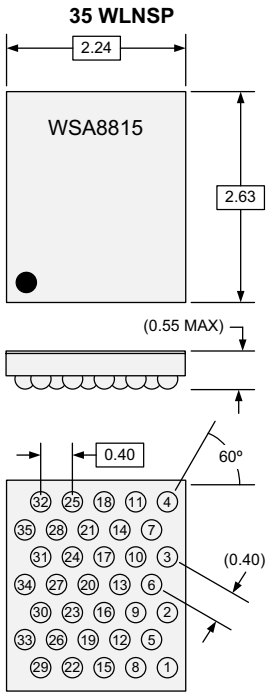
Summary of key features

- Single speaker amplifier; add second for stereo support
  - Flexible solution for configuration, cost, and layout optimizations
- Supports digital SoundWire and analog audio inputs
- Current and voltage sensing for speaker protection
- Up to 2 W (WSA8810) and 4 W (WSA8815) audio output power into 8 Ω
  - WSA8810 and WSA8815 support stereo application
- Temperature sensor for IC over-temp protection and speaker protection
- On-chip multilevel boost SMPS for high voltage, high power applications; bypass mode for lower power
- Single CMOS die in the 2.24 × 2.63 × 0.55 mm 35-pad wafer-level nanoscale package (35 WLNSP)

See Section 1.2 for a complete list of features.

WSA8810/WSA8815 High-level block diagram and package type





Supply voltage summary

Two supplies are required:

- Primary phone power (VPH_PWR or VBAT)
- Regulated 1.8 V from power management

On-chip smart boost SMPS for high-power audio

Revision history

Revision	Date	Description
A	February 2018	Initial release

Contents

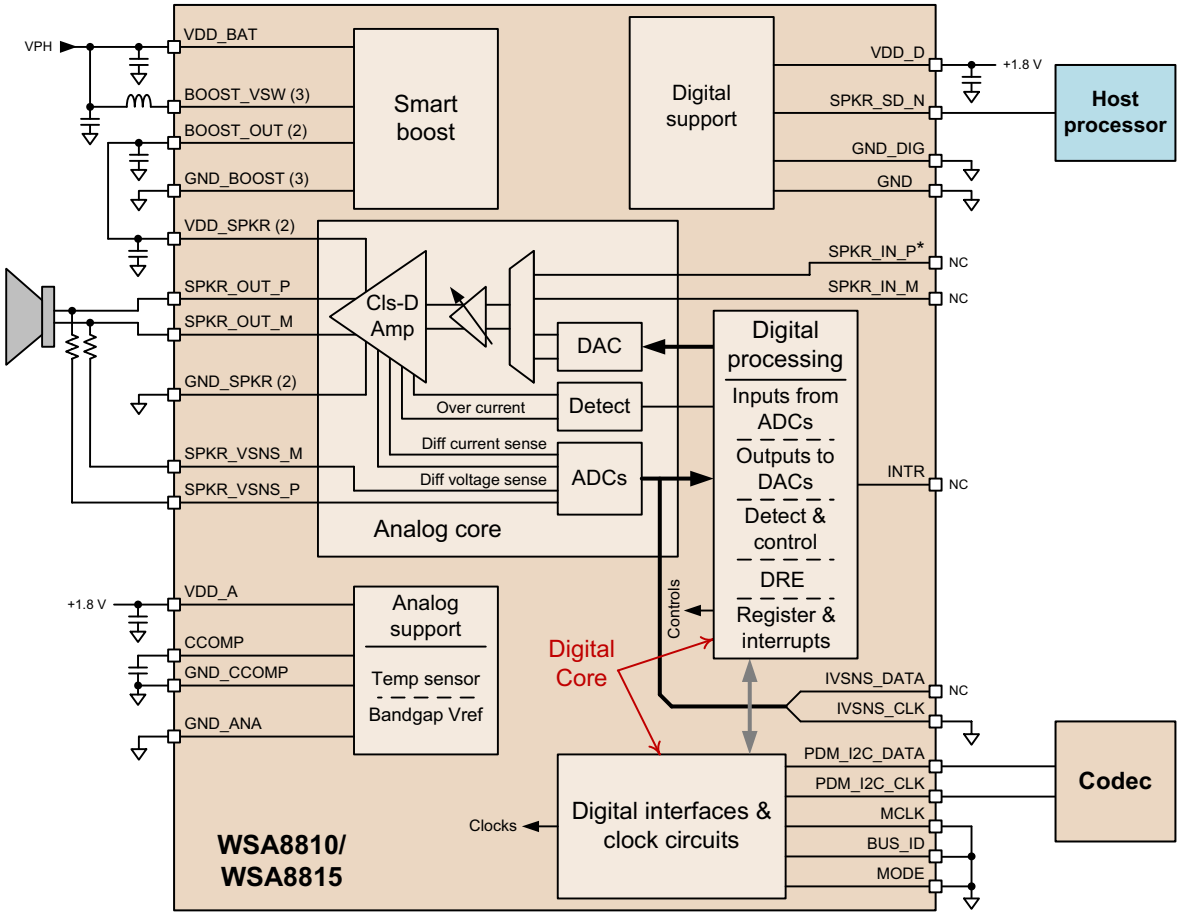
Figures

Tables

1 Introduction

NOTE This document provides a description of chipset capabilities. Not all features are available, nor are all features supported in the software. Enabling some features may require additional licensing fees.

1.1 Detailed functional block diagram



* Using SPKR_IN for analog test mode. DragonBoard 820c supports Soundwire mode only.

Figure 1-1 WSA8810/WSA8815 detailed functional block diagram

1.2 Features

Feature	WSA8810/WSA8815 capabilities
SoundWire digital audio	New digital audio interface supporting bi-directional audio and control
Test (analog) mode	Analog input for audio I2C for status & control
Current and voltage sensing	Supports excursion and temperature control feedback speaker protection
High audio output power	2.0 W (WSA8810) and 4.0 W (WSA8815) into 8 Ω operating off +4.2 V with 1% THD
Speaker load impedance	4, 6, and 8 Ω
Frequency response	20 Hz to 20 kHz
Low THD	0.01% when delivering 1.2 W into 8 Ω
Dynamic range enhancement	Yes, SoundWire mode only
Combination earpiece driver	Yes
Temperature sensor	IC over-temp protection and speaker protection
Multilevel boost	For high voltage, high power applications Bypass boost output for higher efficiency at lower operating points Multilevel smart boost feature for higher boost efficiency available in SoundWire mode
Output current	Protects from amplifier damage in speaker short circuit failure mode
Interrupts	Overcurrent and overtemperature ■ Conveyed through the SoundWire interface during SoundWire mode ■ Dedicated pad (INTR) for analog mode
Analog gain adjustments	0 to 13.5 dB (WSA8810) and 18 dB (WSA8815) in 1.5 steps
Small, thermally efficient package	35 WLNSP: 2.24 × 2.63 × 0.55 mm

2 Pad definitions

2.1 I/O parameter definitions

WSA8810 and WSA8815 are available in the 35 WLNSP; a high-level view of the pad assignments is shown in Figure 2-1.

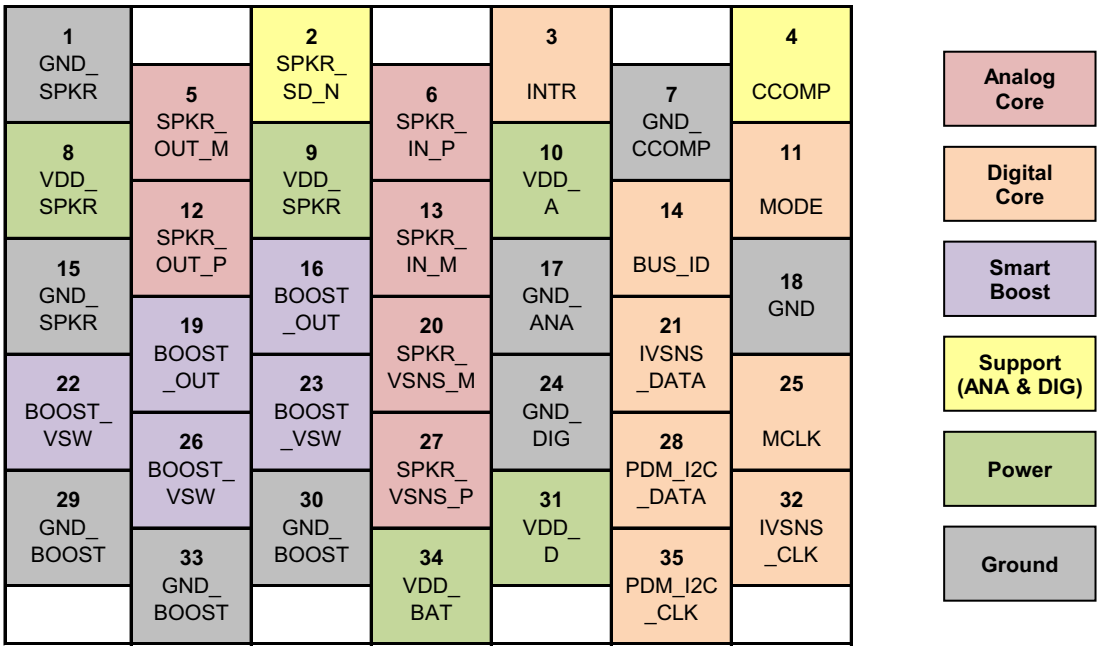


Figure 2-1 Pad assignments for WSA8810 and WSA8815 (top view)

2.2 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input
AO	Analog output
DI	Digital input (CMOS)
DO	Digital output (CMOS)
Pad voltages for digital I/Os	
DIO	Digital I/Os supply (VDD_D = 1.8 V)

2.3 Pad descriptions

Descriptions of all pads are presented in the following tables, organized by functional group:

Table 2-2 Analog core

Table 2-3 Digital core

Table 2-4 Smart boost

Table 2-5 Support functions (analog and digital)

Table 2-6 Power supply pads

Table 2-7 Ground pads

Table 2-2 Pad descriptions – analog core

Pad #	Pad name	Pad type [1]	Functional description
6	SPKR_IN_P	AI	Speaker amplifier input For test mode only; leave open for normal operations.
13	SPKR_IN_M	AI	Speaker amplifier input
12	SPKR_OUT_P	AO	Speaker amplifier output, plus
5	SPKR_OUT_M	AO	Speaker amplifier output, minus
27	SPKR_VSNS_P	AI	Speaker voltage sense node, plus
20	SPKR_VSNS_M	AI	Speaker voltage sense node, minus

1. See Table 2-1 for parameter and acronym definitions.

Table 2-3 Pad descriptions – digital core

Pad #	Pad name	Pad type [1]	Functional description
35	PDM_I2C_CLK	DI	Soundwire clock or analog (I2C) mode clock
28	PDM_I2C_DATA	DI, DO	Soundwire data or analog (I2C) mode data
25	MCLK	DI	Master clock from WCD for analog mode; GND for SoundWire mode
14	BUS_ID	DI	Bus ID that sets left or right amplifier for stereo configuration (two WSA ICs) ■ Low (GND) = left speaker ■ High (VDD) = right speaker ■ Use Low (GND) for mono configuration
11	MODE	DI	Mode control ■ Low (GND) = SoundWire mode ■ High (VDD) = Analog mode
3	INTR	DO	Interrupt to Host processor for analog mode that signals over-temperature and over-current; leave open for SoundWire mode (NC)
21	IVSNS_DATA	DO	Current and voltage sense ADC data to WCD DMIC_DATA pad for analog mode; leave open for SoundWire mode (NC)
32	IVSNS_CLK	DI	Current and voltage sense ADC clock from WCD DMIC_CLK pad for analog mode; GND for SoundWire mode

1. See Table 2-1 for parameter and acronym definitions.

Table 2-4 Pad descriptions – smart boost

Pad #	Pad name	Pad type [1]	Functional description
22, 23, 26	BOOST_VSW	PI, PO	Boost SMPS switching node
16, 19	BOOST_OUT	PO	Boost SMPS output

1. See Table 2-1 for parameter and acronym definitions.

Table 2-5 Pad descriptions – support functions (analog & digital)

Pad #	Pad name	Pad type [1]	Functional description
Analog			
4	CCOMP	AO	Bandgap reference circuit compensation capacitor
Digital			
2	SPKR_SD_N	DI	WSA shutdown control from host IC

1. See Table 2-1 for parameter and acronym definitions.

Table 2-6 Pad descriptions – power supply pads

Pad #	Pad name	Functional description
10	VDD_A	Power for analog circuits
34	VDD_BAT	Power for smart boost SMPS circuits
31	VDD_D	Power for digital circuits
8, 9	VDD_SPKR	Power for speaker amplifier high power output stages

Table 2-7 Pad descriptions – ground pads

Pad #	Pad name	Functional description
17	GND_ANA	Ground for analog circuits
29, 30, 33	GND_BOOST	Ground for smart boost SMPS circuits
7	GND_CCOMP	Ground for bandgap reference compensation capacitor
18	GND	
24	GND_DIG	Ground for digital circuits
1, 15	GND_SPKR	Ground for speaker amplifier high power output stages

3 Electrical specifications

3.1 Absolute maximum ratings

The absolute maximum ratings (Table 3-1) reflect the stress levels that, if exceeded, cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating conditions defined within Section 3.2.

Table 3-1 Absolute maximum ratings

Parameter		Min	Max	Units
Power supply voltages				
VDD_A	Power for analog circuits	-0.3	+2.0	V
VDD_BAT	Power for smart boost SMPS circuits	-0.3	+6.0	V
VDD_D	Power for digital circuits	-0.3	+2.0	V
VDD_SPKR	Power for speaker amplifier high power output stages	-0.3	+6.5 (WSA8810) +10.5 (WSA8815)	V
Signal pads				
V_IN	Voltage on any nonpower supply pad [1]	-0.3	V_{XX} + 0.3	V
ESD protection and thermal conditions – see Section 7.1				
Continuous power dissipation	T_A = +70 °C, multilayer board, see Thermal characteristics	–	1.9	W

1. V_{XX} is the supply voltage associated with the input or output pad to which the test voltage is applied.

3.2 Operating conditions

Operating conditions include parameters that are under the control of the design team: power supply voltage, power distribution impedances, and thermal conditions (Table 3-2). WSA8810 and WSA8815 meet all the performance specifications listed in Section 3.3.1 through Section 3.6, when used within the operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

Table 3-2 Operating conditions

Parameter		Min	Typ	Max	Units
Power supply voltages					
VDD_A	Power for analog circuits	1.71	1.80	1.89	V

Table 3-2 Operating conditions (cont.)

Parameter		Min	Typ	Max	Units
VDD_BAT	Power for smart boost SMPS circuits	3.00	3.60	5.50	V
VDD_D	Power for digital circuits	1.71	1.80	1.89	V
VDD_SPKR	Power for speaker amplifier high power output stages	3.00	–	6.00 (WSA8810) 9.5 (WSA8815)	V
Thermal conditions					
T_C	Operating temperature (case)	-30	25	85	°C
T_D	Device temperature	-30	25	150	°C

3.3 DC power characteristics

3.3.1 Power consumption

Table 3-3 Quiescent current at VDD_BAT for SoundWire mode

Use case	VBAT = 3.0 V (mA)	VBAT = 3.6 V (mA)	VBAT = 4.2 V (mA)
MCLK = 9.6 MHz, 300 kHz PA carrier frequency	4.18	4.85	5.53
MCLK = 12.288 MHz, 300 kHz PA carrier frequency	4.24	4.93	5.63

Table 3-4 Power consumption for typical use cases

Use case	Test condition	Typical current (uA)			Total power (µW)
		VDD_BAT	VDD_A	VDD_D	
Reset	WSA in reset (SPKR_SD_N = 0); VDD_BAT=3.6 V	0.1	0.05	0.05	0.54

3.4 Digital logic characteristics

The WSA8810/WA8815 digital I/O characteristics such as voltage levels, current levels, and capacitance are specified in Table 3-5. All digital I/Os connect with the digital support circuits.

Table 3-5 SoundWire mode – SoundWire interface

Parameter		Comments	Min	Typ	Max	Units
V_{IH}	High-level input voltage	–	0.65 × VDD_D	–	VDD_D	V
V_{IL}	Low-level input voltage	–	0	–	0.35 × VDD_D	V
V_{OH}	High-level output voltage	–	0.8 × VDD_D	–	VDD_D	V
V_{OL}	Low-level output voltage	–	0	–	0.2 × VDD_D	V
C_{IN}	Input capacitance [1]	–	–	–	3	pF

1. Input capacitance is guaranteed by design, but is not 100% tested.

Table 3-6 Analog mode – I2C interface

Parameter		Comments	Min	Typ	Max	Units
V_{IH}	High-level input voltage	–	0.7 × VDD_D	–	VDD_D	V
V_{IL}	Low-level input voltage	–	0	–	0.3 × VDD_D	V
V_{OL}	Low-level output voltage	–	0	–	0.2 × VDD_D	V
C_{IN}	Input capacitance [1]	–	–	–	3	pF

1. Input capacitance is guaranteed by design, but is not 100% tested.

3.5 Smart speaker amplifier performance

Table 3-7 (for WSA8810) and Table 3-8 (for WSA8815) specifies the smart speaker amplifier performance with its boost mode enabled in both analog and SoundWire modes unless otherwise stated.

Table 3-7 Smart speaker amplifier performance specifications for WSA8810

Parameter	Comments	Min	Typ	Max	Units
Output power [1]	1 kHz tone, 12 dB gain				
	4.2 V VBAT, 8 Ω load [2], ≤ 1% THD + N	–	2.00	–	W
	3.6 V VBAT, 8 Ω load, ≤ 1% THD + N	–	2.00	–	W
	3.0 V VBAT, 8 Ω load, ≤ 1% THD + N	–	2.00	–	W
	4.2 V VBAT, 4 Ω load [3], ≤ 1% THD + N	–	3.65	–	W
	3.6 V VBAT, 4 Ω load, ≤ 1% THD + N	–	3.65	–	W
	3.0 V VBAT, 4 Ω load, ≤ 1% THD + N	–	3.30	–	W
Output noise	SoundWire mode: A-weighted, PDM signal mute, DRE on, 300 kHz PA carrier frequency, VBAT ≥ 3.6 V	–	12.8	–	µVrms
	SoundWire mode: A-weighted, PDM signal mute, DRE on, 300 kHz PA carrier frequency, VBAT = 3.0 V	–	14.8	–	µVrms
Gain steps	10 steps at 1.5 dB steps each	0	–	13.5	dB
Gain accuracy	Any 1.5 dB gain step, 1 kHz tone	-0.1	–	+0.1	dB
SNR	SoundWire mode: A-weighted, DRE on, 12 dB gain, 0 dBFS input, 300 kHz carrier frequency, VBAT ≥ 3.6 V	–	109	–	dB
Frequency response	-20 dBV, 13.5 dB gain				
	20 Hz to 20 kHz	-0.5	–	+0.5	dB
Efficiency, amplifier + boost SMPS	1 kHz tone				
	4.2 V VBAT, 8 Ω load, 2 W, 6 V boost	–	81.5	–	%
	4.2 V VBAT, 4 Ω load, 2 W, 6 V boost	–	78.0	–	%
	4.2 V VBAT, 8 Ω load, 1 W, 6 V boost	–	78.5	–	%
	4.2 V VBAT, 4 Ω load, 1 W, 6 V boost	–	76.0	–	%
	4.2 V VBAT, 8 Ω load, 0.1 W, boost bypass	–	74.0	–	%
	4.2 V VBAT, 4 Ω load, 0.1 W, boost bypass	–	72.0	–	%

Table 3-7 Smart speaker amplifier performance specifications for WSA8810 (cont.)

Parameter	Comments	Min	Typ	Max	Units
Level translation	0 dBV, 0 dB analog gain, 1 kHz tone, 8 Ω load	-0.5	0	+0.5	dBV
Click-and-pop (A-weighted)	A-weighted, turn on or turn off, VBAT = 3.6 V SoundWire mode	 –	 1	 5	 mVpp
Supported output load	–	3.2	–	–	Ω
Disable output impedance	SPKR_SD_N is low level	25	–	–	kΩ
Power supply ripple rejection	200 mVpp superimposed on VBAT, 0 dB gain, boost bypass At 217 Hz At 1 kHz At 10 kHz At 20 kHz	 – – – –	 86.0 85.0 70.5 60.5	 – – – –	 dB dB dB dB
Boost SMPS switching frequency	MCLK = 9.6 MHz MCLK = 12.288 MHz	– –	2.4 3.072	– –	MHz MHz
Other specifications					
Output DC offset	VBAT = 3.6 V, any gain, no input signal	-1	–	+1	mV
Thermal resistance from junction to ambient	In free air; natural convection 4-layer application board	– –	– 42	– –	– C/W

1. Any power number above 2 W is only for short term duration. See Section 10.3 for more information.
2. The 8 Ω load in Table 3-7 consists of 15 µH + 8 Ω + 15 µH.
3. The 4 Ω load in Table 3-7 consists of 15 µH + 4 Ω + 15 µH.

Table 3-8 Smart speaker amplifier performance specifications for WSA8815

Parameter	Comments	Min	Typ	Max	Units
Output power [1]	See Table 9-1 for the maximum boost level settings and gain selection, 1 kHz tone, ≤ 1% THD+N 8 Ω load [2], 4 A boost limit, 9 V boost, VDD_VBAT = 3.6 V 4 Ω load [3], 4 A boost limit, 7.5 V boost, VDD_VBAT = 3.6 V	 – –	 4.00 4.00	 – –	 W W
Output noise	SoundWire mode: A-weighted, PDM signal mute, 300 kHz PA carrier frequency, VBAT ≥ 3.6 V SoundWire mode: A-weighted, PDM signal mute, 300 kHz PA carrier frequency, VBAT = 3.0 V	– –	12.8 14.8	– –	µVrms µVrms
Gain steps	13 steps at 1.5 dB steps each	0	–	18	dB
Gain accuracy	Any 1.5 dB gain step, 1 kHz tone	-0.1	–	+0.1	dB
SNR	SoundWire mode: A-weighted, 15 dB gain, 0 dBFS input, 300 kHz carrier frequency, VBAT ≥ 3.6 V	–	112	–	dB
Frequency response	-20 dBV, 15 dB gain 20 Hz to 20 kHz	 -0.5	 –	 +0.5	 dB

Table 3-8 Smart speaker amplifier performance specifications for WSA8815 (cont.)

Parameter	Comments	Min	Typ	Max	Units
Efficiency, amplifier + boost SMPS	1 kHz tone				
	4.2 V VBAT, 8 Ω load, 4 W, 9.5 V boost output	–	76.0	–	%
	4.2 V VBAT, 4 Ω load, 4 W, 7.5 V boost output	–	75.5	–	%
	4.2 V VBAT, 8 Ω load, 1 W, 6 V boost	–	78.5	–	%
	4.2 V VBAT, 4 Ω load, 1 W, 6 V boost	–	76.0	–	%
	4.2 V VBAT, 8 Ω load, 0.1 W, boost bypass	–	74.0	–	%
	4.2 V VBAT, 4 Ω load, 0.1 W, boost bypass	–	72.0	–	%
Level translation	0 dBV, 0 dB analog gain, 1 kHz tone, 8 Ω load	-0.5	0	+0.5	dBV
Click-and-pop (A-weighted)	A-weighted, turn on or turn off, VBAT = 3.6 V				
	SoundWire mode	–	1	5	mVpp
Supported output load	–	3.2	–	–	Ω
Disable output impedance	SPKR_SD_N is low level	25	–	–	kΩ
Power supply ripple rejection	200 mVpp superimposed on VBAT, 0 dB gain, boost bypass				
	At 217 Hz	–	86.0	–	dB
	At 1 kHz	–	85.0	–	dB
	At 10 kHz	–	70.5	–	dB
	At 20 kHz	–	60.5	–	dB
Boost SMPS switching frequency	MCLK = 9.6 MHz	–	2.4	–	MHz
	MCLK = 12.288 MHz	–	3.072	–	MHz
Other specifications					
Output DC offset	VBAT = 3.6 V, any gain, no input signal	-1	–	+1	mV
Thermal resistance from junction to ambient	In free air; natural convection	–	–	–	–
	4-layer application board	–	42	–	C/W

1. See Section 10.3 for more information.
2. The 8 Ω load in Table 3-8 consists of 15 µH + 8 Ω + 15 µH.
3. The 4 Ω load in Table 3-8 consists of 15 µH + 4 Ω + 15 µH.

3.6 Digital I/Os and digital processing

3.6.1 SoundWire interface timing requirements

WSA8810/WSA8815 SoundWire PHY timing parameters in Table 3-9 and Table 3-10 are compliant to clock and data specifications as specified in the MIPI Alliance Specification for SoundWire Version 0.8, Revision 04.

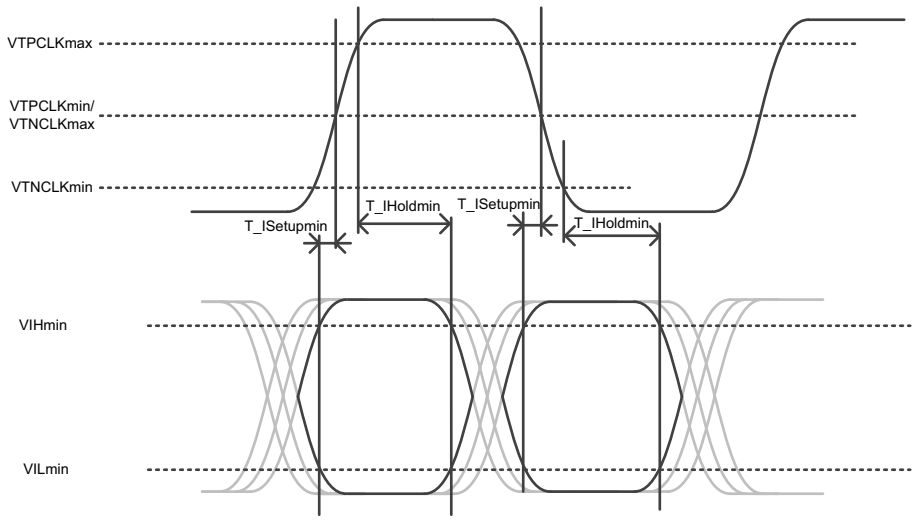


Figure 3-1 Received clock and data signals constraints

Table 3-9 Voltage and timing requirements for clock input and data input

Symbol	Parameter	Min	Max	Units
V_{TPCLK}	Voltage threshold for positive-going clock edges	0.9	1.17	V
V_{TNCLK}	Voltage threshold for negative-going clock edges	0.63	0.9	V
T_ISetupmin	Minimum setup time demanded by a data input prior to a positive or negative edge on clock input	–	0	ns
T_IHoldmin	Minimum hold time demanded by a data input after to a positive or negative edge on clock input	–	4	ns

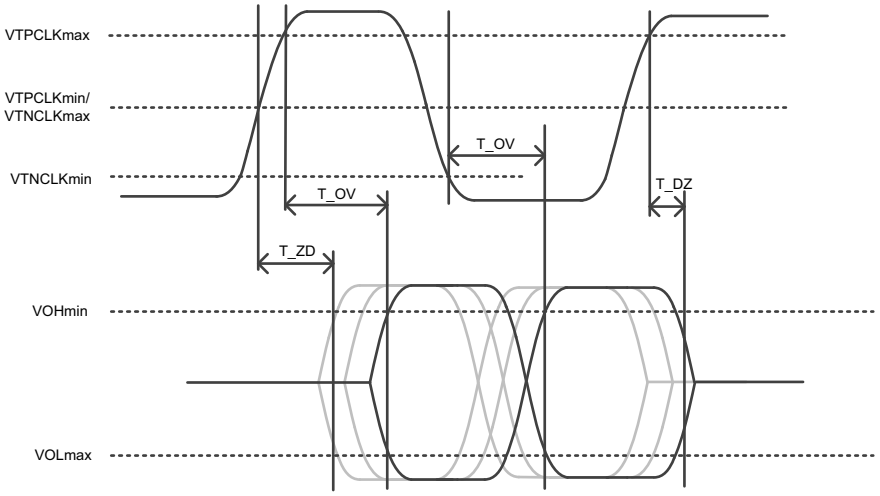


Figure 3-2 Received clock and output data signals constraints

Table 3-10 Voltage and timing requirements for clock input and data output

Symbol	Parameter	Min	Max	Units
T_OV	Time for data output to remain stable or valid after positive or negative edge on clock input	–	28	ns
T_ZD	Time to enable data output after positive or negative edge on clock input	7.9	–	ns
T_DZ	Time to disable data output after positive or negative edge on clock input	–	4	ns

3.6.2 Inter-integrated circuit (I2C)

Table 3-11 Supported I2C standards and exceptions

Applicable standards	Feature exceptions	WSA8810/WSA8815
I2C Specification, version 2.1, January 2000 (Philips Semiconductor document number 9398 393 40011)	■ Master mode ■ Maximum I2C clock frequency is 400 KHz ■ 3.3V signals	None

4 Mechanical information

4.1 Device physical dimensions

WSA8810/WSA8815 is available in the 35 WLNSP that includes dedicated ground pads for improved grounding, mechanical strength, and thermal continuity. The 35 WLNSP has a 2.24 mm by 2.63 mm body, with a maximum height of 0.55 mm. Pad 1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. A simplified version of the 35 WLNSP outline drawing is shown in Figure 4-1.

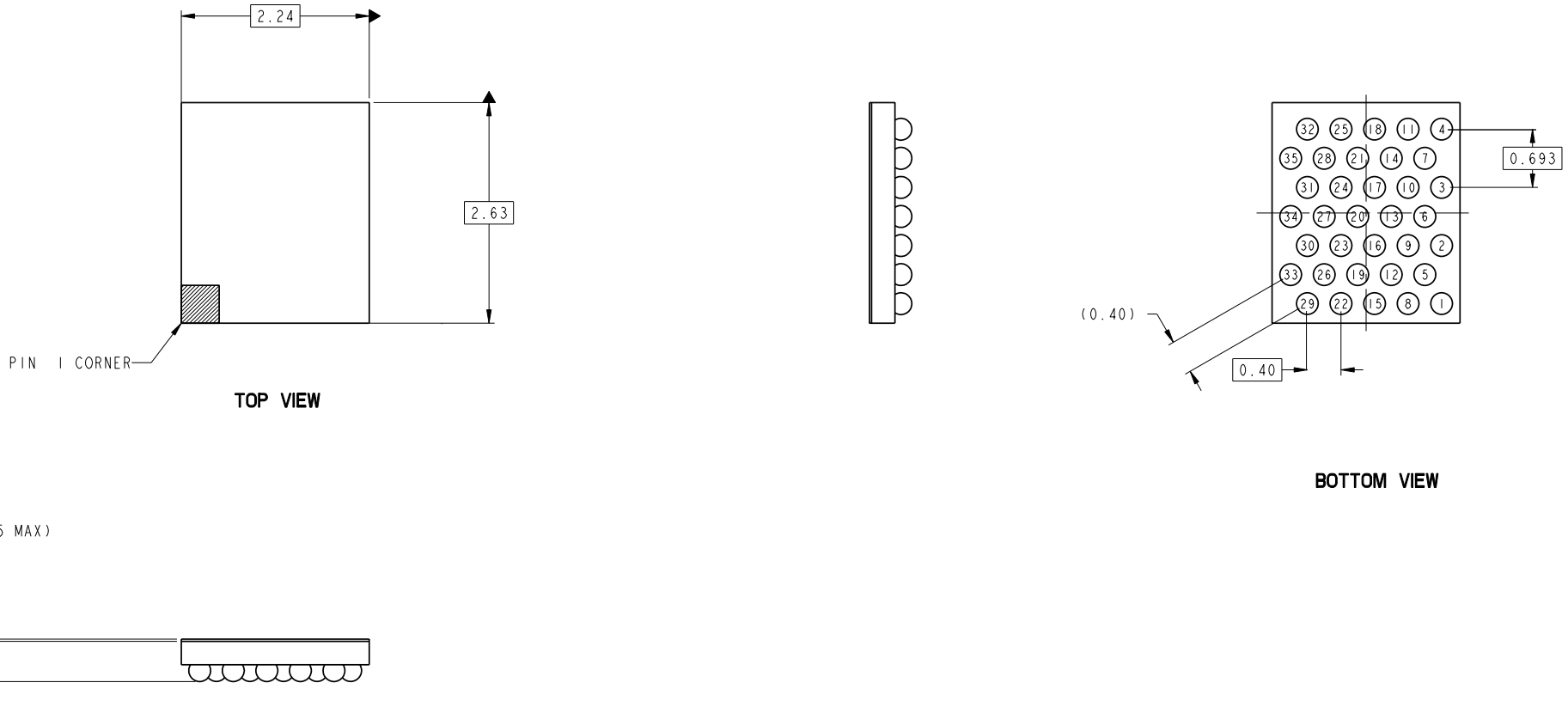


Figure 4-1 35 WLNSP (2.24 x 2.63 x 0.55 mm) outline drawing

4.2 Part marking

4.2.1 Specification-compliant devices

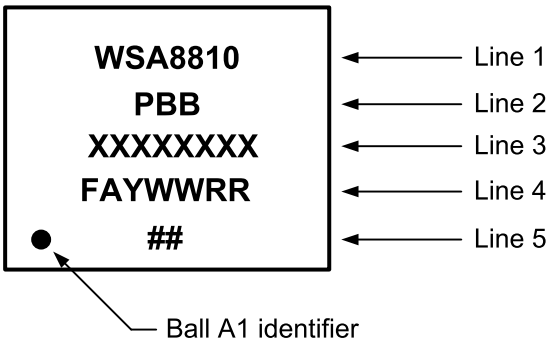


Figure 4-2 WSA8810 device marking (top view, not to scale)

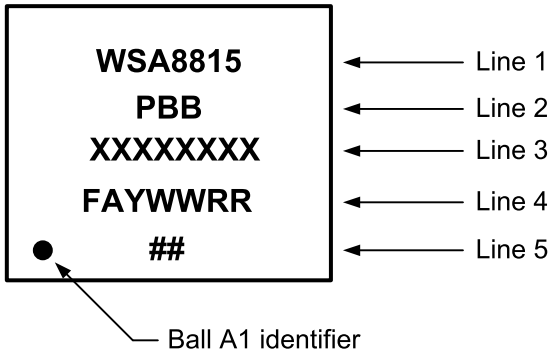


Figure 4-3 WSA8815 device marking (top view, not to scale)

Table 4-1 WSA8810/WSA8815 marking line definitions

Line	Marking	Description
1	WSA8810/ WSA8815	Qualcomm Technologies, Inc. (QTI) product name
2	PBB	P = product configuration code BB = feature code ■ VV
3	XXXXXXXX	XXXXXXXX = traceability number

Table 4-1 WSA8810/WSA8815 marking line definitions (cont.)

Line	Marking	Description
4	FAYWWRR	F = supply source code A = assembly site code Y = single-digit year WW = date code RR = product revision
5	● ##	● = dot identifying pad 1 location ## = traceability information **Note:** This line contains additional engineering information after the traceability information.

4.3 Device ordering information

4.3.1 Specification-compliant devices

This device can be ordered using the identification code in the following figures:

Device ID code ►	AAA-AAAA	— P	— CC	DDDDD	— EE	— RR	— S	— BB
Symbol definition ►	Product name	Config code	Number of pads	Package type	Shipping package	Product revision	Source code	Feature code
Example ►	WSA-8810	— 0	— 35	WLNSP	— TR	— 02	— 0	— VV
Feature code (BB) may not be included when identifying older devices. ↗								

Figure 4-4 WSA8810 device identification code

Device ID code ►	AAA-AAAA	— P	— CC	DDDDD	— EE	— RR	— S	— BB
Symbol definition ►	Product name	Config code	Number of pads	Package type	Shipping package	Product revision	Source code	Feature code
Example ►	WSA-8815	— 0	— 35	WLNSP	— TR	— 02	— 0	— VV
Feature code (BB) may not be included when identifying older devices. ↗								

Figure 4-5 WSA8815 device identification code

4.4 Device moisture sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. Moisture sensitivity level (MSL) of a package indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 4-2.

Table 4-2 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% RH, WSA8810/WSA8815 rating
2	1 year	≤ 30°C/60% RH
2a	4 weeks	≤ 30°C/60% RH
3	168 hours	≤ 30°C/60% RH
4	72 hours	≤ 30°C/60% RH
5	48 hours	≤ 30°C/60% RH
5a	24 hours	≤ 30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C/60% RH

The latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification is followed. ***The devices WSA8810 and WSA8815 are classified as MSL1; the qualification temperature was 255ºC + 5ºC/-0ºC.*** This qualification temperature (255°C + 5ºC/-0°C) must not be confused with the peak temperature within the recommended solder reflow profile; see Section 6.2.3 for more details.

Thermal characteristics

Rather than provide thermal resistance values θ_{JC} and θ_{JA}, validated thermal package models can be accessed from https://www.96boards.org/product/dragonboard820c/. Designers can extract thermal resistance values by conducting their own thermal simulations.

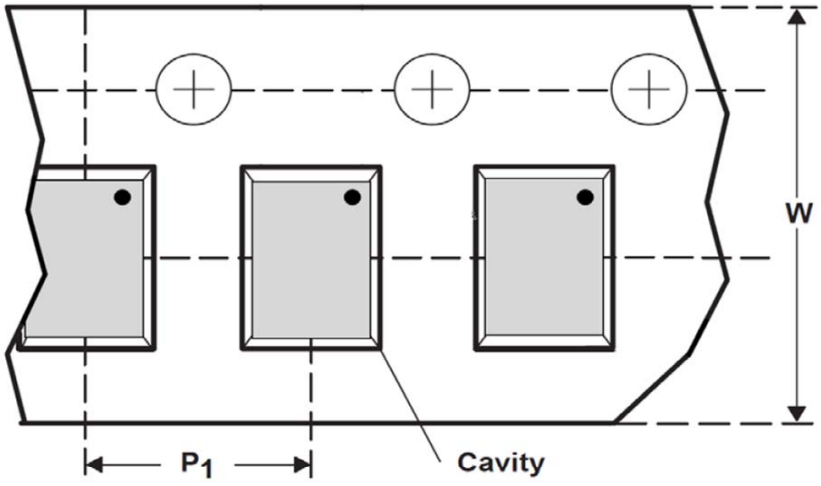
5 Carrier, storage, and handling information

5.1 Carrier

5.1.1 Tape and reel information

The tape carrier system conforms to EIA-481 standards.

A simplified sketch of the WSA8810/WSA8815 tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed: Single	Reel diameter: 178 mm	Tape width (W): 12 mm
Units per reel: 2000	Hub diameter: 55 mm	Pocket pitch (P1): 8 mm

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in Figure 5-2.

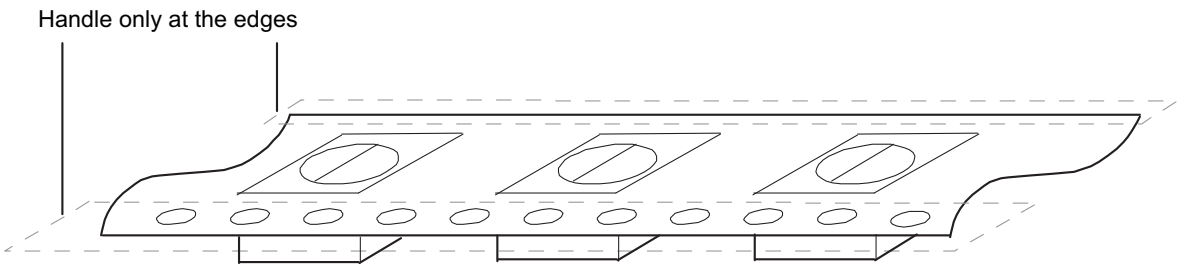


Figure 5-2 Tape handling

5.2 Storage

5.2.1 Bagged storage conditions

WSA8810/WSA8815 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags. See *IC Products Packing Method* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.4.

5.3 Handling

Tape handling was described in Section 5.1.1. Other (IC-specific) handling guidelines are explained in the following sections.

5.3.1 Baking

Wafer-level packages such as the 35 WLNSP must not be baked.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. Destructive damage can be expected if the discharge path is through a semiconductor device. ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

Products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*. See Section 7.1 for the WSA8810/WSA8815 ESD ratings.

6 PCB mounting guidelines

6.1 RoHS compliance

WSA8810/WSA8815 devices are lead-free and RoHS-compliant. Its SnAgCu solder balls use SAC405 composition. Lead-free (or Pb-free) semiconductor products are defined as having a maximum lead concentration of 1000 ppm (0.1% by weight) in raw (homogeneous) materials and end products.

6.2 SMT assembly guidelines

This section describes the board-level characterization process parameters. It is included to assist customers with their SMT process development; it is not intended to be a specification for their SMT processes.

6.2.1 Land pad and stencil design

The land pattern and stencil recommendations presented in this section are based on internal characterizations for lead-free solder pastes on an eight-layer PCB, built primarily to the specifications described in JEDEC JESD22-B111.

Prior to PCB production, characterization of the land patterns according to the processes, materials, equipment, stencil design, and reflow profile of each customer is recommended. Optimizing the solder stencil pattern design and print process is critical to ensure print uniformity, decrease voiding, and increase board-level reliability.

General land pattern guidelines:

- Non-solder mask defined (NSMD) pads provide the best reliability.
- Keep the solderable area consistent for each pad, especially when mixing via-in-pad and non-via-in-pad in the same array.
- Avoid large solder mask openings over ground planes.
- Traces for external routing are recommended to be less than or equal to half the pad diameter, to ensure consistent solder-joint shapes.

6.2.2 Reflow profile

Reflow profile conditions for lead-free systems are listed in Table 6-1, and are shown in Figure 6-1.

Table 6-1 Typical SMT reflow profile conditions (for reference only)

Profile stage	Description	Temperature range	Condition
Preheat	Initial ramp	< 150°C	3°C/sec max
Soak	Flux activation	150 to 190°C	60 to 75 sec
Ramp	Transition to liquidus (solder-paste melting point)	190 to 220°C	< 30 sec
Reflow	Time above liquidus	220 to 245°C [1]	50 to 70 sec
Cool down	Cool rate – ramp to ambient	< 220°C	6°C/sec max

1. During the reflow process, the recommended peak temperature is 245°C (minimum). This temperature must not be confused with the peak temperature reached during MSL testing, as described in Section 6.2.3.

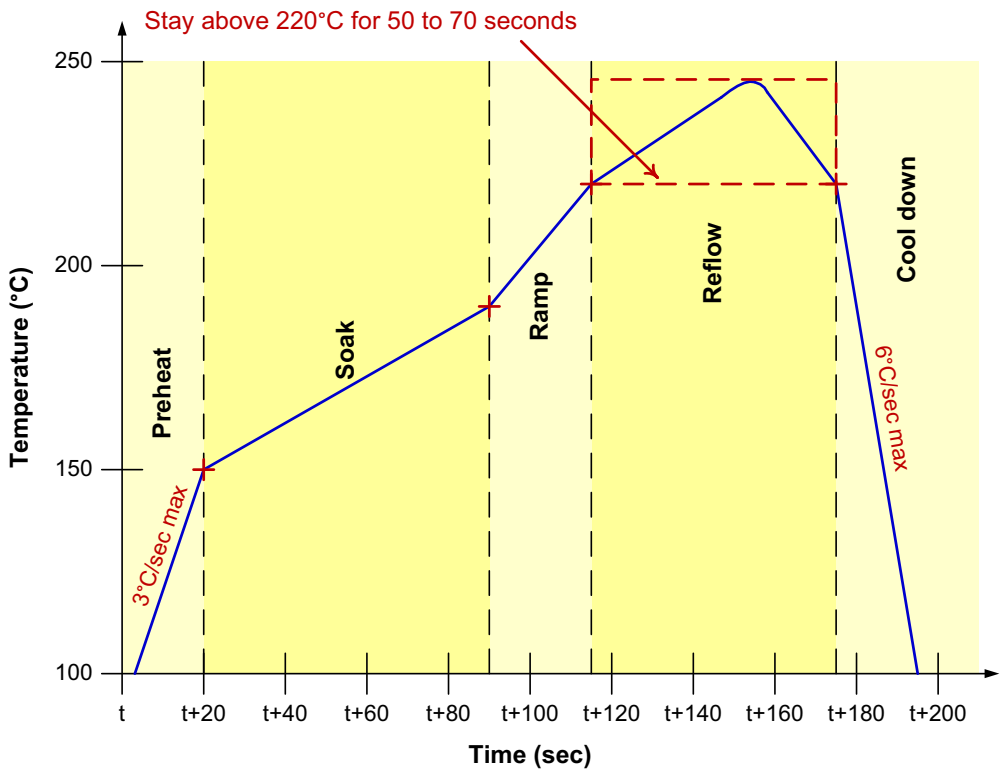


Figure 6-1 Typical SMT reflow profile

6.2.3 SMT peak package-body temperature

This document states a peak package-body temperature in three other sections within this document; without explanation, they appear to conflict. Following are the three sections along with an explanation of the stated value and its meaning within the context of that section.

- Section 4.4: Device moisture sensitivity level

  WSA8810/WSA8815 devices are classified as MSL1 at 255°C +5/-0°C. The temperature included in this designation is the lower limit of the range stated for moisture resistance testing during the device qualification process.

- Section 7.1: Reliability qualifications summary

  One of the tests conducted for device qualification is the moisture resistance test. As per J-STD-020-C, the reflow temperature hits a peak that falls within the range of 255°C +5/-0°C (255°C to 260°C).

- Section 6.2.2: Reflow profile

  During the reflow process of a production board, the temperature experienced by the package must be controlled. Obviously, the temperature must be high enough to melt the solder and provide reliable connections, but it must not go so high that the device can be damaged. The recommended peak temperature during production assembly is 245°C. This is comfortably above the solder melting point (220°C), yet well below the proven temperature reached during qualification (245°C or more).

6.2.4 SMT process verification

Verification of SMT process prior to high volume board assembly is recommended, including:

- In-line solder-paste deposition monitoring
- Reflow profile measurement and verification
- Visual and x-ray inspection after soldering to confirm adequate alignment, solder voids, solder-ball shape, and solder bridging
- Cross-section inspection of solder joints for wetting, solder-ball shape, and voiding

6.3 Board-level reliability

Characterization tests to assess the board-level reliability of the device should be conducted to verify the following tests on evaluation boards:

- Drop shock (JESD22-B111)
- Temperature cycling (JESD22-A104)
- Cyclic bend testing: optional (JESD22-B113)

7 Device reliability

7.1 Reliability qualifications summary

Table 7-1 Silicon reliability results – SMIC

Tests, standards, and conditions	Sample size	Results
ELFR in DPPM HTOL: JESD22-A108-A (Total samples from three different wafer lots)	320	Passed DPPM < 1000 [1]
HTOL in FIT (λ) failure in billion device hours HTOL: JESD22-A108-A (Total samples from three different wafer lots)	320	Passed FIT < 50 [1]
Mean time to failure (MTTF) t = 1/λ in million hours (Total samples from three different wafer lots)	320	Passed MTTF > 20 [1]
ESD: HBM rating JESD22-A114-F Target 2000 V (Total samples from one wafer lot)	3	2000 V
ESD: CDM rating JESD22-C101-D Target 500 V (Total samples from one wafer lot)	3	500 V
Latch-up (I-test): EIA/JESD-78A Trigger current: ±100 mA Temperature: 85°C (Total samples from one wafer lot)	6	Passed
Latch-up (V-supply over voltage): EIA/JESD-78A Trigger voltage: each VDD pad, stress at 1.5 × VDD maximum per the device specification Temperature: 85°C (Total samples from one wafer lot)	6	Passed

1. The cumulative DPPM, FIT, and MTTF values are based on multiple products.

Table 7-2 Package reliability results –SMIC

Tests, standards, and conditions	AST	ATC	SCS	SPIL	Results
Moisture resistance test (MRT): J-STD-020C Reflow at 260 +0/-5°C Total samples from three different assembly lots	693	693	693	693	Passed [1]
Temperature cycle: JESD22-A104-D Temperature: -55°C to 125°C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8-10 minutes Cycle rate: 2 cycles per hour (CPH) **Preconditioning**: JESD22-A113-F MSL 1, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots	231	231	231	231	Passed [1]
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96 hours duration OR 110°C/85% RH and 264 hours duration Preconditioning: JESD22-A113-F MSL 1, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots	231	231	231	231	Passed [1]
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 96 hours duration OR 110°C/85% RH and 264 hours duration Preconditioning: JESD22-A113-F MSL 1, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots	96	96	96	96	Passed [1]
High-temperature storage life: JESD22-A103-C Temperature: 150°C, 500, 1000 hours Total samples from three different assembly lots	231	231	231	231	Passed [1]
Flammability UL-STD-94 **Note**: Flammability test - not required WSA8810 and WSA8815 devices are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which these devices mounted are rated V-0 (better than V-1).	–	–	–	–	N/A
Physical dimensions: JESD22-B100-A Case outline drawing: QTI internal document (Total samples from three different assembly lots at each SAT)	30	30	30	30	Passed [1]

1. Data is bridged from other previously qualified 3L-WLP packages that are larger than this configuration.

8 Hardware register descriptions

NOTE Some registers are intentionally excluded from this chapter. OEMs must not change these excluded registers from their default values in the baseline software release.

0x000 WSA_DIGITAL_CHIP_ID0

Type: Read only

Reset state: 0x00

Bits	Name	Description
7:0	BYTE_0	Chip ID

0x001 WSA_DIGITAL_CHIP_ID1

Type: Read only

Reset state: 0x01

Bits	Name	Description
7:0	BYTE_1	Chip ID

0x002 WSA_DIGITAL_CHIP_ID2

Type: Read only

Reset state: 0x00

Bits	Name	Description
7:0	BYTE_2	Chip ID 0x01: WSA8810/WSA8815

0x003 WSA_DIGITAL_CHIP_ID3

Type: Read only

Reset state: 0x02

Bits	Name	Description
7:0	BYTE_3	Chip ID

0x004 WSA_DIGITAL_BUS_ID

Type: Read only

Reset state: 0x00

Bits	Name	Description
7:1	RESERVED	
0	BUS_ID	0: Left 1: Right

0x006 WSA_DIGITAL_CDC_TOP_CLK_CTL

Type: Read/write

Reset state: 0x03

Bits	Name	Description
7:2	RESERVED	
1	D_MCLK_EN	Specifies MCLK enable 0: Disable 1: Enable
0	D_SCLK_EN	Specifies SCLK enable 0: Disable 1: Enable

0x007 WSA_DIGITAL_CDC_ANA_CLK_CTL

Type: Read/write

Reset state: 0x00

Bits	Name	Description
7:1	RESERVED	
0	A_CDC_SCLK_EN	Specifies SCLK clock gating signal 0: Disable 1: Enable

0x009 WSA_DIGITAL_CLOCK_CONFIG

Type: Read/write

Reset state: 0x00

Bits	Name	Description
7:4	RESERVED	
3	SCLK_DIV2_EN	0x0: Bypass 0x1: SCLK_DIV2
2:0	CLOCK_CONFIG	MCLK: 0x0: CK_4P8M 0x1: CK_9P6M 0x2: CK_19P2M 0x4: CK_6P144M 0x5: CK_12P288M 0x6: CK_24P576M

0x00A WSA_DIGITAL_ANA_CTL

Type: Read/write

Reset state: 0x08

Bits	Name	Description
7:4	RESERVED	
3	OFFSET_CAL_DONE_EN	0: Disable 1: Enable
2	BOOST_VALUE_EN	0: Disable 1: Enable
1:0	BOOST_VALUE	0x0: Bypass 0x1: V_6V (WSA8810 only) 0x1: V_5P5V (WSA8815 only) 0x2: V_7P5V (WSA8815 only) 0x3: V_9P5V (WSA8815 only)

0x010 WSA_DIGITAL_TEMP_DETECT_CTL

Type: Read/write

Reset state: 0x01

Bits	Name	Description
7:1	RESERVED	
0	TEMP_DETECT_EN	0: Disable 1: Enable

0x013 WSA_DIGITAL_TEMP_CONFIG0

Type: Read/write

Reset state: 0x00

Bits	Name	Description
7:6	RESERVED	
5:4	CTL_THRD_WAR2DIS	Configure the temperature threshold from warning to disable in three steps 0x0: D140 0x1: D145 0x2: D150
3	Reserved	
2:0	CTL_THRD_SAF2WAR	Configure the temperature threshold from safe to warning in eight steps 0x0: D110 0x1: D115 0x2: D120 0x3: D125 0x4: D130 0x5: D135 0x6: D140 0x7: D145

0x014 WSA_DIGITAL_TEMP_CONFIG1

Type: Read/write

Reset state: 0x00

Bits	Name	Description
7:3	Reserved	
2:0	CTL_THRD_WAR2SAF	Configure the temperature threshold from safe to warning in eight steps 0x0: D100 0x1: D105 0x2: D110 0x3: D115 0x4: D120 0x5: D125 0x6: D130 0x7: D135

0x020 WSA_DIGITAL_INTR_MODE

Type: Read/write

Reset state: 0x00

Bits	Name	Description
7:1	RESERVED	
0	INT_POLARITY	0: LEVEL_HIGH 1: LEVEL_LOW

0x021 WSA_DIGITAL_INTR_MASK

Type: Read/write

Reset state: 0x1B

Bits	Name	Description
7:5	RESERVED	
4:0	VAL	Control interrupts. See Table 8-1 for the interrupt map.

Table 8-1 Interrupt map

Register	Bit position	Source
INRT_*	4	Clip interrupt
	3	Over-current protection
	2	Warning to disable interrupt
	1	Warning to safe interrupt
	0	Safe to warning interrupt

0x022 WSA_DIGITAL_INTR_STATUS

Type: Read only

Reset state: 0x00

Bits	Name	Description
7:5	RESERVED	
4:0	VAL	Provides status of interrupts. See Table 8-1 for the interrupt map.

0x023 WSA_DIGITAL_INTR_CLEAR

Type: Read/write

Reset state: 0x00

Writing ‘0’ to this register has no effect. Writing ‘1’ clears the corresponding interrupt status.

Bits	Name	Description
7:5	RESERVED	
4:0	VAL	Clear corresponding interrupt status. See Table 8-1 for the interrupt map.

0x024 WSA_DIGITAL_INTR_LEVEL

Type: Read/write

Reset state: 0x00

This register controls whether an interrupt must be treated as an edge or a level interrupt.

- Edge interrupts are monitored for low-to-high transitions and must be glitch free.
- Level interrupts are monitored for the signal level. The interrupt condition is considered active until it is either explicitly or implicitly removed.

Bits	Name	Description
7:5	RESERVED	
4:0	VAL	Interrupt level set. See Table 8-1 for the interrupt map.

0x025 WSA_DIGITAL_INTR_SET

Type: Read/write

Reset state: 0x00

Bits	Name	Description
7:5	RESERVED	
4:0	VAL	Interrupt set. See Table 8-1 for the interrupt map.

0x026 WSA_DIGITAL_INTR_TEST

Type: Read/write

Reset state: 0x00

This provide interrupt test functionality for the software. When set, it bypasses the hardware interrupt sources and passes the INTR_SET value to the interrupt status.

Bits	Name	Description
7:5	RESERVED	
4:0	VAL	Bypass interrupt. See Table 8-1 for the interrupt map.

0x044 WSA_DIGITAL_SAMPLE_EDGE_SEL

Type: Read/write

Reset state: 0x0C

Bits	Name	Description
7:4	RESERVED	
3	ISENSE	0: RISING_EDGE 1: FALLING_EDGE
2	VSENSE	0: RISING_EDGE 1: FALLING_EDGE
1	TS_DOUT_READY	0: RISING_EDGE 1: FALLING_EDGE
0	TS_DOUT	0: RISING_EDGE 1: FALLING_EDGE

0x100 WSA_ANALOG_BIAS_REF_CTRL

Type: Read/write

Reset state: 0x6C

Bits	Name	Description
7	RESRV	Reserved
6	DC_STARTUP_EN	0: Disable 1: Enable
5	DC_STARTUP_HOLD	0: Disable 1: Enable
4	TRAN_STARTUP_EN_CORE	0: Disable 1: Enable
3	TRAN_STARTUP_EN_PTAT	0: Disable 1: Enable
2:0	VBG_PRG	0x0: V1P221 (-) 0x1: V1P227 (-) 0x2: V1P233 (-) 0x3: V1P239 (-) 0x4: V1P245 (-) 0x5: V1P251 (-) 0x6: V1P257 (-) 0x7: V1P263 (-)

0x103 WSA_ANALOG_TEMP_OP

Type: Read/write

Reset state: 0x00

Bits	Name	Description
7:6	MCLK_DIVIDER	0x0: MCLK_DIV_1 0x1: MCLK_DIV_2 0x2: Disable 0x3: MCLK_DIV_4
5:4	RESERVED	
3	BG_EN	0: Disable 1: Enable
2	TEMP_EN	0: Disable 1: Enable
1:0	TEMP_FREQ	0x0: F_2K 0x1: F_1K 0x2: F_500 0x3: F_250

0x109 WSA_ANALOG_TEMP_ADC_CTRL

Type: Read/write

Reset state: 0x03

Bits	Name	Description
7	VBAT_EN	0: Disable 1: Enable
6:4	VBAT_FREQ	- 3 kHz (temperature sense off) 0x0: F_2KHZ 0x1: F_1KHZ 0x2: F_500HZ 0x3: F_250HZ 0x4: F_3KHZ
3	RESERVED	
2	TEMP_FREQ_MSB	- 3 kHz (VBAT sense forced off) 0: F_3KHZ 1: F_2KHZ
1:0	RESERVED	

0x11A WSA_ANALOG_SPKR_DRV_EN

Type: Read/write

Reset state: 0x74

Bits	Name	Description
7	CLASSD_PA_EN	0: Disable 1: Enable
6	INT1_EN	0: Disable 1: Enable
5	INT2_EN	0: Disable 1: Enable
4	INT_LDO_EN	0: Disable 1: Enable
3	INT_LDO_VOUT	0: V_5P0 1: V_5P5
2	INT_COMP_EN	0: Disable 1: Enable
1	INT_VLIM_EN	0: Disable 1: Enable
0	AUXIN_EN	0: Disable 1: Enable

0x11B WSA_ANALOG_SPKR_DRV_GAIN

Type: Read/write

Reset state: 0xC1

Bits	Name	Description
7:4	PA_GAIN	0x0: G_18DB (WSA8815 only) 0x1: G_16P5DB (WSA8815 only) 0x2: G_15DB (WSA8815 only) 0x3: G_13P5DB 0x4: G_12DB 0x5: G_10P5DB 0x6: G_9DB 0x7: G_7P5DB 0x8: G_6DB 0x9: G_4P5DB 0xA: G_3DB 0xB: G_1P5DB 0xC: G_0DB
3	PA_GAIN_SEL	0: DRE 1: Register
2	CLASSD_PWM_FREQ	0: F_300_KHZ 1: F_600_KHZ
1	VLASS_PWM_FREQ_DIV	0: DIV_BY_8 1: DIV_BY_10
0	RDAC_CLK_SEL	0: ANALOG_CLK 1: DIGITAL_CLK

0x11C WSA_ANALOG_SPKR_DAC_CTL

Type: Read/write

Reset state: 0x42

Bits	Name	Description
7	DAC_EN	0: Disable 1: Enable
6	DAC_REF_EN	0: Disable 1: Enable
5	DAC_RESET	0: Normal 1: Reset

Bits	Name	Description
4:3	DAC_GAIN	0x0: POS_0P00_DB 0x1: POS_0P27_DB 0x2: POS_0P54_DB 0x3: NEG_0P27_DB
2	INV_DATA	0: Non-invert 1: Invert
1	CLK_POLARITY	0: Falling 1: Rising
0	DAC_ATEST	0: Disable 1: Enable

0x11F WSA_ANALOG_SPKR_OCP_CTL

Type: Read/write

Reset state: 0xD4

Bits	Name	Description
7	OCP_EN	0: Disable 1: Enable
6	OCP_HOLD	0: Disable 1: Enable
5:4	RESERVED	
3:2	GLITCH_FILTER	0x0: T_128NS 0x1: T_96NS 0x2: T_64NS 0x3: T_32NS
1:0	RESERVED	

0x128 WSA_ANALOG_SPKR_STATUS1

Type: Read only

Reset state: 0x00

Bits	Name	Description
7:3	RESERVED	
2	OCP_INT	Read only
1	CLIP_DET_P	Read only
0	CLIP_DET_N	Read only

0x129 WSA_ANALOG_SPKR_STATUS2

Type: Read only

Reset state: 0x00

Bits	Name	Description
7:0	CAL_STATUS	Read only

0x12A WSA_ANALOG_BOOST_EN_CTL

Type: Read/write

Reset state: 0x18

Bits	Name	Description
7	BOOST_ENABLE	0: Disable 1: Enable
6:5	BOOST_CLOCK_DIV_SEL	0x0: DIV2 0x1: DIV3 0x2: DIV4 0x3: DIV1
4:0	Reserved	

0x12D WSA_ANALOG_BOOST_PRESET_OUT1

NOTE This register information is applicable only for WSA8815.

Type: Read/write

Reset state: 0xB7

Bits	Name	Description
7:4	RESERVED	
3:0	SMART_BOOST_SECOND_ LEVEL	- 0000 = 6.625 V; 0001 = 6.750 V; 0010 = 6.875 V; 0011 = 7.000 V - 0100 = 7.125 V; 0101 = 7.250 V; 0110 = 7.375 V; 0111 = 7.500 V - 1000 = 7.625 V; 1001 = 7.750 V; 1010 = 7.875 V; 1011 = 8.000 V - 1100 = 8.125 V; 1101 = 8.250 V; 1110 = 8.375 V; 1111 = 8.500 V

0x12E WSA_ANALOG_BOOST_PRESET_OUT2

NOTE This register information is applicable only for WSA8815.

Type: Read/write

Reset state: 0x70

Bits	Name	Description
7	RESERVED	
6:4	SMART_BOOST_THIRD_LEVEL	- 000 = 8.625 V; 001 = 8.750 V; 010 = 8.875 V; 011 = 9.000 V - 100 = 9.125 V; 101 = 9.250 V; 110 = 9.375 V; 111 = 9.500 V
3:0	RESERVED	

0x130 WSA_ANALOG_BOOST_LDO_PROG

Type: Read/write

Reset state: 0x16

Bits	Name	Description
7:6	RESERVED_BITS7_6	
5:4	ANA_LDO_PROG	0x0: V_4P5V 0x1: V_5P0V 0x2: V_5P5V 0x3: V_5P50V
3:2	LDO_NDRIVE_PROG	0x0: V_4P5V 0x1: V_5P0V 0x2: V_5P5V 0x3: V_5P50V
1:0	LDO_PDRIVE_PROG	0x0: V_4P0V 0x1: V_4P5V 0x2: V_5P0V 0x3: V_5P5V

0x13A WSA_ANALOG_SPKR_PROT_FE_GAIN

Type: Read/write

Reset state: 0x46

Bits	Name	Description
7:6	ISENSE_FE_STAGE2_GAIN	0x0: G_4DB 0x1: G_2DB 0x2: G_1DB 0x3: G_M1DB

5:4	ISENSE_FE_STAGE1_GAIN	0x0: G_16DB 0x1: G_14DB 0x2: G_10DB
3	VSENSE_FE_GAIN	0: G_DB15 1: G_DB18
2	VSENSE_OPAMP_ENABLE	0: Disable 1: Enable
1	VSENSE_LDO_OTA_ENABLE	0: Disable 1: Enable
0	SPKR_PROT_EN	0: Disable 1: Enable

9 Detailed description of features

9.1 Feature overview

WSA8810 and WSA8815 are high-efficiency, smart class-D speaker amplifiers, and can drive as low as a 4 Ω speaker load. An on-chip integrated smart-boost circuit provides higher voltage supply than battery voltage for speaker amplifier operation to enhance speaker performance without losing efficiency. Since WSA8810/WSA8815 and speaker transducers carry large current and voltage in operation, multiple protection-function algorithms are implemented on these devices without affecting the speaker output levels. WSA8810/WSA8815 also provides current and voltage sense feedback signals to host processor to support a fully real-time feedback speaker-protection function.

WSA8810/WSA8815 smart speaker amplifiers integrate multiple functions for high speaker performance with full protection. These are the following three protections:

- Feedback speaker protection (WSA8810/WSA8815 devices provide feedback signals to host processor)
- Chip-level over-temperature protection
- Over-current protection

WSA8810/WSA8815 devices can operate in two different input modes – SoundWire mode and analog mode; this provides more flexibility. The two modes are differentiated based on audio input data format, control signal, and feedback signal transmitted interface.

For WSA8810, the programmable amplifier analog gain can be set from 0 dB to 13.5 dB with 1.5 dB gain step (10 steps in total) for both input modes.

For WSA8815, the programmable gain can be set from 0 dB to 18 dB with 1.5 dB gain step (13 steps in total) for both input modes.

9.2 Detailed signal-path diagram

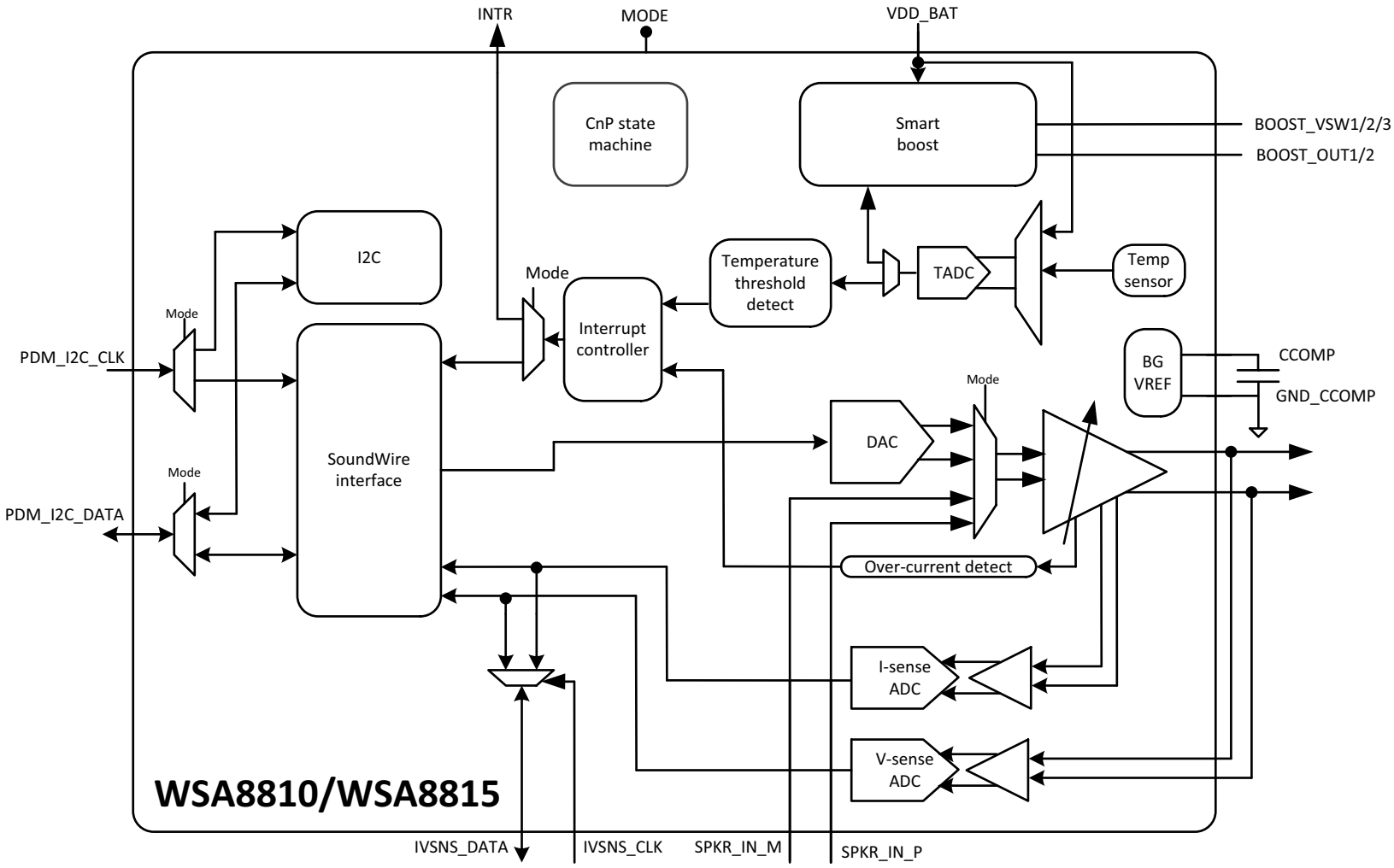


Figure 9-1 WSA8810/WSA8815 detailed signal-path diagram

9.3 Feedback speaker protection data

Integrated feedback speaker protection provides real time current and voltage of speaker transducer, which supports the host processor to achieve more accurate speaker temperature monitoring and control.

Since the WSA8810/WSA8815 outputs (up to 3.2 W for WSA8810 and 4 W for WSA8815) to a 4 Ω speaker load with 1% THD, the transducer carries large current and generates a lot of heat, which could potentially damage the speaker transducer. Accurate feedback speaker protection is necessary to ensure speaker transducers work safely with maximum loudness.

WSA8810/WSA8815 integrates two dedicated ADCs for real-time feedback voltage and current sense signals. Feedback sense data is sent to the host processor through the SoundWire interface in SoundWire mode, and through the IVSNS_DATA/CLK in analog mode. These sense signals help the processor measure speaker impedance and temperature.

Transducer temperature is proportional to the speaker coil resistance. During the over-temperature monitor processing, the host processor can calculate speaker temperature by speaker voltage and current from WSA8810/WSA8815. To obtain accurate prediction results in protection processing, the feedback speaker-protection function needs one-time initial calibration for the life of amplifier use, which can be done by the on-chip temperature sensor. During speaker over-temperature monitoring, the speaker protection algorithm uses feedback voltage and current data to calculate and predict speaker-transducer temperature. Once the predicted temperature of the transducer is larger than the threshold, speaker output loudness is reduced by the host processor to protect transducer.

9.4 Chip-level over-temperature protection

The temperature sensor for the feedback speaker-protection one-time calibration is also used for chip-level over-temperature protection. This feature provides continuous chip temperature measurements, and allows system software to control the gain of the smart amplifier or turn off the device to prevent WSA8810/WSA8815 from overheating. During the temperature monitoring process, three kinds of interrupts can be triggered to protect this smart amplifier – safe-to-warning interrupt, disabled interrupt, and warning-to-safe interrupt. These temperature thresholds can be set through registers.

- Safe-to-warning interrupt: When amplifier temperature increases over the safe-to-warning threshold, software reduces the gain of the amplifier to prevent amplifier shutdown. The safe-to warning threshold can be set using the register 0x013 WSA_DIGITAL_TEMP_CONFIG0 [2:0], from 110°C to 145°C with a 5°C step. The threshold setting includes eight steps in total.
- Disable interrupt: When chip temperature continually increases and exceeds the maximum operating temperature, a disable interrupt is generated to the host processor. The disable threshold can be set using the register 0x013 WSA_DIGITAL_TEMP_CONFIG0 [5:4], from 140°C to 150°C with a 5°C step. The threshold setting includes three steps in total.
- Warning-to-safe interrupt: When amplifier temperature decreases to the safe zone after being in the warning range, software controls the amplifier gain and allows it to work normally. The warning-to-safe threshold can be set using the register 0x014 WSA_DIGITAL_TEMP_ CONFIG1 [2:0], from 100°C to 35°C with a 5°C step. Threshold setting includes eight steps in total.

9.5 Over-current protection (OCP)

If output terminals are shorted or connect to ground by mistake without any protection function, large amplifier output current damages the chip. Over-current protection is implemented inside the WSA8810/WSA8815 to ensure the WSA8810/WSA8815 chipset works within the current limit, and always monitors speaker output current. Once it exceeds current limit, which can be set via registers, the over-current protection circuit is engaged and prevents chip damage. OCP current limit is fixed at 5.0 A.

9.6 Receiver mode operation

Low noise in WSA8810/WSA8815 allows this amplifier to be used as a receiver amplifier with a 32 Ω earpiece load for a high quality device use case. In receiver mode, the carrier frequency of the Class-D amplifier operates at 600 kHz as opposed to 300 kHz for lower output noise.

NOTE The feedback speaker protection feature cannot be used for a 32 Ω load in the receiver mode.

When WSA8810/WSA8815 works in the SoundWire mode with pairing devices like WCD9335, they could act as a receiver amplifier only to support a 32 Ω earpiece load and amplify digital signal from SoundWire interface.

9.6.1 Shared transducer for receiver mode and speaker mode

To save BOM further, the WSA device can be used to drive the shared earpiece and speaker transducer. The block diagram is shown in Figure 9-2.

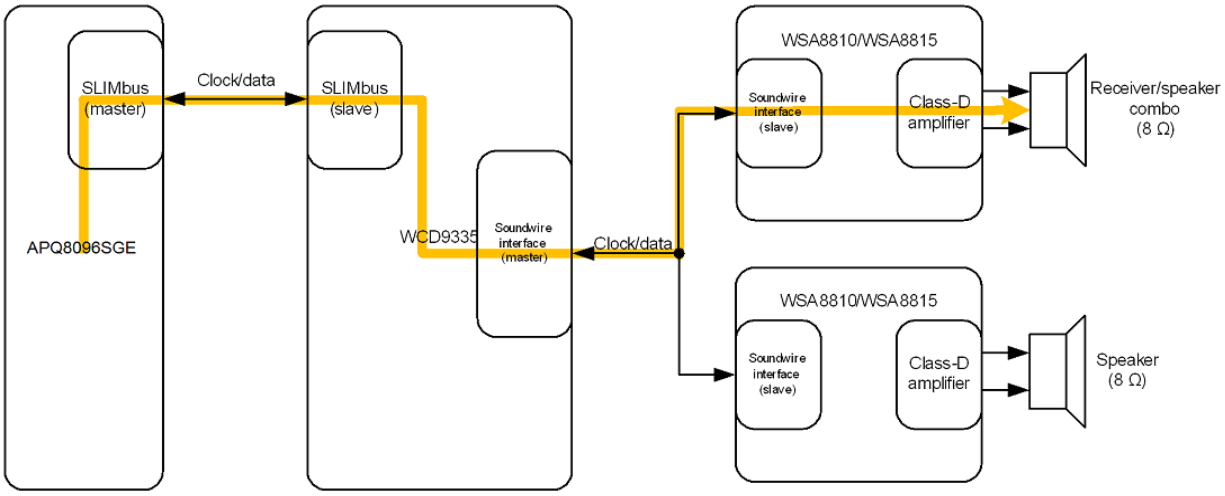


Figure 9-2 Shared transducer application signal path in SoundWire mode

To change from loud speaker use case to receiver use case, speaker path digital gain is reduced in the WCD9335 audio codec to reduce the output power. Boost operates in bypass mode since the output power is low.

9.7 Support circuit and smart boost

To boost larger speaker output power with low distortion, larger voltage supply is necessary for amplifier operation. An on-chip smart-boost block is integrated in WSA8810/WSA8815. It can provide as high as 6 V (WSA8810) and 9.5 V (WSA8815) to amplifier voltage supply with several boost levels. This provides great convenience and saves a lot of BOM to use this amplifier with high output power.

Smart boost in WSA8810 has two states: 6 V boost output and boost bypass, whereas smart boost in WSA8815 has four states: 9.5 V, 7.5 V, and 5.5 V boost output and boost bypass, for different output power capability. The smart boost controller, which is located in the WCD9335, monitors real-time speaker output and speaker-amplifier analog gain to determine proper smart-boost output level. Multiple smart-boost output levels enhance the amplifier efficiency. However, since the smart boost controller is inside WCD9335, the smart boost feature is ONLY available in the WSA8810/WSA8815 SoundWire mode. In WSA8810/WSA8815 analog mode, the boost block level could only be set statically through I2C interface.

Formula 1 for the recommended settings for maximum boost output level and gain selection (WSA8815 only)

To maximize efficiency for a given target system full scale output, the following formula is recommended to calculate the highest boost level.

Maximum boost output level = $\sqrt{P \times R} \times \sqrt{2} + 1.0\,V$

where,

P = 1% THD + N target power to the load with a sinewave applied. The WSA8815 maximum output power is 4 W.

R = Load impedance.

Additional 1 V is applied for headroom.

For example:

For a 4 W, 1% THD + N target system with an 8 W load,

Maximum boost output level = $\sqrt{4 \times 8} \times \sqrt{2} + 1.0\,V = 9.0\,V$

As a guideline, the following formulas can be used to choose a proper gain for the system. Simply plug in the load impedance for a less than or equal to 4 W maximum system.

It is understood that load impedances has a variation from the ideal. This formula tolerates normal expected variations (simply insert the typical value), further keeping extreme conditions in check.

System gain here means end-to-end gain, which includes gain settings in tuning, codec, and WSA. For example, if WCD codec has -1.5 dB digital gain and WSA has 13.5 dB analog PA gain, then system gain is -1.5 + 13.5 = 12 dB.

dB system gain selection: dB = 20 × log (sqrt(4 × R))

For example, when load (R) = 8 Ω: dB = 20 × log(sqrt(4 × 8) = 15 dB

For example, when load (R) = 5 Ω: dB = 20 × log(sqrt(4 × 5) = 13 dB

Table 9-1 Guidance for system gain setting and boost voltage for different speaker loads

Speaker impedance (Ω)	System gain (dB)	Maximum boost voltage (V) [1]	Maximum boost stage [2]
8	15.0	9.0	3
7	14.5	8.5	2
6	14.0	8.0	2
5	13.0	7.5	2
4	12.0	7.0	2

1. Maximum boost voltage can be set with the WSA registers 0x12D WSA_ANALOG_BOOST_PRESET_OUT1[3:0] for second boost level voltage and 0x12E WSA_ANALOG_BOOST_PRESET_OUT2[6:4] for third boost level voltage.
2. The boost output stage controller register is located at the WCD codec.

10 Application information

10.1 SoundWire mode

In SoundWire mode, all the audio data, control signals, feedback speaker protection data, smart boost control signals, interrupts and clocks are transmitted in SoundWire mode by the WSA8810/WSA8815 SoundWire audio interface.

- Smart boost: Higher amplifier efficiency and lower power consumption
- Dynamic range enhancement (DRE): Dynamic analog PA gain control
- Feedback speaker protection IV sense data
- Chip-level over temperature monitor and protection
- Only two lines are necessary for multichannel data transmission: PDM_I2C_CLK and PDM_I2C_DATA
- WSA8810/WSA8815 acts as SoundWire slave when it connects to host processor

10.1.1 Timing requirements

For timing requirements information, see Section 3.6.1.

10.1.2 Application performance plots

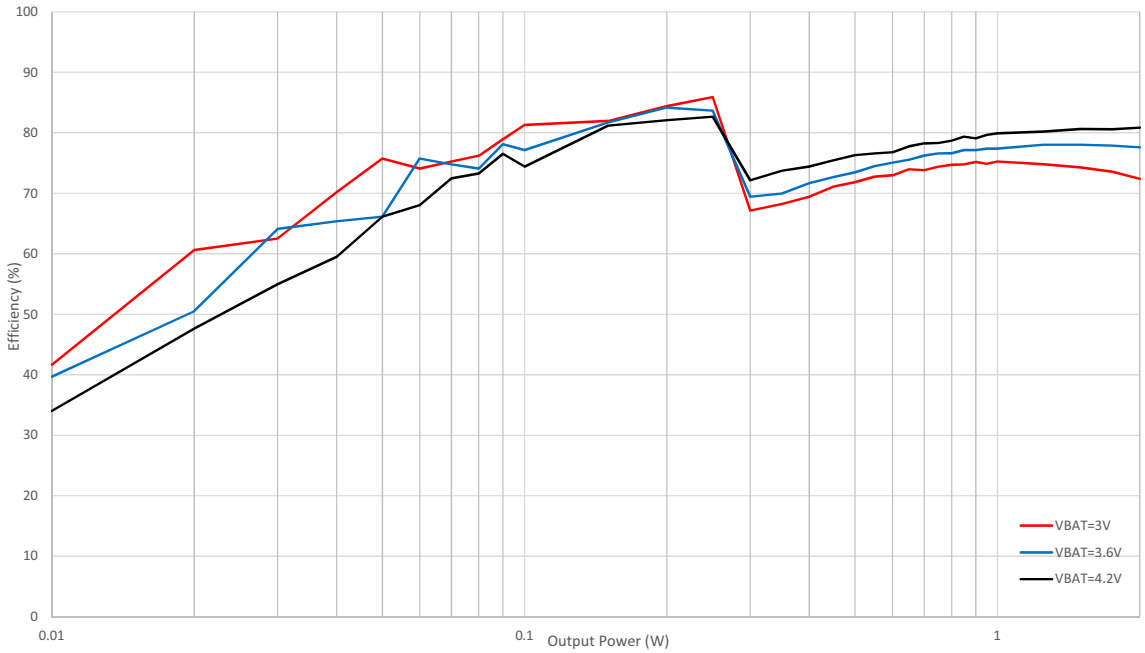


Figure 10-1 Efficiency vs. output power at different battery voltages (8 Ω load) – WSA8810

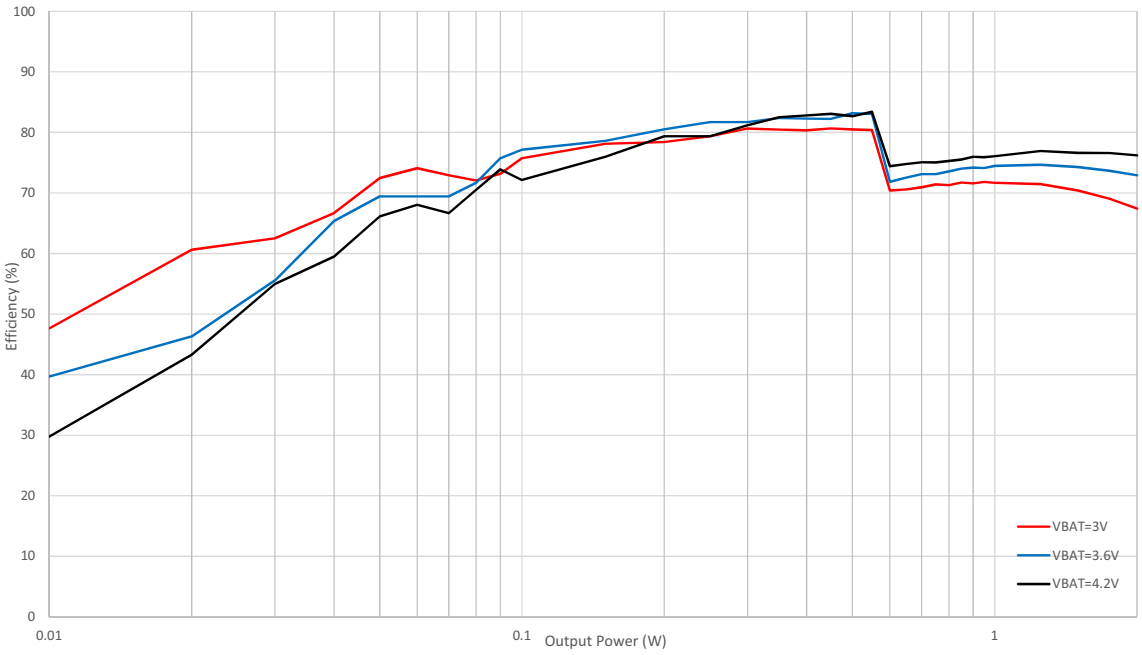


Figure 10-2 Efficiency vs. output power at different battery voltages (4 Ω load) – WSA8810

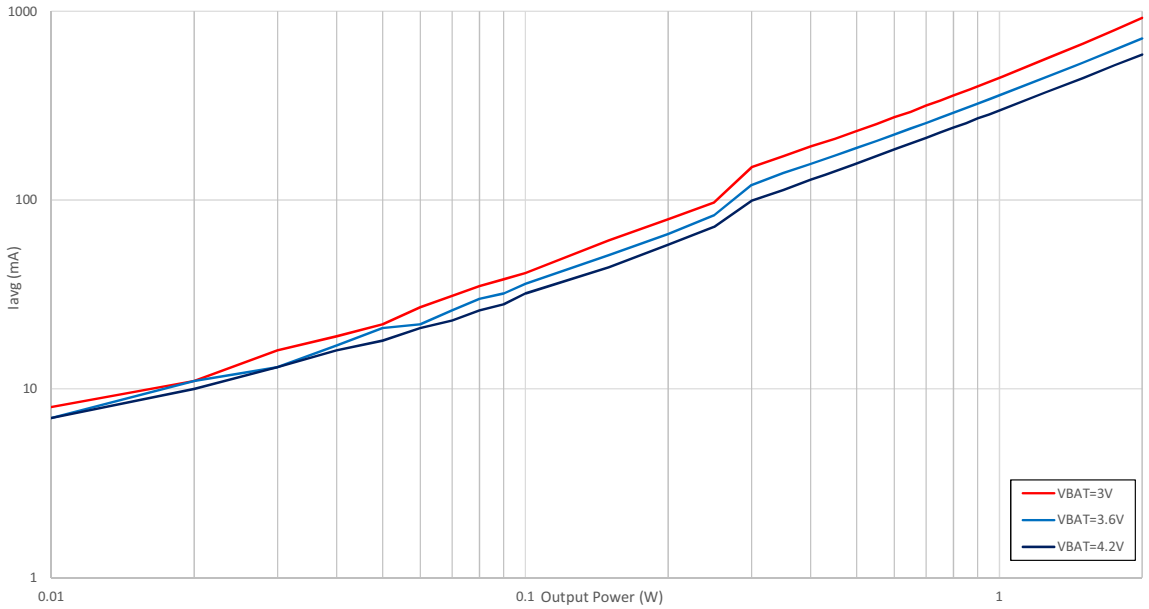


Figure 10-3 Average battery current vs. output power at different battery voltages (8 Ω load) – WSA8810

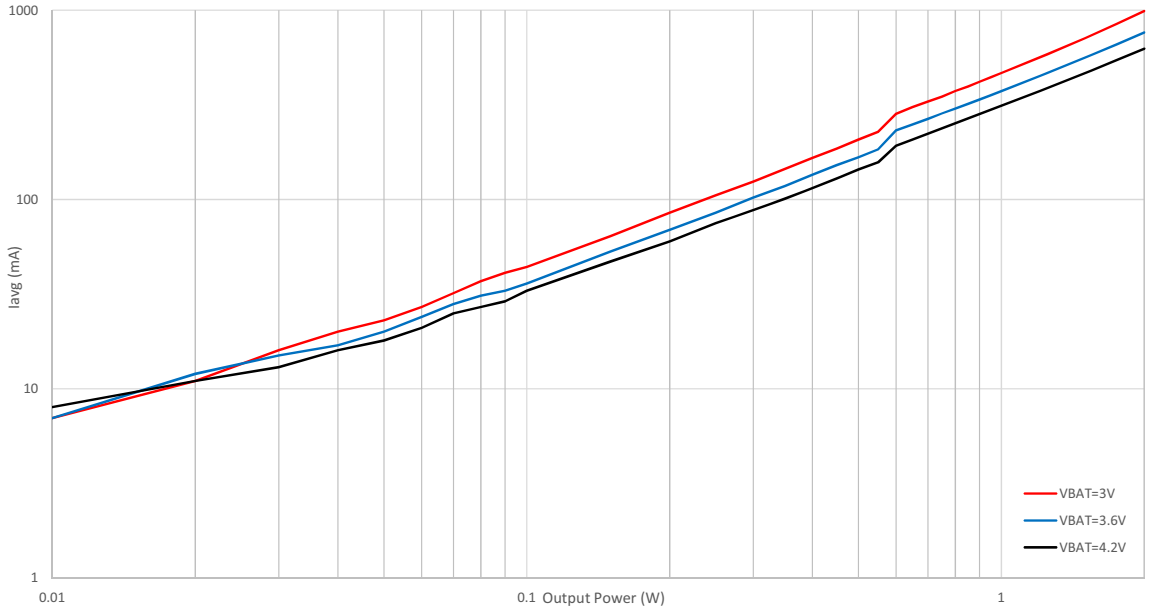


Figure 10-4 Average battery current vs. output power at different battery voltages (4 Ω load) – WSA8810

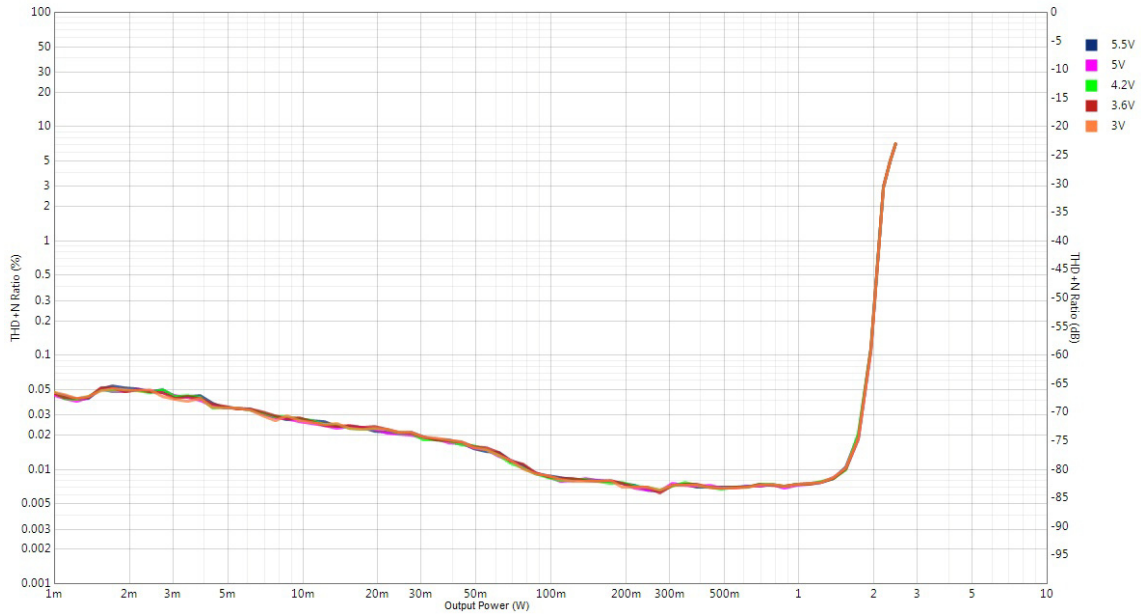


Figure 10-5 THD+N vs. output power at different battery voltages (8 Ω load) – WSA8810

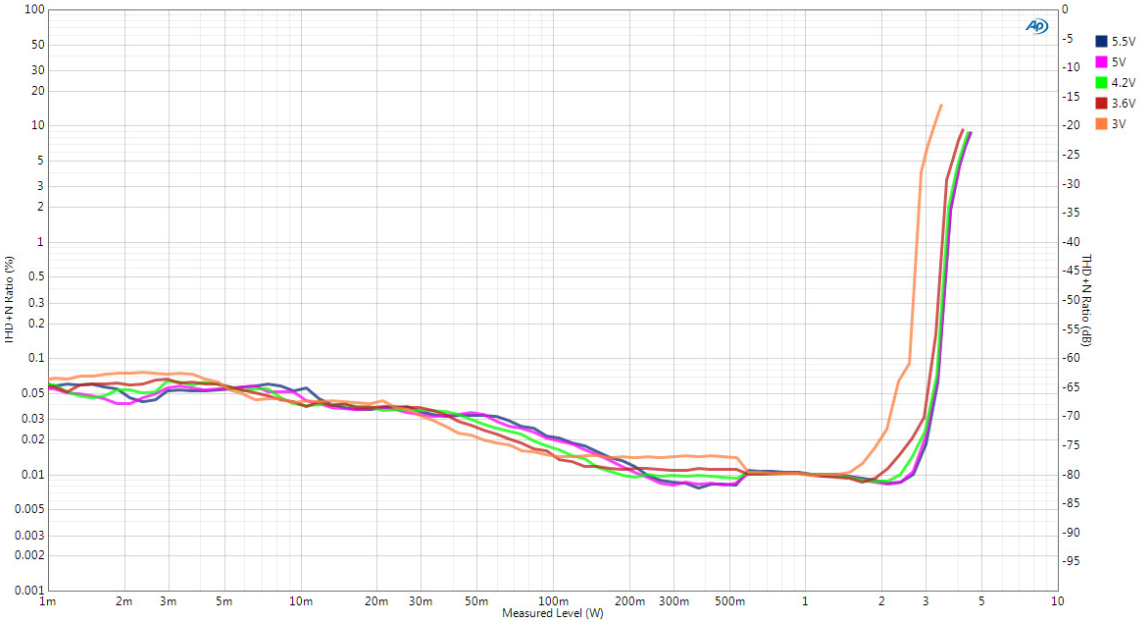


Figure 10-6 THD+N vs. output power at different battery voltages (4 Ω load) – WSA8810

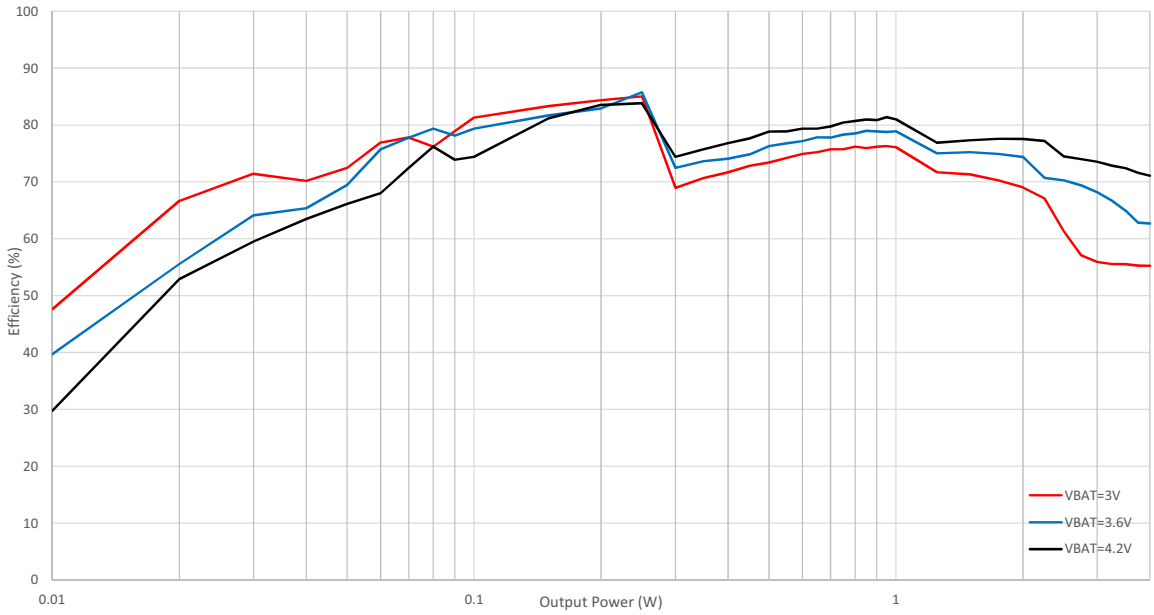


Figure 10-7 Efficiency vs. output power at different battery voltages (8 Ω load) – WSA8815

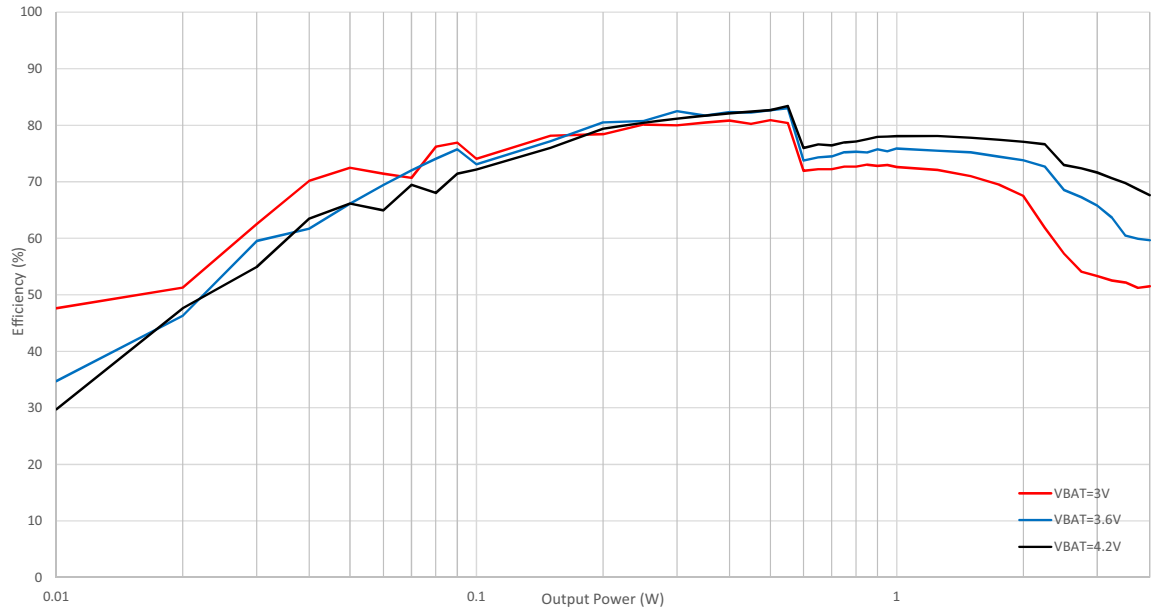


Figure 10-8 Efficiency vs. output power at different battery voltages (4 Ω load) – WSA8815

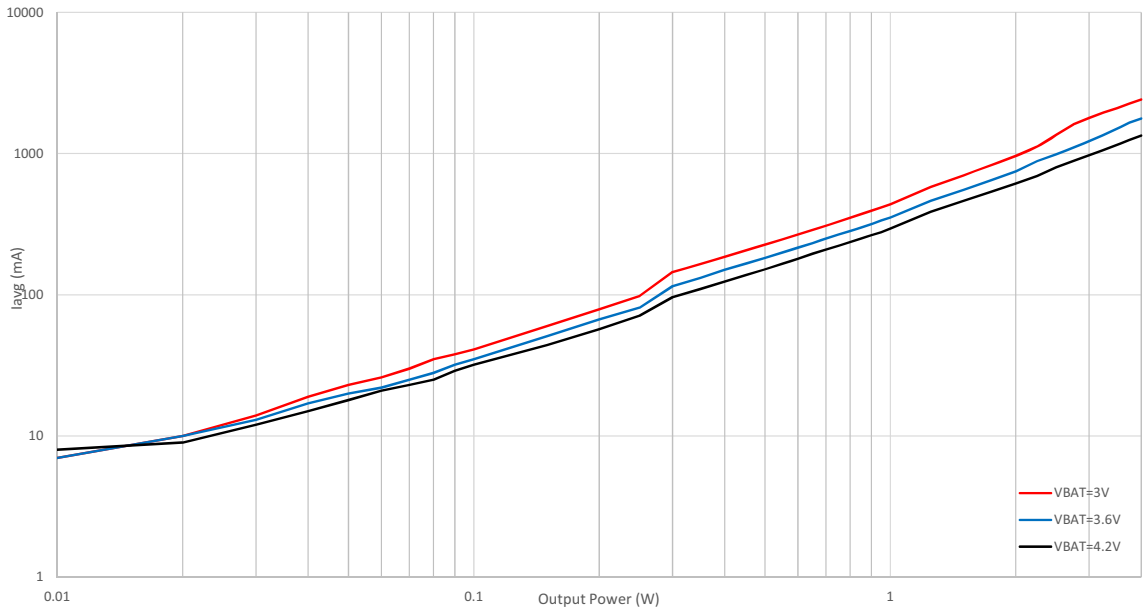


Figure 10-9 Average battery current vs. output power at different battery voltages (8 Ω load) – WSA8815

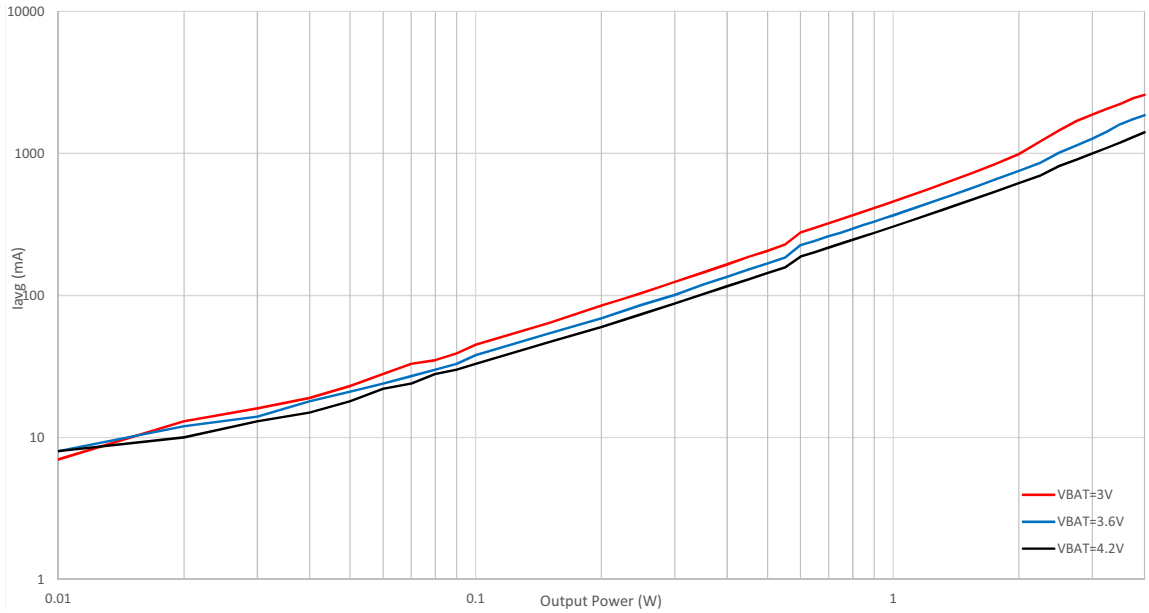


Figure 10-10 Average battery current vs. output power at different battery voltages (4 Ω load) – WSA8815

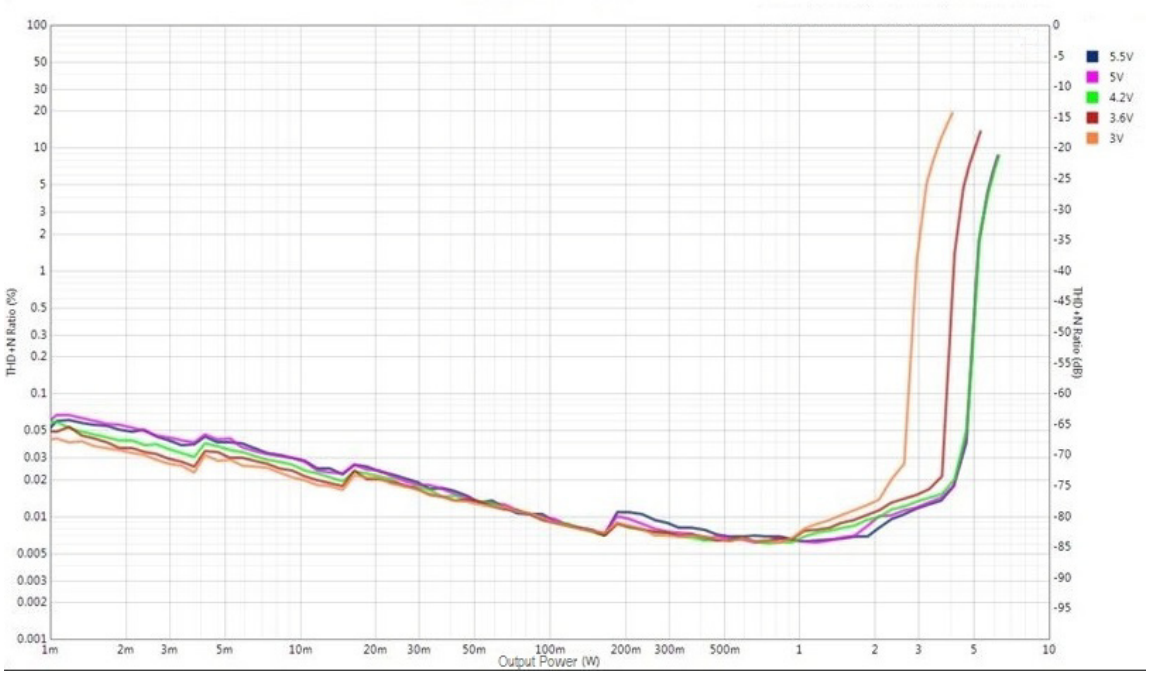


Figure 10-11 THD+N vs. output power at different battery voltages (8 Ω load) – WSA8815

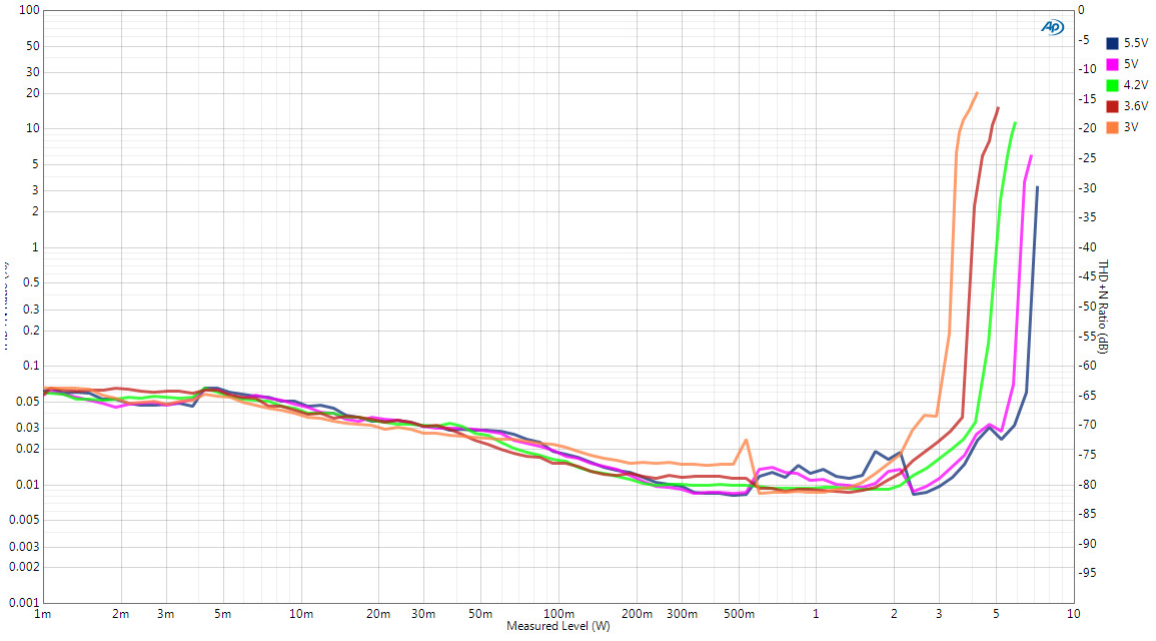


Figure 10-12 THD+N vs. output power at different battery voltages (4 Ω load) – WSA8815

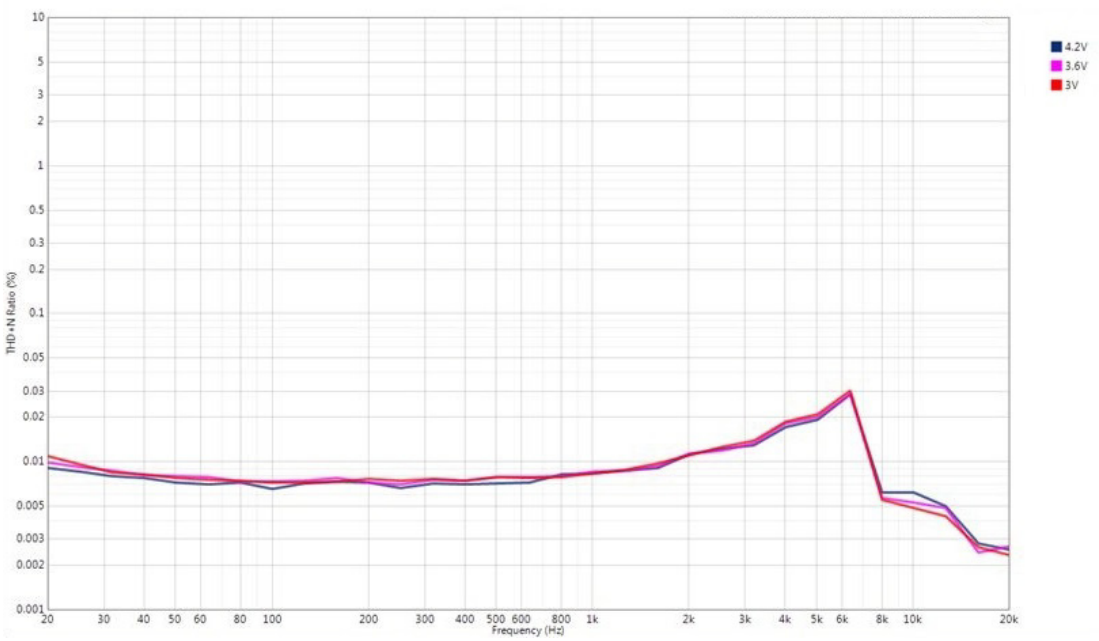


Figure 10-13 THD+N vs. frequency at different battery voltages (8 Ω load, Pout = 1 W)

10.1.3 Clock

In SoundWire mode, no separate MCLK source is needed. CLK for WSA8810/WSA8815 operation is generated from SoundWire clock divided by 2, 4, or 8.

In SoundWire mode, device clock provided to WSA8810/WSA8815 is divided through PDM_I2C_CLK. Multiple divide options provide more flexibility for the chosen clock. Clock rate can be one of the following:

- 4.8 MHz, 9.6 MHz (if codec uses 9.6 MHz MCLK)
- 6.144 MHz, 12.288 MHz (if codec uses 12.288 MHz MCLK)

10.1.4 Schematic examples

10.1.4.1 Mono-speaker mode or receiver mode operation

In Figure 10-14, note the following for mono-speaker operation:

- The MODE pad connects to ground for the chosen SoundWire mode.
- Device SCLK is derived from SoundWire clock, and the MCLK pad must be grounded in SoundWire mode. The clock from the SoundWire interface is the only clock source for WSA8810/WSA8815.
- Speaker-protection sense data goes through the SoundWire interface. No additional connection is required for feedback speaker-protection data.

- Connect a 4 Ω or 8 Ω speaker transducer for mono-speaker operation or a 32 Ω earpiece load for the receiver mode only.

NOTE Speaker protection is not available for the receiver mode with a 32 Ω earpiece load.

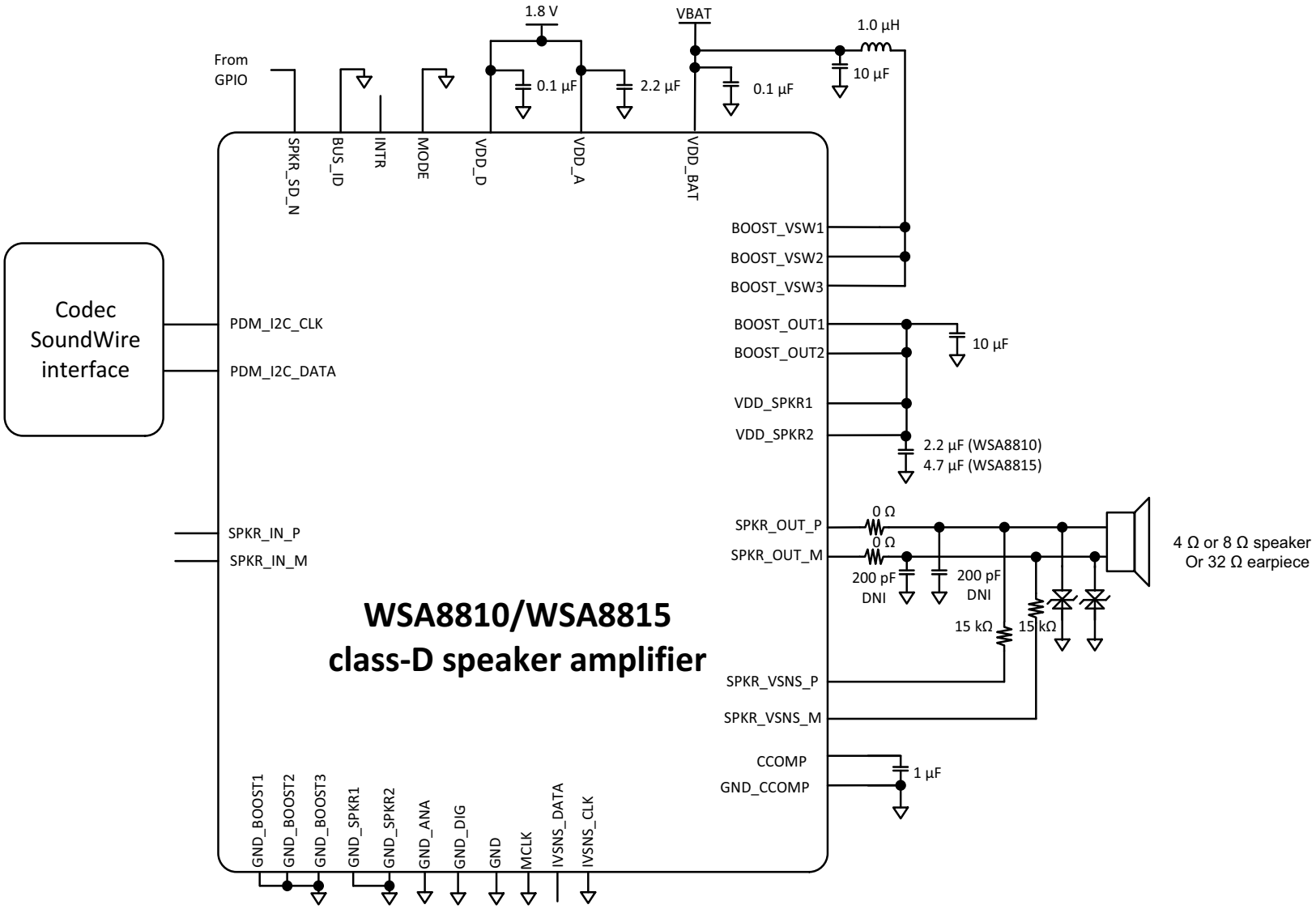


Figure 10-14 WSA8810/WSA8815 mono-speaker operation in SoundWire mode

10.1.4.2 Stereo-speaker operation

Two WSA8810s or WSA8815s can be used for the stereo-speaker output use case. The BUS_ID pad helps distinguish left-channel and right-channel input for the amplifier.

- BUS_ID is connected to ground for the left channel.
- BUS_ID is pulled up to high for the right channel.

Application circuit examples for WSA8810/WSA8815 is shown in Figure 10-15.

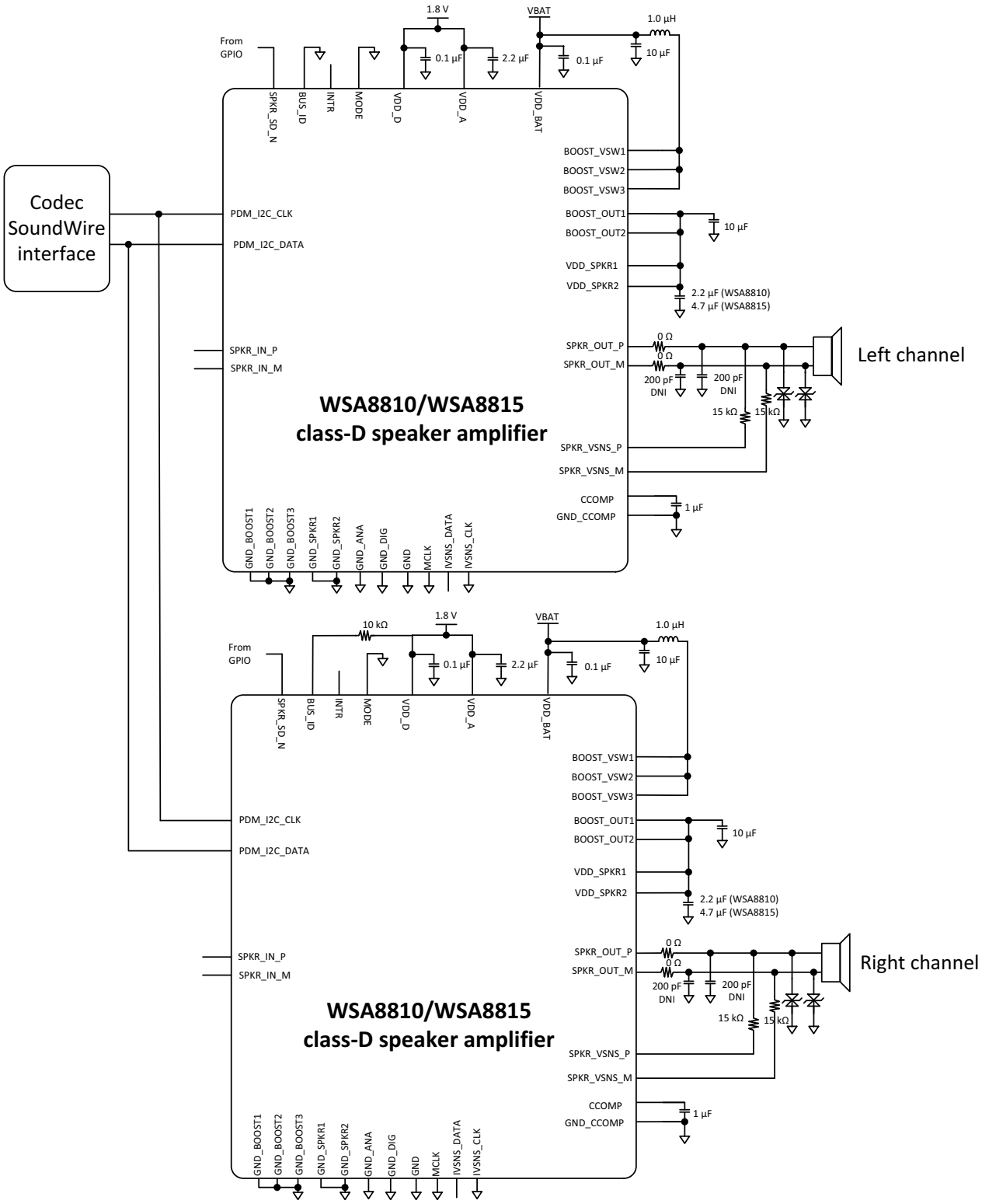


Figure 10-15 WSA8810/WSA8815 stereo-speaker application in SoundWire mode

10.1.5 Power up/down sequence

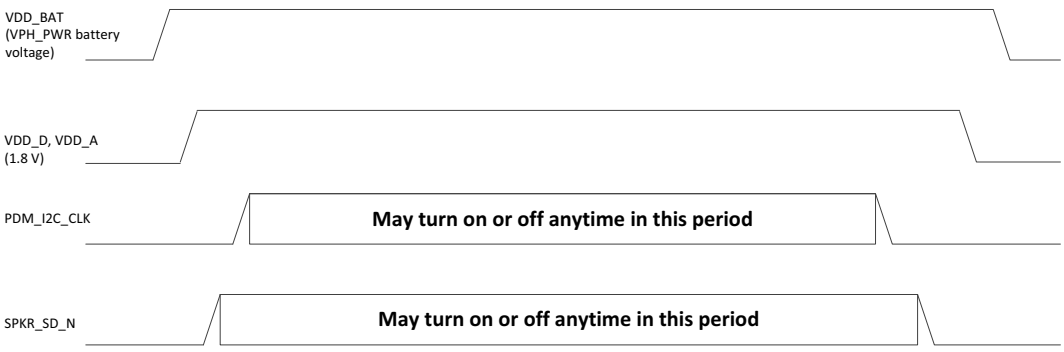


Figure 10-16 Power up/down sequence for SWR mode

10.2 Layout design guidelines

10.2.1 External-component list

Table 10-1 WSA external components

Pad name	Padpad description	Components	Part requirements
VDD_D	Power for digital	0.1 μF	±10%, voltage rating 6 V or greater
VDD_A	Power for analog	2.2 μF	±20%, voltage rating 6 V or greater
VDD_BAT	Battery voltage	10 μF	±10%, voltage rating 10 V
		0.1 μF	±10%, voltage rating 10 V
BOOST_VSW1/2/3	Boost switch	1 μH	±20%, I = 2.5 A (WSA8810) or 4 A (WSA8815), R < 50 mΩ, f = 3.072 MHz for 8 Ω speaker ±20%, I = 3 A (WSA8810) or 5 A (WSA8815), R < 50 mΩ, f = 3.072 MHz for 4 Ω speaker
BOOST_OUT1/2	Boost output	10 μF	±10%, voltage rating 10 V (WSA8810) or 16 V (WSA8815), must maintain larger than 7 μF at 6.5 VDC (WSA8810) or 9.5 VDC (WSA8815) across corners
CCOMP	Compensation capacitor	1.0 μF	±20%, voltage rating 6 V or greater
VDD_SPKR1/2	Power for speaker amplifier	2.2 μF (WSA8810) 4.7 μF (WSA8810)	±10%, voltage rating 10 V (WSA8810) or 16 V (WSA8815) or greater
SPKR_VSNS_P/M	Feedback speaker protection sense lines	15 kΩ	5%, series resistors reduce voltage ringing into the Vsense ADC input that impacts the speaker protection performance

10.2.2 External component placement layout guidelines and GND connection guidelines

WSA8810/WSA8815:

- Place WSA8810/WSA8815 as close to speaker as possible to minimize radiated emissions.

Boost:

- Place BOOST_VSW inductor close to the associated pad.
- Place 10 µF capacitor close to the inductor.
- Trace resistance from inductor to 10 µF capacitor must be < 5 mΩ.
- Place 0.1 µF capacitor near the VDD_BAT pad.
- Place boost output capacitor close to the associated pad.
- Star-routing from VPH_PWR to VDD_BAT and inductor.
- Trace resistance from inductor to VPH_PWR must be < 5 mΩ.
- Trace resistance from VDD_BAT to VPH_PWR must be < 1 Ω.
- Trace resistance from boost output capacitor to the pad must be < 5 mΩ.
- Trace inductance from boost output capacitor to the pad must be < 1 nH.
- Ground boost output capacitor at the capacitor itself. Ground connection must be < 5 mΩ.
- Ground GND_BOOST1/2/3 pads at the pads. Ground connection must be < 5 mΩ and < 1 nH.

Charge pump:

- CCOMP capacitor placement and routing close to the pad.
- Route GND_CCOMP to the capacitor and ground at the capacitor, not at the pad.

VDD_D:

- VDD_D bypass capacitor must be placed and routed close to the pad.

VDD_A:

- VDD_A bypass capacitor must be placed and routed close to the pad.

Speaker amplifier:

- Place capacitor close to the associated VDD pads.
- Trace resistance from capacitor to VDD pads must be < 10 mΩ.
- Trace inductance from capacitor to pads must be < 1 nH.
- Route GND_SPK1/2 pads to the capacitor and then tie to ground at the capacitor, not at the pads.
- Trace resistance from ground side of capacitor to GND_SPK1/2 must be < 10 mΩ.
- Trace inductance from ground side of capacitor to GND_SPK1/2 must be < 1 nH.
- Route the speaker output as differential pair with ground isolation at side, top, and bottom layers to avoid radiation emissions and impact on other sensitive signals.

- The recommended speaker output trace width for:
  - WSA8810:
    - 20 mil or greater for 8 Ω load;
    - 25 mil or greater for 4 Ω load
  - WSA8815:
    - 25 mil or greater for 8 Ω load;
    - 30 mil or greater for 4 Ω load
- Route the speaker protection data traces as a differential pair all the way to transducer pads with fully ground isolation. Series 15 kΩ resistors on speaker protection path are required to reduce ringing on feedback speaker protection path. The placement is not critical.
- EMI filter for speaker output. Place ferrite beads and capacitors close to speaker amplifier in case EMI filter is needed.

Dual speaker in parallel application:

- The speakers must be of the same manufacturer and model.
- The speakers must be located next to each other.
- The speakers must have a shared back volume or identical back volumes.
- One speaker must not be thermally exposed to other components on the board more than the other and they must be equally close to that source to avoid one being heated more than the other.
- Low impedance connection between the speakers with no ferrite beads between them.

SoundWire interface:

- Route signals together for length matching with trace width of 0.1 mm to 0.12 mm and away from any power supply planes.
- Use single linear path (daisy chain) connections to connect from WCD device to each WSA device (do not star-route) to avoid disturbing the clock arrival time at other nodes in the system due to extra reflections.
- Interface is an edge-rate-controlled bidirectional bus. Do not add any series resistors or other components on the lines.
- For system with MCLK = 9.6 MHz, keep trace capacitance below 100 pF and trace length below 50 cm.
- For system with MCLK = 12.288 MHz, keep trace capacitance below 60 pF and trace length below 30 cm.

ESD diodes:

- Place near the speaker. 12 V clamping voltage is required.

10.2.3 External components placement and layout example

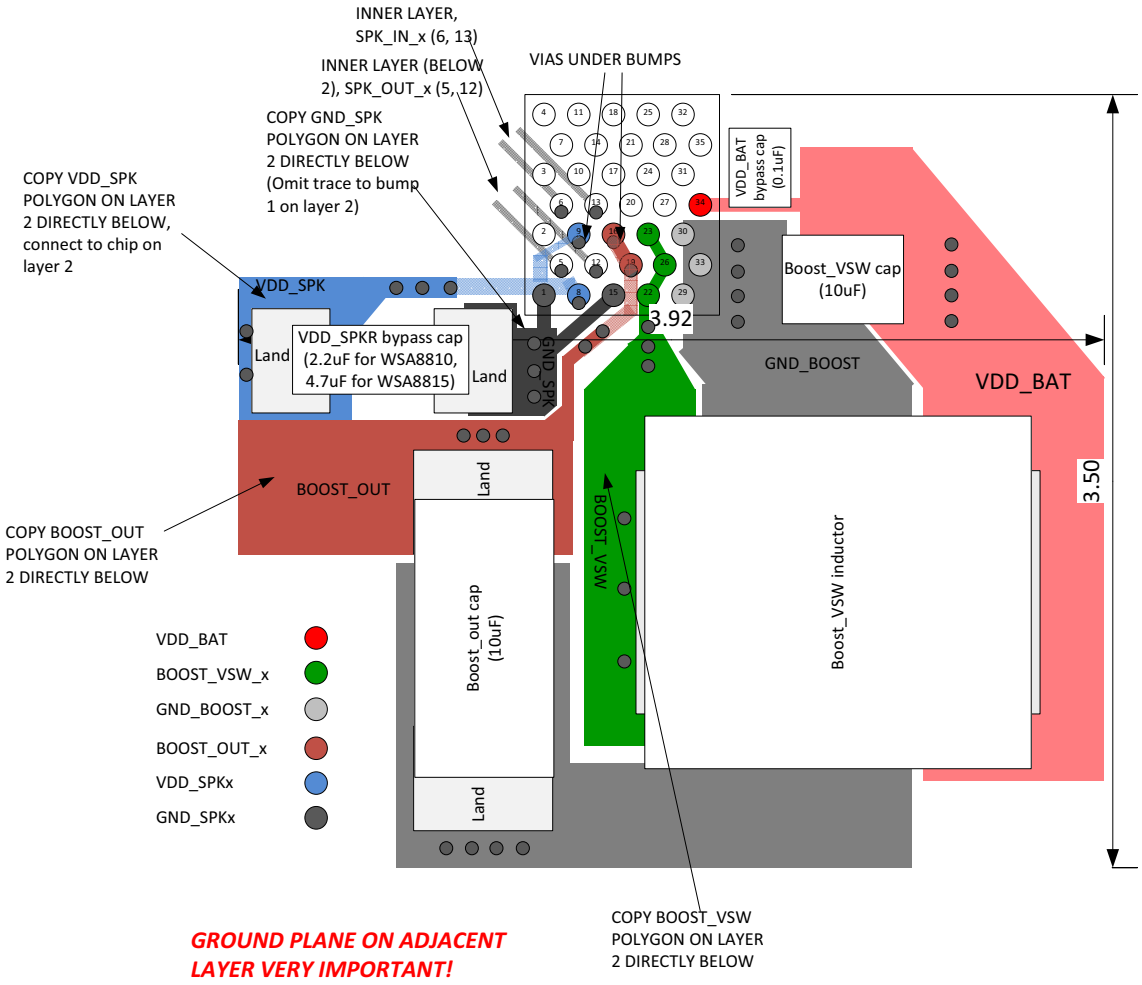


Figure 10-17 WSA8810/WSA8815 layout example

10.3 Maximum output power application note

10.3.1 WSA8810

The maximum power numbers in Table 3-7 are obtained with power sweeps up through the 1% THD + N levels under various VBAT and load conditions to show the maximum power delivery limits of the device. Although the maximum power numbers stated in the table can be achieved for short term durations, long term continuous power dissipation is limited by the thermal characteristics of the device and the target maximum ambient temperature of the system.

It is not recommended to set the full scale output of the system to a target of more than 2 Wrms.

10.3.2 WSA8815

The maximum power numbers in Table 3-8 show the maximum power delivery limits of the device. It is not recommended to set the full scale output of the system to target more than 4 Wrms. It is important to ensure power dissipation on die does not exceed 1.9 Wrms or the die temperature could exceed absolute maximum operation junction temperature limit and over-temperature protection is triggered. Therefore, when setting the target system gain and power, thermal considerations need to be taken into account.

A References

A.1 Acronyms and terms

Acronym or term	Definition
ADC	Analog to digital converter
CDM	Charged device model
CMOS	Complementary metal oxide semiconductor
CPH	Cycles per hour
DAC	Digital to analog converter
DMIC	Demultiplexing and multiplexing interface circuit
DPPM	Defective parts per million
ESD	Electrostatic discharge
FIT	Failure in time
GND	Ground
HBM	Human body model
I/O	Input/output
I2C	Inter-integrated circuit
IC	Integrated circuit
MIPI	Mobile industry processor interface
MRT	Moisture resistance test
MSL	Moisture sensitivity level
MTTF	Mean time to failure
NSMD	Non-solder mask defined
OCP	Over-current protection
PCB	Printed circuit board
PHY	Physical layer
PWB	Printed wiring board
PWR	Power
RoHS	Restriction of hazardous substances
SMPS	Switched-mode power supply
SMT	Surface mount technology
SWR	SoundWire

Acronym or term	Definition
THD	Threshold
VBAT	Battery level
VDC	Video codec
VDD	Video display data
WCD	WLP coder decoder
WLNSP	Wafer level nano scale package
WLP	Wafer level packaging
WSA	WSP Smart Amplifier
WSP	Wafer scale package

EXHIBIT 1

PLEASE READ THIS LICENSE AGREEMENT ("AGREEMENT") CAREFULLY. THIS AGREEMENT IS A BINDING LEGAL AGREEMENT ENTERED INTO BY AND BETWEEN YOU (OR IF YOU ARE ENTERING INTO THIS AGREEMENT ON BEHALF OF AN ENTITY, THEN THE ENTITY THAT YOU REPRESENT) AND QUALCOMM TECHNOLOGIES, INC. ("QTI" "WE" "OUR" OR "US"). THIS IS THE AGREEMENT THAT APPLIES TO YOUR USE OF THE DESIGNATED AND/OR ATTACHED DOCUMENTATION AND ANY UPDATES OR IMPROVEMENTS THEREOF (COLLECTIVELY, "MATERIALS"). BY USING, ACCESSING, DOWNLOADING OR COMPLETING THE INSTALLATION OF THE MATERIALS, YOU ARE ACCEPTING THIS AGREEMENT AND YOU AGREE TO BE BOUND BY ITS TERMS AND CONDITIONS. IF YOU DO NOT AGREE TO THESE TERMS, QTI IS UNWILLING TO AND DOES NOT LICENSE THE MATERIALS TO YOU. IF YOU DO NOT AGREE TO THESE TERMS YOU MUST DISCONTINUE AND YOU MAY NOT USE THE MATERIALS OR RETAIN ANY COPIES OF THE MATERIALS. ANY USE OR POSSESSION OF THE MATERIALS BY YOU IS SUBJECT TO THE TERMS AND CONDITIONS SET FORTH IN THIS AGREEMENT.

1.1 **License.** Subject to the terms and conditions of this Agreement, including, without limitation, the restrictions, conditions, limitations and exclusions set forth in this Agreement, Qualcomm Technologies, Inc. ("QTI") hereby grants to you a nonexclusive, limited license under QTI's copyrights to use the attached Materials; and to reproduce and redistribute a reasonable number of copies of the Materials. You may not use Qualcomm Technologies or its affiliates or subsidiaries name, logo or trademarks; and copyright, trademark, patent and any other notices that appear on the Materials may not be removed or obscured. QTI shall be free to use suggestions, feedback or other information received from You, without obligation of any kind to You. QTI may immediately terminate this Agreement upon your breach. Upon termination of this Agreement, Sections 1.2-4 shall survive.

1.2 **Indemnification.** You agree to indemnify and hold harmless QTI and its officers, directors, employees and successors and assigns against any and all third party claims, demands, causes of action, losses, liabilities, damages, costs and expenses, incurred by QTI (including but not limited to costs of defense, investigation and reasonable attorney's fees) arising out of, resulting from or related to: (i) any breach of this Agreement by You; and (ii) your acts, omissions, products and services. If requested by QTI, You agree to defend QTI in connection with any third party claims, demands, or causes of action resulting from, arising out of or in connection with any of the foregoing.

1.3 **Ownership.** QTI (or its licensors) shall retain title and all ownership rights in and to the Materials and all copies thereof, and nothing herein shall be deemed to grant any right to You under any of QTI's or its affiliates' patents. You shall not subject the Materials to any third party license terms (e.g., open source license terms). You shall not use the Materials for the purpose of identifying or providing evidence to support any potential patent infringement claim against QTI, its affiliates, or any of QTI's or QTI's affiliates' suppliers and/or direct or indirect customers. QTI hereby reserves all rights not expressly granted herein.

1.4 **WARRANTY DISCLAIMER.** YOU EXPRESSLY ACKNOWLEDGE AND AGREE THAT THE USE OF THE MATERIALS IS AT YOUR SOLE RISK. THE MATERIALS AND TECHNICAL SUPPORT, IF ANY, ARE PROVIDED "AS IS" AND WITHOUT WARRANTY OF ANY KIND, WHETHER EXPRESS OR IMPLIED. QTI ITS LICENSORS AND AFFILIATES MAKE NO WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THE MATERIALS OR ANY OTHER INFORMATION OR DOCUMENTATION PROVIDED UNDER THIS AGREEMENT, INCLUDING BUT NOT LIMITED TO ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR AGAINST INFRINGEMENT, OR ANY EXPRESS OR IMPLIED WARRANTY ARISING OUT OF TRADE USAGE OR OUT OF A COURSE OF DEALING OR COURSE OF PERFORMANCE. NOTHING CONTAINED IN THIS AGREEMENT SHALL BE CONSTRUED AS (I) A WARRANTY OR REPRESENTATION BY QTI, ITS LICENSORS OR AFFILIATES AS TO THE VALIDITY OR SCOPE OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT OR (II) A WARRANTY OR REPRESENTATION BY QTI THAT ANY MANUFACTURE OR USE WILL BE FREE FROM INFRINGEMENT OF PATENTS, COPYRIGHTS OR OTHER INTELLECTUAL PROPERTY RIGHTS OF OTHERS, AND IT SHALL BE THE SOLE RESPONSIBILITY OF YOU TO MAKE SUCH DETERMINATION AS IS NECESSARY WITH RESPECT TO THE ACQUISITION OF LICENSES UNDER PATENTS AND OTHER INTELLECTUAL PROPERTY OF THIRD PARTIES.

1.5 **LIMITATION OF LIABILITY.** IN NO EVENT SHALL QTI, QTI'S AFFILIATES OR ITS LICENSORS BE LIABLE TO YOU FOR ANY INCIDENTAL, CONSEQUENTIAL OR SPECIAL DAMAGES, INCLUDING BUT NOT LIMITED TO ANY LOST PROFITS, LOST SAVINGS, OR OTHER INCIDENTAL DAMAGES, ARISING OUT OF THE USE OR INABILITY TO USE, OR THE DELIVERY OR FAILURE TO DELIVER, ANY OF THE MATERIALS, OR ANY BREACH OF ANY OBLIGATION UNDER THIS AGREEMENT, EVEN IF QTI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. THE FOREGOING LIMITATION OF LIABILITY SHALL REMAIN IN FULL FORCE AND EFFECT REGARDLESS OF WHETHER YOUR REMEDIES HEREUNDER ARE DETERMINED TO HAVE FAILED OF THEIR ESSENTIAL PURPOSE. THE ENTIRE LIABILITY OF QTI, QTI's AFFILIATES AND ITS LICENSORS, AND THE SOLE AND EXCLUSIVE REMEDY OF YOU, FOR ANY CLAIM OR CAUSE OF ACTION ARISING HEREUNDER (WHETHER IN CONTRACT, TORT, OR OTHERWISE) SHALL NOT EXCEED US$10.

2. **COMPLIANCE WITH LAWS; APPLICABLE LAW.** Any litigation or other dispute resolution between You and Us arising out of or relating to this Agreement, or Your relationship with Us will take place in the Southern District of California, and You and QTI hereby consent to the personal jurisdiction of and exclusive venue in the state and federal courts within that District with respect any such litigation or dispute resolution. This Agreement will be governed by and construed in accordance with the laws of the United States and the State of California, except that body of California law concerning conflicts of law. This Agreement shall not be governed by the United Nations Convention on Contracts for the International Sale of Goods, the application of which is expressly excluded.

3. **CONTRACTING PARTIES.** If the Materials are downloaded on any computer owned by a corporation or other legal entity, then this Agreement is formed by and between QTI and such entity. The individual accepting the terms of this Agreement represents and warrants to QTI that they have the authority to bind such entity to the terms and conditions of this Agreement.

4.**MISCELLANEOUS PROVISIONS.** This Agreement, together with all exhibits attached hereto, which are incorporated herein by this reference, constitutes the entire agreement between QTI and You and supersedes all prior negotiations, representations and agreements between the parties with respect to the subject matter hereof. No addition or modification of this Agreement shall be effective unless made in writing and signed by the respective representatives of QTI and You. The restrictions, limitations, exclusions and conditions set forth in this Agreement shall apply even if QTI or any of its affiliates becomes aware of or fails to act in a manner to address any violation or failure to comply therewith. You hereby acknowledge and agree that the restrictions, limitations, conditions and exclusions imposed in this Agreement on the rights granted in this Agreement are not a derogation of the benefits of such rights. You further acknowledges that, in the absence of such restrictions, limitations, con-

ditions and exclusions, QTI would not have entered into this Agreement with You. Each party shall be responsible for and shall bear its own expenses in connection with this Agreement. If any of the provisions of this Agreement are determined to be invalid, illegal, or otherwise unenforceable, the remaining provisions shall remain in full force and effect. This Agreement is entered into solely in the English language, and if for any reason any other language version is prepared by any party, it shall be solely for convenience and the English version shall govern and control all aspects. If You are located in the province of Quebec, Canada, the following applies: The Parties hereby confirm they have requested this Agreement and all related documents be prepared in English.