

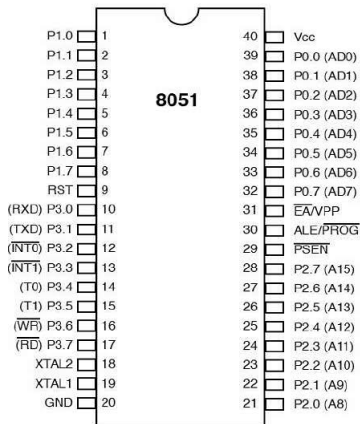
# 8051 Pinouts and Basic Circuitry

Richard Myrick T. Arellaga

Urdaneta City University

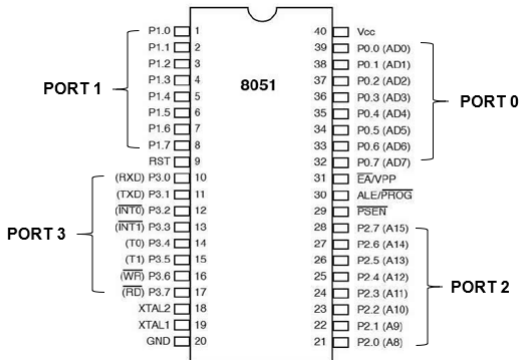
# 8051 Pinouts

- 40 Pins DIP Package
- Some pins have dual functionality



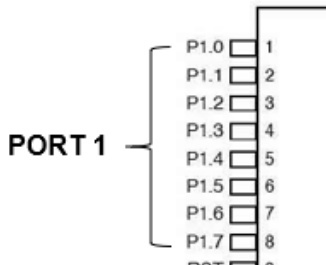
# I/O Ports

- Has 4 I/O Ports
- Each port is 8-bit wide



# I/O Ports

- Example Port 1, has 8 pins P1.0-P1.7
- Same is true for other ports.

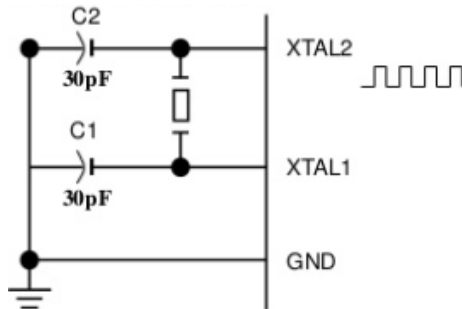


# Pins of 8051

- VCC (pin 40)
  - Provides supply voltage to the chip
  - Voltage source is +5V
- GND (pin 20) : Ground Pin
- XTAL1 and XTAL2 (pins 19,18):
  - Provides external Clock
  - Option 1 : Quartz Crystal Oscillator
  - Option 2: TTL Oscillator

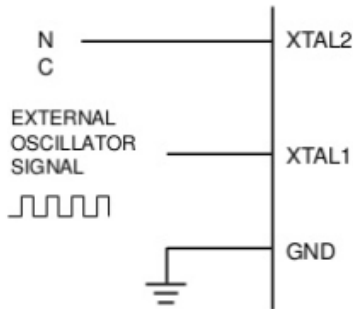
# Crystal Oscillator Connection

- Using a crystal oscillator
- 11.0592MHz  
Typical Value



## TTL Oscillator Connection

- TTL Oscillator can be formed from 74HC14
- XTAL2 is unconnected

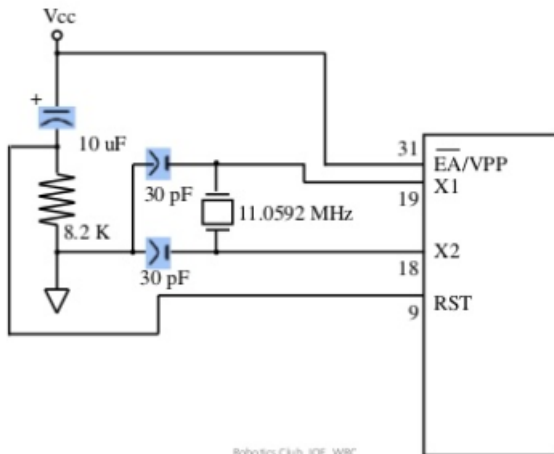


# Pins of 8051 - Reset Pin

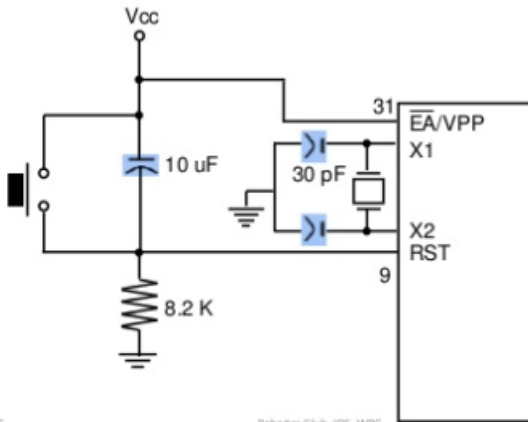
- RST (pin 9): Reset Pin
  - It is an input pin and is active high (normally low)
  - The high pulse must be high at least 2 machine cycles.
  - It is a power-on reset
  - Upon applying high pulse to RST, the microcontroller will reset and all values in registers will be lost.
  - Reset Circuit 1: Power-on Reset Circuit
  - Reset Circuit 2: Power-on Reset with Reset Switch



# Power-On Reset Circuit



# Power-On Reset Circuit with Switch



## Pins of 8051 - EA and PSEN

- /EA (pin 31): External Access
  - There is no on-chip ROM in 8031 and 8032
  - The /EA pin is connected to GND to indicate the code is stored externally.
  - /PSEN and ALE are used for external ROM.
  - For 8051, the /EA pin is connected to VCC.
  - " /" means active low.
- /PSEN (pin 29): Program Store Enable
  - This is an output pin and is connected to the OE of the ROM.

# Pins of 8051 - EA and PSEN

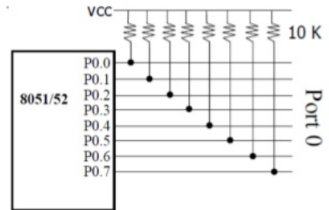
- $\overline{\text{ALE}}$  (pin 30): Address Latch Enable
  - It is an output pin and is active high.
  - 8051 port 0 provides both address and data.
  - The ALE pin is used for de-multiplexing the address and data by connecting to the G pin of the 74LS373 Latch
- I/O Port Pins
  - The four Ports P0, P1, P2 and P3
  - Each port uses 8 pins.
  - All I/O pins are bi-directional

# Pins of 8051 - I/O Port

- The 8051 four I/O Ports
  - Port 0 (pins 32-39) — P0 (P0.0-P0.7) Bit Address (0x80-0x87)
  - Port 1 (pins 1-8) — P1 (P1.0-P1.7) Bit Address (0x90-0x97)
  - Port 2 (pins 21-28) — P2 (P2.0-P2.7) Bit Address (0xA0-0xA7)
  - Port 3 (pins 10-17) — P3 (P3.0-P3.7) Bit Address (0xB0-0xB7)
  - Each port has **8 pins**
    - Named P0.x (x=0,1...7) — P1.x, P2.x, P3.x
    - Ex: P0.0 is the bit 0 (LSB) of P0
    - Ex: P0.7 is the bit 7 (MSB) of P0
    - These 8 bits form a byte
- Each port can be used as an input or output.

# PORT P0

- Provide three functions: I/O Port, Lower Order Address (A0-A7) and Data (D0-D7).
- Can be used for input or output
- Must be connected externally to a 10Kohm Pull-up Resistor.
- When  $ALE = 0$  it provides D0-D7
- When  $ALE = 1$  it had address A0-A7



# Pull-up Resistor

- Pull-up resistors pull the voltage of the signal it is connected to towards its voltage source level.
- It ensures that the wire is at a defined logic level even if no active devices are connected to it.
- At reset condition, the port zero will be at floating condition, i.e. no 0 no 1 something other state which we cannot predict (tri-state) so to ensure proper logic level we use Pull-up resistors.

## Port P1 and Port P2

- PORT 1 (Pin 1-8)
  - P1 is simple I/O Port
  - Internal pull up resistor is provided.
- PORT 2 (Pin 21 - 28)
  - P2 has dual functionality
  - It provides higher order address (A8-A15)
  - Must be used along with P0 to provide 16-bit address for external memory.
  - Internal pull-up resistor is provided.



# Port P3

- Pins 10-17
- can be used as input or output
- does not need any pull-up resistors.
- has additional function of providing some extremely important signals.

P3 Bit	Function	Pin	
P3.0	RxD	10	Serial communications
P3.1	TxD	11	
P3.2	$\overline{\text{INT0}}$	12	External interrupts
P3.3	$\overline{\text{INT1}}$	13	
P3.4	T0	14	Timers
P3.5	T1	15	
P3.6	$\overline{\text{WR}}$	16	Read/Write signals of external memories
P3.7	$\overline{\text{RD}}$	17	