

FPGA Based Braille to Text & Speech For Blind Persons

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Abstract—Blind people are an integral part of the society. However, their disabilities have made them to have less access to computers, the Internet, and high quality educational software than the people with clear vision. Consequently, they have not been able to improve on their own knowledge, and have significant influence and impact on the economic, commercial, and educational ventures in the society. One way to narrow this widening gap and see a reversal of this trend is to develop a system, within their economic reach, and which will empower them to communicate freely and widely using the Internet or any other information infrastructure. Over time, the Braille system has been used by the visually impaired for communication and contact with the outside world. This paper presents the implementation of Braille to Text/Speech Converter on FPGA Spartan3 kit. The actual Braille language is converted into English language in normal domain. The input is given through braille keypad which consists of different combinations of cells. This input goes to the FPGA Spartan3 Kit. According to the combinations given, FPGA converts the input into corresponding english text through the decoding logic in VHDL language. After decoding, the corresponding alphabet is converted to speech through algorithm. Also it is displayed on the LCD by interfacing the LCD to the Spartan3 kit.

Index Terms— FPGA, Braille language, text and speech converter, Visually impaired people, Web Browser for blind, content reorganization, Text to-speech, text to Braille.

1. Introduction

A key turning point for braille literacy was the passage of the Rehabilitation Act of 1973, an act of Congress that moved mainstream public schools. Because only a small percentage of public schools could afford to train and hire braille-qualified teachers, braille literacy has declined since the law took effect. Braille literacy rates have improved slightly since the bill was passed, in part because of pressure from consumers and advocacy groups that has led 27 states to pass legislation mandating that children who are legally blind be given the opportunity to learn braille. Early Braille education is crucial to literacy for a visually impaired child. A study conducted in the state of Washington found that people who learned braille at an early age did just as well, if not better, than their sighted peers in several areas, including vocabulary and comprehension. In the preliminary adult study, while evaluating the correlation between adult literacy skills and employment, it was found that 44% of the participants who had learned to read in braille were unemployed, compared to the 77% unemployment rate of those who had learned to read using print.

The National Census of India has estimated around 21.9 Million disabled people in the country. Out of which more than 15 million people in India are blind. This is considered to be the highest among all other disabilities. Three out of every five disabled children in the age group of 0-9 years have been reported to be visually impaired in India. Due to their inability in accessing information from written text documents, blind people face tremendous difficulties in accessing information[2]. Thus, in order to provide proper information access and to bridge the communication gap between the visually impaired and the sighted community, the need to build some advance technologically supported systems are utterly essential.

BRAILLE was invented by a blind Frenchman, Louis Braille, in 1829. Braille is comprised of a rectangular six-dot cell on its end, with up to 63 possible combinations using one or more of the six dots. Braille is embossed by hand (or with a machine) onto thick paper, and read with the fingers moving across on top of the dots. BRAILLE

thousands of children from specialized schools for the blind into

comprises of basic six dots, which are arranged in the form of matrix. The matrix is expressed in a 3 * 2 form as shown in fig 01.

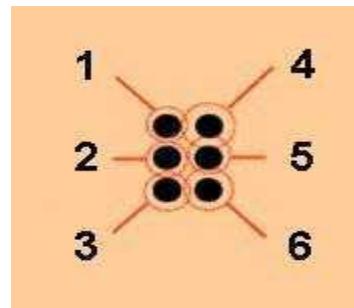


Fig. 01 Braille Cell.

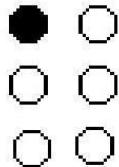
2. Literature review

A sight-blessed person can interact with the computer via different Input/Output devices, while a visually impaired person, on the other hand, is somehow forced to use specially designed devices or programs to interact with computers. The visually impaired person uses a variety of equipments and programs that enable him/her to enter data into computers or control them. Among these input devices are Braille keyboards Braille/Character scanners (Halousek, 1999; Sighted Electronics 2007; neovision, 2007; Mennens et al, 1994). However, with respect to the output devices, there is a wide difference in the use of computers by these two categories of users. A sight-blessed user eyereads the direct results of his/her work on the monitor or on a regular paper print, whereas a visually impaired person hand-read his/her output produced on a specially designed paper or device. Among the output devices used by the visually impaired are Braille displays (ATRC, 2007; Frontier Computing 2007; RINB 2007; Visio Technology, 2007), Screen readers (ATRC, 2007; Freedom Scientific,

2007; Ibsar, 2007), Braille Embossers (ATRC, 2007; Sighted Electronics 2007; neovision, 2007), and Screen magnifiers (ATRC, 2007; Sensus, 2007). There are also other assistive software packages and devices, designed exclusively for visually impaired people. Among these packages are Scientific Braille packages (Ley, 1999; Gardner, 1993, Sahyun, 1998), Braille Note Taker (Freedom Scientific, 2007), and The Reading Edge machine (Telesensory, 2007), tactile graphic display (NIST, 2007), PAC Mate BNS PocketPC (Freedom Scientific, 2007), and Digital Talking-Book Player (NLS, 2007).

3. System Implementation

The crux of the Design, Implementation is the conversion from the basic "Braille" language to real life English using FPGA. It is an acronym of Field Programmable Gate Array (FPGA). It is a union of the senses, hearing as well as sight. Braille comprises of a rectangular six-dot cell on its end, with up to 63 possible combinations using one or more of the six dots. Derivation of the 26 letters of the alphabet and the 10 numeric digits are shown in table 01. These 63 combination are converted into English language as follows, For example, the alphabet A isbet'A' is expressed as,



The alphabet 'C' is written as,

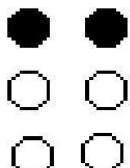


Fig. 02 Braille word interpretation

Braille Keyboard (I/P device), LCD (O/P device) and speaker (O/P device) are all interfaced to FPGA. Software will take the combination of all the six cells from I/P hardware, decode it and give the appropriate O/P on hardware. Whenever user provides Braille input, the same will be accepted and displayed on the screen, and accordingly speech output of character will be output. After accepting few characters, user will press play button. Device has to search that word in look up table and accordingly output it on speech device. The system block diagram is shown in fig. 03.

3.1 Spartan-3 FPGA

The Spartan-3 family of Field-Programmable Gate Arrays is specifically designed to meet the needs of high volume, cost-sensitive consumer electronic applications. The Spartan-3 family builds on the success of the earlier Spartan-IIIE family by increasing the amount of logic resources, the capacity of internal RAM, the total number of I/Os, and the overall level of performance as well as by improving clock management functions. Spartan-3 FPGA enhancements, combined with advanced process technology, deliver more functionality and

bandwidth per dollar than was previously possible, setting new standards in the programmable logic industry.

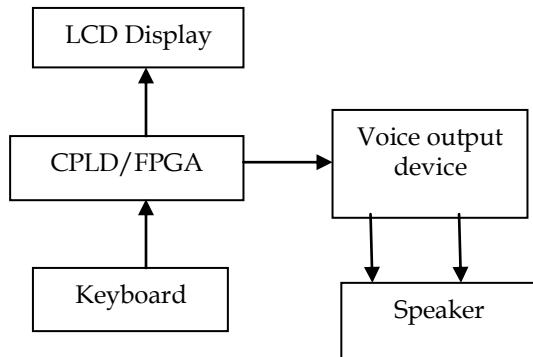


Fig 03 Sysytem block diagram

4. Architectural Overview

The Spartan-3 family architecture consists of five functional elements:

1. Configurable Logic Blocks (CLBs).
2. Input/Output Blocks (IOBs).
3. Block RAM.
4. Multiplier blocks.
5. Digital Clock Manager (DCM) are shown in fig. 04

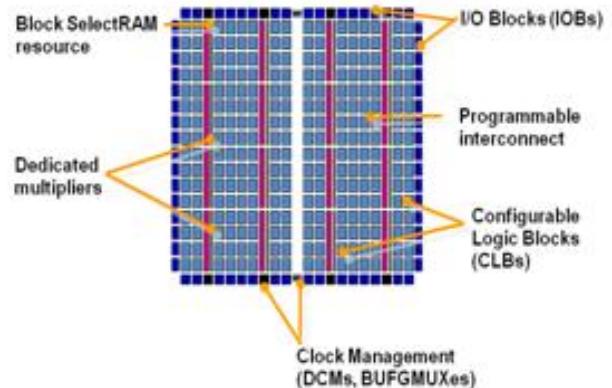


Fig. 04 Architecure of Spartan-3 family

4.1 Configurable Logic Blocks (CLBs)

CLB contain RAM-based Look-Up Tables (LUTs) to implement logic and storage elements that can be used as ip/ops or latches. CLBs can be programmed to perform a wide variety of logical functions. Each slice has four outputs, two registered outputs, two non-registered outputs, two BUFTs associated with each CLB, accessible by all 16 CLB outputs. Carry logic runs vertically, up only, two independent carry chains per CLB as shown in fig. 05.

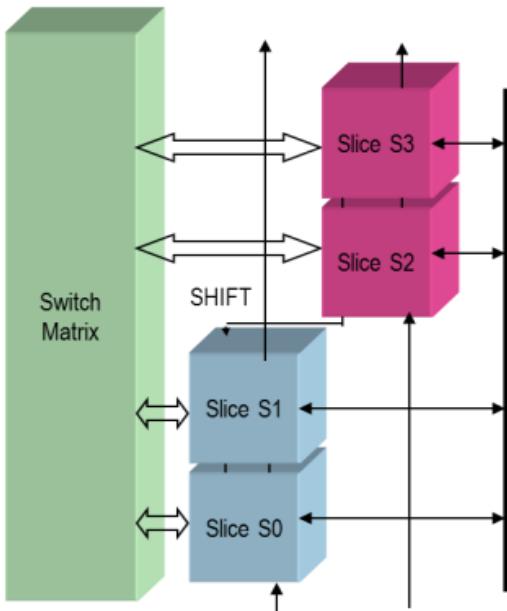


Fig. 05 Configurable Logic Blocks (CLBs)

4.2 Input/Output Blocks (IOBs)

Control the flow of data between the I/O pins and internal logic of the device. Each IOB supports bidirectional data flow plus 3-state operation. Twenty-six different signal standards, including eight high-performance differential standards, are available as shown in fig. 06. Double Data-Rate (DDR) registers are included. Input path, Two DDR registers. Output path, Two DDR registers, Two 3-state enable DDR registers. Separate clocks and clock enables for I and O. Set and reset signals are shared.

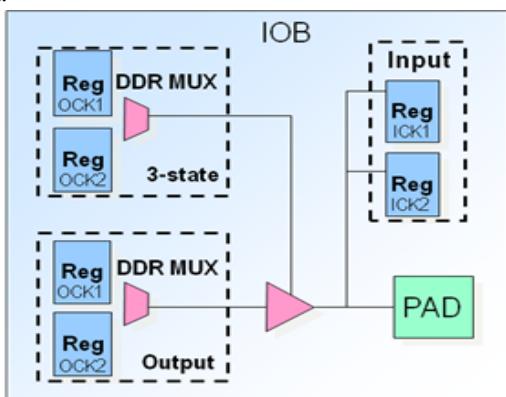


Fig. 06 Input/Output Blocks (IOBs)

4.3 Block RAM

Provides data storage in the form of 18-Kbit dual-port blocks. Up to 3.5 Mb of RAM in 18-kb blocks. Synchronous read and writes. True dual-port memory, each port has synchronous read and write capability. Different clocks for each port. Supports initial values. Synchronous reset on output latches. Supports parity bits. One parity bit per eight data bits as shown in fig. 07.

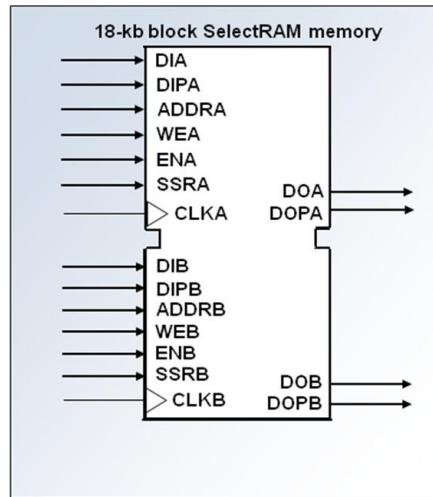


Fig. 07 Block RAM

4.4 Digital Clock Manager (DCM)

Multiplier blocks accept two 18-bit binary numbers as inputs and calculate the product. Digital Clock Manager (DCM) blocks provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase shifting clock signals. These elements are organized as shown in fig. 08. Ring of IOBs surrounds a regular array of CLBs. The XC3S50 has a single column of block RAM embedded in the array.

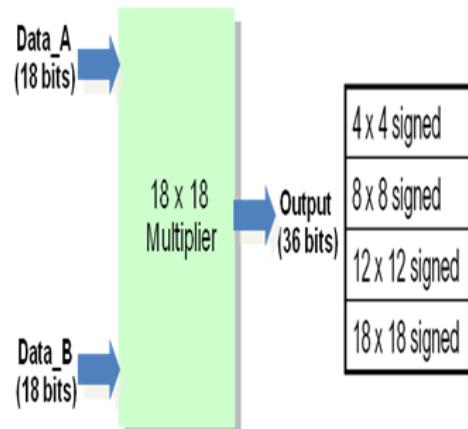


Fig. 08 Digital Clock Manager (DCM)

Those devices ranging from the XC3S200 to the XC3S2000 have two columns of block RAM. The XC3S4000 and XC3S5000 devices have four RAM columns. Each column is made up of several 18-Kbit RAM blocks; each block is associated with a dedicated multiplier. The DCMs are positioned at the ends of the outer block RAM columns.

4.5 Configuration

Spartan-3 devices are configured by loading application specific configuration data into the internal configuration memory. Configuration is carried out using a subset of the device pins, some of which are "Dedicated" to one function only, while others, indicated by the term "Dual-Purpose", can be re-used as general-purpose User I/Os once configuration is complete. Depending on the system design, several configuration modes are supported, selectable via mode pins. The mode pins M0,

M1, and M2 are dedicated pins. The mode pin settings are shown in Table 02.

Configuration Mode Pins						
Configura-tion Mode(1)	M0	M1	M2	Synchro-nization clock	Data Width	Serial D out
Master Serial	0	0	0	CCLK Output	1	Yes
Slave serial	1	1	1	CCLK Input	1	Yes
Master Parallel	1	1	0	CCLK Output	8	No
Slave parallel	0	1	1	CCLK Input	8	No
JTAG	1	0	1	TCK Input	1	No

Table 02 : Detailing about configuration of FPGA

Following are the steps followed when programming is done, 1. The HSWAPEN input pin defines whether the I/O pins that are not actively used during configuration have pull-up resistors during configuration. By default, HSWAPEN is tied High (via an internal pull-up resistor if left floating) which shuts off the pull-up resistors on the user I/O pins during configuration. When HSWAPEN is tied Low, user I/Os have pull-ups during configuration.

2. The dedicated configuration pins (CCLK, DONE, PROGB, M2, M1, M0, HSWAPEN) and the JTAG pins (TDI, TMS, TCK, and TDO) always have a pull-up resistor to VCCAUX during configuration, regardless of the value on the HSWAPEN pin. Similarly, the dual-purpose INITB pin has an internal pull-up resistor to VCCO4 or VCCOBOTTOM, depending on the package style.

3. Depending on the chosen configuration mode, the FPGA either generates a CCLK output, or CCLK is an input accepting an externally generated clock. A persist option is available which can be used to force the configuration pins to retain their configuration function even after device configuration is complete. If the persist option is not selected then the configuration pins with the exception of CCLK, PROGB, and DONE can be used as user I/O in normal operation.

The maximum bitstream length that Spartan-3 FPGAs support in serial daisy-chains is 4,294,967,264 bits (4 Gbits), roughly equivalent to a daisy-chain with 323 XC3S5000 FPGAs. This is a limit only for serial daisy-chains where configuration data is passed via the FPGAs DOUT pin. There is no such limit for JTAG chains.

5. Programming Technologies

It is used to control the programmable switches that give FPGAs their programmability.

1. Flash/EEPROM Programming Technology is Non Volatile, Fast, Cannot reprogrammed an infinite no. of time, use non standard cmos process

2. Anti-fuse Programming Technology - Here link is permanent,The primary advantage of anti-fuse programming technology is its low area,Non-volatility also means that the device works instantly once programmed.

3. Static Memory Programming Technology: SRAM-based re-programmable:Must be reprogrammed each time powered up,This is usually accomplished by using a small serial PROM.

5.1 System Flowchart

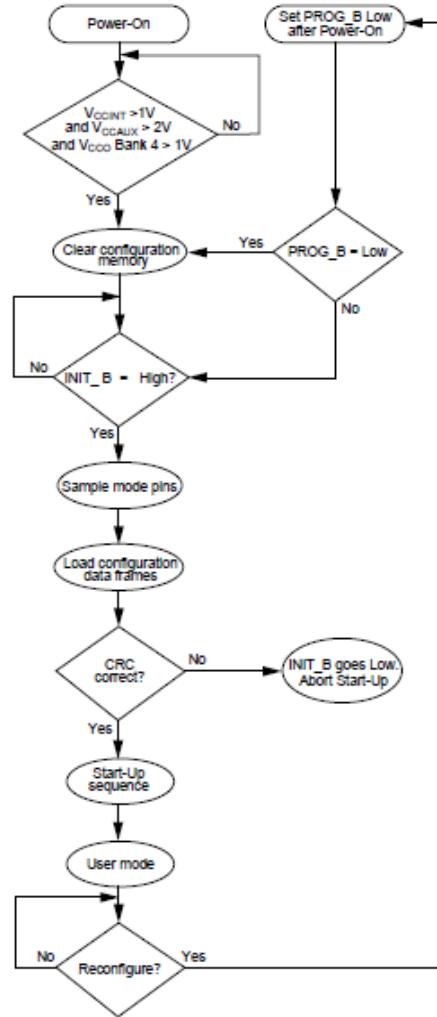


Fig. 09 Flowchart for Slave Serial mode

Of all the above XC3S400 contains Static Memory Programming Technology Steps Involved in designing are shown in following flowchart. Fig. 09 & Fig 10 gives the flowchart for the designed system.

- Design description
- Behavioral simulation (Source code interpretation)
- Synthesis
- Functional or Gate level simulation
- Implementation
- Fitting
- Place and Route
- Timing or Post layout simulation
- Programming, Test and Debug

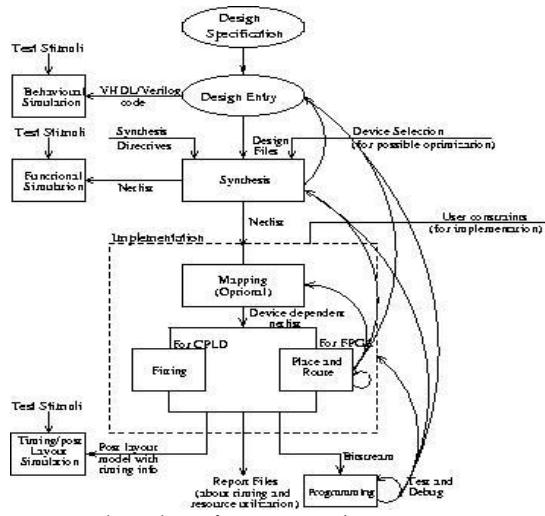


Fig. 10 Flowchart for system design

6. Applications

1. Braille language is basically for blind people and hence the only way they can get literate is through this language. If a new personnel wishes to learn this language this project will help him to get acquainted with this language. As he presses the Braille keyboard, the character will be displayed and he will be able to hear that character or word.

2. Apart from the one discussed above, it can also be used for typing e.g. if a blind personnel wants to write or type then the Braille equivalent that has been given as input will be converted to English and the person who is typing can also get a confirmation about what is being typed. Say if "hello" is being typed then this system will pronounce h, e, l, l, o every time that character is being pressed and prevent the occurrence of mistakes.

7. Conclusion & Result

The implementation of FPGA based Braille to Text Converter is successful. Here we have succeeded in giving input to FPGA through Xilinx Impact software and corresponding text output is displayed on the LCD screen. We simulated the program, and downloaded it on the FPGA kit. FPGA Spartan 3 IC XC3S400 is a very fast, low power consuming and efficient IC. One main advantage of the Spartan 3 IC is we can adjust the internal hardware circuitry according to the software coding. The rustle of the projects are shown in fig. 11, fig. 12, Fig. 13, Fig. 14 and

Fig. 11 Prgram running succesfully

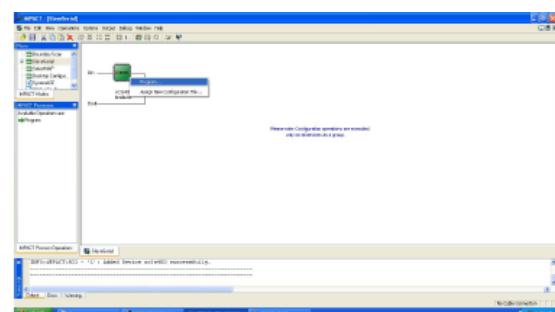


Fig. 12 Program output

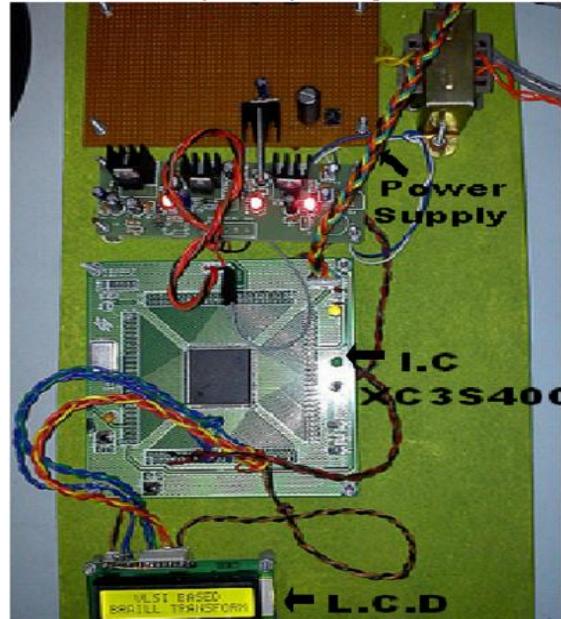


Fig. 13 Implemented circuit for the designed system



Fig. 14 Output for the designed system

Derivation of the 26 letters of the alphabet from the 10 numeric digits									
● ○ ○ ○ ○ ○	● ○ ● ○ ○ ○	● ● ○ ○ ○ ○	● ● ○ ○ ○ ○	● ○ ○ ○ ○ ○	● ● ● ○ ○ ○	● ● ● ○ ○ ○	● ○ ● ○ ○ ○	○ ● ● ○ ○ ○	○ ● ● ○ ○ ○
a/1	b/2	c/3	d/4	e/5	f/6	g/7	h/8	i/9	j/0
● ○ ○ ○ ● ○	● ○ ● ○ ● ○	● ● ○ ○ ● ○	● ● ○ ○ ● ○	● ○ ○ ○ ● ○	● ● ● ○ ● ○	● ● ● ○ ● ○	● ○ ● ○ ● ○	○ ● ● ○ ● ○	○ ● ● ○ ● ○
k	l	m	n	o	p	q	r	s	t
● ○ ○ ○ ● ○ ● ● ● ●	● ○ ● ○ ● ○ ● ● ● ●	● ● ○ ○ ● ○ ● ● ● ●	● ● ○ ○ ● ○ ● ● ● ●	● ○ ○ ○ ● ○ ● ● ● ●					○ ● ● ● ● ● ● ● ● ●
u	v	x	y	z					w

Table 01. Derivation of the 26 letters of the alphabet from the 10 numeric digits

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