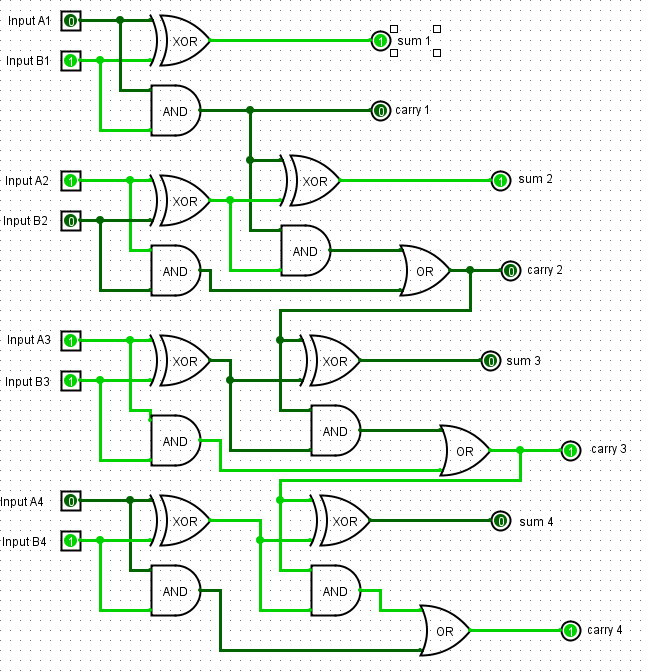
**COS 10004 Computer Systems – Lab 01**

**Mario Stavreski ID: 103055993**

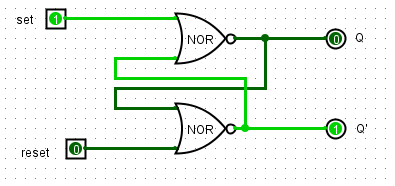
# 4 bit Adder



|  |  |  |
| --- | --- | --- |
| Input A | Input B | Output |
| 0101 | 0000 | 0101 |
| 0101 | 0001 | 0110 |
| 0101 | 0010 | 0111 |
| 0101 | 0011 | 1000 |
| 0101 | 0100 | 1001 |
| 0101 | 0101 | 1010 |
| 0101 | 0110 | 1011 |
| 0101 | 0111 | 1100 |
| 0101 | 1000 | 1101 |
| 0101 | 1001 | 1110 |
| 0101 | 1010 | 1111 |
| 0101 | 1011 | 0000 |
| 0101 | 1100 | 0001 |
| 0101 | 1101 | 0010 |
| 0101 | 1110 | 0011 |
| 0101 | 1111 | 0100 |

# Part 2: Storing bits with Flip Flops

# R-S Flip Flop



|  |  |  |  |
| --- | --- | --- | --- |
| Set | Reset | Q | Q’ |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 |

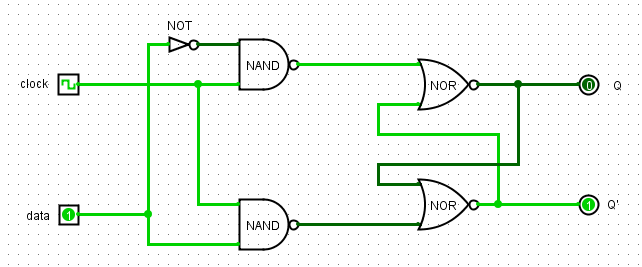
Describe in a sentence, the behaviour of the circuit when one of the inputs is 1 (but not both) and why this is useful for digital circuit design.

* **The R-S Flip Flop is composed of coupled NOR gates which have been crossed in the diagram. It provides a simple switching function whereby a pulse on one input line of the flip flop sets the circuit in one state.**

What do you notice about the two times you set both inputs to 1. Briefly explain what is happening here and why this is an issue for digital circuit design ?

* **If we set both the set and reset to 1 it will enter an illegal state. This creates an issue for the circuit design as the flip flop output should support and supplement each other.**

# D Flip Flops



|  |  |  |  |
| --- | --- | --- | --- |
| Clock | Data | Q | Q’ |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |

Briefly explain the behaviour of a D Flip Flop and how it is useful for digital circuit design.

* **The D flip flop only has 1 data input and the clock is used to control the signal. Q is set to be reversed as D and Q’ is the same as D when the clock is on.**

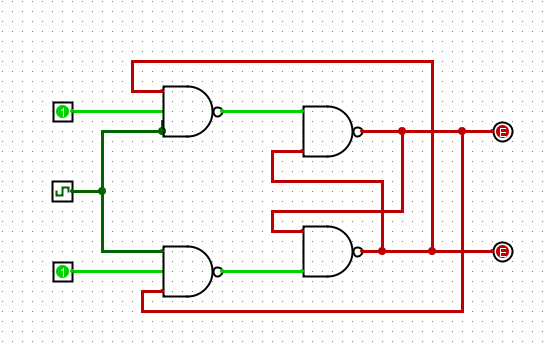
What is the role of the clock ? How does it impact the changing of state of Q and Q’?

* **The clock is used to control the signal**

Why is it generally preferred over the R-S Flip Flop ?

* **It prevents the circuit from entering an illegal state and the clock can be used to synchronise data.**

# J-K Flip Flop



How can a J-K Flip Flop be made to behave like a D Flip Flop?

**The J-K Flop Flop can behave like a D Flip Flop as it adds one more input which connects with the NAND gate and removes the NOT gate.**

How can a J-K Flip Flop be made to behave like a toggle (T Flip Flop)?

**If the two inputs are on, the J-K Flip Flop behaves like a toggle.**