SAM L10/L11 Family

Silicon Errata and Data Sheet Clarification

SAM L10/L11 Family

The SAM L10/L11 family of devices that you have received conform functionally to the current Device Data Sheet (DS60001513G), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the following tables. The silicon issues are summarized in the Silicon Issue Summary.

The errata described in this document will be addressed in future revisions of the SAM L10/L11 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data Sheet clarifications and corrections (if applicable) are located in 3. Data Sheet Clarifications, following the discussion of silicon issues.

Table 1. SAM L10 Family Silicon Device Identification

Part Number	Device ID (DID[31:0])	Revision (DID.REVISION[3:0])
		B
SAML10E16A	0x2084xx00	0x1
SAML10E15A	0x2084xx01	
SAML10E14A	0x2084xx02	
SAML10D16A	0x2084xx03	
SAML10D15A	0x2084xx04	
SAML10D14A	0x2084xx05	

Table 2. SAM L11 Family Silicon Device Identification

Part Number	Device ID (DID[31:0])	Revision (DID.REVISION[3:0])
		B
SAML11E16A	0x2083xx00	0x1
SAML11E15A	0x2083xx01	
SAML11E14A	0x2083xx02	
SAML11D16A	0x2083xx03	
SAML11D15A	0x2083xx04	
SAML11D14A	0x2083xx05	

Note: Refer to the “Device Service Unit” chapter in the current Device Data Sheet (DS60001513G) for detailed information on Device Identification and Revision IDs for your specific device.

Table of Contents

1. Silicon Issue Summary

Table 1-1. Silicon Issue Summary

Module	Feature	Errata Number	Summary	Device	Affected Silicon Revisions
					B
ADC	Reference Buffer Offset Compensation	2.1.1	First ADC conversions are incorrect when using Reference Buffer Offset Compensation.	SAM L10	X
				SAM L11	X
ADC	Offset Correction	2.1.2	Offset correction is not supported in the 8-bit and 10-bit conversion resolution.	SAM L10	X
				SAM L11	X
CCL	PAC protection	2.2.1	Writing the Software Reset bit in the Control A register will trigger a PAC protection error.	SAM L10	X
				SAM L11	X
CCL	Enable-protected Registers	2.2.2	The SEQCTRL0 and LUCTRL0/1 registers are enable-protected by the CTRL.ENABLE bit.	SAM L10	X
				SAM L11	X
CCL	Sequential logic	2.2.3	LUT Output is corrupted after enabling CCL when sequential logic is used.	SAM L10	X
				SAM L11	X
Device	Temperature sensor	2.3.1	Temperature sensor is not functional.	SAM L10	X
				SAM L11	X
Device	Standby Entry	2.3.2	Potential hard fault upon standby entry when Systick interrupt is enabled	SAM L10	X
				SAM L11	X
DMAC	Concurrent Channels Trigger	2.4.1	When using concurrent channel triggers, DMA write-back descriptors may get corrupted.	SAM L10	X
				SAM L11	X
EIC	PAC protection	2.5.1	8-bit and 16-bit reads/writes on the reserved areas of the EIC registers mapping starting from EVCTRL register do not generate a PAC protection error.	SAM L10	X
				SAM L11	X
FREQM	PAC protection	2.6.1	FREQM reads on the Control B register generate a PAC protection error.	SAM L10	X
				SAM L11	X
MCLK	PAC protection	2.7.1	Writes to the MCLK Control A register do not generate a PAC protection error even if this register has been write-protected using the PAC.	SAM L10	X
				SAM L11	X
MCLK	DFLLULP clock	2.7.2	Hardfault exception after having selected DFLLULP clock as main clock.	SAM L10	X
				SAM L11	X
OPAMP	Reference buffer	2.8.1	The internal reference REFBUF is not generated when the voltage doubler is disabled.	SAM L10	X
				SAM L11	X
OPAMP	High Gain Instrumentation Amplifier	2.8.2	High Gain Instrumentation Amplifier is not functional.	SAM L10	X
				SAM L11	X
RTC	Tamper detection	2.9.1	Tamper detection limitation when CTRLB.SEPTO = 0.	SAM L10	X
				SAM L11	X
RTC	Event generation	2.9.2	Periodic Daily Event (PERD) Event Generator never occurs in Clock/Calendar mode.	SAM L10	X
				SAM L11	X
RTC	Write corruption	2.9.3	RTC COUNT and CLOCK registers write corruption.	SAM L10	X
				SAM L11	X

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Module	Feature	Errata Number	Summary	Device	Affected Silicon Revisions
					B
RTC	Tamper Detection Timestamp	2.9.4	If an external reset occurs during a tamper detection, the TIMESTAMP register will not be updated when next tamper detection is triggered.	SAM L10	X
				SAM L11	X
RTC	Prescaler	2.9.5	When the tamper or debouncing features (TAMPCTRL) are enabled, periodic interrupts and events are generated when the prescaler is OFF (CTRLA.PRESCALER=0).	SAM L10	X
				SAM L11	X
RTC	Active Layer Protection	2.9.6	Active Layer Protection feature is limited to one tamper channel n (i.e. one RTC INn/OUTn pair).	SAM L10	X
				SAM L11	X
RTC	Tamper Detection Timestamp	2.9.7	The INTFLAG.TAMPER bit is not reset by reading the TIMESTAMP register.	SAM L10	X
				SAM L11	X
RTC	Tamper Detection Timestamp	2.9.8	A wrong timestamp value can be returned if more than one CPU and DMA accesses to the TIMESTAMP register are performed upon a INTFLAG.TAMPER assertion.	SAM L10	X
				SAM L11	X
RTC	Tamper Detection	2.9.9	If the Tamper Channel n Action is set to WAKE or CAPTURE and the Active Layer Protection is enabled for this channel, no tampers are detected on this channel n.	SAM L10	X
				SAM L11	X
RTC	Tamper Detection	2.9.10	False tamper detections may occur when configuring the RTC INn and OUTn pins.	SAM L10	X
				SAM L11	X
RTC	General Purpose Registers	2.9.11	General Purpose Registers n (GPn) are reset on tamper detection even if GPTRST = 0.	SAM L10	X
				SAM L11	X
RTC	Active Layer Protection	2.9.12	When the RTC is configured in Active Layer Protection mode (TAMPCTRL.INACT = 0x3) and the RTC CTRLA.ENABLE bit is not set, a tamper can be detected and a timestamp captured. The TAMPID register and INTFLAG.TAMPER bit may not be set.	SAM L10	X
				SAM L11	X
SERCOM I^2C	High-speed mode	2.10.1	When configured in HS or Fast-Mode Plus, SDA and SCL fall times are shorter than I^2C specification requirement and can lead to reflection.	SAM L10	X
				SAM L11	X
SERCOM I^2C	Repeated start	2.10.2	Bus error is generated during a Repeated Start (when QCEN = 1 and SCLSM = 1).	SAM L10	X
				SAM L11	X
SERCOM I^2C	Repeated Start / Host mode 10-bit	2.10.3	Repeated Start in 10-bit addressing mode for Host Write operations does not work.	SAM L10	X
				SAM L11	X
SERCOM I^2C	Repeated Start / Host mode 10-bit	2.10.4	Repeated Start is not supported for High-Speed mode Host Read operations.	SAM L10	X
				SAM L11	X
SERCOM I^2C	Repeated Start / High-Speed mode	2.10.5	Repeated Start is not supported for High-Speed mode Host Write operations.	SAM L10	X
				SAM L11	X
SERCOM I^2C	Client Mode with DMA	2.10.6	Character lost in I^2C Client mode with DMA when a NACK occurs.	SAM L10	X
				SAM L11	X
SERCOM I^2C	Client mode 10-bit	2.10.7	I^2C Client 10-bit addressing mode is not functional.	SAM L10	X
				SAM L11	X
SERCOM I^2C	Status Flags	2.10.8	BUSERR, COLL, LOWTOUT, SEXTTOUT and LENERR Status register bits are not automatically cleared.	SAM L10	X
				SAM L11	X
SERCOM I^2C	Status Flags	2.10.9	The CLKHOLD Status bit is not read only.	SAM L10	X
				SAM L11	X

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Module	Feature	Errata Number	Summary	Device	Affected Silicon Revisions
					B
SERCOM I2C	Status Flags	2.10.10	When an unexpected STOP occurs on the I2C bus the STATUS.BUSERR & INTFLAG.ERROR bits are set but may not wake the system from sleep mode.	SAM L10	X
				SAM L11	X
SERCOM I2C	Automatic Acknowledge	2.10.11	The I2C Client Automatic Acknowledge feature (CTRLB.AACKEN = 1) is not supported when doing a repeated start.	SAM L10	X
				SAM L11	X
SERCOM SPI	Data Preload	2.11.1	In SPI Client mode with Client Data Preload Enabled, the client transmitter may discard some data if the host cannot keep the SPI Select pin low until the end of transmission.	SAM L10	X
				SAM L11	X
SERCOM SPI	Hardware SPI Select Control	2.11.2	When Hardware SPI Select Control is enabled, the SPI Select ($\overline{SS}$) pin goes high after each byte transfer.	SAM L10	X
				SAM L11	X
SERCOM SPI	Client Data Preload	2.11.3	Preloading a new SPI data before going into Standby Sleep mode, may lead to extra power consumption.	SAM L10	X
				SAM L11	X
SERCOM SPI	Wakeup Interrupt	2.11.4	The Data Register Empty (DRE) wake-up interrupt is not de-asserted when the register interrupt is cleared (INTFLAG.DRE=0).	SAM L10	X
				SAM L11	X
SERCOM USART	Inverted Bits	2.12.1	The TXINV and RXINV bits in the CTRLA register have inverted functionality.	SAM L10	X
				SAM L11	X
SERCOM USART	ISO7816 Mode	2.12.2	In ISO7816 mode, the SERCOM bus clock continues to run in Stand-by Sleep mode causing an extra power consumption.	SAM L10	X
				SAM L11	X
SERCOM USART	Debug Mode	2.12.3	Debug mode is not functional.	SAM L10	X
				SAM L11	X
SERCOM USART	Collision Detection	2.12.4	Collision Detection does not stop Data Transfer.	SAM L10	X
				SAM L11	X
SERCOM USART	Wakeup	2.12.5	The USART does not wake up the device on Error (INTFLAG.ERROR=1) interrupt.	SAM L10	X
				SAM L11	X
SERCOM USART	Overconsumption in Standby Mode	2.12.6	Unexpected over-consumption in standby mode	SAM L10	X
				SAM L11	X
SERCOM USART	Wakeup Interrupt	2.12.7	The Data Register Empty (DRE) wake-up interrupt is not de-asserted when the register interrupt is cleared (INTFLAG.DRE = 0).	SAM L10	X
				SAM L11	X
TC	Flags Synchronization	2.13.1	The SYNCBUSY.PER/SYNCBUSY.CCx flags are released before the PERBUF/CCBUFx registers are restored to their expected value.	SAM L10	X
				SAM L11	X
TC	Capture mode / Over consumption	2.13.2	Over consumption in Capture mode when entering Standby mode.	SAM L10	X
				SAM L11	X
TC	Retrigger	2.13.3	If a Retrigger event occurs at the Channel Compare Match [n] time, the next Waveform Output [n] is missing or disturbed.	SAM L10	X
				SAM L11	X
TC	PER Register (8-bit mode)	2.13.4	In 8-bit Mode, PER register updates using the DMA are not possible in standby mode.	SAM L10	X
				SAM L11	X
TRNG	Over consumption	2.14.1	When TRNG is disabled, some internal logic could continue to operate causing an over consumption.	SAM L10	X
				SAM L11	X

.....continued

Module	Feature	Errata Number	Summary	Device	Affected Silicon Revisions
					B
SUPC	Buck Converter Mode	2.15.1	Digital Phase-Locked Loop FDPLL96M cannot be used with main voltage regulator in Buck Converter mode.	SAM L10	X
				SAM L11	X
OSC32KCTRL	External 32.768KHz Crystal Oscillator	2.16.1	External 32.768KHz crystal oscillator operation is not supported over the full temperature range of -40°C to +125°C.	SAM L10	X
				SAM L11	X
OSC32KCTRL	1024 Hz Clock Output	2.16.2	1024 Hz clock output spikes can lead to wrong RTC or Watchdog counting.	SAM L10	X
				SAM L11	X
OSC32KCTRL	Clock Failure Detection	2.16.3	Re-enabling the Clock Failure Detector when the XOSC32K is enabled can lead to a false Clock Failure Detection.	SAM L10	X
				SAM L11	X
OSC32KCTRL	XOSC32K Ready bit	2.16.4	The XOSC32K Ready bit of the STATUS register is not cleared when disabling the XOSC32K bit at the same time as the Crystal Oscillator	SAM L10	X
				SAM L11	X
Boot ROM	GCM API	2.17.1	GCM API does not follow the Procedure Call Standard for the ARM Architecture (AAPCS)	SAM L10	
				SAM L11	X
EVSYS	Synchronous and Resynchronized Modes	2.18.1	Spurious Overrun Interrupt following a software event.	SAM L10	X
				SAM L11	X
EVSYS	Synchronous Mode	2.18.2	Spurious Overrun Interrupt when the generic clock for a channel is always on.	SAM L10	X
				SAM L11	X
EVSYS	Spurious Overrun	2.18.3	Overrun interrupt flag may be incorrectly set upon software events in synchronous/resynchronized path modes with event detection on both rising and falling edges.	SAM L10	X
				SAM L11	X
EVSYS	Software Event	2.18.4	CHBUSY flag never reset upon software events in synchronous/ resynchronized path modes with event detection on falling edges.	SAM L10	X
				SAM L11	X
EVSYS	PAC Write-Protection	2.18.5	PAC Write-Protection is not functional for the NSCHKCHAN and NSCHKUSER registers.	SAM L10	X
				SAM L11	X
OSCCTRL	Clock Failure Detection	2.19.1	When the XOSC Clock Failure Detector is enabled and a failure is detected, the XOSC Ready bit is not cleared.	SAM L10	X
				SAM L11	X
OSCCTRL	Clock Failure Detection	2.19.2	Re-enabling the Clock Failure Detector when the XOSC is enabled can lead to a false Clock Failure Detection.	SAM L10	X
				SAM L11	X
OSCCTRL	XOSC Ready Bit	2.19.3	The XOSC Ready bit of the STATUS register is not cleared when disabling the XOSC at the same time as the Crystal Oscillator.	SAM L10	X
				SAM L11	X
OSCCTRL	FDPLL96M On Demand in Standby	2.19.4	The FDPLL96M On Demand mode is not functional in Standby sleep mode.	SAM L10	X
				SAM L11	X
OSCCTRL	DFLLULP Dithering Mode	2.19.5	DFLLULP dithering mode is not functional.	SAM L10	X
				SAM L11	X
PORT	IOBUS	2.20.1	Concurrent accesses on the PORT peripheral registers between the ARM APB and the ARM CPU IOBUS are not supported.	SAM L10	X
				SAM L11	X
TRAM	PAC Protection	2.21.1	Security RAM n registers (RAMn) are not PAC Write-Protected.	SAM L10	X
				SAM L11	X

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Module	Feature	Errata Number	Summary	Device	Affected Silicon Revisions
					B
NVMCTRL	Data FLASH Silent Access and Scrambling	2.22.1	Silent Access and Scrambling on the Data FLASH are not functional when both are enabled.	SAM L10	
				SAM L11	X

2. SAM L10/L11 Errata Issues

The following issues apply to the SAM L10/L11 Family devices.

2.1 Analog-to-Digital Converter (ADC)

2.1.1 Reference Buffer Offset Compensation Reference:CHIP003-247, ADC101-11

TUE of the ADC conversion result is out of specification when,

- Using the reference source as REFCTRL.REFSEL ≠ VDDANA
  and
- Reference Buffer Offset Compensation is enabled (REFCTRL.REFCOMP = 1)

Workaround

The first five conversions after enabling ADC must be ignored. All further ADC conversions are within the specification.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.1.2 Offset Correction Reference:ADC101-16

Offset correction using the OFFSETCORR register is not supported in the 8-bit and 10-bit conversion resolution.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.2 Configurable Custom Logic (CCL)

2.2.1 PAC Protection Reference: CLA100-6

Writing the Software Reset bit in the Control A register (CTRLA.SWRST) will trigger a PAC protection error.

Workaround

Clear the CCL PAC error each time a CCL software reset is executed.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.2.2 Enable Protected Registers Reference: CLA100-33

The SEQCTRL0 and LUCTRL0/1 registers are enable-protected by the CTRL.ENABLE bit whereas they should be enable-protected by the LUTCTRL0/1.ENABLE bits.

Workaround
None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.2.3 Sequential Logic Reference: CLA100-32

LUT Output is corrupted after enabling CCL when sequential logic is used.

Workaround
Write the CTRL register twice when enabling the CCL.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.3 DEVICE

2.3.1 Temperature Sensor Reference: CHIP003-299

Temperature Sensor is not functional.

Workaround
None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.3.2 Standby Entry Reference: CHIP003-325

When the Systick interrupt is enabled and the standby back-bias option is set (STDBYCFG.BBIAS = 1), a hard fault can occur when the Systick interrupt coincides with the standby entry.

Workaround

Disable the Systick interrupt before entering standby and re-enable it after wake up.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.4 Direct Memory Access Controller (DMAC)

2.4.1 Concurrent Channels Trigger Reference: DMA100-17

When using concurrent channels triggers, DMAC write-back descriptors may get corrupted.

Workaround

Multiple transfers must only be sequenced using linked descriptors on a single channel.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.5 External Interrupt Controller (EIC)

2.5.1 PAC Protection Reference: INT103-3, INT103-46

8-bit and 16-bit reads/writes on the reserved areas of the EIC registers mapping starting from the EVCTRL register do not generate a PAC protection error.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.6 Frequency Meter (FREQM)

2.6.1 PAC Protection Reference: CLK101-9

FREQM reads on the Control B register (FREQM.CTRLB) generate a PAC protection error.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.7 Main Clock (MCLK)

2.7.1 PAC Protection Reference: CLK107-7

Writes to the MCLK Control A register (MCLK.CTRLA) do not generate a PAC protection error even if this register has been write-protected using the PAC.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.7.2 DFLLULP Clock Reference: CLK107-8

A Hard fault exception can occur after selecting the DFLLULP clock as main clock source (CTRLA.CKSEL = 1).

Workaround

Add 6 NOP instructions after writing the CTRAL.CKSEL bit.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.8 Operational Amplifier Controller (OPAMP)

2.8.1 Reference Buffer Reference: OPAMP100-4

The internal reference REFBUF is not generated when the Low-Power Mux feature is enabled (CTRLA.LPMUX = 1).

Workaround

Disable the Low-Power Mux feature (CTRLA.LPMUX = 0) when the internal REFBUF is used.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.8.2 High Gain Instrumentation Amplifier Reference: OPAMP100-7

High Gain Instrumentation Amplifier is not functional.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9 Real Time Clock (RTC)

2.9.1 Tamper Detection Reference: TMR102-44

When the RTC Separate Tamper Outputs (SEPTO) bit of the CTRLB register is cleared (CTRLB.SEPTO = 0) and the Active layer protection 0 (ALSI0) bit of the TAMPCTRLB register is set (TAMCTRLB.ALSI0 = 1), the RTC pseudo random pattern is only generated on the TrustRAM Active layer.

Workaround
Set the CTRLB.SEPTO bit to '1' if Tamper Detection is required on the RTC Tamper pins.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9.2 Event Generation Reference: TMR102-45

In RTC Clock mode or Calendar mode (CTRLA.MODE = 2), the Periodic Daily Event (PERD) is not generated.

Workaround
None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9.3 Write Corruption Reference: TMR102-46

A 8-bit or 16-bit write access for a 32-bit register, or 8-bit write access for a 16-bit register can fail for the following registers:

- The COUNT register in COUNT32 mode
- The COUNT register in COUNT16 mode
- The CLOCK register in CLOCK mode

Workaround
Write the registers with:

- A 32-bit write access for:
  - The COUNT register in COUNT32 mode
  - The CLOCK register in CLOCK mode
- A 16-bit write access for:
  - The COUNT register in COUNT16 mode

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9.4 Tamper Detection Timestamp Reference: TMR102-48

If an external reset occurs during a tamper detection, the TIMESTAMP register will not be updated when next tamper detection is triggered.

Workaround

Enable RTC tamper interrupt and copy the timestamp from the RTC CLOCK register to one of the following locations:

- SRAM
- GPx register in RTC

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9.5 Prescaler Reference: TMR102-52

When the tamper or debouncing features (TAMPCTRL) are enabled, periodic interrupts and events are generated when the prescaler is OFF (CTRLA.PRESCALER = 0).

Workaround

When the prescaler is OFF (CTRLA.PRESCALER = 0), clear the Periodic Interval n Event Output Enable bits (EVCTRL.PEREOn [n = 7...0]) and the respective Periodic Interval n Interrupt Enable (INTENCLR.PERn [n = 7...0]) bits.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9.6 Active Layer Protection Reference: TMR102-66

Active Layer Protection feature is limited to one tamper channel n (i.e. one RTC INn/OUTn pair). Any other tamper channels can be used either in Wake mode or Capture mode.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9.7 Tamper Detection Timestamp Reference: TMR102-67

The INTFLAG.TAMPER bit is not reset by reading the TIMESTAMP register.

Workaround

Clear the INTFLAG.TAMPER bit by writing a '1' to this bit when the Timestamp value has been read from the TIMESTAMP register.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9.8 Tamper Detection Timestamp Reference: TMR102-60

A wrong timestamp value can be returned if more than one CPU and DMA accesses to the TIMESTAMP register are performed upon a INTFLAG.TAMPER assertion.

Workaround

The timestamp value captured in the TIMESTAMP register must be retrieved as described below:

- If RTC can trigger a DMA request when the timestamp value is available (CTRLB.DMAEN = 1):
  - Wait for DMA transfer completion to read the timestamp value from the DMA buffers.
  - Clear the INTFLAG.TAMPER bit.

Note: Do not read the timestamp value from the TIMESTAMP register.

- If RTC cannot trigger a DMA request when the timestamp value is available (CTRLB.DMAEN = 0):
  - Wait for the INTFLAG.TAMPER bit to read the timestamp value from the TIMESTAMP register.
  - Clear the INTFLAG.TAMPER bit.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9.9 Tamper Detection Reference: TMR102-62

If the Tamper Channel n Action (TAMPCTRL.INnACT) is set to WAKE or CAPTURE and the Active Layer Protection is enabled for this channel (TAMPCTRLB.ALSIn = 1), no tampers are detected on this channel n.

Workaround

Clear the TAMPCTRLB.ALSIn bits for the channels configured in WAKE or CAPTURE modes.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9.10 Tamper Detection Reference: TMR102-63

False tamper detections may occur when configuring the RTC INn and OUTn pins.

Workaround
First configure the different RTC registers, and then select the RTC INn and OUTn peripheral functions on the PORT peripheral (PMUX registers).

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9.11 General Purpose Registers Reference: TMR102-56

The General Purpose Registers n (GPn) are reset on tamper detection even if GPTRST = 0.

Workaround
None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9.12 Active Layer Protection Reference: TMR102-65

When the RTC is configured in Active Layer Protection mode (TAMPCTRL.INACT = 0x3), and the RTC CTRLA.ENABLE bit is not set, a tamper can be detected and a timestamp captured. The TAMPID register and the INTFLAG.TAMPER bit may not be set.

Workaround
When the RTC is configured in Active Layer Protection mode, after setting the CTRLA.ENABLE control bit, the user must wait for 10 RTC clock periods. Then the user must clear the TAMPID register and the INTFLAG.TAMPER bit, and do a dummy read of the TIMESTAMP register to remove the lock condition on the TIMESTAMP register.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10 Serial Communication Interface Inter-Integrated Circuit (SERCOM I²C)

2.10.1 High-Speed Mode Reference: CHIP003-145

When configured in HS or Fast-Mode Plus, SDA and SCL fall times are shorter than I²C specification requirement and can lead to reflection.

Workaround
When reflection is observed, a 100 ohm serial resistor can be added on the impacted line.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.2 Repeated Start Reference: COM100-84

When Quick command is enabled (CTRLB.QCEN = 1), the software can issue a Repeated Start by either writing the CTRLB.CMD or ADDR.ADDR bit fields. If in these conditions, SCL Stretch Mode is CTRLA.SCLSM = 1, a bus error will be generated.

Workaround
Use Quick Command mode (CTRLB.QCEN = 1) only if SCL Stretch mode is CTRLA.SCLSM = 0.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.3 Repeated Start Reference: COM100-128

For Host Write operations (excluding High-Speed mode), in 10-bit addressing mode, writing CTRLB.CMD = 0x1 does not issue correctly a Repeated Start command.

Workaround
Write the same 10-bit address with the same direction bit to the ADDR.ADDR register to generate properly a Repeated Start.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.4 Repeated Start Reference: COM100-123

For High-Speed Host Read operations, sending a NACK (CTRLB.CMD = 0x2) forces a STOP to be issued making repeated start not possible in that mode.

Workaround
None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.5 Repeated Start Reference: COM100-122

For High-Speed Host Write operations, writing CTRLB.CMD = 0x1 issues a STOP command instead of a Repeated Start making repeated start not possible in that mode.

Workaround
None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.6 Client Mode with DMA Reference: COM100-94

In I^2C Client Transmitter mode, at the reception of a NACK, if there is still data to be sent in the DMA buffer, the DMA will push a data to the DATA register. Because a NACK was received, the transfer on the I^2C bus will not occur causing the loss of this data.

Workaround
Configure the DMA transfer size to the number of data to be received by the I^2C host. DMA cannot be used if the number of data to be received by the host is not known.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.7 Client Mode 10-bit Reference: COM100-101

I^2C client 10-bit addressing mode is not functional.

Workaround
None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						

.....continued							
Device Family	**B**						
SAM L11	X						

2.10.8 Status Flags Reference: COM100-102

In Client mode, the BUSERR, COLL, LOWTOUT, SEXTTOUT and LENERR STATUS register bits are not automatically cleared when INTFLAG.AMATCH is cleared.

Workaround
Clear the STATUS register bits, BUSERR, COLL, LOWTOUT, SEXTTOUT and LENERR, by writing these STATUS bits to '1' when INTFLAG.AMATCH is cleared.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.9 Status Flags Reference: COM100-114

The STATUS.CLKHOLD bit in host and client modes can be written whereas it is a read-only status bit.

Workaround
Do not clear the STATUS.CLKHOLD bit to preserve the current clock hold state.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.10 Status Flags Reference: COM100-157

When an unexpected STOP occurs on the I^2C bus, the STATUS.BUSERR and INTFLAG.ERROR bits are set, but may not wake the system from Sleep mode. An unexpected START will not produce this issue.

Workaround
None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.11 Automatic Acknowledge Reference: COM100-216

The I^2C Client Automatic Acknowledge feature (CTRLB.AACKEN = 1) is not supported when doing a repeated start.

Workaround
Do not use the AACKEN feature, implement a AMATCH handler instead.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.11 Serial Communication Serial Peripheral Interface (SERCOM SPI)

2.11.1 Data Preload Reference: COM100-83

In SPI Client mode with Client Data Preload Enabled (CTRLB.PLOADEN = 1), the client transmitter may discard some data if the host cannot keep the SPI Select ($\overline{SS}$) pin low until the end of transmission.

Workaround
In SPI Client mode, the SPI Select ($\overline{SS}$) pin must be kept low by the host until the end of the transmission if the Client Data Preload feature is used (CTRLB.PLOADEN = 1).

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.11.2 Hardware SPI Select Control Reference: COM100-203

When Hardware SPI Select Control is enabled (CTRLB.MSSEN = 1), the SPI Select ($\overline{SS}$) pin goes high after each byte transfer even if a new data is ready to be sent.

Workaround
Set CTRLB.MSSEN = 0 and handle the SPI Select ($\overline{SS}$) pin by software.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.11.3 Client Data Preload Reference: COM100-202

Preloading a new SPI data (CTRLB.PLOADEN = 1) before going into Standby mode, may lead to extra power consumption.

Workaround
None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.11.4 Wake-up Interrupt Reference: COM100-192

The Data Register Empty (DRE) wake-up interrupt is not de-asserted when the register interrupt is cleared (INTFLAG.DRE = 0).

The issue occurs if the DRE interrupt is enabled (INTSET.DRE = 1) when the device enters in Standby mode.

Workaround
Write DATA register before going back to Standby mode.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.12 Serial Communication Interface USART (SERCOM USART)

2.12.1 Inverted Bits Reference: COM100-61

The TXINV and RXINV bits in the CTRLA register have inverted functionality.

Workaround
In software, interpret the TXINV bit as a functionality of RXINV, and conversely, interpret the RXINV bit as a functionality of TXINV.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.12.2 ISO7816 Mode Reference: COM100-55

When the SERCOM USART is in ISO7816 mode, the SERCOM bus clock continues to run in Standby mode causing extra power consumption.

Workaround
Disable the USART before entering Standby mode.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.12.3 Debug Mode Reference: COM100-80

In USART operating mode, if DBGCTRL.DBGSTOP = 1, data transmission is not halted when entering Debug mode.

Workaround
None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.12.4 Collision Detection Reference: COM100-75

In USART operating mode with Collision Detection enabled (CTRLB.COLDEN = 1), the SERCOM will not abort the current transfer as expected if a collision is detected and if the SERCOM APB clock is lower than the SERCOM generic clock.

Workaround
The SERCOM APB clock must always be higher than the SERCOM generic clock to support collision detection.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.12.5 Wakeup Reference: COM100-41

The USART does not wake up the device on Error Interrupt (INTFLAG.ERROR = 1).

Workaround
Configure the USART to wake up the device on the RX Complete Interrupt (INTENSET.RXC = 1) to check the PERR/FERR status (STATUS.PERR = 1 or STATUS.FERR = 1).

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.12.6 Overconsumption in Standby Mode Reference: COM100-185

When SERCOM USART CTRLA.RUNSTDBY = 0 and the Receiver is disabled (CTRLB.RXEN = 0), the clock request to the GCLK generator feeding the SERCOM will stay asserted during Standby mode, leading to unexpected overconsumption.

Workaround

Configure CTRLA.RXPO and CTRLA.TXPO to use the same SERCOM PAD for RX and TX, or add an external pull-up on the RX pin.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.12.7 Wake-up Interrupt Reference: COM100-192

The Data Register Empty (DRE) wake-up interrupt is not de-asserted when the register interrupt is cleared (INTFLAG.DRE = 0).

The issue occurs if the DRE interrupt is enabled (INTSET.DRE = 1) when the device enters in Standby mode.

Workaround

Write DATA register before going back to Standby mode.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.13 Timer Counter (TC)

2.13.1 Flags Synchronization Reference: TMR100-12

When clearing the STATUS.PERBUFV/STATUS.CCBUFVx flags, the SYNCBUSY.PER/SYNCBUSY.CCx flags are released before the PERBUF/CCBUFx registers are restored to their expected value.

Workaround

Successively, clear the STATUS.PERBUFV/STATUS.CCBUFVx flags twice to ensure that the PERBUF/CCBUFx registers value is properly restored before updating it.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.13.2 Capture Mode / Over consumption Reference: TMR100-8

If the Time Counter x (TCx) is in Capture mode (TC.CTRLA.CAPTENx = 1) and TC.CTRLA.RUNSTBY = 0, the clock source driving GCLK_TCx can be kept running in Standby mode causing extra power consumption.

Workaround

Disable the Time Counter x (TCx) (TC.CTRLA.ENABLE = 0) which has a channel configured in Capture mode before going to Standby mode.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.13.3 Retrigger Reference: TMR100-51

If a Retrigger event (EVCTRL.EVACTn = 0x1, RETRIGGER) occurs at the Channel Compare Match [n] time, the next Waveform Output [n] is corrupted.

Workaround

Use two channels to store their two successive (n and n+1) CC register values and combine their related waveform outputs to make signal redundancy.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.13.4 PER Register Reference: TMR100-54

In 8-bit mode, the PER register updates using the DMA are not possible in Standby mode.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.14 True Random Number Generator (TRNG)

2.14.1 Over consumption Reference: MATH100-7

When TRNG is disabled, some internal logic could continue to operate causing an over consumption.

Workaround

Disable the TRNG module twice:

- CTRLA.ENABLE = 0;
- CTRLA.ENABLE = 0;

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.15 Supply Controller (SUPC)

2.15.1 Buck Converter Mode Reference: CHIP003-311

Buck Converter mode is not supported when using FDPLL96M. As a result, the data provided in Tables 46-8 and 47-2 “Active Current Consumption for Buck converter mode with FDPLL96M at Performance Level 2 (PL2) setting” is not valid and must be disregarded.

Workaround
Use the LDO Regulator mode when using FDPLL96M.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.16 OSC32KCTRL

2.16.1 External 32.768 kHz Crystal Oscillator Reference: UANA163-1

External 32.768 kHz crystal oscillator operation is not supported over the full temperature range of -40°C to +125°C.

Workaround
Limit external 32.768 kHz crystal oscillator operation temperature range from 0°C to 125°C with a crystal ESR <70 kΩ.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.16.2 1024 Hz Clock Output Reference: OSC102-13

When the XOSC32K is configured for 1024 Hz clock output and is used to clock the Watchdog (OSCULP32K.ULP32KSW = 1) or the RTC (RTCCTRL.RTCSEL = 4), the 1024 Hz clock can generate spikes in Standby Low-Power mode if the XOSC32K is not always ON, leading to incorrect RTC/WDT counting.

Workaround
Set XOSC32K.RUNSTBY = 1 and clear XOSC32K.ONDEMAND = 0 to force the XOSC32K to be always ON in Standby Low-Power mode.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.16.3 Clock Failure Detection Reference: OSC102-17

Disabling the Clock Failure Detector (CFDCTRL.CFDEN = 0) and re-enabling it (CFDCTRL.CFDEN = 1) when the XOSC32K is enabled (XOSC32K.ENABLE = 1) can lead to a false Clock Failure Detection.

Workaround
Re-enable the Clock Failure Detector as follows:

1. Disable the XOSC32K (XOSC32K.ENABLE = 0).
2. Disable the Clock Failure Detector (CFDCTRL.CFDEN = 0).
3. Re-enable the Clock Failure Detector (CFDCTRL.CFDEN = 1).
4. Re-enable the XOSC32K (XOSC32K.ENABLE = 1).

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.16.4 XOSC32K Ready Bit Reference: OSC102-20

The XOSC32K Read bit of the STATUS register (STATUS.XOSC32KRDY) is not cleared when disabling the XOSC32K (XOSC32K.ENABLE = 0) at the same time as the Crystal Oscillator Enable bit (XOSC32K.XTALEN = 0).

Workaround
Disable the XOSC32K as follows:

1. Disable the XOSC32K (XOSC32K.ENABLE = 0).
2. Disable the Crystal Oscillator (XOSC32K.XTALEN = 0).

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.17 Boot ROM

2.17.1 GCM API Reference: BROM100-18

The GCM API function crya_gf_mult128_t does not save and restore the core register r8 on return, thereby violating the Procedure Call Standard for the Arm® Architecture (AAPCS).

Workaround

The Arm core register r8 must be saved before calling the crya_gf_mult128_t function and must be restored when returning from it.

Affected Silicon Revisions

Device Family	B						
SAM L10							
SAM L11	X						

2.18 Event System (EVSYS)

2.18.1 Synchronous and Resynchronized Modes Reference: PTG100-31

In synchronous or resynchronized modes, generating a software event can generate a spurious overrun interrupt.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.18.2 Synchronous Mode Reference: PTG100-37

In Synchronous mode, spurious overrun interrupts can be generated when the generic clock for a channel is always ON (CHANNEL.ONDEMAND = 0).

Workaround

Set Generic Clock on Demand feature by setting CHANNEL.ONDEMAND = 1.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.18.3 Spurious Overrun Reference: PTG100-64

If a software event occurs when the EVSYS is set in synchronous/resynchronized path modes (CHANNELn.PATH = 0x0/0x1) with event detection set on both rising and falling edges (CHANNELn.EDGESEL = 0x3), spurious overrun interrupts may occur (INTFLAG.OVRn).

Workaround

Generate software events for the event user through a dedicated channel configured with even detection set on rising edges (CHANNELn.EDGESEL = 0x1).

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.18.4 Software Event Reference: PTG100-65

If a software event occurs when the EVSYS is set in synchronous/resynchronized path modes (CHANNELn.PATH = 0x0/0x1) with event detection set on falling edges (CHANNELn.EDGESEL = 0x2), the CHSTATUS.CHBUSYn flag will be set but will never come back to 0. It is then impossible to know if the event user for this channel is ready or not to accept new events.

Workaround

Generate software events for this user through a dedicated channel configured with even detection set on rising edges (CHANNELn.EDGESEL = 0x1).

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.18.5 PAC Write-Protection Reference: PTG100-43

PAC Write-Protection is not functional for the NSCHKCHAN and NSCHKUSER registers.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.19 Oscillator Controller (OSCCTRL)

2.19.1 Clock Failure Detection Reference: OSC108-12

When the XOSC Clock Failure Detector is enabled (XOSCCTRL.CFDEN = 1) and a failure is detected (STATUS.XOSCFAIL = 1), the XOSC Ready bit is not cleared (STATUS.XOSCRDY = 1).

Workaround
STATUS.XOSCFAIL must always be checked before STATUS.XOSCRDY, and STATUS.XOSCRDY must always be ignored when STATUS.XOSCFAIL = 1.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.19.2 Clock Failure Detection Reference: OSC108-14

Disabling the Clock Failure Detector (XOSCCTRL.CFDEN = 0) and re-enabling it (XOSCCTRL.CFDEN = 1) when the XOSC is enabled (XOSCCTRL.ENABLE = 1) can lead to a false Clock Failure Detection.

Workaround
Re-enable the Clock Failure Detector as follows:

1. Disable the XOSC (XOSCCTRL.ENABLE = 0).
2. Disable the Clock Failure Detector (XOSCCTRL.CFDEN = 0).
3. Re-enable the Clock Failure Detector (XOSCCTRL.CFDEN = 1).
4. Re-enable the XOSC (XOSCCTRL.ENABLE = 1).

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.19.3 XOSC Ready Bit Reference: OSC108-16

The XOSC Read bit of the STATUS register (STATUS.XOSCRDY) is not cleared when disabling the XOSC bit (XOSCCTRL.ENABLE = 0) at the same time as the Crystal Oscillator Enable bit (XOSCCTRL.XTALEN = 0) .

Workaround
Disable the XOSC Ready bit as follows:

1. Disable the XOSC (XOSCCTRL.ENABLE = 0).
2. Disable the Crystal Oscillator (XOSCCTRL.XTALEN = 0).

Affected Silicon Revisions

Device Family	B						
SAM L10	X						

.....continued							
Device Family	**B**						
SAM L11	X						

2.19.4 FDPLL96M On Demand in Standby Reference: PLL100-09, PLL100-20

The FDPLL96M On Demand mode (DPLLCTRLA.ONDEMAND = 1) is not functional in Standby mode.

Workaround

Set DPLLCTRLA.ONDEMAND = 0 which makes the FDPLL96M always running in Standby mode.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.19.5 DFLLULP Dithering Mode Reference: DLL102-7

DFLLULP dithering mode (DFLLULPCTRL.DITHER = 1) is not functional.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.20 PORT I/O Controller (PORT)

2.20.1 IOBUS Reference: GPIO100-64

Concurrent accesses on the PORT peripheral registers between the Arm APB and the Arm CPU IOBUS are not supported.

Workaround

Use exclusively the Arm APB or the Arm CPU IOBUS to access the PORT peripheral registers.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.21 Trust Ram (TRAM)

2.21.1 PAC Protection Reference: RAM102-28

Security RAM n registers (RAMn) are not PAC Write-Protected.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.22 Non Volatile Memory Controller (NVMCTRL)

2.22.1 Data Flash Silent Access and Scrambling Reference: NVM102-26

Silent Access and Scrambling on the Data Flash are not functional when both are enabled.

Silent Access and Data Flash scrambling remain functional if only one of them is configured by the application.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10							
SAM L11	X						

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001513G):

Note: Corrections in tables, registers, and texts are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

There are currently no data sheet clarifications to report.

4. Revision History

Revision E - 07/2021
The SPI, I²S, and I²C standards use the terminology "Master" and "Slave". The equivalent Microchip terminology used in this document is "Host" and "Client" respectively. These terms have been updated throughout this document for this revision.

This revision contains numerous typographical updates, and formatting updates.

Obsolete Data Sheet Clarifications have been removed in this update.

The following errata were added in this revision:

- RTC: 2.9.12 Active Layer Protection
- SERCOM I²C: 2.10.11 Automatic Acknowledge
- TC: 2.13.4 PER register (8-bit mode)
- EVSYS: 2.18.3 Spurious Overrun
- EVSYS: 2.18.4 Software Event
- EVSYS: 2.18.5 PAC Write-Protection
- OSCCTRL: 2.19.4 FDPLL96M On Demand in Standby
- OSCCTRL: 2.19.5 DFLLULP Dithering Mode
- NVMCTRL: 2.22.1 Data FLASH Silent Access and Scrambling

Revision D - 01/2021
This revision contains numerous typographical updates, and formatting updates.

The following errata were updated with new verbiage:

- DMAC: 2.4.1 Concurrent Channels Trigger
- EIC: 2.5.1 PAC Protection
- OPAMP: 2.8.1 Reference Buffer
- SERCOM I2C: 2.10.8 Status Flags
- SERCOM I2C: 2.10.9 Status Flags
- SERCOM SPI: 2.11.1 Data Preload
- SERCOM USART: 2.12.5 Wakeup

The following errata were added in this revision:

- ADC: 2.1.2 Offset Correction
- Device: 2.3.2 Standby Entry
- RTC: 2.9.9 Tamper Detection
- RTC: 2.9.10 Tamper Detection
- RTC: 2.9.11 General Purpose Registers
- SERCOM I2C: 2.10.10 Status Flags
- SERCOM SPI: 2.11.2 Hardware Slave Select Control
- SERCOM SPI: 2.11.3 Slave Data Preload
- SERCOM SPI: 2.11.4 Wakeup Interrupt
- SERCOM USART: 2.12.6 Overconsumption in Standby Mode
- SERCOM USART: 2.12.7 Wakeup Interrupt
- TC: 2.13.3 Retrigger
- OSC32KCTRL: 2.16.2 1024 Hz Clock Output
- OSC32KCTRL: 2.16.3 Clock Failure Detection
- OSC32KCTRL: 2.16.4 XOSC32K Ready Bit
- EVSYS: 2.18.1 Synchronous and Resynchronized Modes
- EVSYS: 2.18.2 Synchronous Mode

- OSCCTRL: 2.19.1 Clock Failure Detection
- OSCCTRL: 2.19.2 Clock Failure Detection
- OSCCTRL: 2.19.3 XOSC Ready Bit
- PORT: 2.20.1 IOBUS
- TRAM: 2.21.1 PAC Protection

Revision C - 05/2019

The following new errata were added:

- RTC:
  - 2.9.5 Prescaler
  - 2.9.6 Active Layer Protection
  - 2.9.7 Tamper Detection Timestamp
  - 2.9.8 Tamper Detection Timestamp
- SERCOM USART:
  - 2.12.5 Wakeup

Revision B - 02/2019

The following new errata were added:

- RTC: 2.9.4 Tamper detection Timestamp
- SUPC: 2.15.1 Buck Converter Mode
- OSC32KCTRL: 2.16.1 External 32.768kHz Crystal Oscillator
- Boot ROM: 2.17.1 GMC API

The following errata is updated:

- ADC: 2.1.1 Reference Buffer Offset Compensation

The following Data Sheet clarifications were added:

- Updates to Electrical Specifications Tables:
  - Table 46-8
  - Table 46-54
  - Table 47-2

Revision A - 5/2018

This is the initial release of this document.

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