LIGHTNING
Semiconductor

LN882H Series Datasheet

A Single-Chip Wireless SOC with Cortex M4F CPU

Supporting 802.11b/g/n (2.4 GHz Wi-Fi) and Bluetooth 5.1 (LE)

Version 1.35

Sep.4th, 2023

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1 Overview

1.1 Block Diagram

LN882H series of SoCs is highly-integrated Cortex-M4F based solution supporting 802.11b/g/n (2.4 GHz Wi-Fi) and Bluetooth 5.1 (LE), as diagram below.

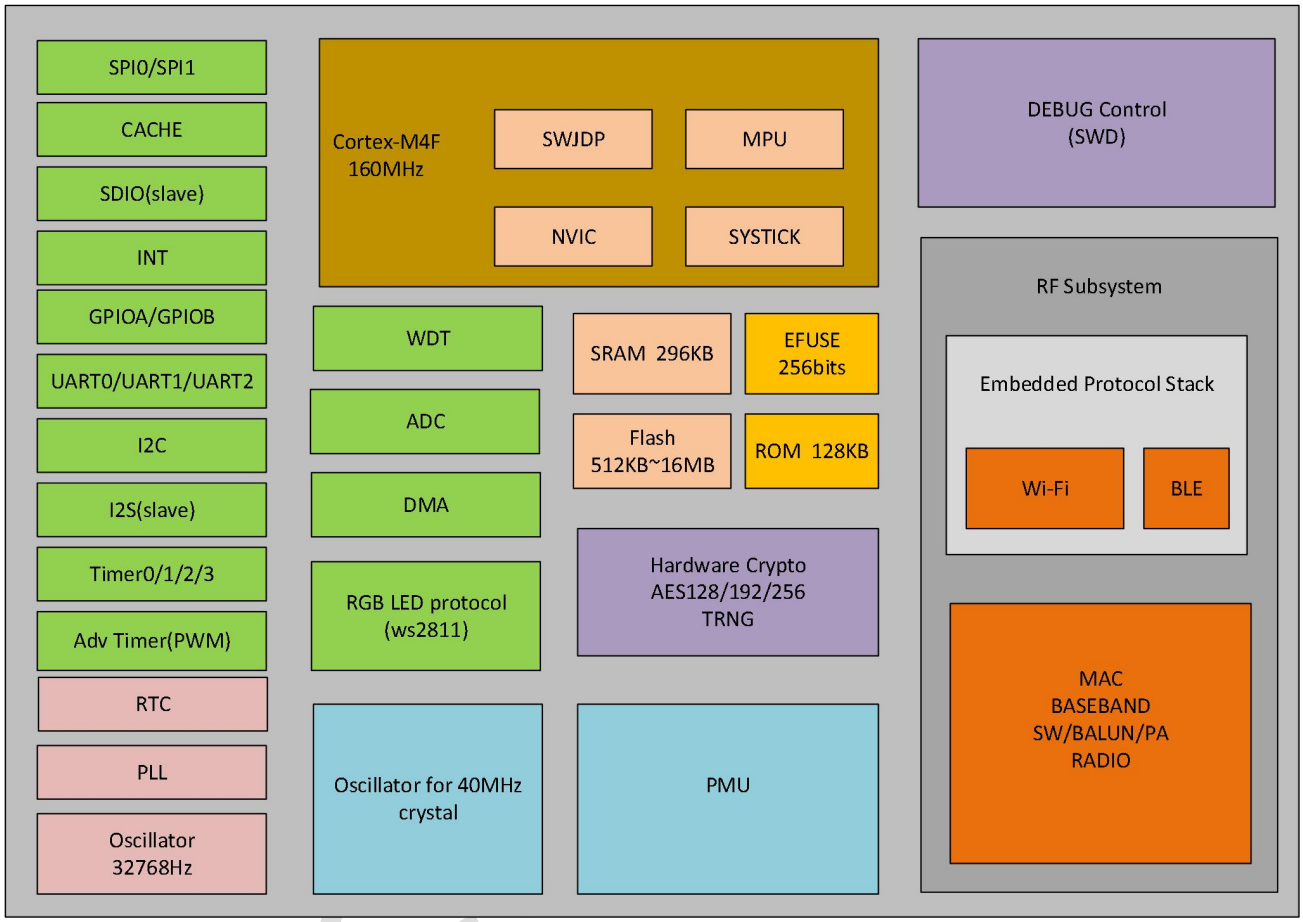


Figure 1: LN882H block diagram

1.2 Function Features

- Wi-Fi
  - 2.4GHz 802.11 b/g/n, 20MHz bandwidth
  - Support STA/SoftAP modes
  - Wi-Fi security: WEP(40/104),WPA,WPA2,WPA3
  - SoC with on chip TCP/IP protocol stack
- BLE
  - Bluetooth LE 5.1
  - Support long range (125Kbps, 500Kbps) and high data rate (2Mbps)
- CPU and Memory
  - ARM Cortex M4F, 40/80/160M

  - 296KB RAM / 128KB ROM
  - 512KB~4MB Flash for XIP application code
  - SWD debug interface
- Advanced Peripheral Interfaces
  - 20 GPIOs (QFN32) or 12 GPIOs (QFN24)
  - SPI/I2S/I2C/SDIO/UART interface
  - Timer/Advance Timer (PWM)
  - Multi-channel ADC with programmed amplifier for voice sense
  - XIP from external QSPI FLASH with high-speed cache
  - RTC
  - WDT
  - DMA controler
  - RGB LED Protocol (Compatible with the WS2811/WS2812)
- High Integration
  - Integrated TR switch, balun, LNA, power amplifier and matching network
  - AES-128\AES-192\AES-256 hardware encryption
  - True random number generator (TRNG)
  - 256 bits EFUSE
  - CHKSUM accelerator to enhance TCP/UDP transfer
- Package
  - QFN32 5mm*5mm
  - QFN24 4mm*4mm

1.3 Memory Map

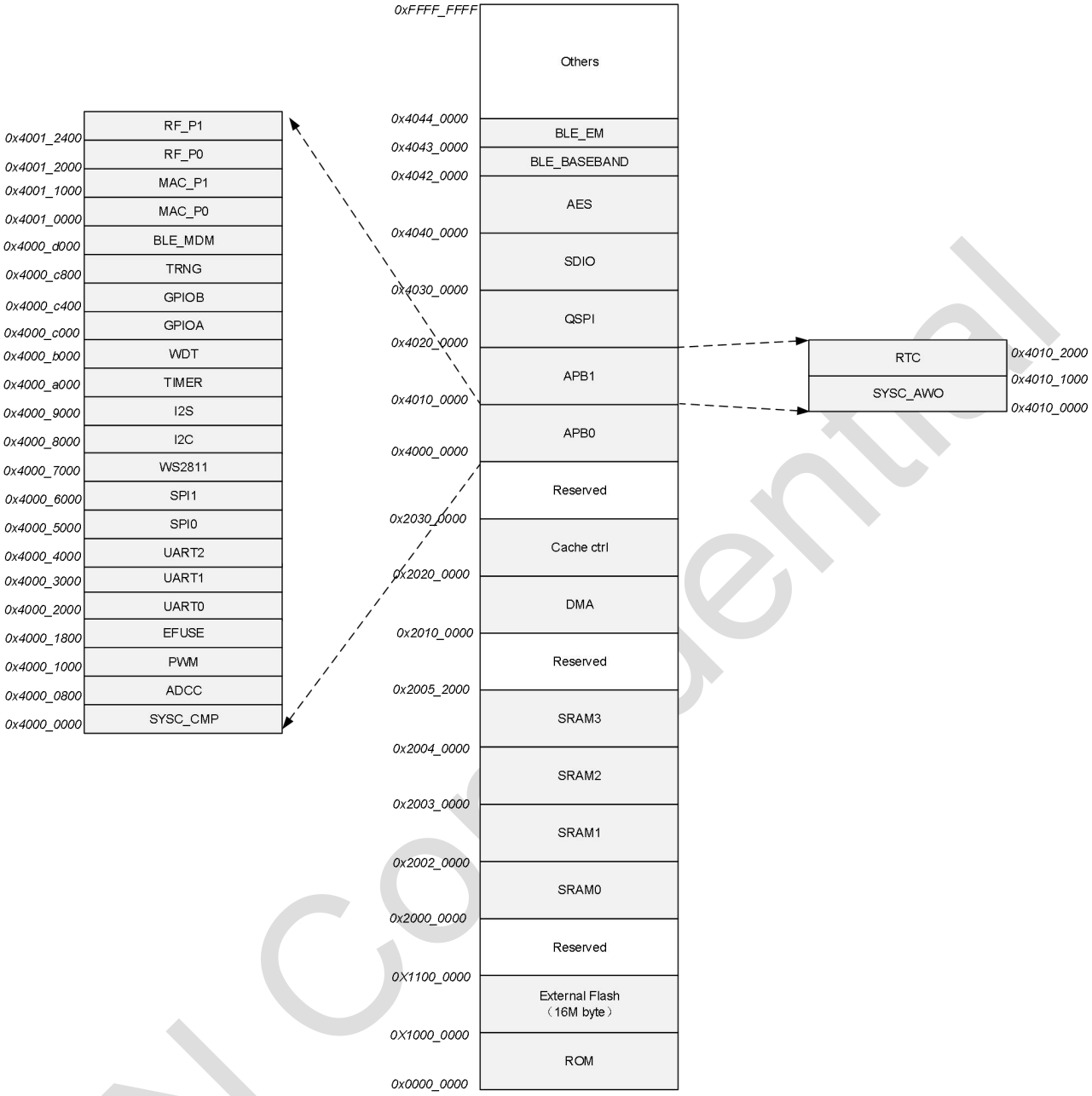


Figure 2：LN882H Memory Map

2 WiFi Subsystem

2.1 Supported Frequencies

Table 1: Supported Frequencies

Parameter	Condition	Min	Typ	Max	Unit
Receive frequency range 2.4GHz		2412		2484	MHz

2.2 Receiver Characteristics

Table 2: Receiver Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
Sensitivity					
11b, 1M	FER<8%, 1024 bytes		-94		dBm
11b, 11M	FER<8%, 1024 bytes		-87		dBm
11g, 6M	FER<10%, 1024bytes		-90		dBm
11g, 54M	FER<10%, 1024 bytes		-74		dBm
11n, MCS0	FER<10%, 1024 bytes		-90		dBm
11n, MCS7	FER<10%, 1024 bytes		-71		dBm
Maximum input level					
11b	FER<8%, 1024 bytes		4		dBm
11g	FER<10%, 1024 bytes		-10		dBm
11n	FER<10%, 1024 bytes		-10		dBm
Operating power consumption					
11b			80		mA
11g			82		mA
11n			82		mA

2.3 Transmitter Characteristics

Table 3: Transmitter Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
Output power					
11b, 11M DSSS	Maximum Burst power		18		dBm
11g, 54M OFDM	Maximum Burst power		16		dBm
11n, MCS7	Maximum Burst power		14		dBm
Power consumption					

11b	100% Duty Cycle @17dBm		320		mA
11g	100% Duty Cycle @14dBm		290		mA
11n	100% Duty Cycle @13dBm		270		mA

3 BlueTooth Subsystem

3.1 Supported Features

- Bluetooth LE 5.1
- Data rate：1M/2Mbps, 125k/500kbps
- -96dBm sensitivity in 1Mbps
- Up to 10dBm output power
- BLE advertising extension
- BLE SIG MESH support

4 Power Management

4.1 Power Mode

There are 4 power modes to manage lower power operation of the system.

- **Active:** Normal mode
  SW can gate clock of some Peripherals.
- **LightSleep:** CPU executes WFI instruction without ‘SLEEPDEEP’, and gates clock by itself.
  Other modules are still in free running.
  CPU exit this mode from wakeup by interrupt.
- **DeepSleep:** CPU executes WFI instruction with ‘SLEEPDEEP’.
  All digital parts are all clock gated except AWO[1] domain but CPU power is still on.
  Voltage supplied to Digital parts can be reduced to save power.
  Clock in AWO is switched to 32KHz
  WIC wakes up CPU, then all clocks and power recover to normal state.
- **Frozen:** All power-down except AWO domain.
  WIC wakeup CPU, then all clock and power recover to normal state.

Any low power mode can’t be switched to another low power mode directly. It must be switched to active mode before going to another one.

Clock and power gating of one domain should be configured before executing WFI.

4.2 Power Save Mode Current

Table 4: Current in WiFi Power Save Mode

Mode	Condition	Min	Typ	Max	Unit
Power Save Mode	DTIM=1[2]		12		mA
	DTIM=3		6		mA

Notes:

[1] AWO: The block whose power is never down is named as Always On

[2] Test condition: keep connected with AP. UART active.

DTIM=n means STA wakes up to listen to beacon from AP in every n times of DTIM interval

4.3 Power Supplies

Table 5: Power Supplies

Power Domain	Description	Min	Typ.	Max	Unit
VDD33	Supply for all chips except PA	2.6	3.3	3.6	V
VDDA33	Supply for PA	2.6	3.3	3.6	V
VIO1	Supply for I/O	2.6	3.3	3.6	V
VIO2	Supply for I/O	2.6	3.3	3.6	V

5 Pin Definition

5.1 Pin Layout

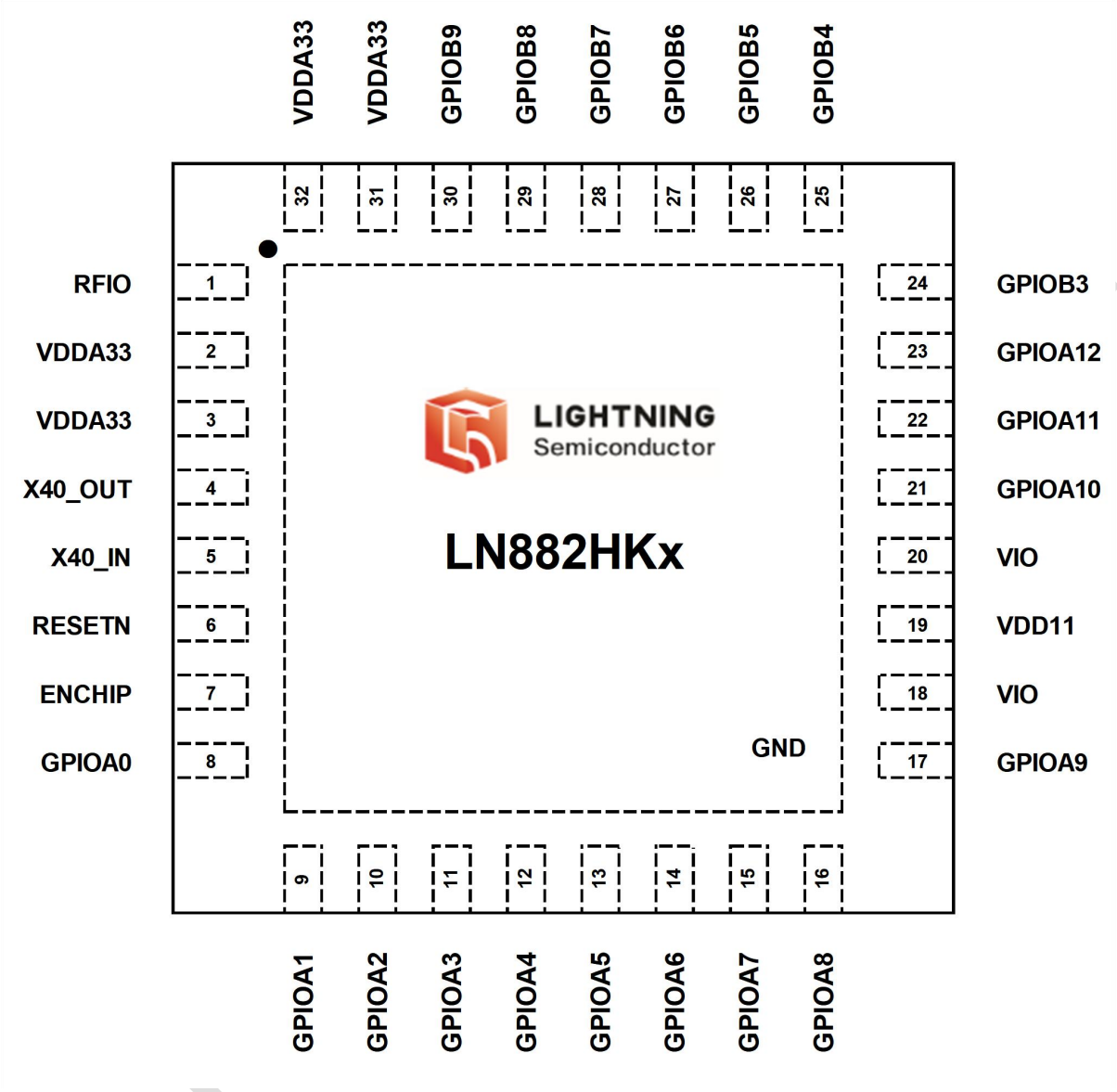


Figure 3: QFN32 Pin Layout

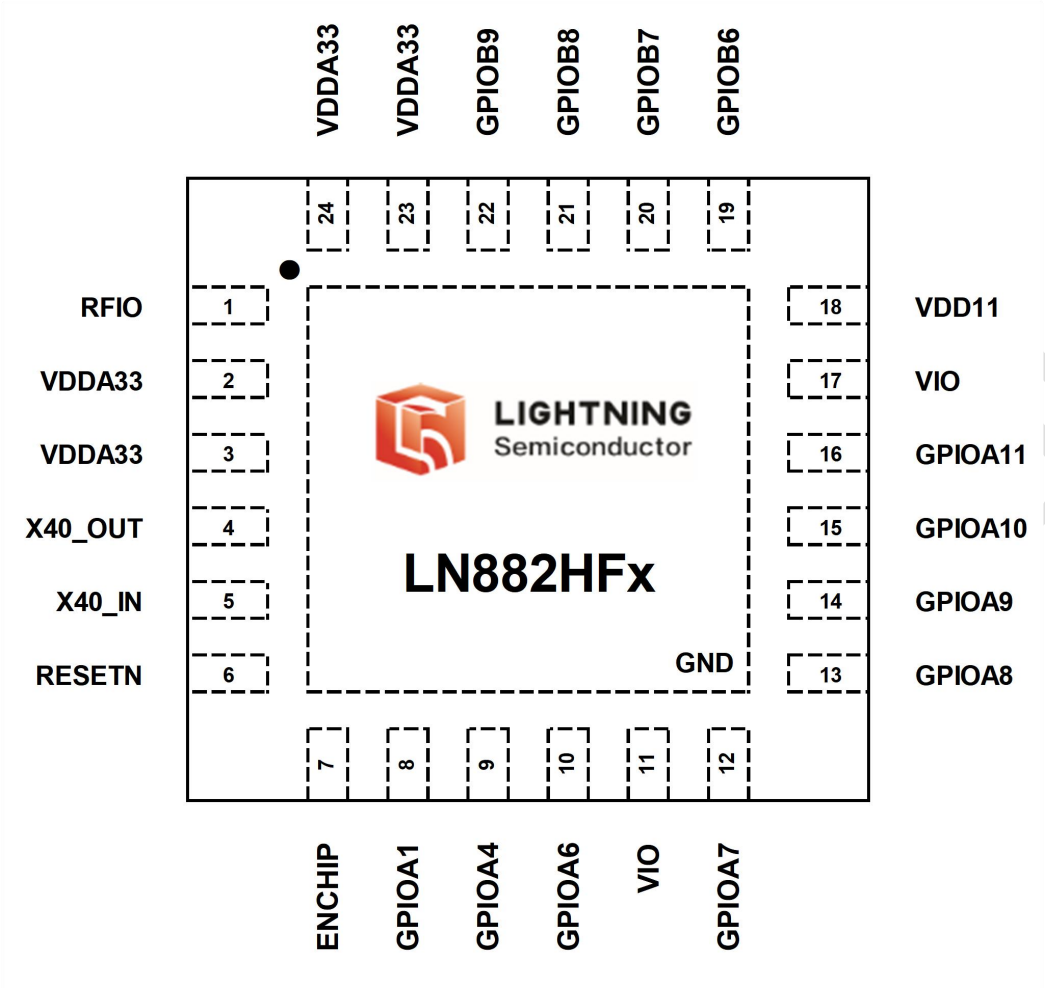


Figure 4 QFN24 Pin Layout

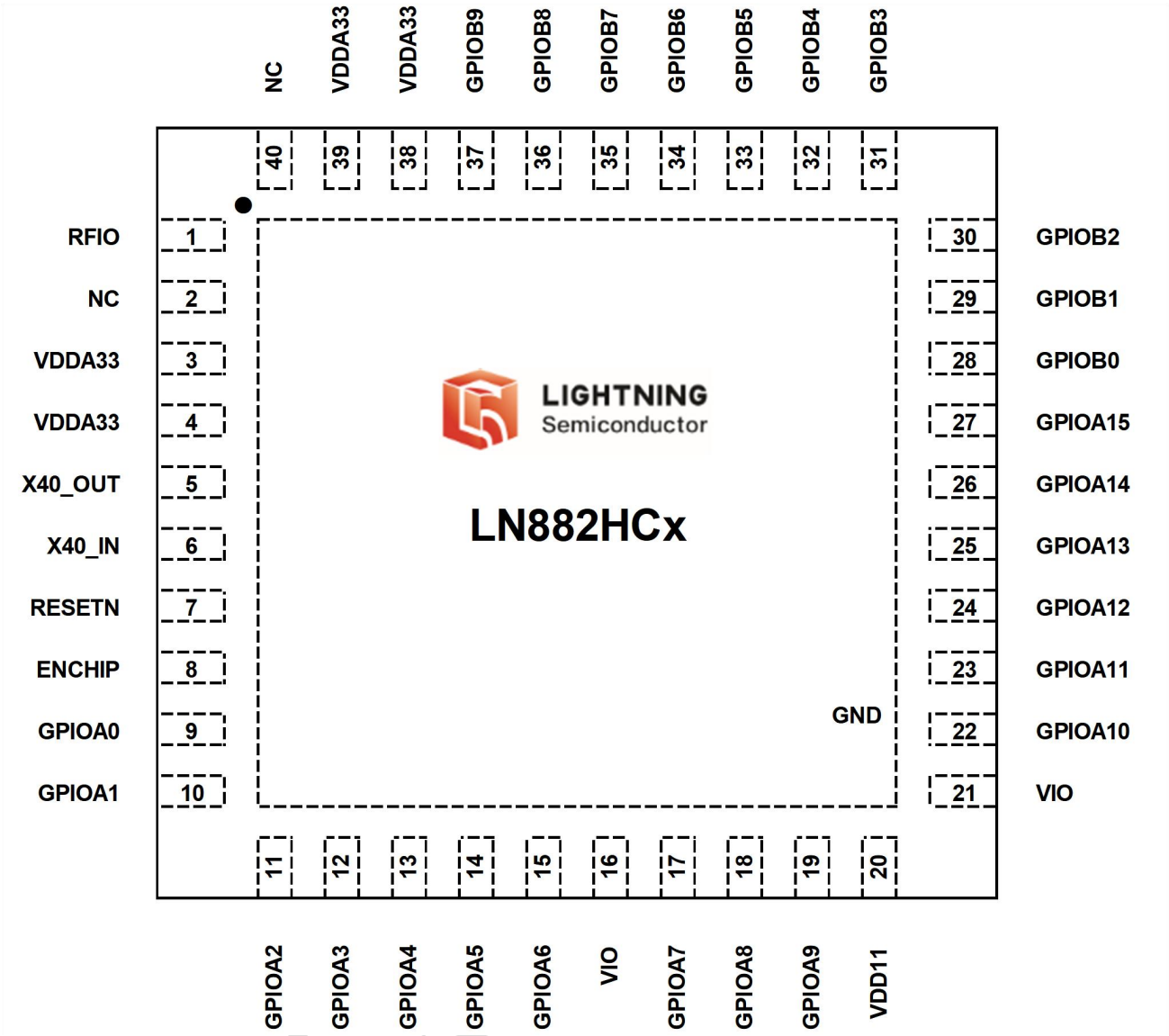


Figure 5: QFN40 Pin Layout

5.2 Pin Description

5.2.1 Programmable I/Os

QFN40	QFN32	QFN24	PAD NAME	Func1	Func2	Func3	Func4	PU/PD
9	8		GPIOA0	ADC2		FULLMUX0	EXT_INT0	PU
10	9	8	GPIOA1	ADC3	SWD	FULLMUX1	EXT_INT1	PU
11	10		GPIOA2			FULLMUX2	EXT_INT2	PU
12	11		GPIOA3			FULLMUX3	EXT_INT3	PU
13	12	9	GPIOA4	ADC4	SWCK	FULLMUX4		PD
14	13		GPIOA5			FULLMUX5	EXT_INT4	PU
15	14	10	GPIOA6	SDIO_IO2	I2S_SDI	FULLMUX6	EXT_INT5	PD
17	15	12	GPIOA7	SDIO_IO3		FULLMUX7	EXT_INT6	PD
18	16	13	GPIOA8	SDIO_CMD	I2S_WS	FULLMUX8	BOOT_MODE0	PD
19	17	14	GPIOA9	SDIO_CLK	I2S_SCLK	FULLMUX9	BOOT_MODE1	PU
22	21	15	GPIOA10	SDIO_IO0	I2S_SDO	FULLMUX10		PU
23	22	16	GPIOA11	SDIO_IO1		FULLMUX11		PD
24	23		GPIOA12			FULLMUX12		PU
25			GPIOA13	QSPI_HOLD				PU
26			GPIOA14	QSPI_WP				PU
27			GPIOA15	QSPI_CSN				PU
28			GPIOB0	QSPI_SCLK				PU
29			GPIOB1	QSPI_SO				PU
30			GPIOB2	QSPI_SI				PU
31	24		GPIOB3	ADC5		FULLMUX13		PD
32	25		GPIOB4	ADC6		FULLMUX14		PU
33	26		GPIOB5	ADC7		FULLMUX15		PU
34	27	19	GPIOB6			FULLMUX16		PU
35	28	20	GPIOB7			FULLMUX17		PU
36	29	21	GPIOB8			FULLMUX18		PU
37	30	22	GPIOB9			FULLMUX19	EXT_INT7	PU

Table 6: Programmable I/Os

LN882H has 12 or 20 GPIOs.

- Two group IOs GPIOA and GPIOB, which are separately configurable
- Configurable hardware and software control for each signal
- Configurable interrupt mode for Port A, debounce logic is used to generate single hi-active interrupts

5.2.2 Power, Clocks and Reset I/Os

Table 7: Power, Clocks and Reset I/Os

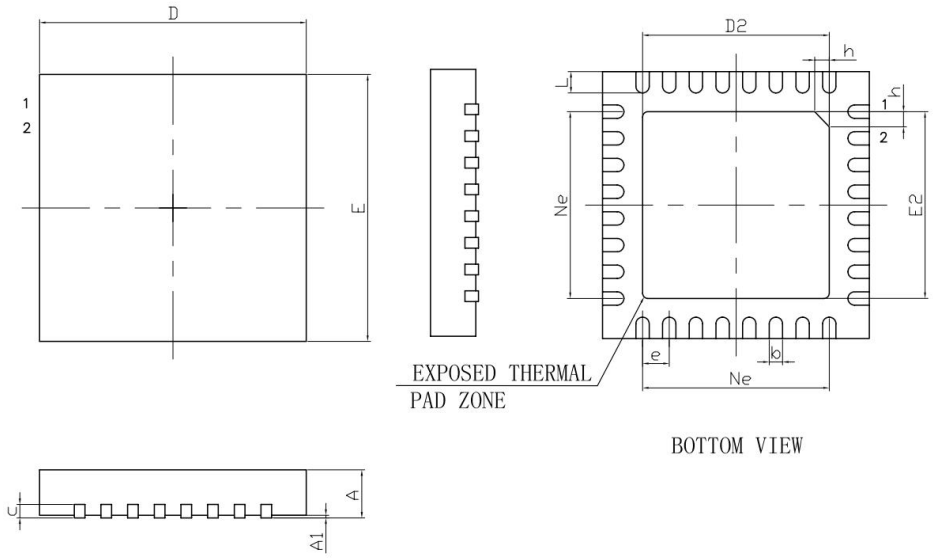
QFN40	QFN32	QFN24	Pin Name	Pin description
1	1	1	RFIO	Wi-Fi RF transmitter/receiver
3	2	2	VDDA33	3.3v power supply
4	3	3	VDDA33	3.3v power supply
5	4	4	XTAL	Crystal output
6	5	5	XIN	Crystal input
7	6	6	RESETn	system reset
8	7	7	CHIP_EN	chip enable
16	18	11	VIO1①	I/O power supply 1
20	19	18	DVDD11	1.1v power output
21	20	17	VIO2②	I/O power supply 2
38	31	23	VDDA33	power supply for PA
39	32	24	VDDA33	3.3v power supply

Notes:

(1) ① ②VIO1,VIO2 must be supplied externally

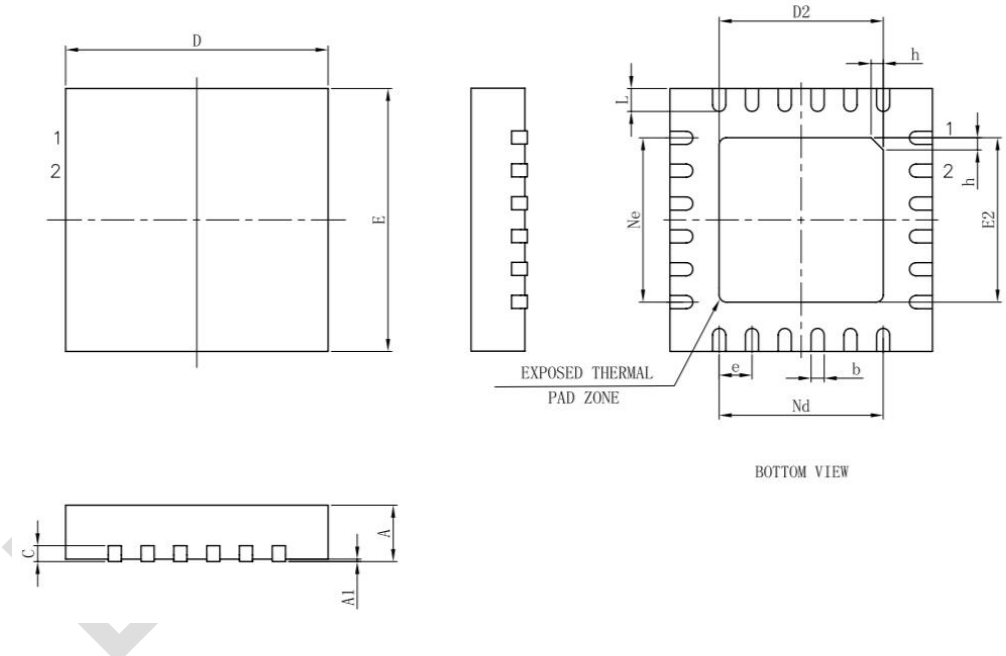
(2) ②VIO2 should be the same as the voltage supplied for SPI flash, 3.3V is recommended

5.3 Package Information



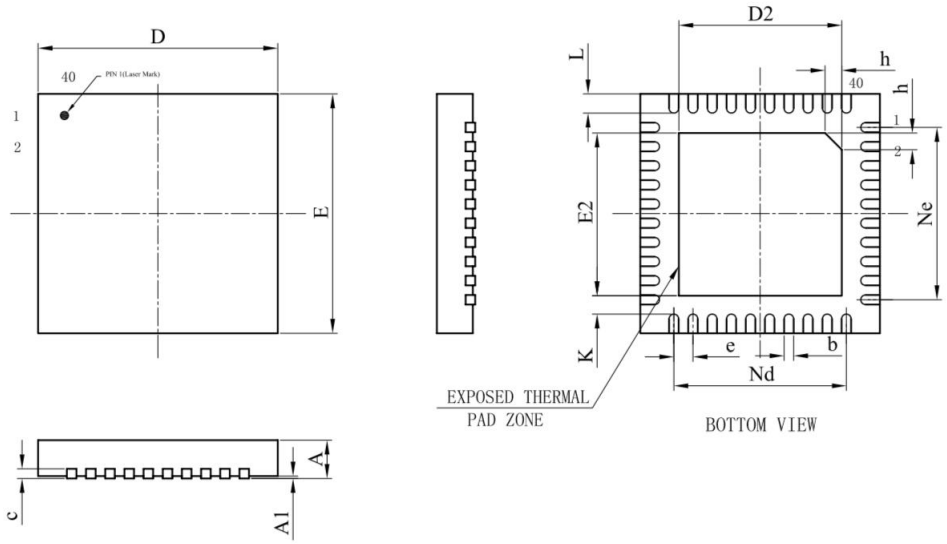
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 70	0.75	0. 80
A1	—	0.02	0. 05
b	0. 18	0.25	0. 30
c	0. 18	0.20	0. 25
D	4. 90	5. 00	5. 10
D2	3. 40	3. 50	3. 60
e	0. 50BSC		
Ne	3. 50BSC		
E	4. 90	5. 00	5. 10
E2	3. 40	3. 50	3. 60
L	0. 35	0.40	0. 45
h	0. 30	0. 35	0. 40
L/F载体尺寸	150x150		130x130

Figure 6: QFN-32 5x5 mm Packag



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 70	0.75	0. 80
A1	—	0.02	0. 05
b	0. 18	0.25	0. 30
c	0. 18	0.20	0. 25
D	3. 90	4. 00	4. 10
D2	2. 40	2. 50	2. 60
e	0. 50BSC		
Ne	2. 50BSC		
Nd	2. 50BSC		
E	3. 90	4. 00	4. 10
E2	2. 40	2. 50	2. 60
L	0. 35	0.40	0. 45
h	0. 30	0. 35	0. 40
L/F载体尺寸	110x110		

Figure 7: QFN-24 4x4 mm Package



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.30	3.40	3.50
e	0.40BSC		
Nd	3.60BSC		
E	4.90	5.00	5.10
E2	3.30	3.40	3.50
Ne	3.60BSC		
L	0.35	0.40	0.45
K	0.20	—	—
h	0.30	0.35	0.40
L/F载体尺寸 (mil)	150*150		

Figure 8: QFN-24 4x4 mm Package

6 Peripheral Interface

6.1 SWD

LN882H supports Serial Wire Debug (SWD) which is used to download flash image and debug. The pins shown in Table 8 are assigned to SWD mode by bootrom program after power on.

Table 8: SWD Pin Assignment

QFN40	QFN32	QFN24	PAD NAME	Function
10	9	8	GPIOA1	SWD
13	12	9	GPIOA4	SWCK

6.2 ADC

LN882H has a 6-channel ,12-bit sampling Analog-to-Digital Converter (ADC). The main features:

- Up to 6 external channels
- Supply voltage and internal temperature is also measured by the ADC
- Input programmed amplifier is integrated, the maxim gain is 50dB.
- Support up to 8 result FIFO with selectable FIFO depth
- Conversion complete flag and interrupt
- Selectable asynchronous hardware conversion trigger
- Automatic comparison against programmable value to generate interrupt

Table 9: ADC Pin Assignment

QFN40	QFN32	QFN24	PAD NAME	Function
9	8		GPIOA0	ADC2
10	9	8	GPIOA1	ADC3
13	12	9	GPIOA4	ADC4
31	24		GPIOB3	ADC5
32	25		GPIOB4	ADC6
33	26		GPIOB5	ADC7

6.3 SDIO

LN882H features one slave sdio interface which supports the standard SDIO version 2.0 and provides high-speed data I/O with low power consumption for mobile electronic devices. The main features:

- DMA supported
- The clock is up to 40MHz
- Supported 1-bit,4-bit data mode

Table 10: SDIO Pin Assignment

QFN40	QFN32	QFN24	PAD NAME	Function
15	14	10	GPIOA6	SDIO_IO2
17	15	12	GPIOA7	SDIO_IO3
18	16	13	GPIOA8	SDIO_CMD
19	17	14	GPIOA9	SDIO_CLK
22	21	15	GPIOA10	SDIO_IO0
23	22	16	GPIOA11	SDIO_IO1

6.4 QSPI

LN882H supports one QSPI interface which is generally used to communicate with flash. The clock of QSPI is programmable and maximum at 80 MHz.

Table 11: QSPI Pins Assignment

QFN40	QFN32	QFN24	PAD NAME	Function
25	-	-	GPIOA13	QSPI_HOLD
26	-	-	GPIOA14	QSPI_WP
27	-	-	GPIOA15	QSPI_CSN
28	-	-	GPIOB0	QSPI_SCLK
29	-	-	GPIOB1	QSPI_SO
30	-	-	GPIOB2	QSPI_SI

6.5 I2S

LN882H features one slave I2S interface, which is generally used to handle the transfer of audio data. The pin definition of I2S is shown in Table 12. The main features are described as below.

- I2S transmitter and/or receiver based on the Philips I2S serial protocol
- Slave mode of operation
- 1 channels for both transmitter and receiver
- APB data bus widths of 8, 16, and 32 bits
- Audio data resolutions of 12, 16, 20, 24, and 32 bits
- External sclk gating and enable signals

Table 12: I2S Pin Assignment

QFN40	QFN32	QFN24	PAD NAME	Function
15	14	10	GPIOA6	I2S_SDI
18	16	13	GPIOA8	I2S_WS
19	17	14	GPIOA9	I2S_SCLK
22	21	15	GPIOA10	I2S_SDO

6.6 Interrupt

There are 16 interrupt sources from external pins and 8 interrupt sources that can wake up the system from sleep. These interrupts support both edge and level mode. The pins assignment of interrupt is listed in Table 13.

Table 13: Interrupt Pin Assignment

QFN40	QFN32	QFN24	PAD NAME	Function
9	8		GPIOA0	EXT_INT0
10	9	8	GPIOA1	EXT_INT1
11	10		GPIOA2	EXT_INT2
12	11		GPIOA3	EXT_INT3
14	13		GPIOA5	EXT_INT4
15	14	10	GPIOA6	EXT_INT5
17	15	12	GPIOA7	EXT_INT6
37	30	22	GPIOB9	EXT_INT7

6.7 Boot Mode

LN882H has two boot modes that depend on the logic value set of GPIOA8, GPIOA9 during power-on stage. GPIOA8 is pulled down while GPIOA9 is pulled up internally. The pin assignment is listed in Table 14 and boot mode configuration is shown inTable 15.

Table 14: Boot Mode Pin Assignment

QFN40	QFN32	QFN24	PAD NAME	Function
18	16	13	GPIOA8	BOOT_MODE0
19	17	14	GPIOA9	BOOT_MODE1

Table 15: Definition of Boot Mode

MODE	GPIOA8	GPIOA9	Description
FLASH Boot	**1**	**0**	Default: GPIOA8 pull-down GPIOA9 pull-up internally.
	0	**1**	
UART Boot	**0**	**0**	CPU will wait data from UART to program flash.
SDIO Boot	**1**	**1**	

6.8 I2C

LN882H has one I2C interface which both support master and slave mode. Any two pins listed in Table 6 FULLMUX can be configured as I2C.Their features:

- Standard, Fast and high-speed mode are supported
- Master or slave I2C operation
- 7 or 10-bit addressing, 7 or 10-bit combined format transfers
- Bulk transmit mode, DMA request signals
- Programmable slave address,
- Interrupt or polled-mode operation
- Programmable SDA hold time
- Parallel-bus/I2C protocol converter
- Analog noise filter
- Optional clock stretching
- • Configurable PEC (packet error checking) generation or verification:

6.9 UART

There are 3 UARTs in LN882H, UART0, UART1 and UART2. UART0 supports hardware flow control, which is generally used to output log. UART1 is suggested to used for transferring data, such as AT command. Any pin listed in Table 6 can be configured as UART. Their features:

- 16 bytes Transmit and receive FIFOs.
- DMA supported
- Transmitter Holding Register Empty (THRE) interrupt mode
- Programmable data word length (8 or 9 bits)
- parity bit and number of stop bits (1 or 2)
- Line break generation and detection
- Prioritized interrupt identification
- Programmable serial data baud rate (up to 2Mbps)
- Programmable data order with MSB-first or LSB-first shifting

6.10 SPI

There are two independent SPI interfaces: SPI0 and SPI1. Both can be configured as master or slave. Any FULLMUX in Table 6 can be configured as dedicated function for SPI. Features:

- 4-wire serial interface: SCK CSn SDI SDO
- DMA interface supported
- Full-duplex synchronous transfers on three lines
- Simplex synchronous transfers on two lines with or without a bidirectional data line

- 8- or 16-bit transfer frame format selection
- Master or slave operation
- Multi-master mode capability
- 8 master mode baud rate pre-scalers (PCLK/2 max.)
- Slave mode frequency (PCLK/2 max)
- Faster communication for both master and slave
- NSS management by hardware or software for both master and slave
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Dedicated transmission and reception flags with interrupt capability
- SPI bus busy status flag
- Hardware CRC feature for reliable communication

6.11 PWM

There are 4 PWMs inside Timer which has 24-bit width counter.

Another 12 PWMs with 16-bit width counter are integrated:

- Prescaler divide-by 1, 2, 3, … ,63
- One 16-bit counter: PWM function mode or Timer function mode.

PWM function mode:

Up or Up/Down mode

Output frequency controlled by a 16-bit load value

Load value updates can be synchronized

Produces output signals at zero and load value

- Two PWM comparators
- PWM generator
- Dead-band generator
- ADC event trigger
- PWM output enable or disable of each PWM signal
- Optional output inversion of each PWM signal (polarity control)
- 16-bit input capture modes: input edge count mode or input edge time mode
- 16-bit timer mode, produces interrupt signals at counter value reach at load value.
- Mode priority: PWM mode > timer mode > input capture mode

6.12 GPIO

Each of the general-purpose I/O ports has two 16-bit configuration registers (GPIOx_CRL, GPIOx_CRH), two 16-bit data registers (GPIOx_IDR, GPIOx_ODR), a 32-bit set/reset register (GPIOx_BSRR), a 16-bit reset register (GPIOx_BRR) , each port bit of the General Purpose IO (GPIO) Ports, can be individually configured by software in several modes:

- Input pull-up
- Input-pull-down
- Analog
- High impedance
- Output push-pull

Each I/O port bit is freely programmable; However the I/O port registers have to be accessed as 32-bit words (half-word or byte accesses are not allowed). The purpose of the GPIOx_BSRR and GPIOx_BRR registers is to allow atomic read/modify accesses to any of the GPIO registers. This way, there is no risk that an IRQ occurs between the read and the modify access.

6.13 WS2811

- Support signal line 256 Gray level 3 channel constant current LED driver IC
- WS2811 0/1 code width comfigurable

6.14 TRNG

- The RNG delivers 128-bit true random numbers, produced by an digital loop ring clock post-processed with linear-feedback shift registers (LFSR).
- It is true random data according to the relationship between the digital ring clock and the APB bus clock.
- It produces 128-bit random data for 128 TRNG gap APB clock cycles after software trigger.

6.15 DMA

- 8 independently configurable channels (requests): 7 for normal DMA and 1 for checksum.
- Each of the 7 channels is connected to dedicated hardware DMA requests, software trigger is also supported on each channel. This configuration is done by software.
- Priorities between requests from channels of one DMA are software programmable (4 levels consisting of very high, high, medium, low).
- Independent source and destination transfer size (byte, half word, word), emulating packing and unpacking. Source/destination addresses must be aligned on the data size.
- Support for circular buffer management.
- Memory-to-memory transfer.
- Peripheral-to-memory and memory-to-peripheral, and peripheral-to-peripheral transfers.
- Access to Flash, SRAM, APB and AHB peripherals as source and destination.
- Programmable number of data to be transferred: up to 65536.

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Table 16: Absolute Maximum Ratings

Symbol	Min.	Max.	Unit
Supply Voltage	0	3.6	V
Logical Voltage	0.3*VIO	VDD33+0.3	V
Storage Temperature	-40	120	ºC

7.2 Recommended Operating Conditions

Table 17: Recommended Operating Conditions

Symbol	Symbol	Min.	Typ.	Max.	Unit
Power Supply	VDD33	2.6	3.3	3.6	V
VIO	VIO1/VIO2	2.6	3.3	3.6	V
Operating Temperature		-40	25	105	ºC

7.3 Input/Output Terminal Characteristics

Table 18: Input/Output Terminal Characteristics

Characteristic	Min.	Typ.	Max.	Unit
Input low voltage V_{IL}	-0.3	0	0.6	V
Input high voltage V_{IH}	VIO-0.6	VIO	VIO+0.3	V
Output low voltage V_{OL}	-0.45	0	0.45	V
Output high voltage V_{OH}	VIO-0.5	VIO	VIO+0.5	V

8 LN882H Series Comparison

8.1 Nomenclature

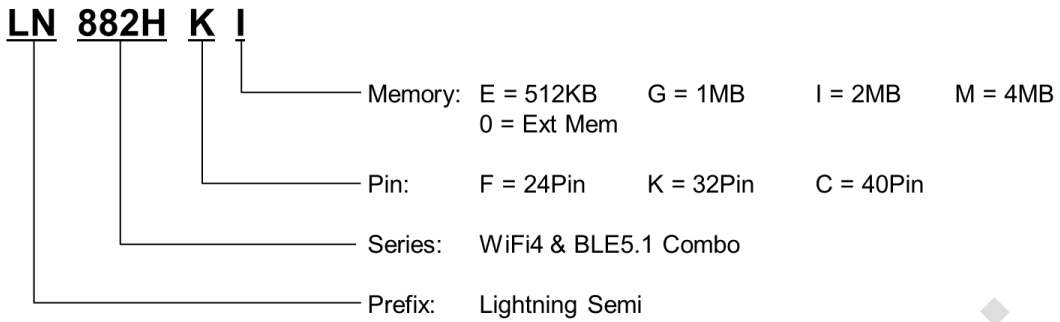


Figure 9: LN882H 1.1 Nomenclature

8.2 Ordering Information

Table 19: Part Ordering Information

Part Number	Package	Flash Size	Temperature
LN882HKI	QFN-32, 5mm pitch	2MB Flash	-40℃~105℃
LN882HKG	QFN-32, 5mm pitch	1MB Flash	-40℃~105℃
LN882HFG	QFN-24, 4mm pitch	1MB Flash	-40℃~105℃
LN882HC0	QFN-40, 5mm pitch	External Flash	-40℃~105℃

9 Revision History

Table 20: Revision History

Version	Changlist	Name	Date
0.10	First version	Zhaogang	2021/01/09
1.00	Update BLE section. Add QFN-32 package Add DMA logic Update package information Add WS2811 section; Update QFN-32 to 5x5 package	WL Jack Wang Rui Huang	2021/10/13
1.10-1.12	QFN32 pitch 0.4->0.5. Update VDDA pin# in Table 5-2 MC7 TX-> 14dBm GPIOB5->GPIOB6 in package page	Jack Wang Rui Huang	2021/11/25 ~ 2022/01/14
1.20-1.25	Update block TX/RX power consumption ordering info,	Rui Huang	2022/02/21
1.30	Datesheet revision Add QFN-24 package	Rui Huang	2022/06/09
1.31	Remove DMA support of IIS	Rui Huang	2022/8/1
1.32	GPIO section typo.	Rui Huang	2022/8/10
1.33	Update QFN24 pitch	Rui Huang	2022/9/26
1.34	Update AP/STA mode	Rui Huang	2023/4/26
1.35	Add Wi-Fi security(WEP,WPA,WPA2,WPA3)	WL	2023/9/4

Declaration