LN882H

Hardware_Design_Guidelines

Shanghai Lightning Semiconductor Technology Co., LTD

www.lightningsemi.com

About

《The LN882H Hardware Design Guidelines》 mainly provides the matters needing attention when using the LN882H for circuit design and PCB layout. This paper also briefly introduces the hardware information of LN882H, including LN882H chip, module, development board and typical application scheme.

Documents and Certificates

The latest version of this document can be downloaded from lightning official website www.lightningsemi.com or ask us for it.

The document is for reference only, If you have any questions, contact FAE engineer. If there are any mistakes or omissions, please correct them and give feedback to the relevant email.

Revision history

Version	History	Name	Date
2.1	expand the details	ys	2022/10/20

Catalogue

1. Product overview

LN882H is a single SOC solution integrating Wi-Fi、BLE、MCU and PMU. It supports 2.4GHz IEEE802.11b/g/n and BLE 5.1 dual-mode wireless communication. It supports SDIO (slave), UART, I2C, I2S, PMW, SPI, and GPIO interfaces.

The LN882H uses a 40nm process, with ultra-high RF performance、stability、versatility and reliability, as well as ultra-low power consumption to meet the needs of different products and be suitable for various application scenarios.

LN882H is the ultra-integrated Wi-Fi + Bluetooth solution in the industry. Its peripheral components are very simple, requiring only one crystal and about 10 Resistance/capacitance/inductance components, which greatly reduces the required PCB area.

LN882H also integrates an advanced self-calibration circuit to achieve dynamic automatic adjustment, which can eliminate the shortcomings of external circuits, better adapt to changes in the external environment, and reduce the cost of production.

In order to better ensure the working performance of LN882H, this document will introduce the schematic diagram of LN882H and the design of PCB layout in detail.

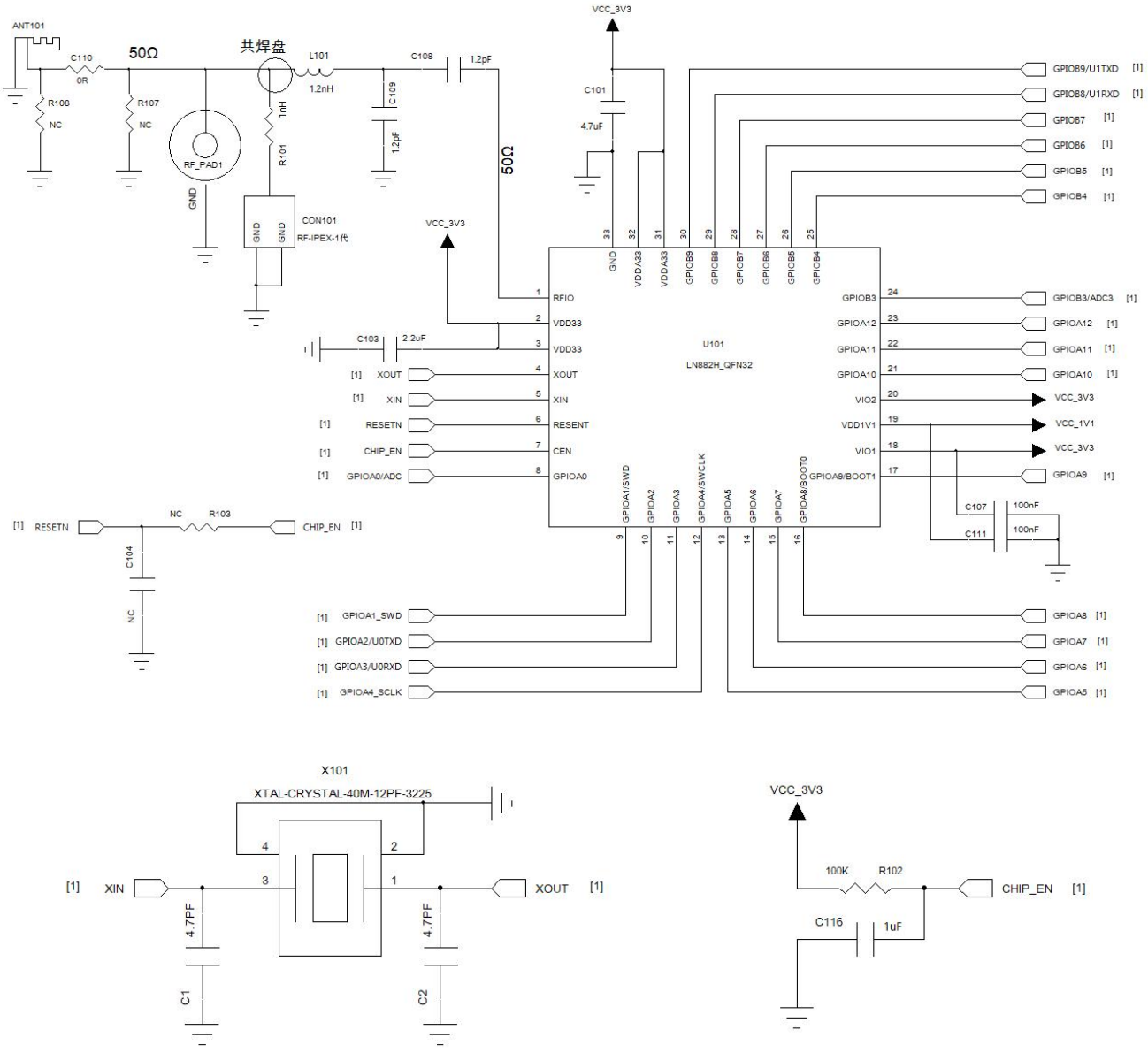
At present, LN882H products are divided into three packages: QFN32, QFN24 and QFN40. Among them, QFN32 package and QFN24 package are built-in Flash, and QFN40 package requires external Flash. The number of GPIOs supported varies; a package with more pins can support more GPIO ports. Please refer to the Product Datasheet for supported Flash capacity and more product model descriptions.

If not specified otherwise, this document defaults to QFN32 packaged products.

2. Reference circuit

The circuit of LN882H only needs one passive crystal and about 10 Resistance/capacitance/inductance components. LN882H integrates Antenna Switch, RF Balun, RF Power Amplifier, Low Noise Amplifier, Filter, Power Management Unit and advanced self-calibration circuit. This high integration makes the design of peripheral circuit very simple.

The reference circuit of LN882H is shown in the following figure. (Screenshots of this document are based on LN882H_QFN32 package as an example).



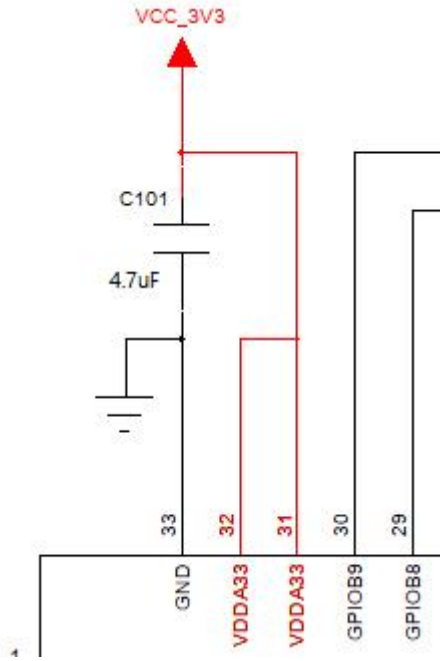
The key parts of the circuit are described in detail as follows.

2.1 Power supply

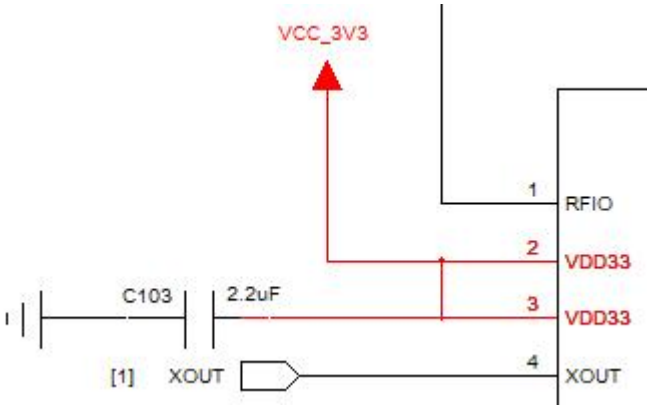
2.1.1 LN882H_QFN32

The detailed description of the power pin of the QFN32 packaged LN882H is as follows:

- PIN 31 and PIN 32 are the power supply input pins of the internal RF PA, using 3.3V operating voltage, and the maximum voltage cannot exceed 3.6V. When LN882H is in TX state, the instantaneous current is large, it is recommended to add 4.7μF large capacitor to the ground near the pin position. If the PCB space is enough, it is recommended to place another 100nF capacitor to the ground.

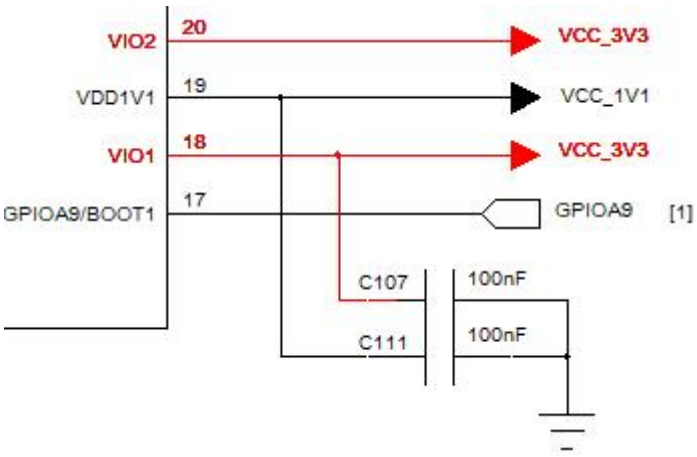


- Pins 2 and 3 are the supply input pins for the internal LNA and PLL, using 3.3V operating voltage, and it is recommended to add a 2.2μF capacitor to ground close to the pins.

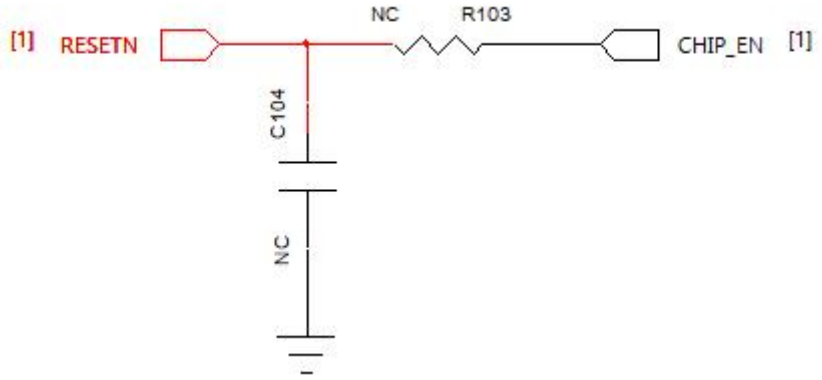


- PIN 18 (VIO1) is the power supply input PIN of the I/O interface, PIN 20 (VIO2) is the power supply input

pin of the I/O interface, which can support 2.6V to 3.6V operating voltage, 3.3V is recommended. It is recommended to add a 100nF capacitor to ground near the pin position.



- PIN 6 is the system Reset pin. One NC capacitor should be reserved to connect to the ground, and one NC resistor should be reserved in series to enable Chip_EN.



- PIN 7 is the chip-enabled pin (Chip_EN) and requires an additional 100K pull-up resistor to 3.3V and a 1μF capacitor to the ground. See "Power-on timing" section.

Notice:

- The recommended power supply voltage for LN882H is 3.3V, and the output current should meet 500mA and above.
- At the power inlet, please evaluate whether to add ESD protection devices according to the use scenario.

2.1.2 LN882H_QFN40

The power characteristics of QFN40 package and QFN32 package are basically the same, only the pin sequence number is different. The power pin of the QFN40 package is detailed as follows:

- PIN 38 and PIN 39 are the power supply input pins of the internal RF PA, which use 3.3V operating voltage and the maximum voltage cannot exceed 3.6V. When the LN882H is in TX state, the instantaneous current is large, it is recommended to add 4.7μF large capacitor to ground near the pin position, and if the PCB space is sufficient, it is recommended to place another 100nF capacitor to ground.
- Pins 3 and 4 are the supply input pins for the internal LNA and PLL, using a 3.3V operating voltage, and it is recommended to add a 2.2μF capacitor to ground close to the PIN location.
- PIN16 (VIO1) is the power supply input PIN of the I/O interface, and PIN21 (VIO2) is the power supply input pin of the I/O interface, supporting 2.6V to 3.6V operating voltage. Among them, the supply input voltage of VIO2 must be consistent with the supply voltage of external SPI Flash, and 3.3V is recommended. It is recommended to add 0.1μF capacitance to ground near the pin position.
- PIN 7 is the system Reset pin. One NC capacitor should be reserved to connect to the ground, and one NC resistor should be reserved in series to enable Chip_EN.
- PIN 8 is the chip-enabled pin (Chip_EN) and requires an additional 100K pull-up resistor to 3.3V and a 1μF capacitor to the ground.

2.1.3 LN882H_QFN24

The power characteristics of QFN24 package and QFN32 package are basically the same, only the pin sequence number is different. This will not be explained in detail here.

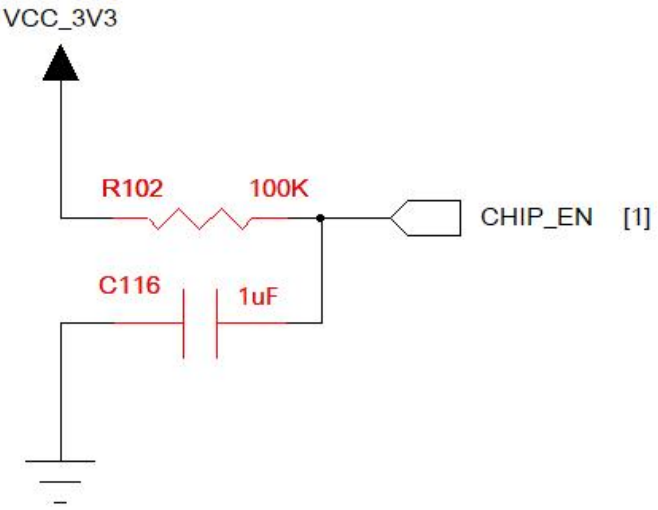
The differences in the power pin definitions for each package are shown in the following table.

QFN40	QFN32	QFN24	Pin Name	Pin description
1	1	1	RFIO	Wi-Fi RF transmitter/receiver
3	2	2	VDDA33	3.3v power supply
4	3	3	VDDA33	3.3v power supply
5	4	4	XTAL	Crystal output
6	5	5	XIN	Crystal input
7	6	6	RESETn	system reset
8	7	7	CHIP_EN	chip enable
16	18	11	VIO1	I/O power supply 1
20	19	18	DVDD11	1.1v power output

21	20	17	VIO2	I/O power supply 2
38	31	23	VDDA33	power supply for PA
39	32	24	VDDA33	3.3v power supply

2.1.4 Power-on timing

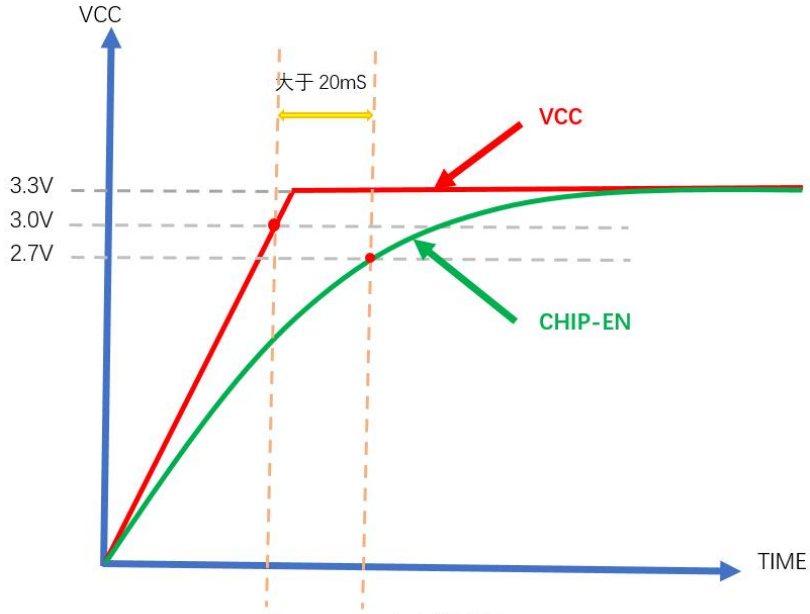
In order to ensure that the chip works properly when powered on, Chip_EN needs to add RC delay circuit. The recommended circuit is as follows:



When designing the RC delay circuit of Chip_EN, it is necessary to ensure that the time interval is at least 20ms from the time when the VCC is powered up to 3.0V to the time when the Chip_EN is raised to 2.7V.

The recommended values for RC circuit devices are R=100 kΩ and C=1 μF, which can be adjusted according to the actual situation if there are anomalies.

Power-on timing diagram is as follows:



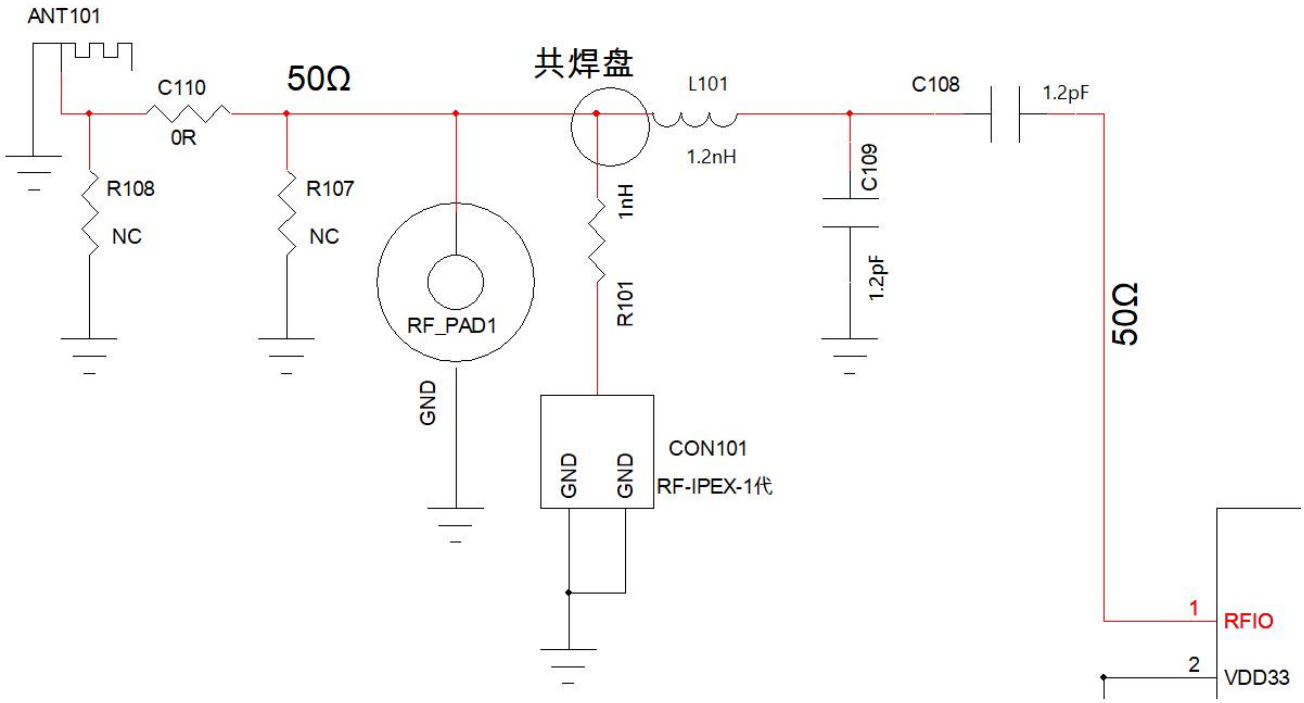
VCC 和 CHIP-EN 上电时序图

2.2 Radio Frequency (RF)

- Conduction matching: T type or π type matching, matching needs to be adjusted according to the actual impedance.
- Antenna matching: it is recommended to reserve the matching position of T type or π type, and the matching should be adjusted according to the actual impedance.
- The RF trace needs to be controlled according to the 50 Ω characteristic impedance.

According to the product requirements, please confirm which antenna connection method should be used, IPEX RF test bench or onboard PCB antenna? And whether RF PAD is required.

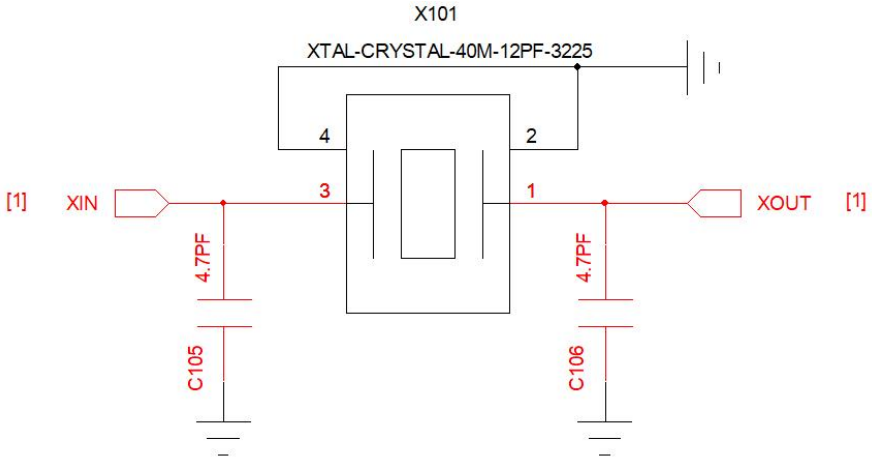
The reference design is as follows:



2.3 Crystal

2.3.1 Reference circuit

In the crystal XIN, XOUT output end, need to add matching capacitor to the ground, to adjust the load capacitance of the crystal. The schematic diagram of the crystal part is as follows:



In the picture above, the values of C105 and C106 are recommended to use 4.7pF. If the crystal model is not verified and the frequency deviation is large, please adjust the matching capacitance value according to the actual test situation.

2.3.2 Selection of crystal specifications

The specifications of crystal selection are as follows:

- f0 (Nominal Frequency)：40MHz；
- Frequency Tolerance：≤±10ppm@ room temperature;
- TC (Frequency Stability)：≤±20ppm@-40℃~+105℃；
- Operating Temperature：-40℃~+105℃；
- CL (Load Capacitance)：12pF；

2.3.3 List of validated crystal models

For different types of crystals, the temperature compensation parameters will have differences. To ensure better performance, it is recommended to use the verified models in the table below.

Model	Manufacturer	Description
E3SB40E005002E	HOSONIC	40M;3.2X2.5mm; CL=12PF; TC=+/-20ppm; -40°C~+105°C;

If you use unverified models, please provide samples to us for verification and use after passing.

2.4 UART

LN882H has three groups of UART ports, only UART0 supports hardware flow control.

Baud rate range supported: 2400~3M, bps.

2.5 GPIO

2.5.1 GPIO overview

LN882H-QFN32 has a total of 20 GPIO ports, divided into GPIOA and GPIOB two groups, which can be configured separately. Group A ports can be configured in interrupt mode.

For each GPIO, once powered on and started, its initial state is the general GPIO function, which can be configured separately by the software in the following modes:

- Pull-up input,
- Pull-down input,
- High impedance input,
- Push-pull output,

In addition, QFN40 packs has 26 GPIO ports, 6 of which are occupied by QSPI Flash (A13-15 and B0-2). The QFN24 package has 12 GPIO ports.

2.5.2 GPIO driver capabilities

The driving ability of the GPIO is different when the output is high and the output is low. The driving currents of the GPIO ports A0-A12 and B3-B9 are shown in the following table (unit: mA) :

GPIO	A0	A1	A2	A3	A4	A5	A6
Output High	5	5	5	5	5	5	10
Output Low	10	10	10	10	10	10	20

A7	A8	A9	A10	A11	A12
10	10	10	10	10	5
20	20	20	20	20	10

B3	B4	B5	B6	B7	B8	B9
5	5	5	5	5	5	5
10	10	10	10	10	10	10

2.5.3 Special Instructions and Precautions

There are a few things to note about reusing GPIOs:

- The Analog Input function (ADC) requires the use of 6 specialized GPIO ports, as described in the "ADC" section.

- If SWD is enabled, it will use GPIOA1 and GPIOA4. These ports will be changed to general purpose GPIO on power on, and then quickly initialized to SWD when the BOOT ROM is running. Note: If the SWD function is turned off after power on, it will not be turned on again.

Notice:

- GPIO A8 has 110K pull-down resistors inside by default. If a pull-down circuit is added outside, it may not be able to enter UART Boot mode after power on.
- GPIO A9 has 110K internal pull-up resistors by default.
- The initial state of GPIO A8 and A9 will involve different Boot modes. Please pay special attention when using them. For details, please refer to the "Boot Mode" section of this document or specification.
- All GPIOs use 110K internal resistors for internal pull up/pull down/high resistance states.

2.6 The Boot mode

LN882H has two starting modes, which are determined by the logical value state of GPIOA8 and GPIOA9 when powered on. The startup configuration is shown in the following table. Please refer to the product datasheet for more details.

Boot Mode	GPIOA8	GPIOA9	Description
FLASH Boot	**1**	**0**	GPIOA8 default internal 110K resistance pull-down; GPIOA9 default internal 110K resistance pull-up;
	0	**1**	
UART Boot	**0**	**0**	CPU will wait data from UART to program flash.
SDIO Boot	**1**	**1**	

2.7 Download firmware

There are two ways to download firmware.

- UART download, GPIOA2 and GPIOA3 are required. The A8 and A9 need to be kept low at the same time (see "Boot mode" section), and then power on, it will enter the UART boot mode, and finally use the serial port to download;
- JILNK download, GPIOA1 and GPIOA4 are required.

2.8 ADC

The LN882H has a 6-channel, 12-bit sampling analog-to-digital converter (ADC).The pin assignment is shown in the table below. For more details, please refer to the datasheet:

QFN40	QFN32	QFN24	PAD NAME	Function
9	8		GPIOA0	ADC2
10	9	8	GPIOA1	ADC3
13	12	9	GPIOA4	ADC4
31	24		GPIOB3	ADC5
32	25		GPIOB4	ADC6
33	26		GPIOB5	ADC7

3. PCB Layout Considerations

3.1 PCB Layout and Layer Definition

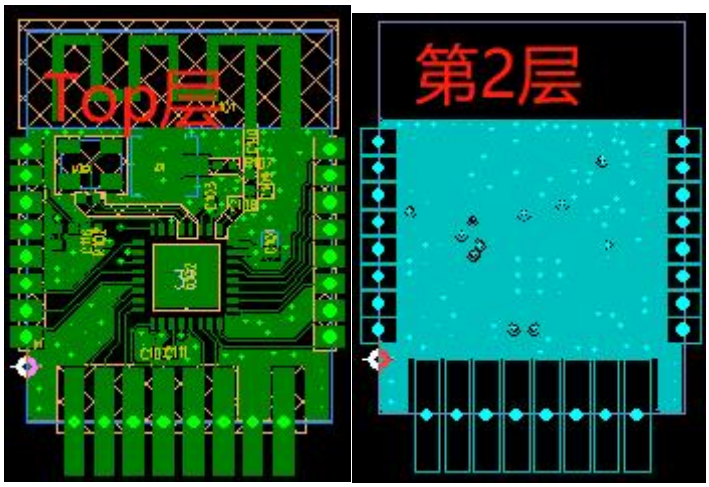
3.1.1 Layer Definition

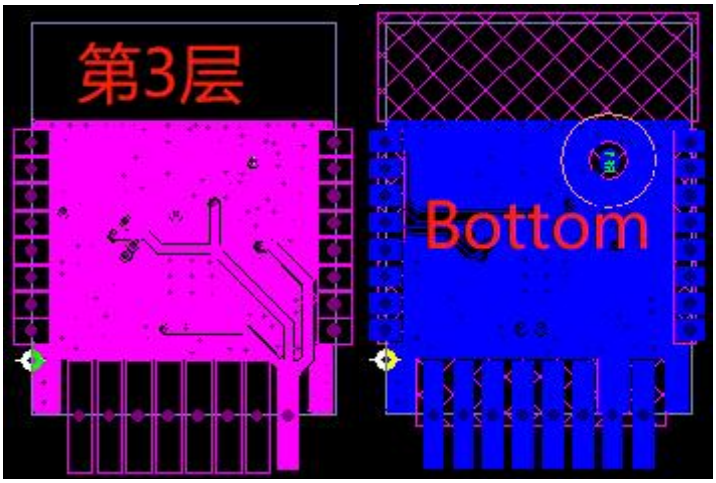
This chapter takes the PCB of LN882H_QFN32 module as an example to introduce the key points of LN882H layout design.

It is recommended to use the layer definition in the table below.

Layer No.	Layer Attribute	Description
Top layer	Component layer	Mainly used for placing component and signal wires;
2nd layer	GND layer	No lines routing, Complete and GND plane must be guaranteed;
3rd layer	GND/Power layer	Mainly used for GND plane and power wires, less signal wires;
Bottom layer	Signal layer	GND plane and signal wires;

The board diagram for each layer is as follows:





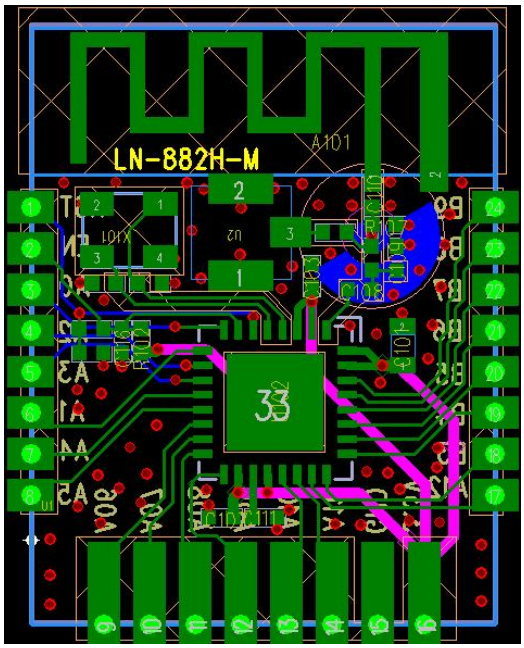
3.1.2 Layout

For the PCB layout scheme of LN882H, it is recommended to use 4-layer through-hole board and place components on a single side.

The overall layout of LN882H is shown below.

Notice:

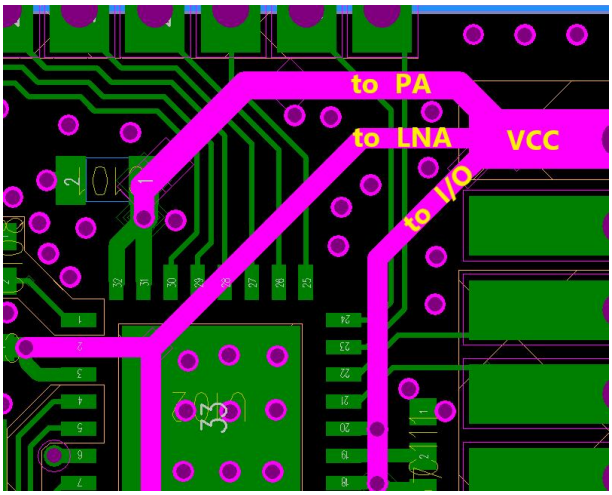
- It is strongly recommended to use a shielding case, and place all components including crystals, IC, RF, surface power wires, etc. in the shielding case, and to place the antenna outside the shielding case.



3.2 Power wire routing principle

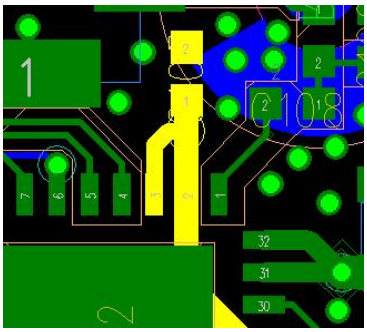
- The power wire must be bifurcated close to the VCC power supply inlet, and connected to the power domain input pins of PA, LNA, and IO functions in a star shape. Please refer to the "Power" section of

this document for the corresponding pins for each power domain. Please refer to the following image:



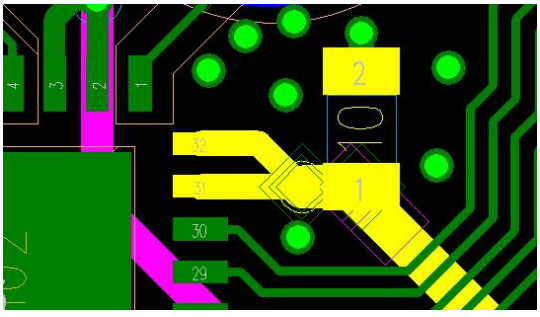
star shape

- The decoupling capacitor C103 of the power supply of the LNA should be placed close to pin2 at the chip end, and the width of the line should be as wide as possible, not less than 15mil.



V_LNA power supply wire

- The power wire should go to the inner layer, as little as possible to go to the surface layer, especially not to the surface layer near the antenna.
- The decoupling capacitor C101 of the PA power supply should be placed as close as possible to pin31 and pin32 at the chip end. The current carrying capacity should be no less than 500mA, and the wire width should not be less than 20mil. If the layer is changed, the number of through holes should be sufficient.



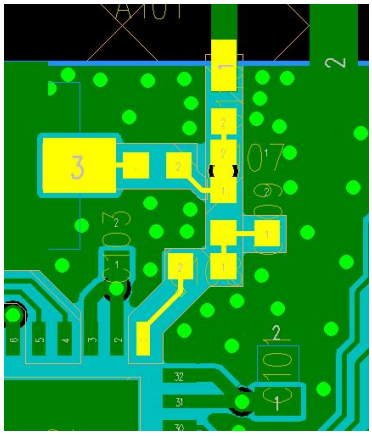
V_PA power supply wire

3.3 Control of RF Wires

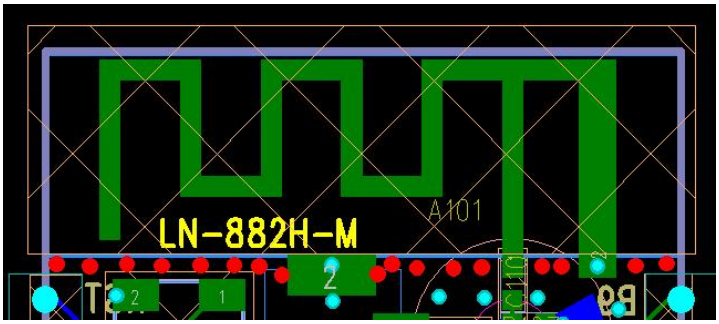
3.3.1 Principle of RF wire routing

RF wire routing needs to pay attention to the following matters:

- The RF impedance wire should routing in the top layer, try not to change layers and punch holes.
- RF components and impedance wires, up, down, left and right must have a complete GND package, the GND layer directly below the reference layer must be complete GND. The spacing between the RF wire and the GND on both sides of the same layer, should not be less than the line width of the impedance wire, the bigger the spacing, the better.



- There should be as many ground holes as possible in the ground near the antenna and RF wires.



- RF impedance wire routing, to avoid acute Angle, to try to use obtuse Angle or arc.
- The impedance matching components at the IC end should be placed close to the chip, and the matching components at the antenna end should be placed close to the antenna.
- RF signal components, wires and antennas must be away from the power supply and high-speed data and other components and wires, but also need to have a good ground separation, so as not to interfere with each other. Such as DCDC, crystal, Flash and other devices and wires, as well as LCD, camera, power,

PWM, UART, SDIO and USB signal wires.

- The width of the RF impedance wire is required to be controlled according to the characteristic impedance of 50 ohms.

3.3.2 Control of characteristic impedance

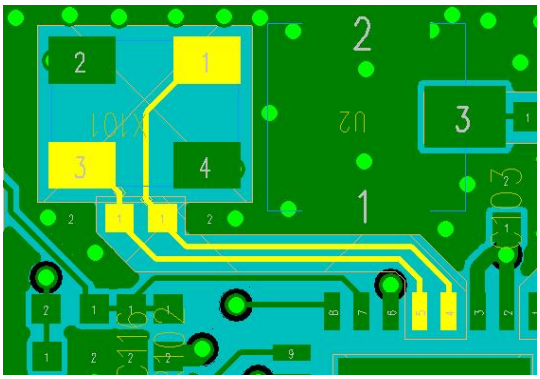
The RF impedance wire must be controlled according to 50Ω. The impedance control is mainly determined by the distance to the reference layer and the line width. The distance to the reference layer is also related to the stacked structure of the PCB board. There are many kinds of PCB stacked structures. If you need to know which one to use, you can consult the PCB board factory.

The impedance wire that needs to be controlled is expressed, and the reference layer of each line is explained, and then it is given to the PCB manufacturer, so that the PCB manufacturer can calculate and adjust the line width.

3.4 Crystal

In PCB, the crystal must pay attention to the following matters:

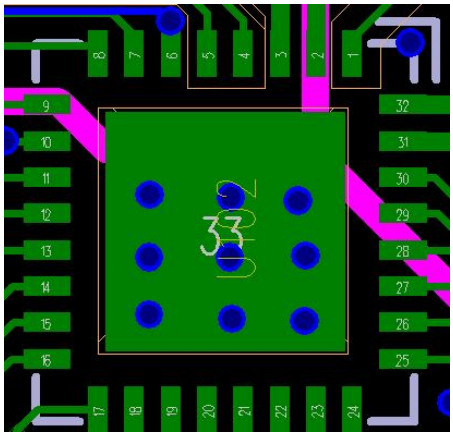
- In the crystal placement area, keepout is required for the surface layer to reduce interference and distribute capacitance.
-
- In the second layer directly below the crystal, the GND should be complete, and no interference wires such as power supply, radio frequency, and high-speed signals can be taken under the crystal.
- The clock signal wire of the crystal should be shielded with complete GND to avoid interference from other signals.
- Crystalline GND pads should be drilled directly into the main formation, not directly into the surface.



3.5 EPAD

Devices with large heat need to dissipate heat, and the EPAD of LN882H is used to dissipate heat.

- The EPAD needs to add VIA to increase heat dissipation. If copper leakage can be designed in the Bottom layer of the back of the chip at the same time, it will be more conducive to heat dissipation.
- EPAD needs to add a copper keepout in the Top layer of PCB to separate EPAD and chip PIN and avoid short circuit.



3.6 Wi-Fi antenna or module placement area

The performance of the antenna is greatly affected by the surrounding environment, and the performance of the antenna will be very different in different positions. Whether using the LN882H chip or the LN882H module, it is necessary to pay attention to the placement of the Wi-Fi antenna on the large baseboard to ensure that the wireless performance is as desired.

3.6.1 Wi-Fi Antenna Placement Principles

The key principles of antenna placement are as follows:

- The antenna must be placed in an open area, must be placed in the edge position, preferably in the four corners of the position, in order to better radiation signals to the space;
- The antenna must be far away from the metal, and there cannot be metal objects higher than the antenna near the antenna, so as not to be occluded by the metal objects.
- Antenna performance must be tuned, impedance should be matched;
- There can be no interference sources near the antenna. The antenna should be away from the power supply, other antennas, high-speed data signals, etc., so as not to interfere with each other.
- Antenna belongs to strong signal, there can be no sensitive weak signal nearby, so as to avoid

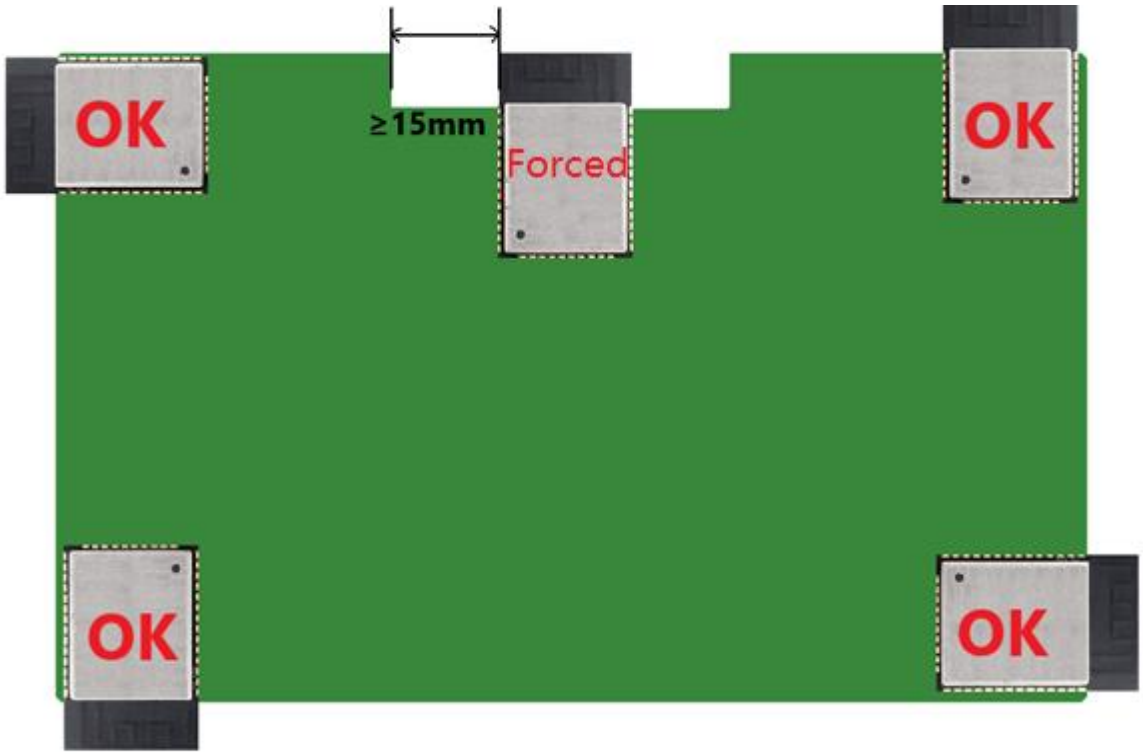
interference by the antenna, such as crystal/clock, important signal and other devices and transmission wires;

3.6.2 The module placement area

If the module is placed on another large PCB board, the placement area of the module needs to be paid special attention to the following aspects:

- The antenna area of the module, which includes the entire antenna keepout on the module, must be completely outside the metal area of the PCB;
- It is recommended to put the module in the four corners to achieve the best performance;
- If the module is placed in the middle area of the board edge, then the performance will inevitably deviate. In this case, make sure that there is sufficient keepout in the antenna area. Make sure that the antenna on the module is at least 15mm away from the metal on both sides of the PCB. Even if this is required, it is also very forced performance, so it is not recommended.

An example is as follows:

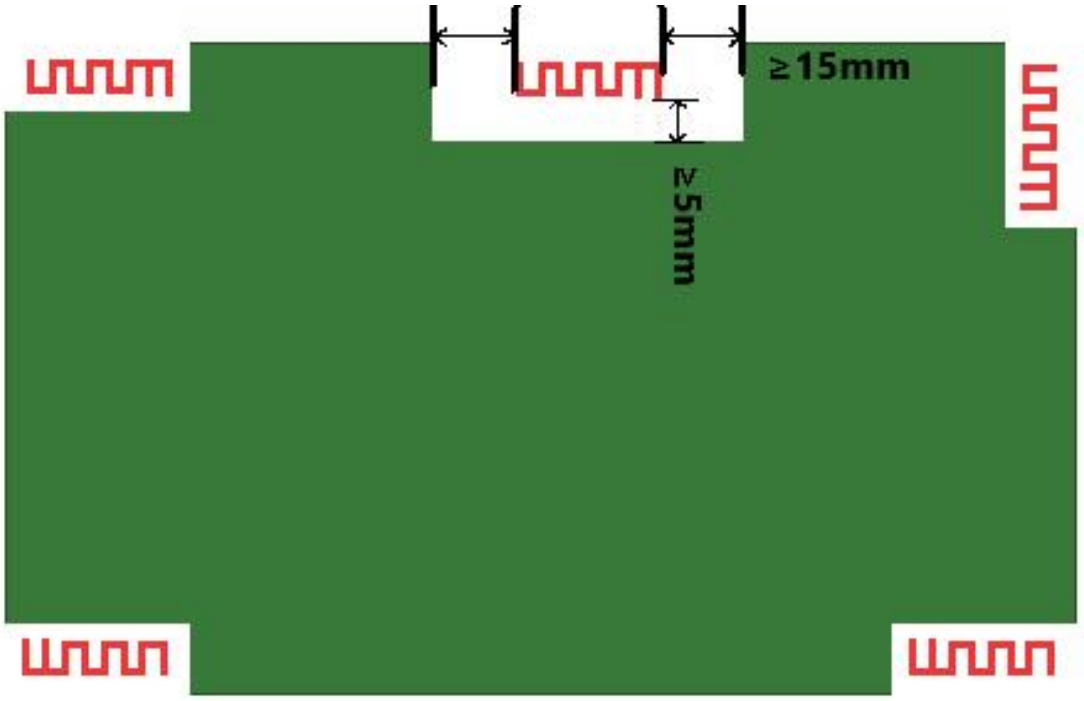


3.6.3 On-board PCB antenna placement area

If the LN882H chip is directly used to design on the large PCB board, and the Wi-Fi antenna is in the way of onboard PCB antenna. The considerations for onboard PCB antennas are the same as for modules.

- It is recommended to place the antenna at the four corners for the best performance.
- If the antenna is placed in the middle area of the board edge, the performance will inevitably deviate. In this case, make sure that there is sufficient keepout in the antenna area. Make sure that the antenna is at least 15mm away from the metal on both sides of the PCB and at least 5mm away from the inner test metal. Even if this is required, it is a forced performance and is not recommended.
- Usually the chip is placed close to the antenna position.

An example is as follows:



3.6.4 Placement area for off-board antennas (IPEX, etc.)

If the antenna uses the IPEX seat connection form, such as the use of FPC antenna or external antenna, also be sure to ensure that the antenna is suspended in the space away from the metal, to ensure that there is no relatively large, relatively high metal objects nearby to block the signal.

4. FAQ

4.1 RF power is low

Reason analysis:

1），The conductive impedance mismatch of the motherboard will lead to low conductive transmit power of the motherboard.
The impedance mismatch will cause the gain of the RF PA inside the chip to decrease, and the output power will naturally decrease. Impedance mismatch also sometimes makes the PA output signal distorted and linear worse, resulting in worse EVM. Chip output to reserve a π type of matching position, be sure to adjust the impedance of the motherboard conduction to around 50Ω.

2），The impedance mismatch of the antenna will lead to the low efficiency of the antenna, and then lead to the low transmission power of the antenna.
To ensure that the motherboard conduction impedance debugging ok, and then find the antenna factory debugging antenna impedance. It is recommended that the antenna side reserve a π-type match in advance.

4.2 The EVM, Frequency Erorr performance of RF TX is poor

Reason analysis:

1），The power ripple is too large.

If the ripple at the source of the power supply is large, try to add more than 10μF capacitance at the power inlet.
If the ripple of the source end of the power supply is normal and the ripple becomes larger when the signal is transmitted, a 10μF filter capacitor can be added near the pin31 and pin32 powered by the PA. The capacitor must be placed close to the chip pin, otherwise the improvement effect is not obvious. In general, the power ripple peak value should be <80 mV when the packet of MCS7@11n is sent. When sending 11m@11b, the power ripple peak should be <120 mV.
If the power ripple at pin2 and pin3 is also large, it can also be tried to increase the capacitance value at pin2 and pin3 pin positions to more than 10μF to see if there is an improvement.

2），The crystal or clock signal is poor.

If the trace of the crystal or clock signal is disturbed, the performance of the RF TX will be affected. It is necessary to keep the crystal as far away from interference devices as possible during PCB layout, and to ground the clock signal during routing. See the "Crystals" section.
If the quality of the crystal itself is not good and the frequency offset is too large, it will affect the performance of the RF TX modulation index. Try to replace the crystals of other models, or adjust the crystals from the OK board.

4.3 RF receiving sensitivity deviation

Reason analysis:

1），The first thing to rule out is that the impedance is not well adjusted.

Firstly, it is necessary to ensure that there are no problems with the transmit performance of the motherboard and antenna, including indicators such as transmit power, EVM, and frequency error. If there is a problem, please debug the matching impedance first. If the impedance is not matched, the insertion loss of the receiving link will be too large, and then the sensitivity will be reduced.

2），Interference caused by external noise.

In terms of motherboard conduction. RF wires should be well isolated, and high-frequency signals and power supplies should not be taken next to them. For detailed requirements, please refer to the chapter of "Control of RF Wires".
In terms of spatial coupling. There should be no other wires on the PCB surface beside the antenna, such as the power line, the trace of the clock signal, the trace of the UART and other high-speed signals, which may be coupled with each other. In addition, other surrounding with the same frequency, the same channel transmitting equipment too much, mutual interference.

5. Disclaimer and copyright notice

This document may refer to the information of third parties. All the referenced information is provided "as is", and Shanghai Lightning Semiconductor Technology Co., LTD (Hereinafter referred to as 'Lightning Semiconductor') does not make any guarantee for the accuracy and authenticity of the information.

Lightning Semiconductor makes no warranties regarding the contents of this document, including its merchantability, fitness for a particular purpose, or any other Lightning semiconductor proposals, specifications, or samples referred to elsewhere.

All information in this document, including url address for reference, is subject to change without notice.

Lightning Semiconductor does not make any warranty as to whether this document infringes the rights of any third party, nor is it responsible for any intellectual property infringement caused by the use of the information in this document. This document does not grant any intellectual property rights license, express or implied, by estoppel or otherwise.

The Wi-Fi Alliance member logo is owned by the Wi-Fi Alliance. The Bluetooth logo is a registered trademark of Bluetooth SIG. All trade names, trademarks and registered trademarks mentioned in the documents are the property of their respective owners and are hereby declared.

The information contained in this document is the exclusive property of Lightning Semiconductor and may not be distributed, reproduced or disclosed in whole or in part without the prior written permission of Lightning Semiconductor.