INTERCONNECT INDUCTANCE EXTRACTION FOR ANALOG AND RF IC DESIGNS

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INTRODUCTION

Mobile networking is a fundamental need for most of us in the 21st century. In addition to the smartphone revolution, the Internet of Things (IoT) creates a paradigm in which communication is essential across a broad range of activities and devices. New products that rely on interconnectivity are being introduced every day, such as autonomous cars that "speak" to each other to avoid collisions, implanted medical devices that monitor and transmit critical health data, and worldwide computer games that enable tens of thousands of concurrent users. Communication has evolved significantly across different generations, from 3G to 4G to 5G, with the operating frequency band increasing with each new generation. For 5G technology, that frequency range can exceed 40GHz [1]. Realizing satisfactory performance in the face of these requirements creates a new design specification for integrated circuit (IC) designs.

Analog and radio frequency (RF) ICs are the hardware backbone supporting these communication technologies. At such high operating frequencies, parasitics can significantly affect the performance of the chips. Specific care is needed to ensure analog/RF designs take into account post-layout resistance, capacitance, and inductance parasitics to confirm design simulation results match the silicon-fabricated results. However, resistance and capacitance parasitics have typically been the main focus for post-layout simulation, while inductance extraction has been limited to custom inductor characterization. That's no longer enough for today's analog/RF designs. The increasing impact of inductance parasitics means inductance extraction for interconnect is now essential to ensuring accurate post-layout simulations.

INTERCONNECT PARASITICS EXTRACTION AT HIGH FREQUENCIES

Interconnects made of a metal conductor and separated by dielectric are not ideal. Signals going through interconnects encounter delays caused by material parasitics consisting of resistance, capacitance, and inductance parasitics. Resistance parasitics are due to the opposition of electrons passing through the metal, while capacitance parasitics are caused by the electric field between two conductors.

Inductance parasitics are the result of the magnetic field created by passing current through a conductor. Any current passing through a conductor creates a magnetic field. This magnetic field then induces a parasitic current either on the same metal (self-inductance), or on another metal crossing the magnetic field (mutual inductance).

Focusing on resistance and inductance, interconnect impedance can be expressed as following:

$$Z = R + j2\pi fL$$

Where Z is impedance, R is the resistance value (in Ohms), f is the operating frequency, and L is the inductance value (in Henrys).

In direct current (DC) and low frequencies, interconnect impedance is dominated by resistance parasitics. However, as the frequency increases, inductive impedance becomes more dominant and affects signal propagation, as shown in Figure 1.

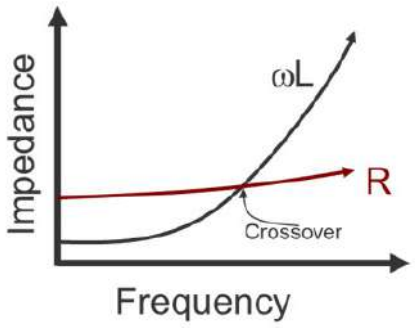

Figure 1: Resistive and inductive impedance versus frequency.

SKIN EFFECT

One interconnect parasitics phenomenon caused by high frequency is called the "skin effect." The skin effect occurs because, as frequency increases, the current distribution is no longer homogenous across the conductor cross-section. The current tends to flow closer to the conductor surface (skin), between the outer surface and a level called the skin depth [2]. The skin depth depends on the frequency of the current and the electrical and magnetic properties of the conductor depth—it is defined as the depth where the current density is just 1/e (about 37%) of the value at the surface. Figure 2 shows a cross-section view of current distribution in two cases: low frequency, where skin depth is higher than the conductor width, and high frequency, where skin depth is smaller than the conductor width.

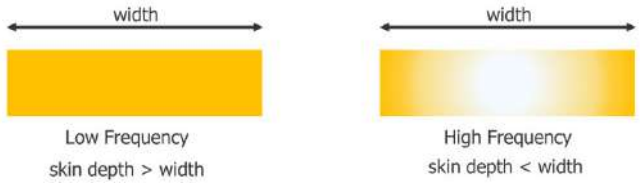

Figure 2: Cross-sectional view of current distribution at low frequency and high frequency. Yellow represents the current flows within the cross-section of the interconnect. At high frequencies, the current flows closer to the conductor surface.

Skin effects increase resistance parasitics of the conductor at high frequency [3]. They also lead to a frequency-dependent value for the effective inductance and resistance seen by the current. Such effects must be taken into account to achieve accurate results during parasitic extraction. Figure 3 shows an RLC network for an interconnect in which frequency-dependent skin effect has been taken into account.

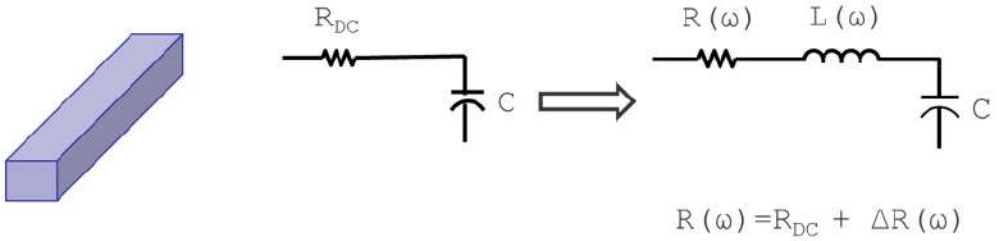

Figure 3: Parasitics modeling for an interconnect, showing the changes due to the skin effect.

INDUCTANCE-RELATED EFFECTS

In general, the objective of parasitics extraction is to be as accurate as possible compared to physical silicon measurements. Inductance parasitics can have several impacts on chip performance. One set of effects appears in long wires (e.g., buses) in the form of changes in delay, ringing (signal oscillation), and overshooting (exceeding target values). Another effect creates reflections in transmission lines due to an impedance mismatch [4]. For RF blocks, inductance parasitics can result in reduced gain and bandwidth. For a voltage-controlled oscillator (VCO) design, inductance parasitics can result in drifting of oscillating frequency. Because of these impacts, running inductance extraction during chip design and analysis is extremely important, especially for analog and RF designs that operate at a high frequency.

INDUCTANCE PARASITICS EXTRACTION

Inductance parasitics occur due to the magnetic field generated by currents passing through conductors. Inductance extraction has two main challenges [5]:

- **Inductance has a long-range effect.** Unlike capacitance extraction, where the electric field is shielded by the conductors (which helps limit the couplings to the closest neighbor), inductance is a long-range effect. The magnetic field is not terminated on neighboring conductors.
- **Inductance is a loop phenomenon.** As inductance is a property of current loops, it is difficult to determine which current loops are significant.

There are two main methodologies for inductance extraction: loop inductance [6] and partial element equivalent circuit (PEEC) [7].

The loop method is used to compute inductance with return paths. Inductance is a property of closed current loops, where a loop is formed between one net carrying the current (signal net) and another net carrying the return current in the opposite direction (return net). In a chip design, there are power/ground wires that carry the return current for signal wires. Loop extraction is typically used for full-chip inductance extraction.

The PEEC method is used to compute inductance for a straight wire segment carrying current. As inductance can only be computed for a closed loop, the current must return through a return path. Using this method, the return path is assumed to be infinitely far away [7]. The advantage of the PEEC method is that it avoids the need to search for all the possible return wires on the chip through which the current might return.

PEEC inductance extraction can be applied on selected critical nets to extract self and mutual inductances for RF and analog designs. It can also be used to extract differential pair nets in designs such as a voltage-controlled oscillator (VCO). Figure 4 shows an RLCK network for signal and ground nets using the PEEC mode, where each net is represented by an inductance value.

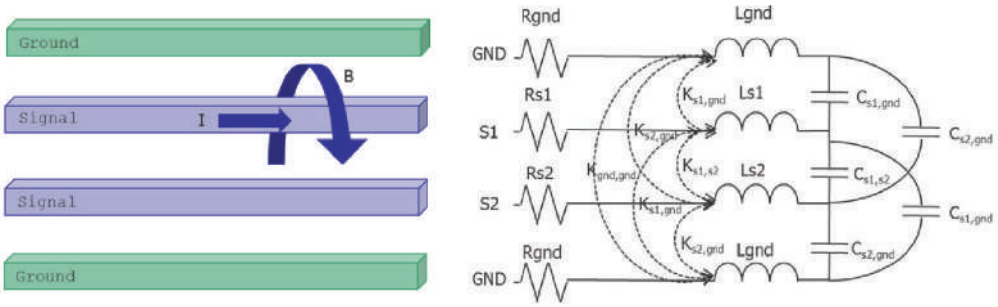

Figure 4: Extraction of signal and ground nets using PEEC mode.

INDUCTANCE EXTRACTION USING THE CALIBRE PLATFORM

The Calibre® xL extraction tool provides a fast and accurate field-solver-based engine for extracting inductance parasitics of on-chip interconnects. The Calibre xL tool is fully integrated with the Calibre physical verification framework, and the Calibre xRC™, Calibre xACT™, and Calibre xACT 3D extraction tools. This integration supports ease-of-use by enabling a fully integrated RCCLK extraction within one extraction run, and a single RCCLK netlist result.

By using the Calibre xL tool in conjunction with one of the Calibre RC extraction tools, designers can extract both self and mutual inductance parasitics, as well as resistance and capacitance extraction, and generate a single RCCLK netlist. The Calibre xL tool provides two use models for interconnect extraction: RCCLK extraction for selective user-defined critical nets, or full-chip RCCLK extraction. Calibre xL inductance results are viewed and debugged in the Calibre RVE™ results viewer.

Designers can select either loop or PEEC extraction mode, based on the application. Once a method is selected, designers enter the specific values as appropriate (Figure 5).

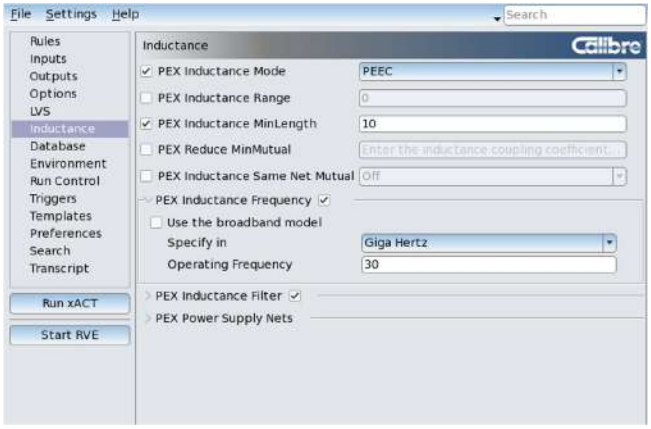

Figure 5: Inductance extraction setup within a Calibre xACT flow.

Figure 6 shows Calibre xL S-parameters results for a shield transmission line, where the results are highly correlated to full-wave field solver reference results up to 40 GHz.

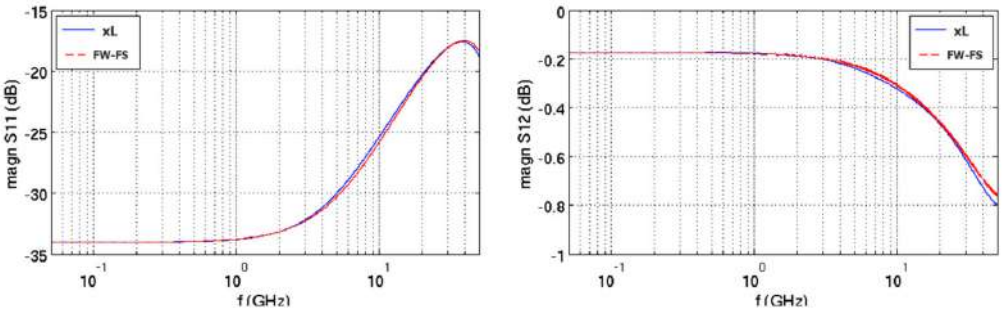

Figure 6: S-parameters for a shielded transmission line using Calibre xL compared to full-wave field solver results up to 40 GHz.

SUMMARY

Parasitics extraction is essential for accurate post-layout simulation. While resistance and capacitance parasitics have typically been the main focus for interconnect parasitics extraction, increasing operating frequencies for analog and RF designs require self and mutual inductance parasitic extraction to ensure accurate circuit performance and high reliability. The Calibre xL tool provides a fast, accurate inductance extraction engine that is fully integrated with other Calibre extraction tools to generate a single RCCLK netlist, enabling designers to extract inductance for all the layout interconnects, or just for specified critical nets.

The list of products that depend on high frequency communications is growing rapidly, helping us navigate, innovate, and thrive in an increasingly connected world. At the same time, the success of these products depends on the accuracy and performance of the electronics driving them. By including inductance parasitic extraction in the design and verification flow, IC companies are ensuring their chips will deliver the highest level of circuit performance and reliability possible.

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