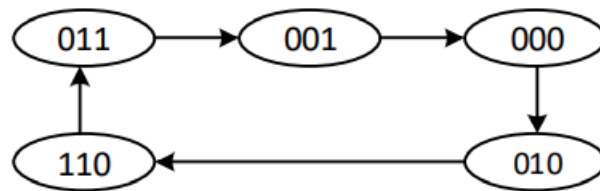


# Proiect CID

Să se proiecteze automatul de tranziții (a) folosind un numărător pe 4 biți descris de tabelul de adevăr (n) și un multiplexor (m).



## Automat de tranziții

1.



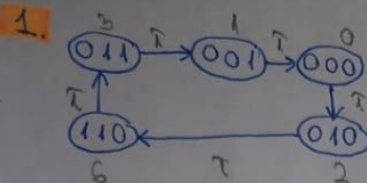
## Tabel de adevăr pentru numărătoare

A

r	clk	ld	en	Action
1	x	x	x	Reset
0		1	x	Load
0		0	1	Count
otherwise				Wait

## Multiplexor

### I. Numai MUX 2:1



A.

$\tau$	$ld$	$en$	Action
1	X	X	Reset
0	$\bar{X}$	1	Load
0	$\bar{X}$	0	Count
otherwise			Wait

1. Chemați 110X 2:1

numărător cu descărcare

$Q_C Q_B Q_A$	acțiune	Ld	En	DCBA
0 0 0 0	1	1	X	0 0 1 0
0 0 0 1	2	1	X	0 0 0 0
0 0 1 0	2	1	X	0 1 1 0
0 0 1 1	2	1	X	0 0 0 1
0 1 0 0	-	X	X	X X X X
0 1 0 1	-	X	X	X X X X
0 1 1 0	2	1	X	0 0 1 1
0 1 1 1	-	X	X	X X X X

Pentru C

$Q_C Q_B Q_A$	C
0 0 0	0
0 0 1	0
0 1 0	1
0 1 1	0
1 0 0	X
1 0 1	X
1 1 0	0
1 1 1	X

Pentru B:

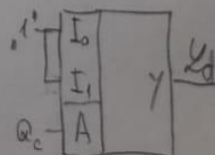
$Q_C Q_B Q_A$	B
0 0 0	1
0 0 1	0
0 1 0	1
0 1 1	0
1 0 0	X
1 0 1	X
1 1 0	1
1 1 1	X

Pentru A:

$Q_C Q_B Q_A$	A
0 0 0	0
0 0 1	0
0 1 0	0
0 1 1	1
1 0 0	X
1 0 1	X
1 1 0	1
1 1 1	X

Pentru Ld

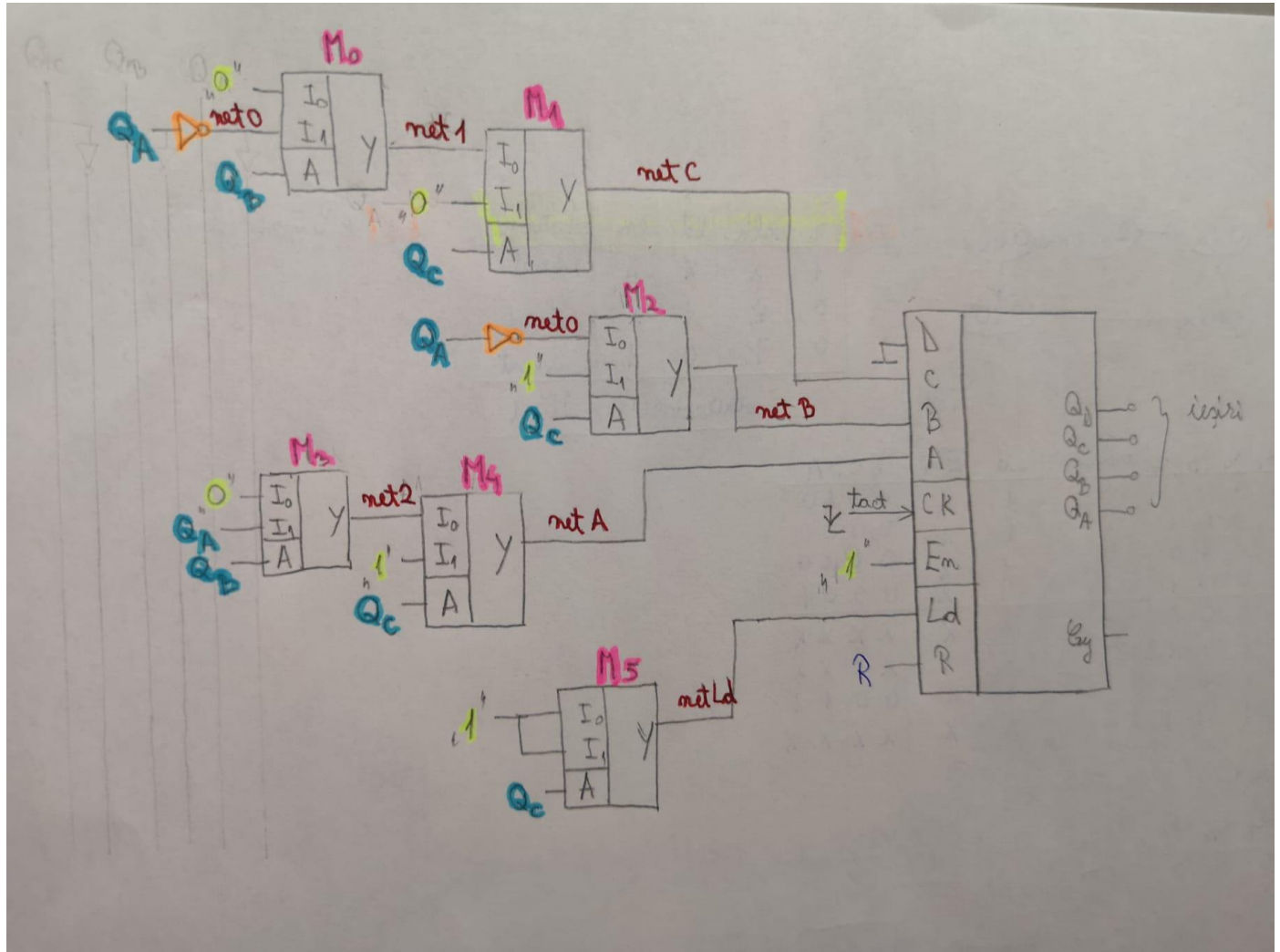
$Q_C Q_B Q_A$	Ld
0 0 0	1
0 0 1	1
0 1 0	1
0 1 1	1
1 0 0	X
1 0 1	X
1 1 0	1
1 1 1	X



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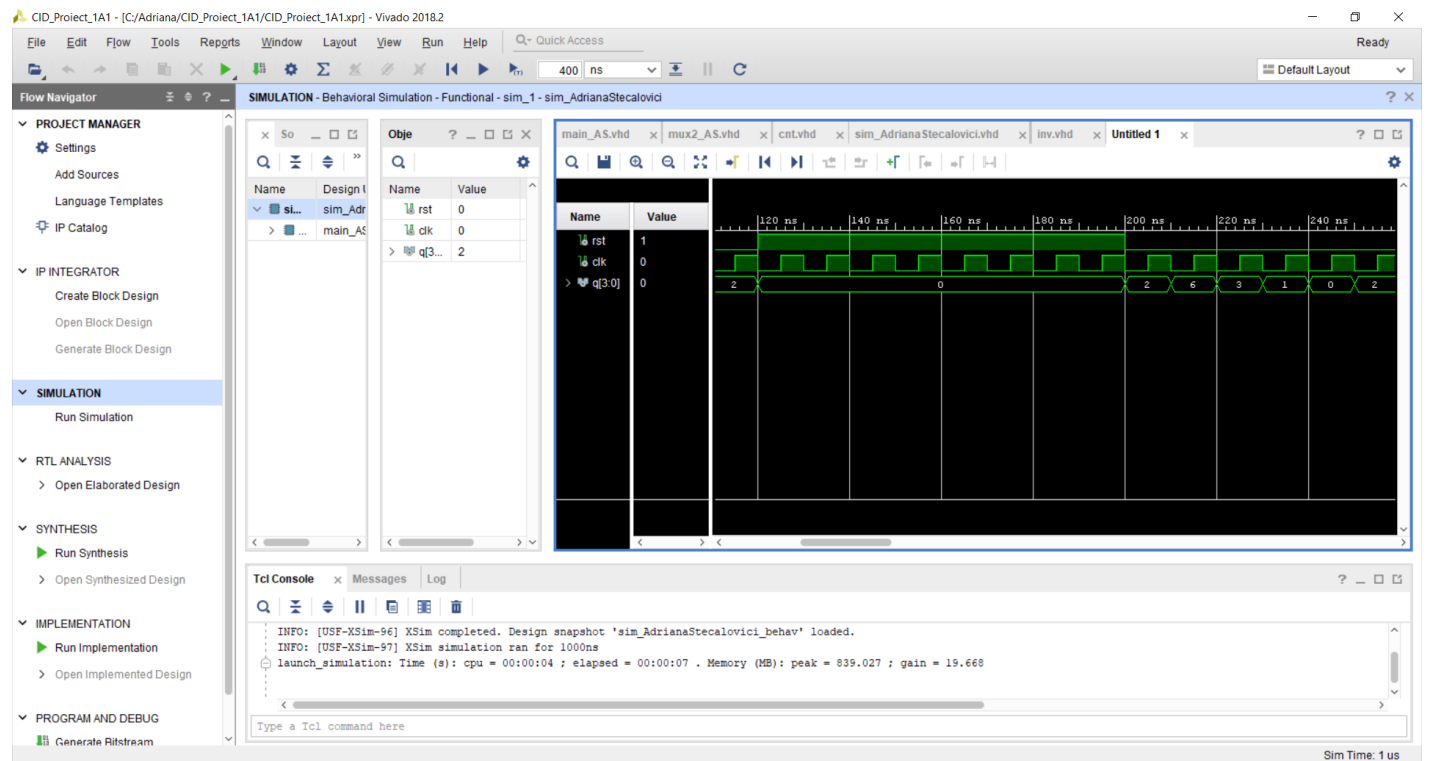
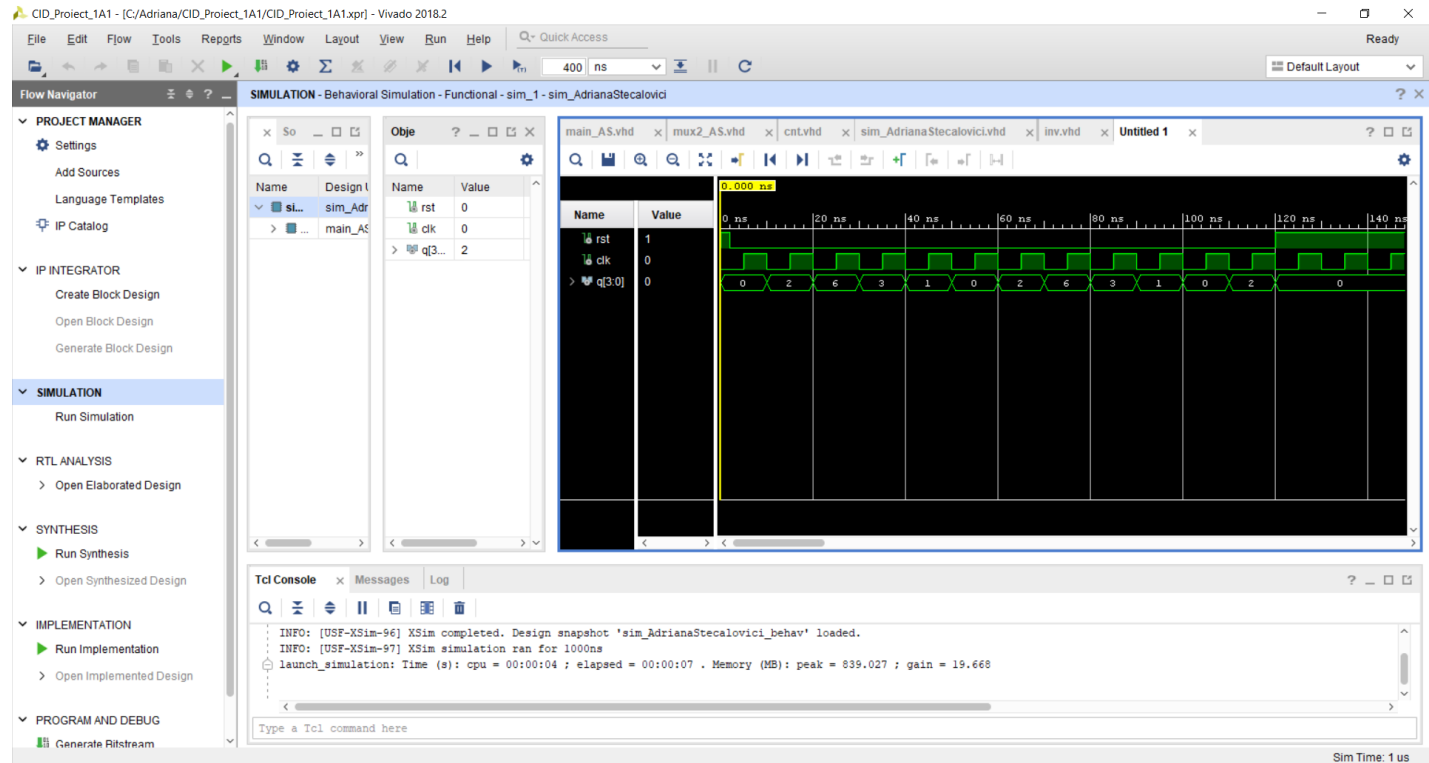
Grupa: 2123, semigrupa 2

Seria A



Adriana-Vasilica Stecalovici  
Grupa: 2123, semigrupa 2  
Seria A

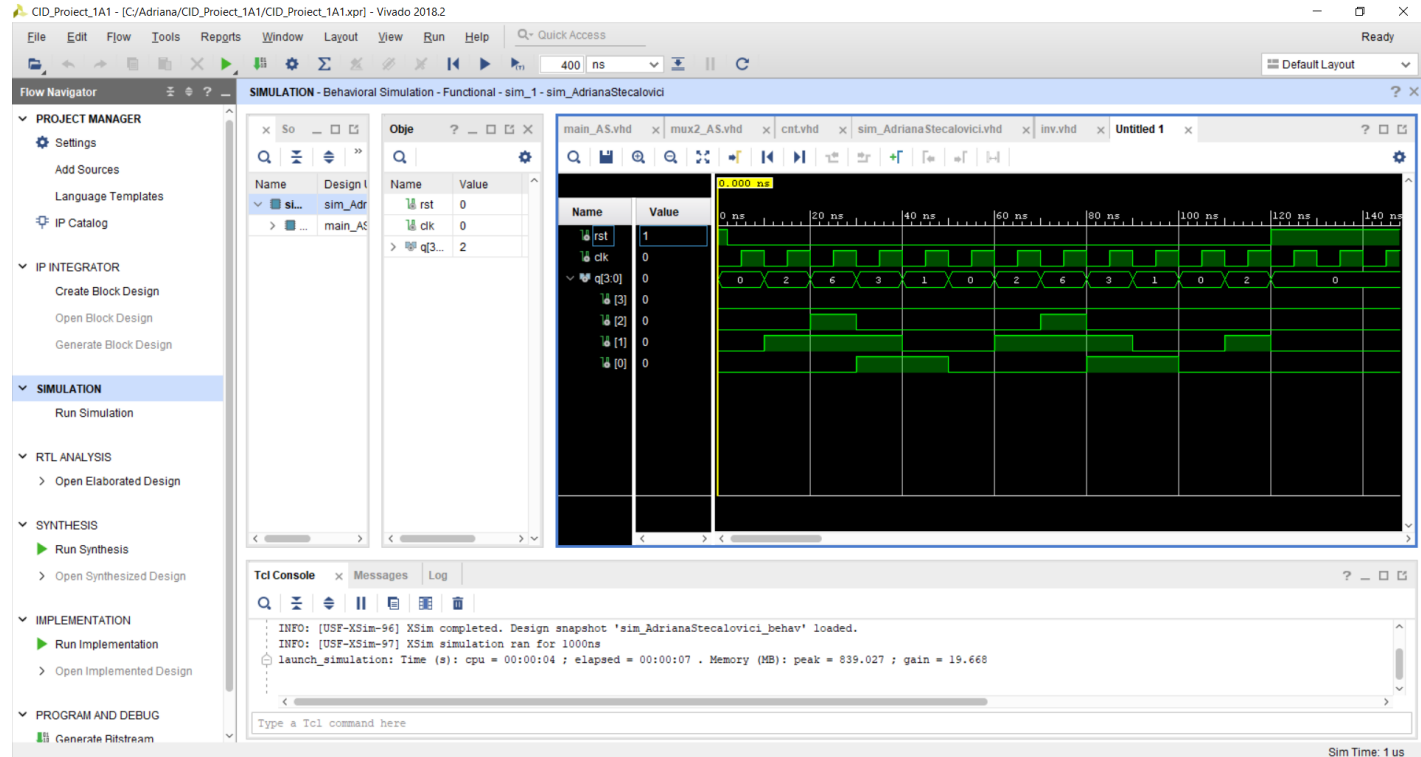
## ➤ Simularea:



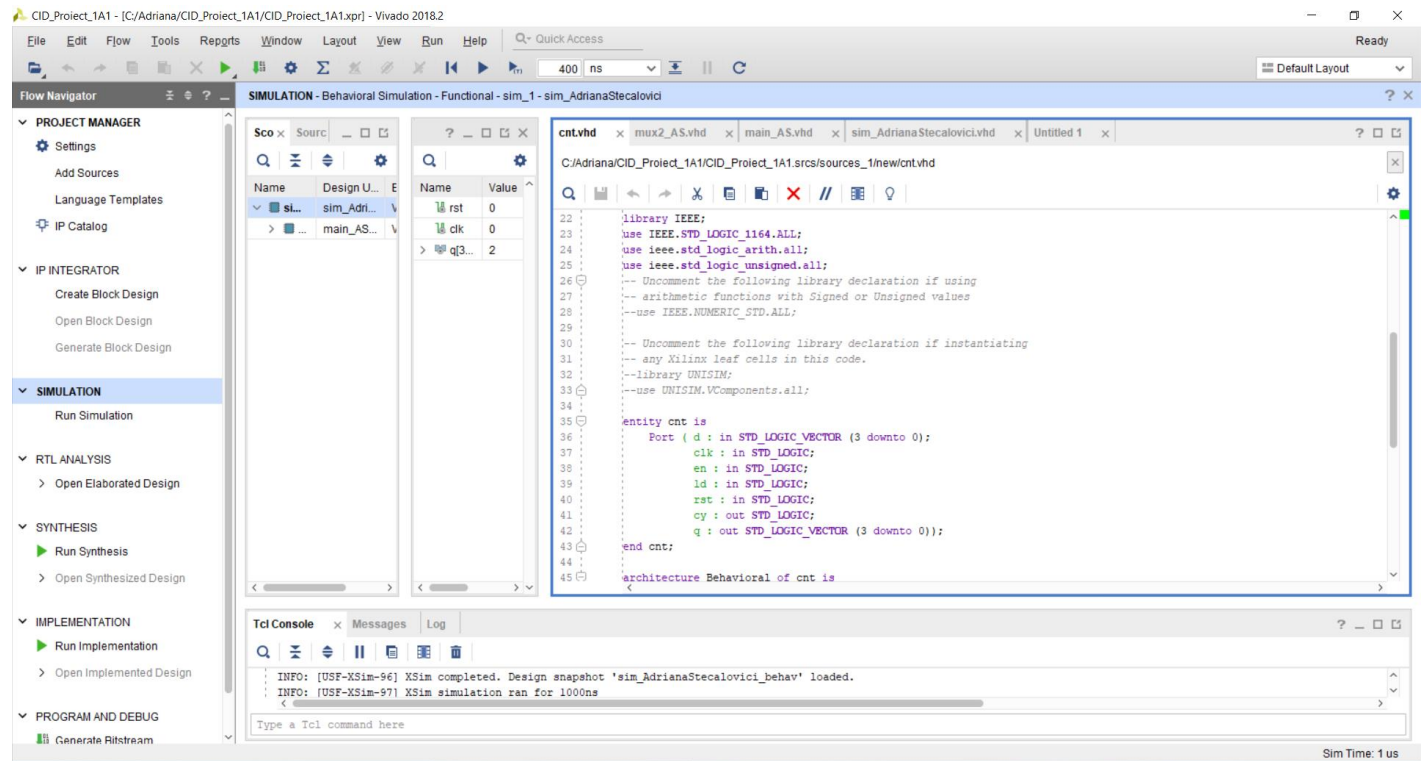
Adriana-Vasilica Stecalovici

Grupa: 2123, semigrupa 2

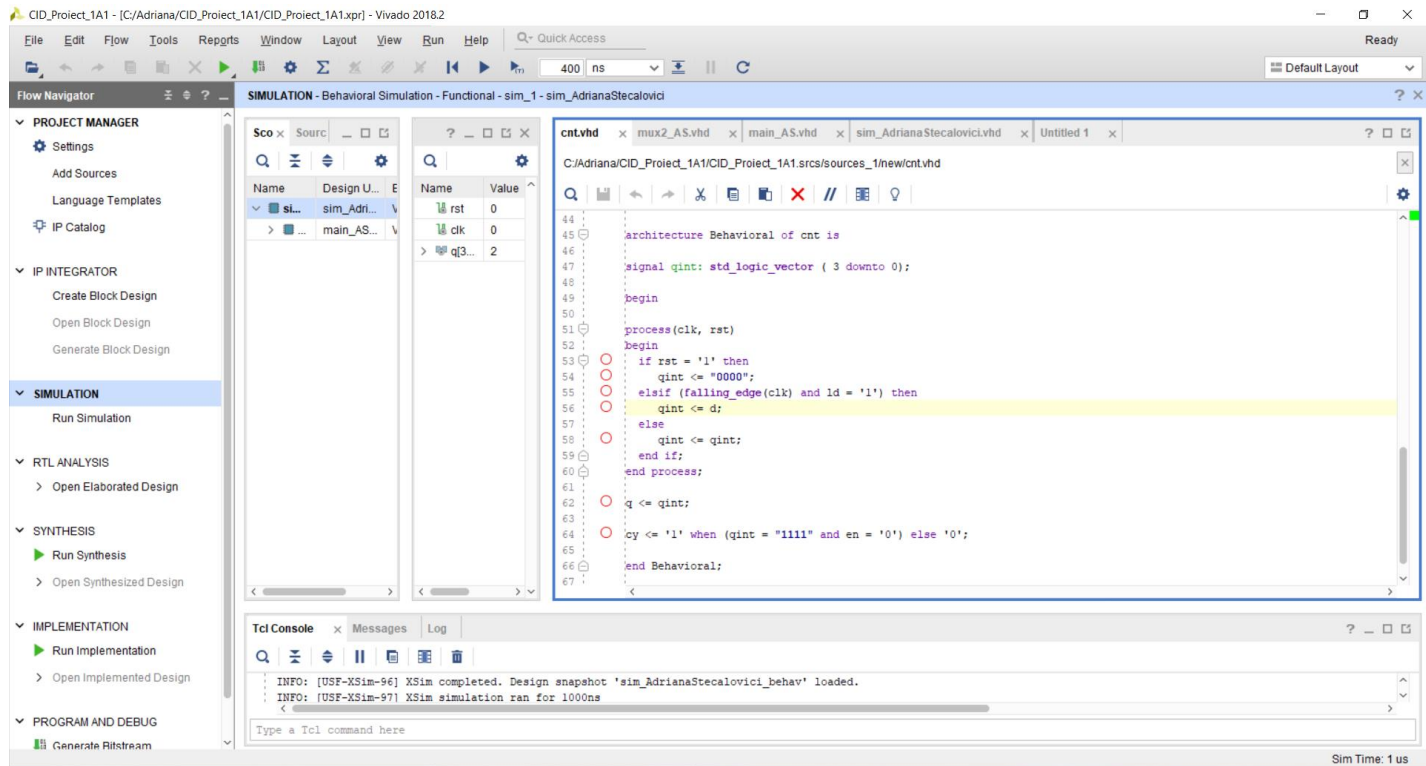
Seria A



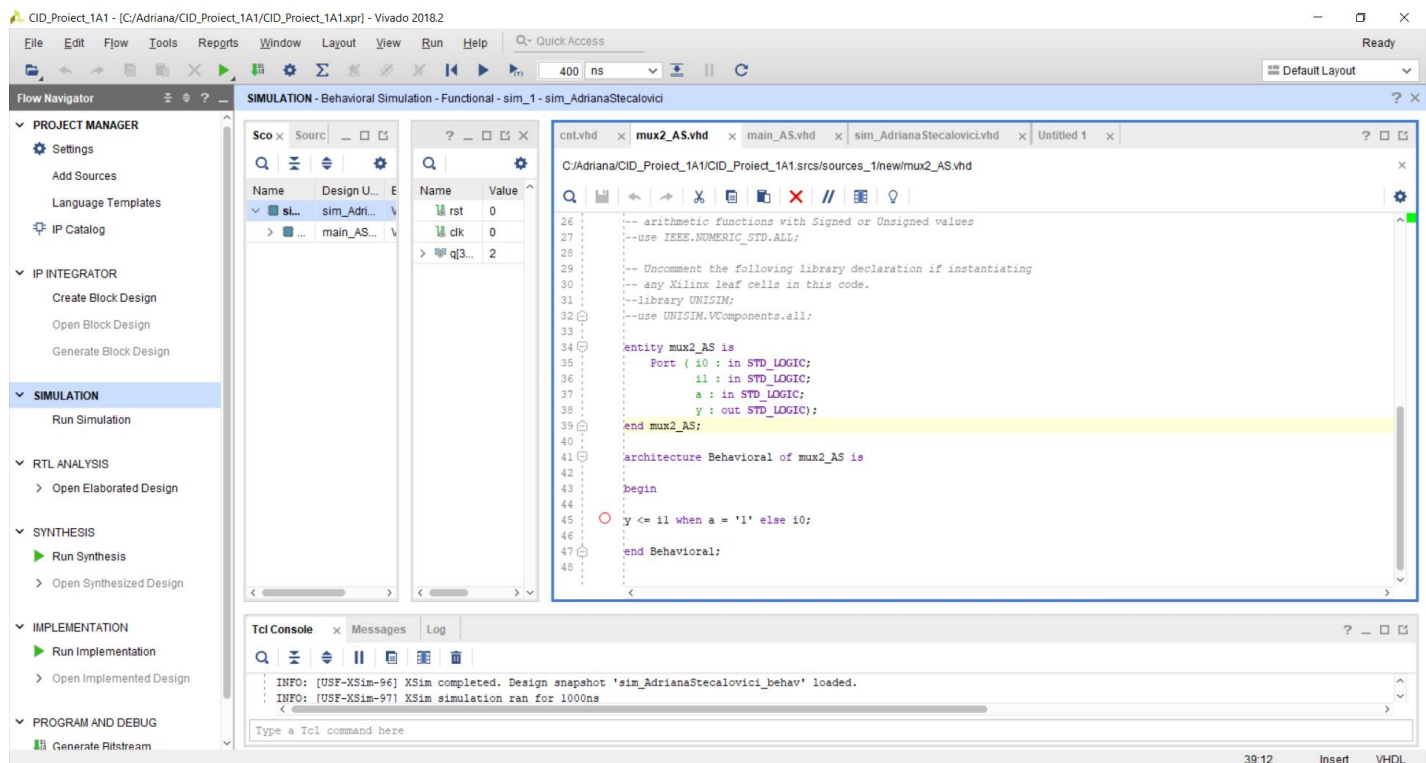
## ➤ Sursa cnt:



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Grupa: 2123, semigrupa 2  
Seria A



## ➤ Sursa mux2\_AS:



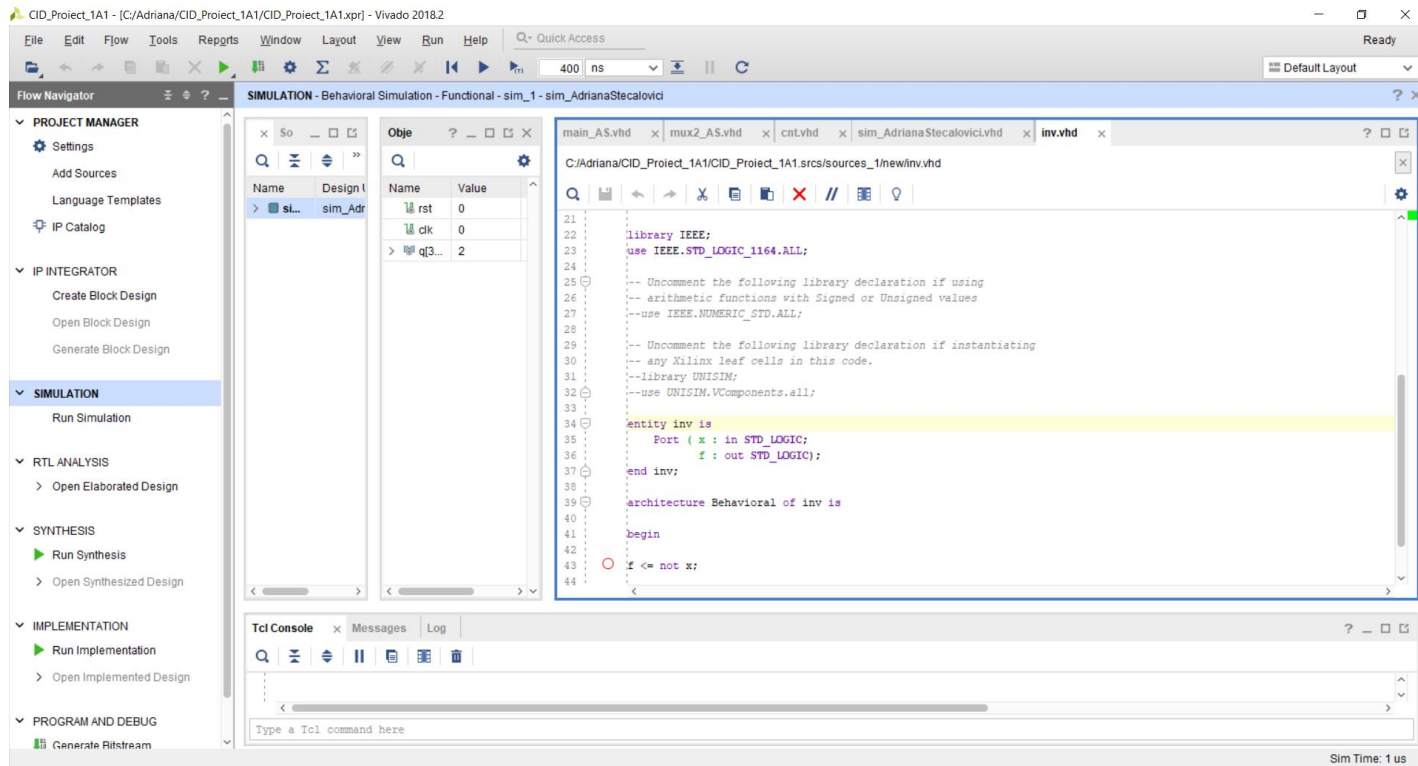


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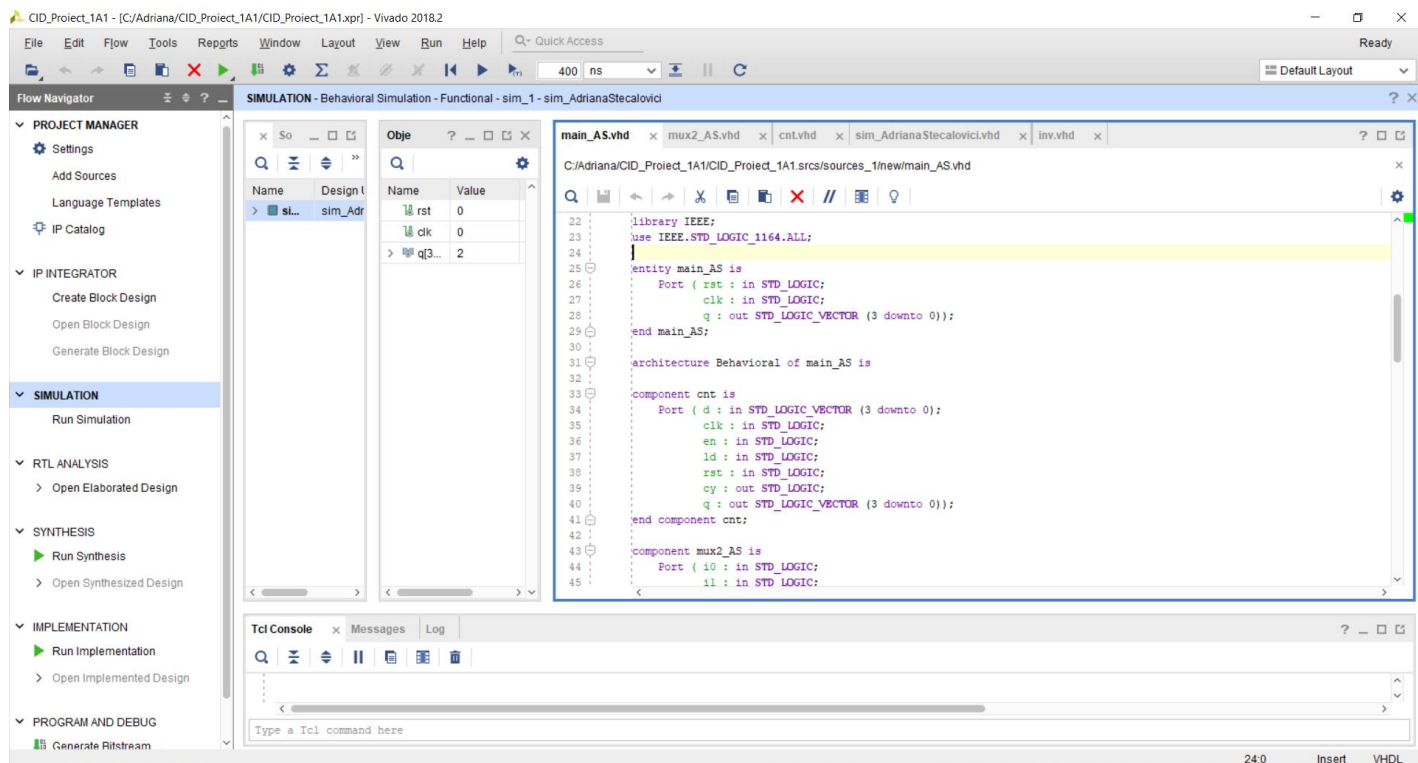
Grupa: 2123, semigrupa 2

Seria A

## ➤ Sursa inv:



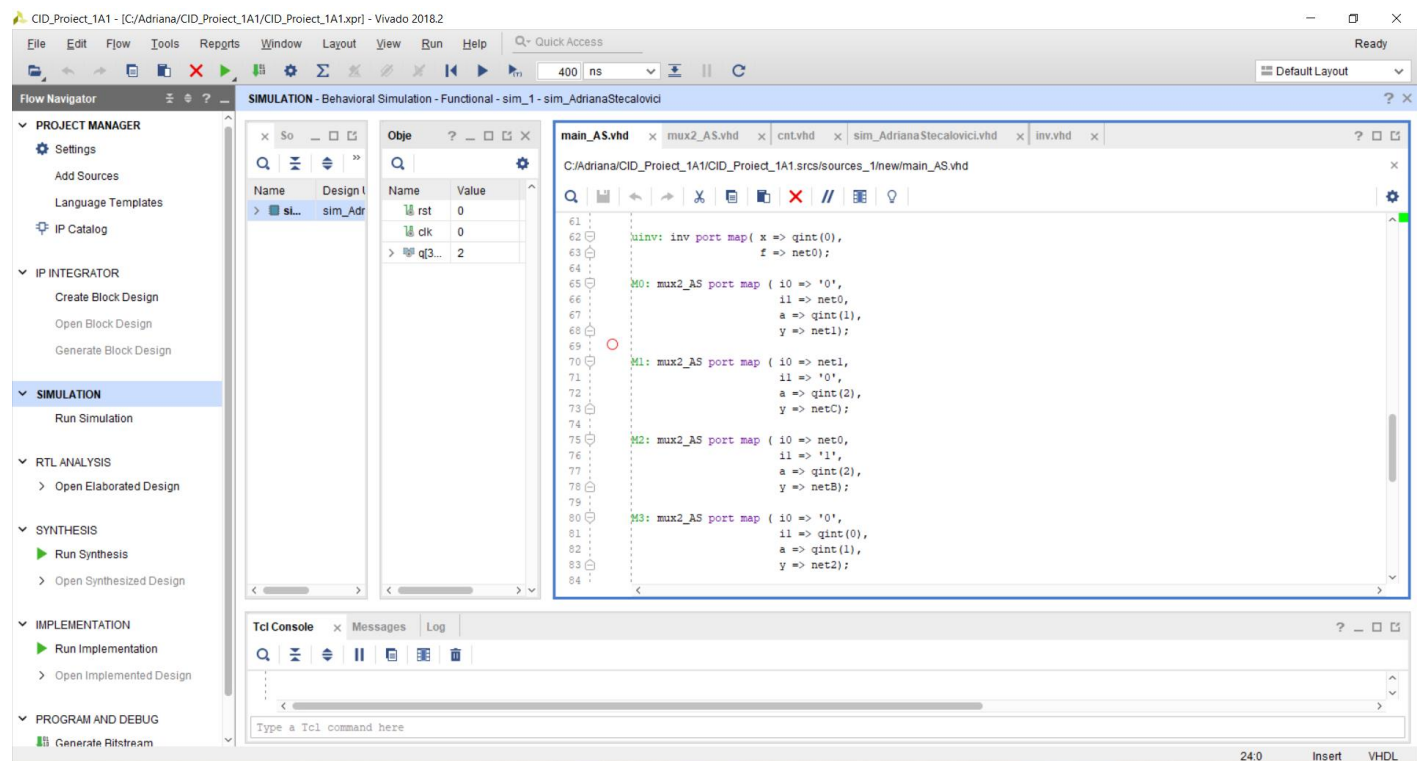
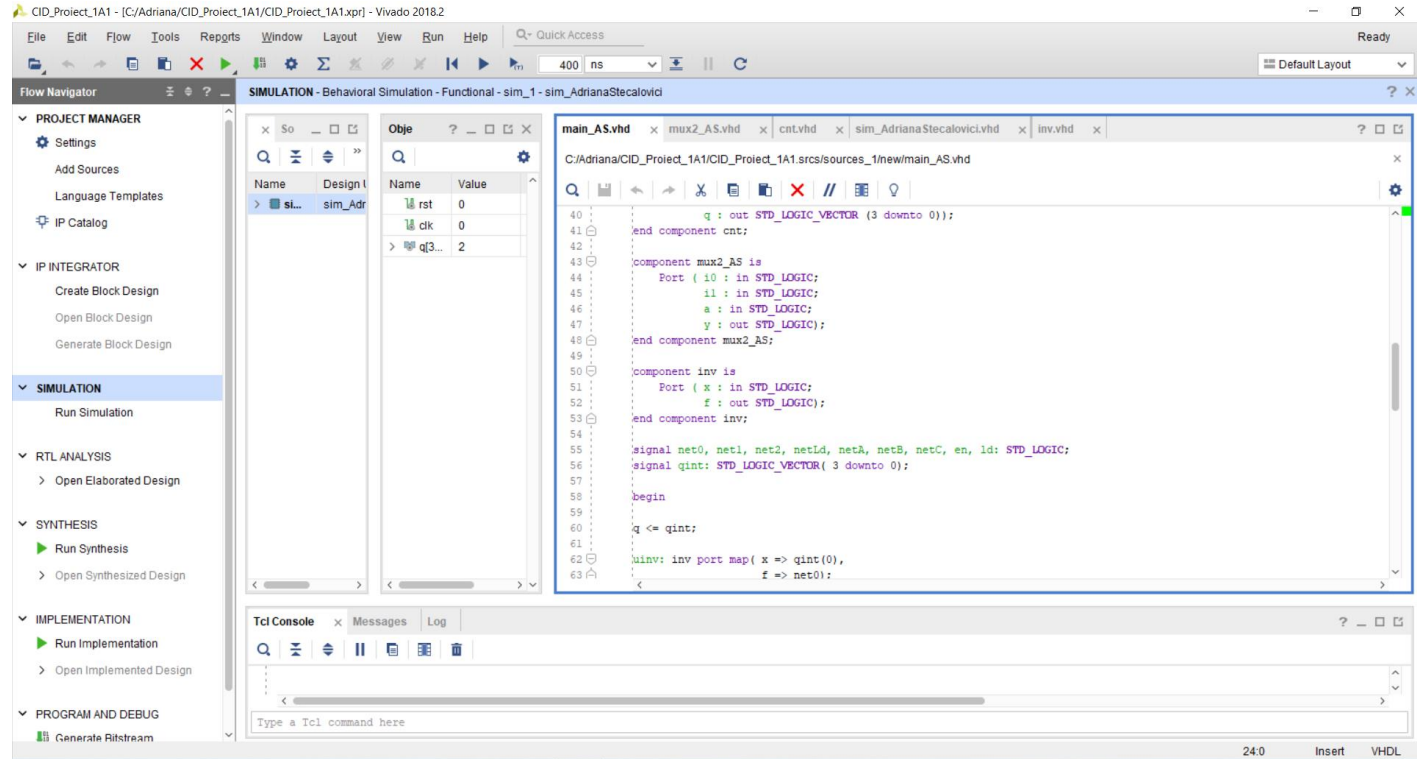
## ➤ Sursa main\_AS:



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Grupa: 2123, semigrupa 2

Seria A

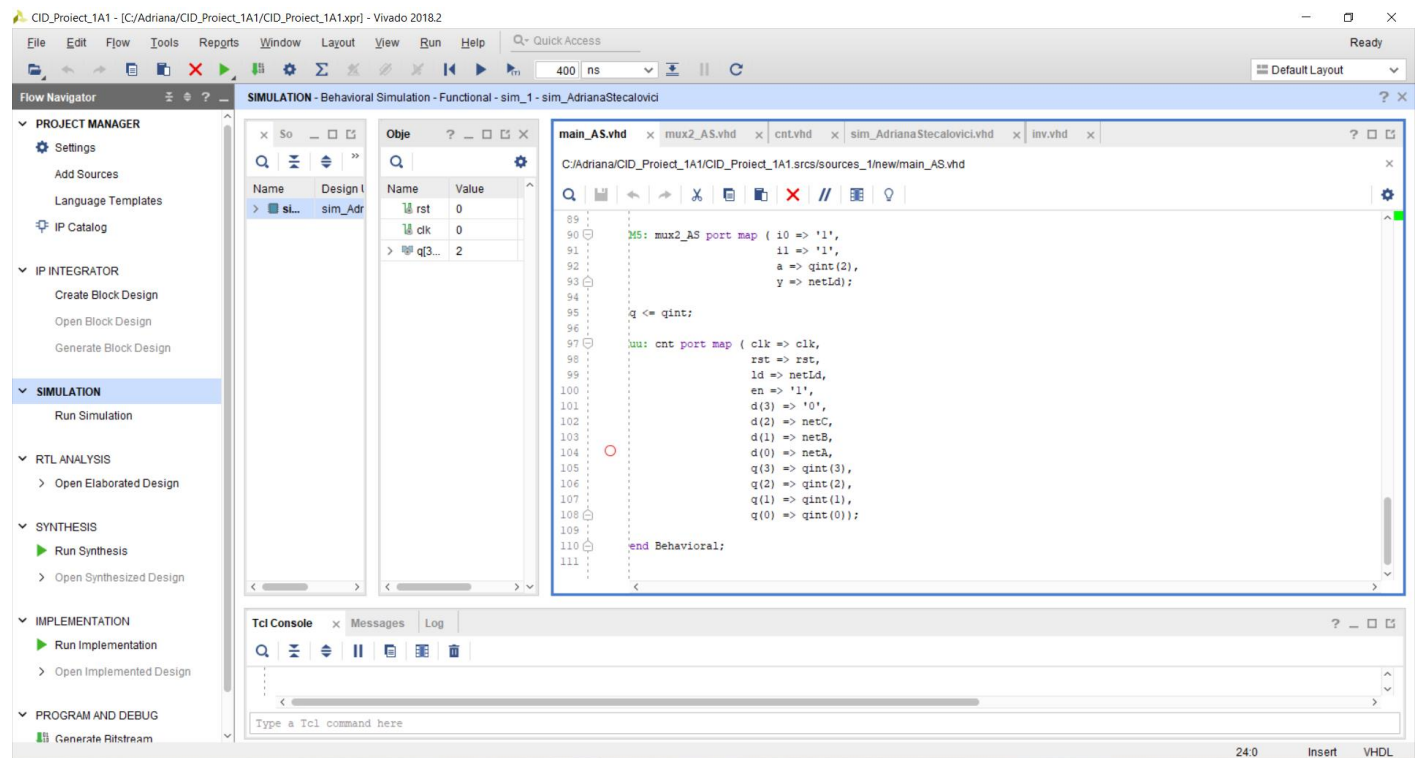
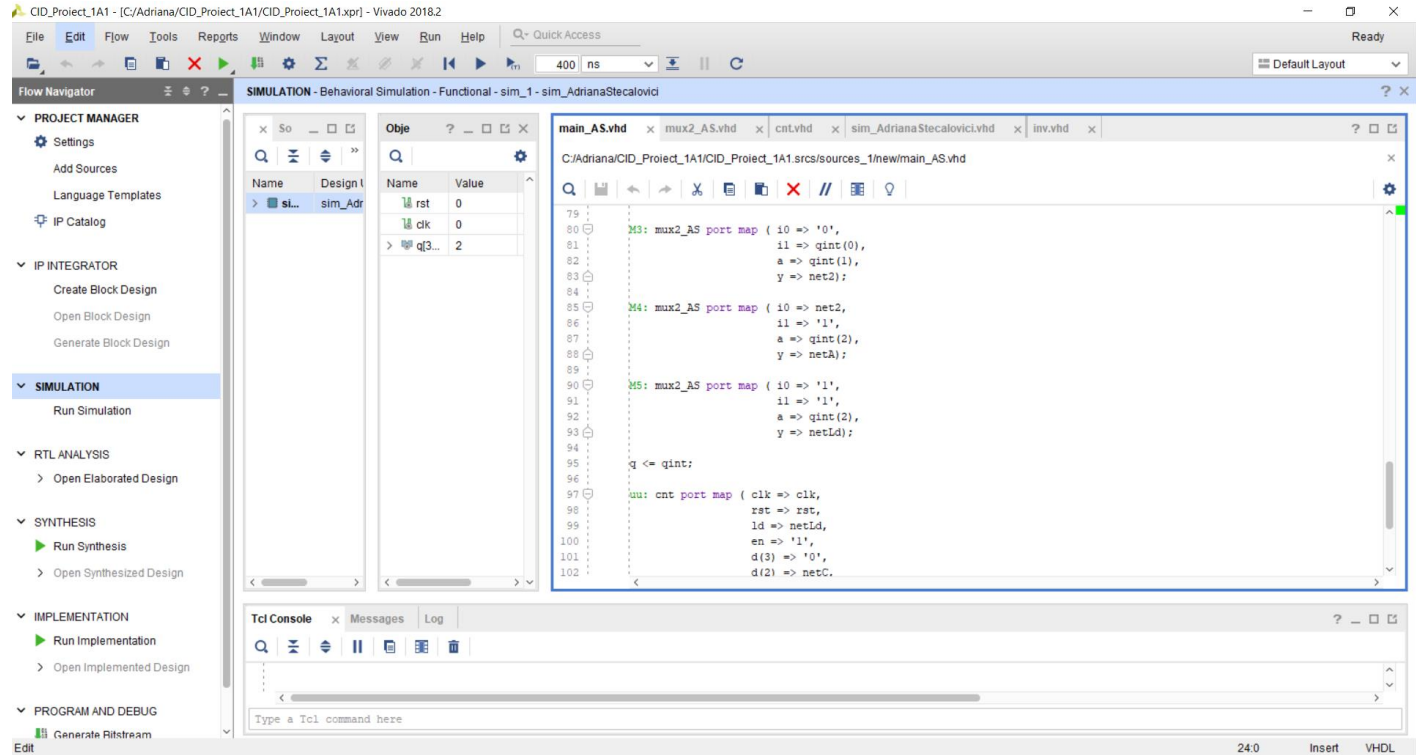




Adriana-Vasilica Stecalovici

Grupa: 2123, semigrupa 2

Seria A

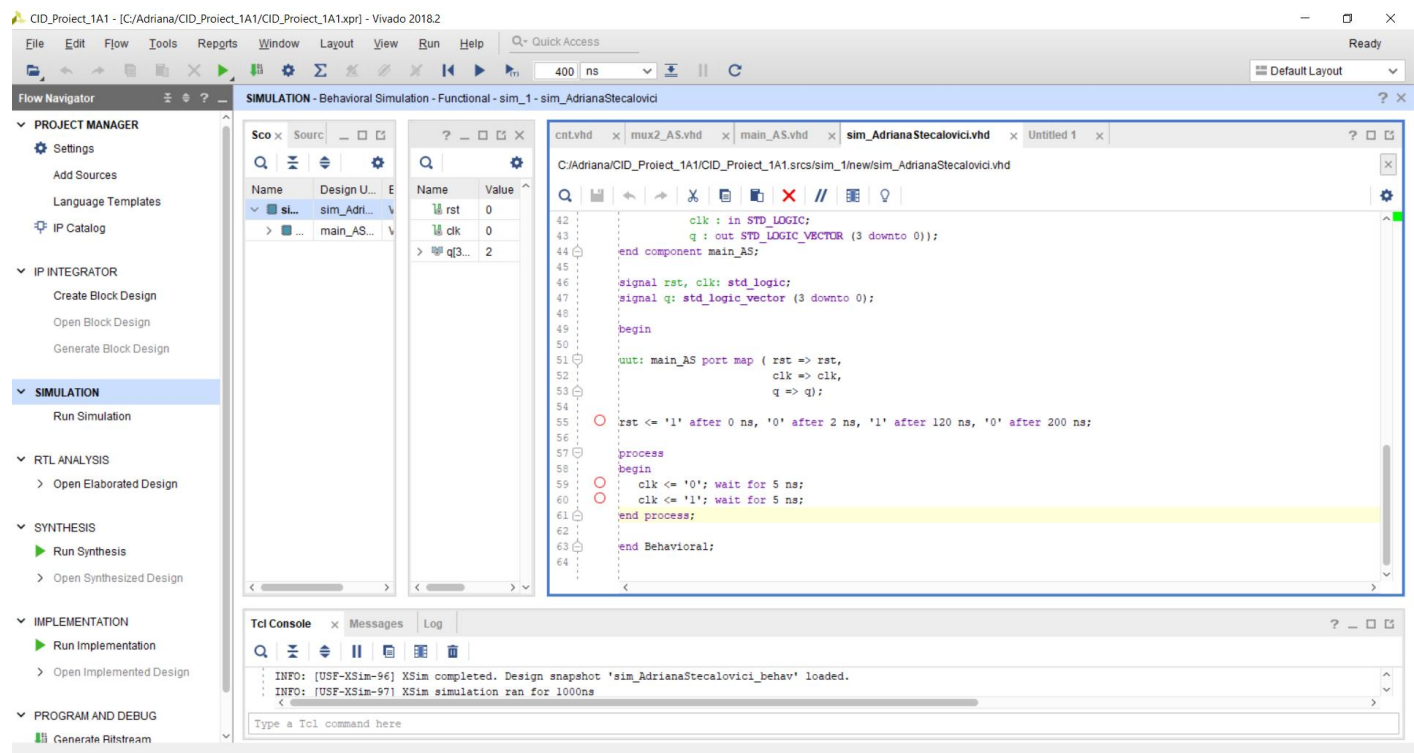
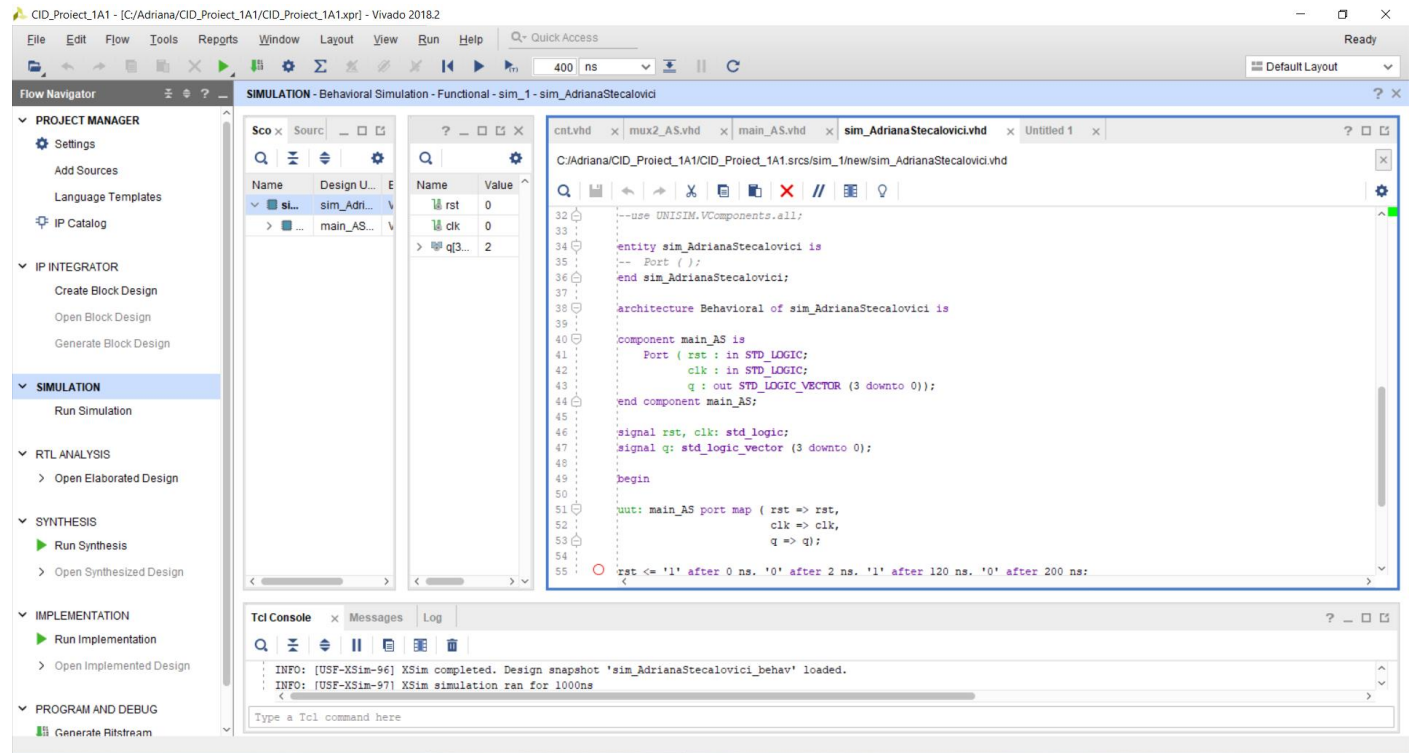


Adriana-Vasilica Stecalovici

Grupa: 2123, semigrupa 2

Seria A

## ➤ Sursa sim\_AdrianaStecalovici:



Adriana-Vasilica Stecalovici

Grupa: 2123, semigrupa 2

Seria A

## ➤ Schema electrică:

CID\_Proiect\_1A1 - [C:/Adriana/CID\_Proiect\_1A1/CID\_Proiect\_1A1.xpr] - Vivado 2018.2

File Edit Flow Tools Reports Window Layout View Help Quick Access

Flow Navigator ELABORATED DESIGN - xc7a35tcbg236-1 (active)

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design
  - Report Methodology
  - Report DRC
  - Report Noise
  - Schematic

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

Sources Netlist

- main\_AS
  - Nets (15)
  - Leaf Cells (2)
    - M0 (mux2\_AS)
    - M1 (mux2\_AS)
    - M2 (mux2\_AS)
    - M3 (mux2\_AS)
    - M4 (mux2\_AS)
    - M5 (mux2\_AS)
    - uinv (xil\_defaultlib\_uinv)
    - u0 (cnf)

Source File Properties

sim\_AdrianaStecalovici.vhd

Enabled

Location: C:/Adriana/CID\_Proiect\_1A1/CID\_Proiect\_1A1

Type: VHDL

General Properties

Project Summary Schematic

8 Cells 6 I/O Ports 15 Nets

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMS	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthes
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado In