Placement study for a simple overclocked DSP48E1 design on Artix-7 device

Packing input data registers into IOBs resulted in hold time violations of 2ns per bit when min input delay was 0.5ns.
After changing the min input delay to 3ns, timing was met.
Figure: in_fifo_a DFFs packed into IOBs with associated connectivity

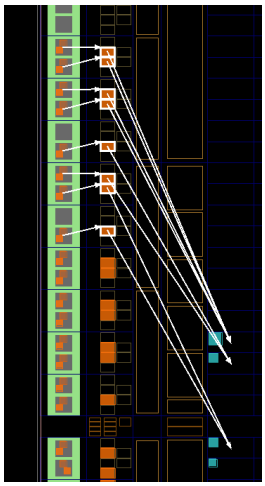
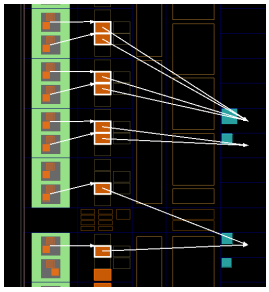
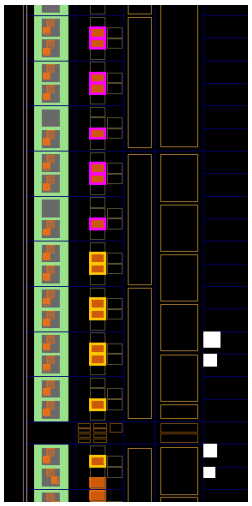


Figure: in_fifo_b DFFs packed into IOBs with associated connectivity



din_rr_mux is implemented rather tightly given there is minimal logic density.
The area where the logic is placed is composed solely logic related to the mux with top level data input words.
The LUTs and end of path FFs are placed into the same slice



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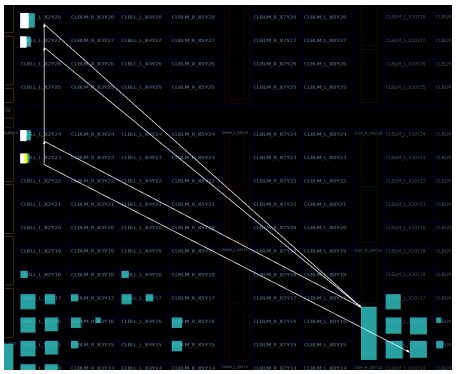
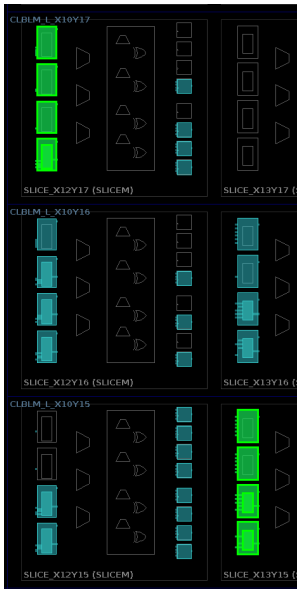
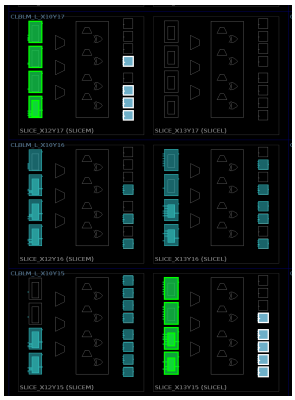
FFs from the registered selected data from din_rr_mux are routed to the fabric area with the inferred DSP48E1 (7 series device).
The din_rr_mux was placed much closer to the IOBs rather than the DSP
Perhaps this is just because the device view is not drawn to scale
We should check the net delays from the IOBs vs to the DSP and compare values.



LUTs of incr_inst. We can see some of the LUT6 BELs contain placed LUT5 BELs too.



FFs of incr_inst



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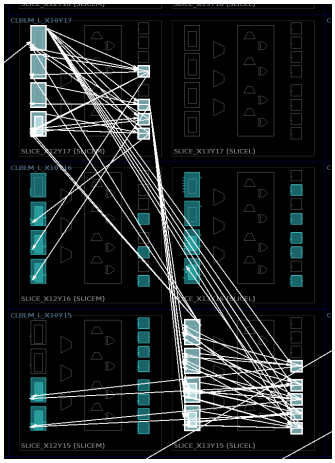
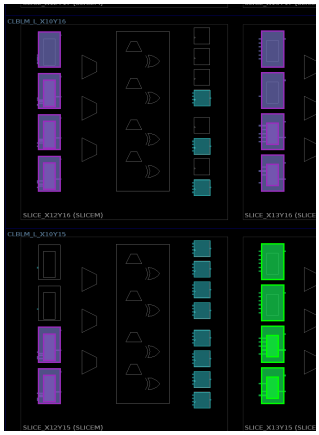
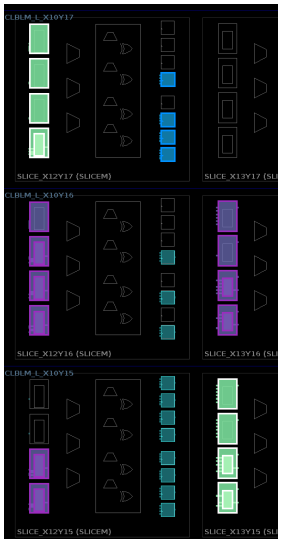
Cell connectivity of incr_inst



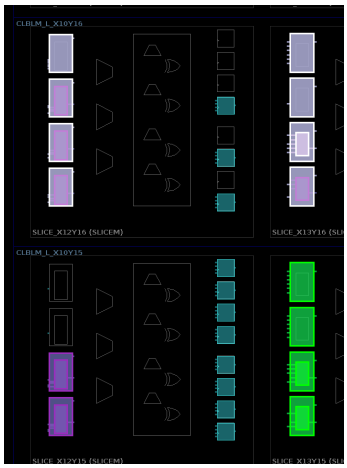
LUTs of decr_inst



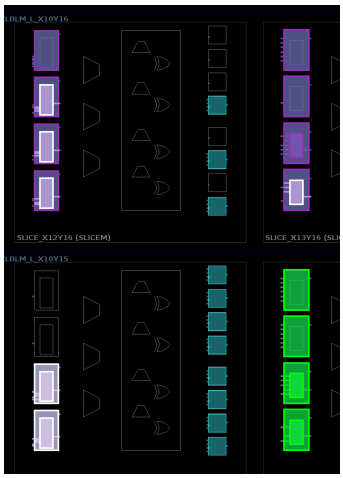
There are more LUTs for decr_inst compared to incr_inst. Why so?
Back to incr_inst, if I search for LUTs containing “dout” here is the result.
Every LUT in the incr_inst hierarchy is a dout LUT.



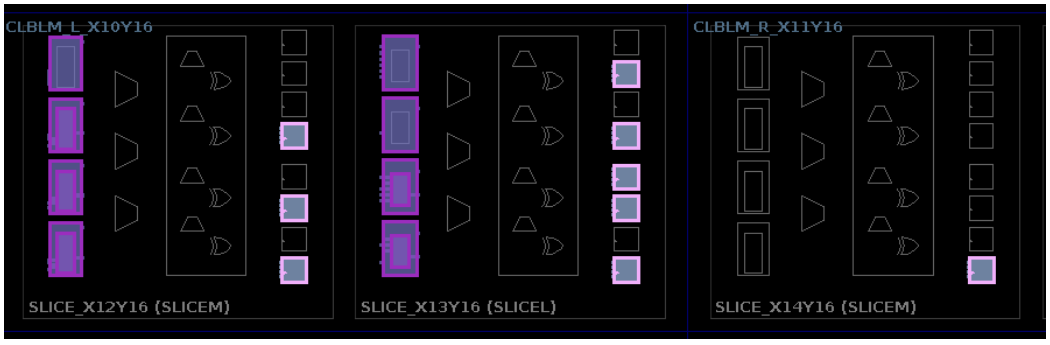
Back to decr_inst, here is the result of a similar “dout” LUT search
Not all decr_inst LUTs were found by the query! (decr_inst LUTs are highlighted magenta).



What are the other LUTs then? The other LUTs are for the selected data logic from the incr-decr mux logic.
There are 8 LUTs for the 8 bits of the selected data from the mux, 6 LUT5s and 2 LUT6s.



FFs in the decr_inst hierarchy.
There is a small interesting detail. In the incr_inst, the reset from the locked signal is connected to a LUT input, for the decr_inst the reset signal is connected to the D input of a FF.
This was inferred by the synthesis tools.



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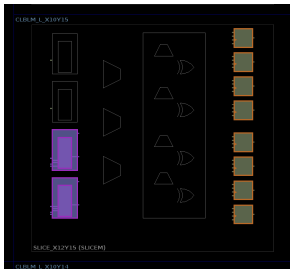
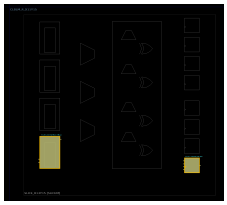
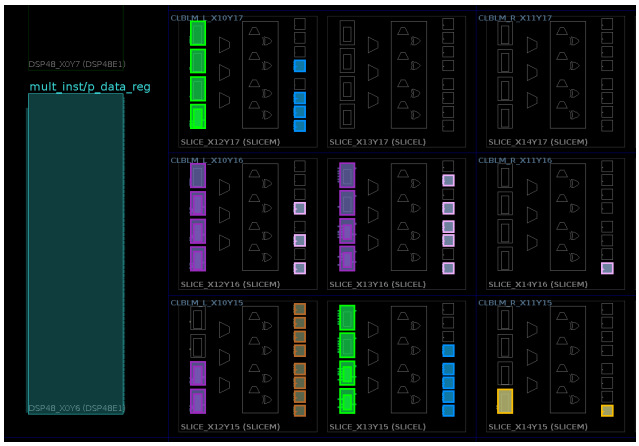
8 data bits from incr_decr_rr_mux inst.



The other cells of the incr_decr_rr_mux inst. Used for toggling sel input to the mux.



Summary of our physical annotations of the incr, decr, and incr-decr mux logic, which is placed near the DSP used under the multiplication operation.



The data from each mux is then pipelined into registers which are packed into the DSP48E1. So the DSP cell is connected directly from these mux FFs.
Here is the FFs connected from the output of the DSP48E1. Note these are for additional pipelining, as the Mreg and Preg are also already used, however you cannot see them as they are packed into the DSP site.

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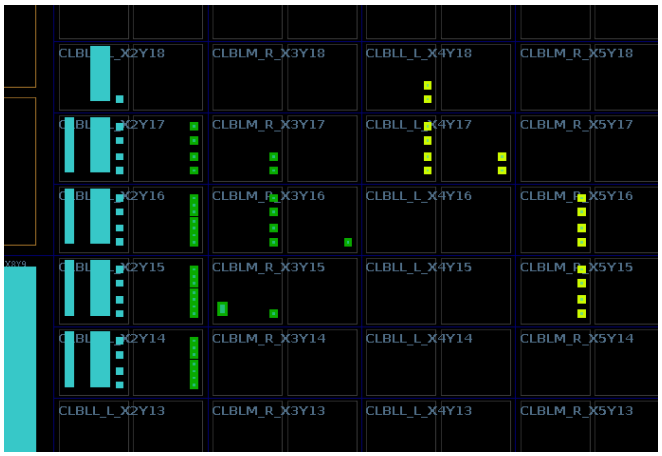
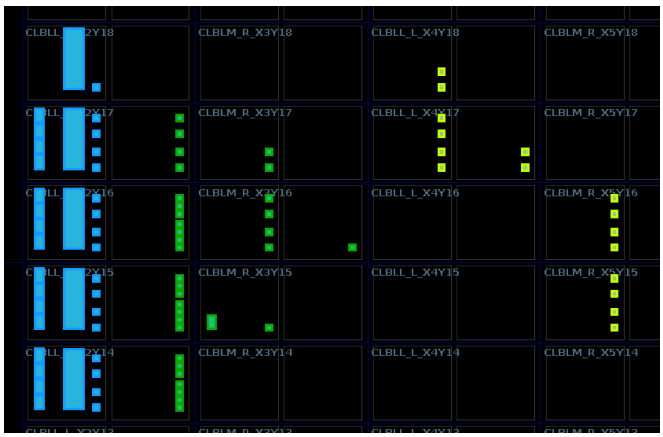
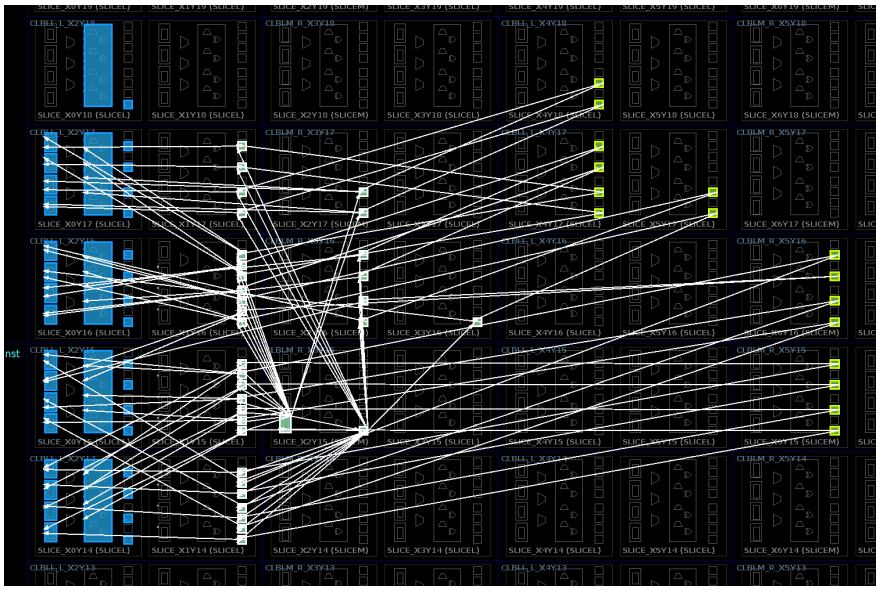
Next, placed in a homogeneous group of cells, is the funnel_inst logic.
funnel_inst cells in green (mult_inst FFs in yellow).



Post processing logic (pproc_inst) is in blue, in its own homogenous group of cells.



Connectivity between hierarchies



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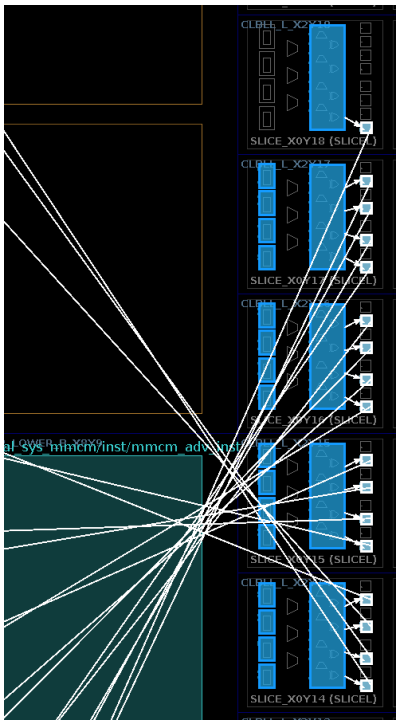
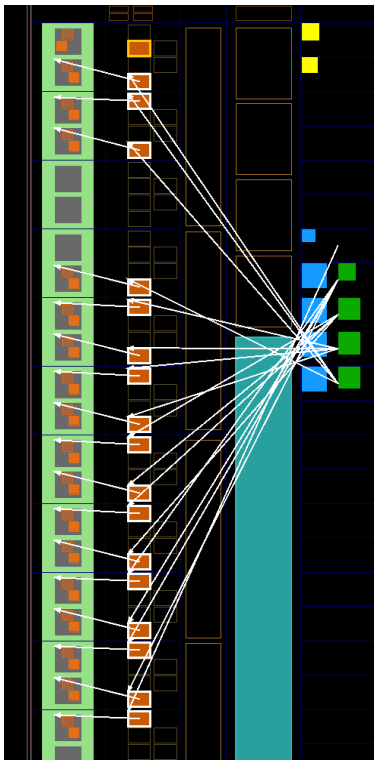
Connectivity of carry chain FFs in the post processing logic. The 17-bit resulting add uses 5 carry chains with registers in an adjacent column and in the same slices as the CARRY4 primitives.
The outputs of the FFs are connected directly to the OLOGIC IOBs of the top level data output.



The IOB FFs Q outputs are connected directly to their associated top level IO pads.



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The entire design fits in a single clock region (X0Y0) with minimal difficulty.