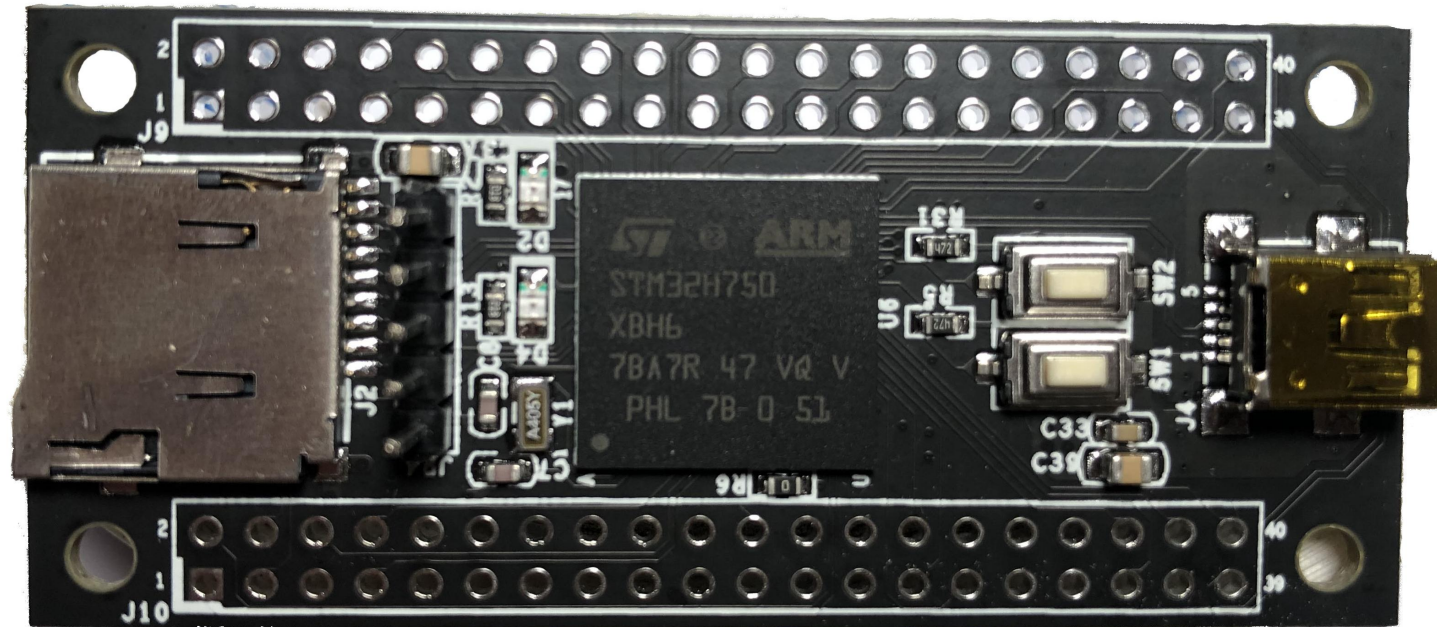
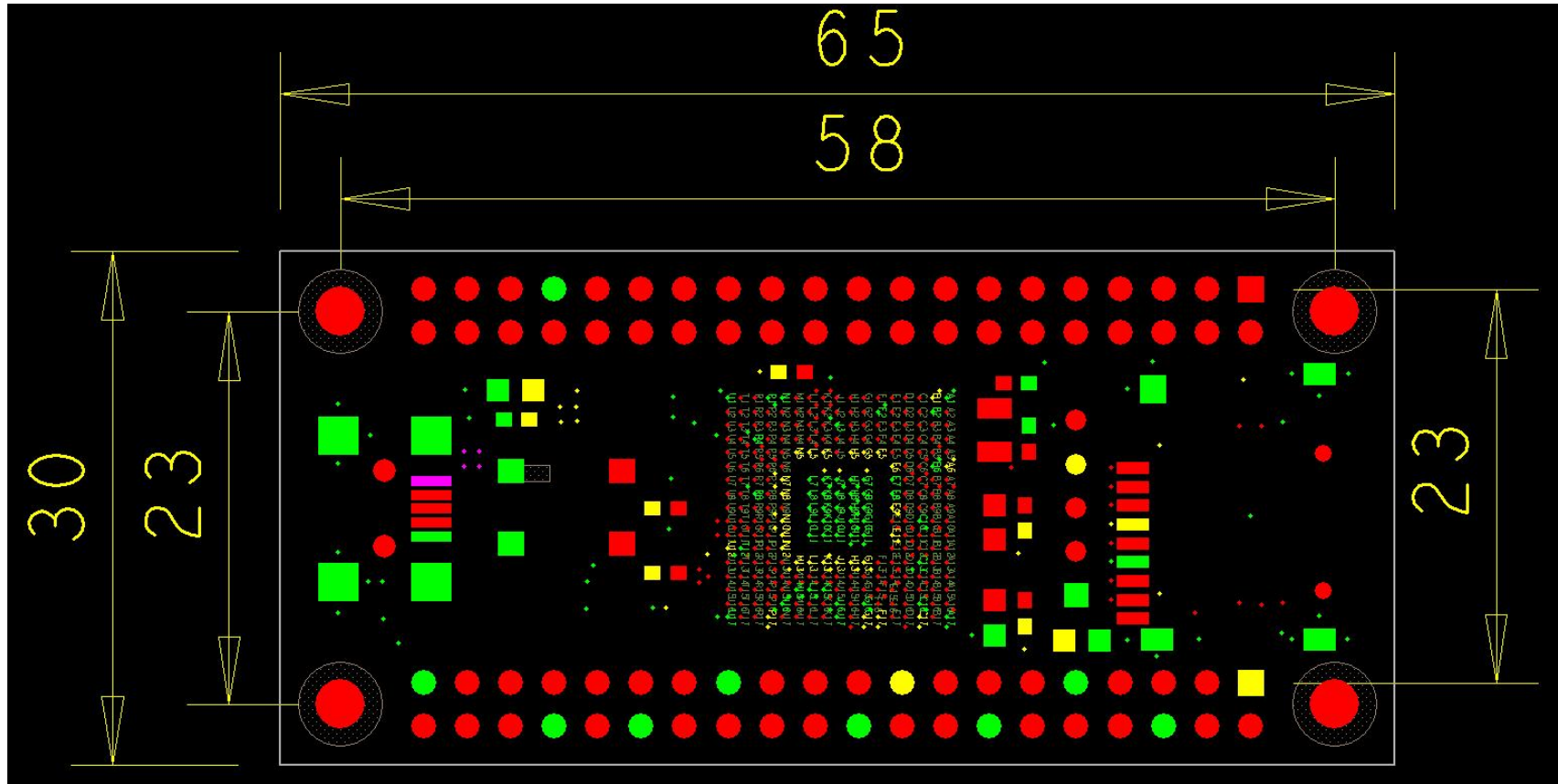


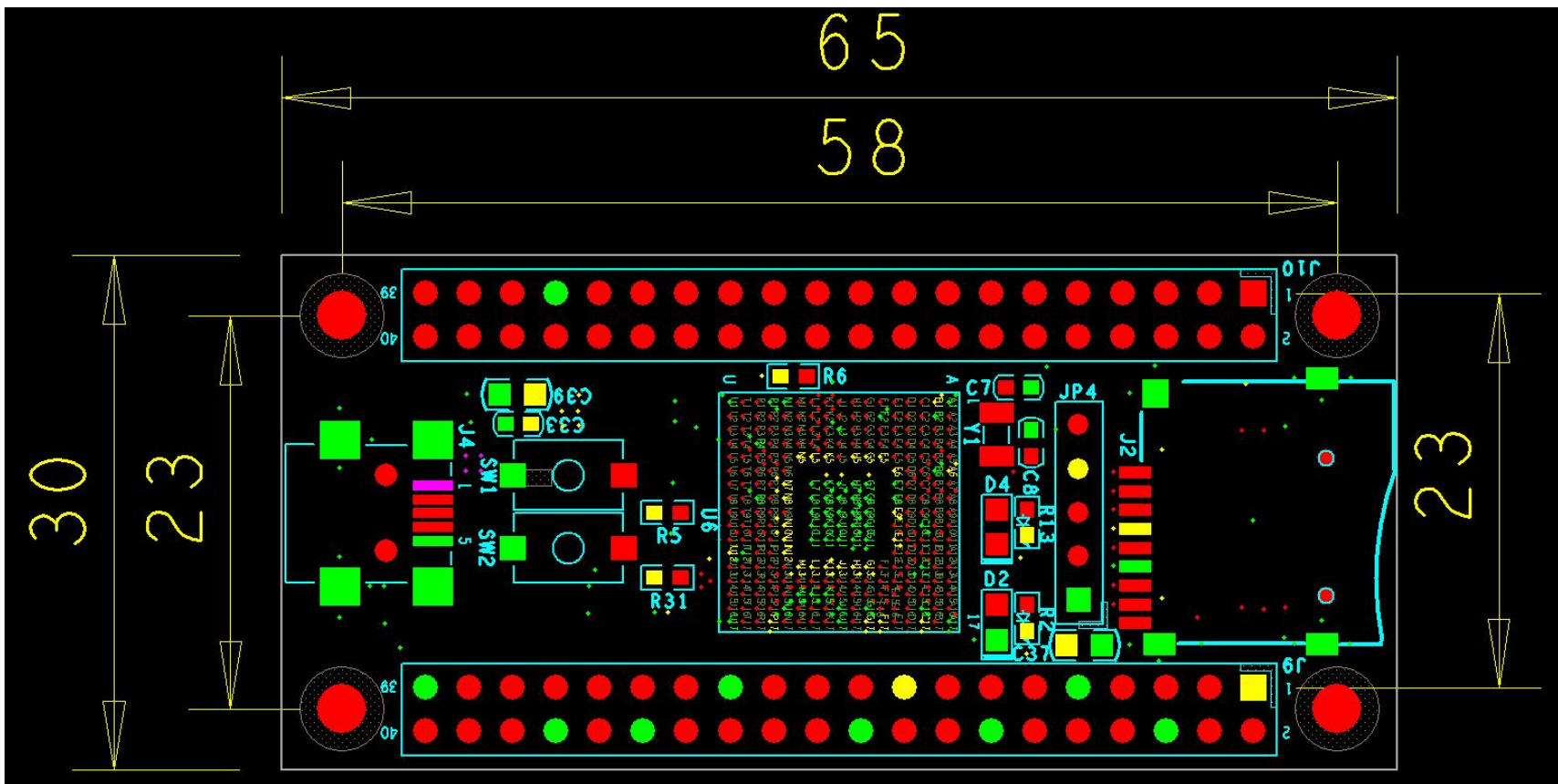
How to Drive QMTECH STM32H750XBH6 Core Board



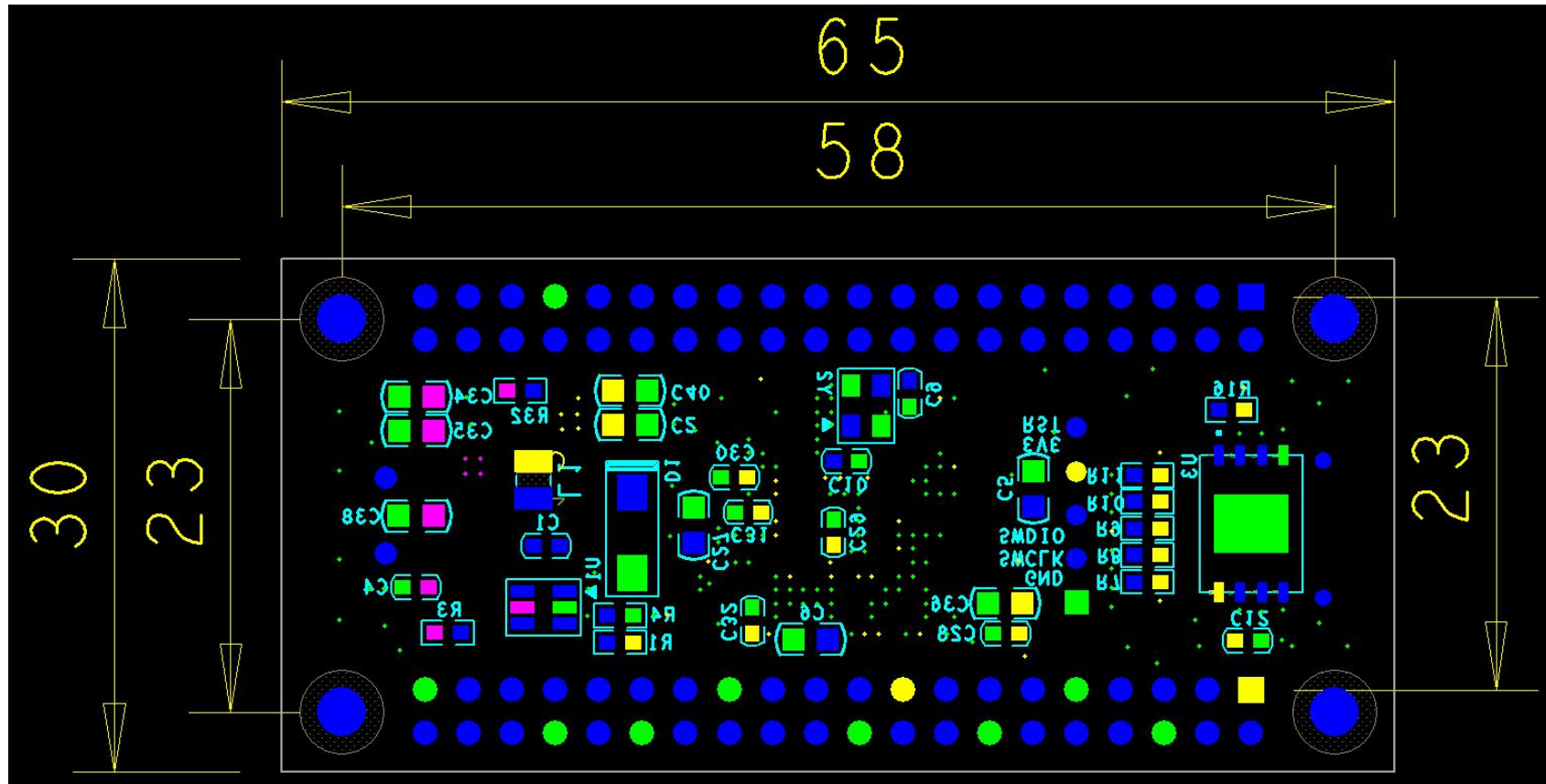
Dimension (mm)



Silk Screen Top



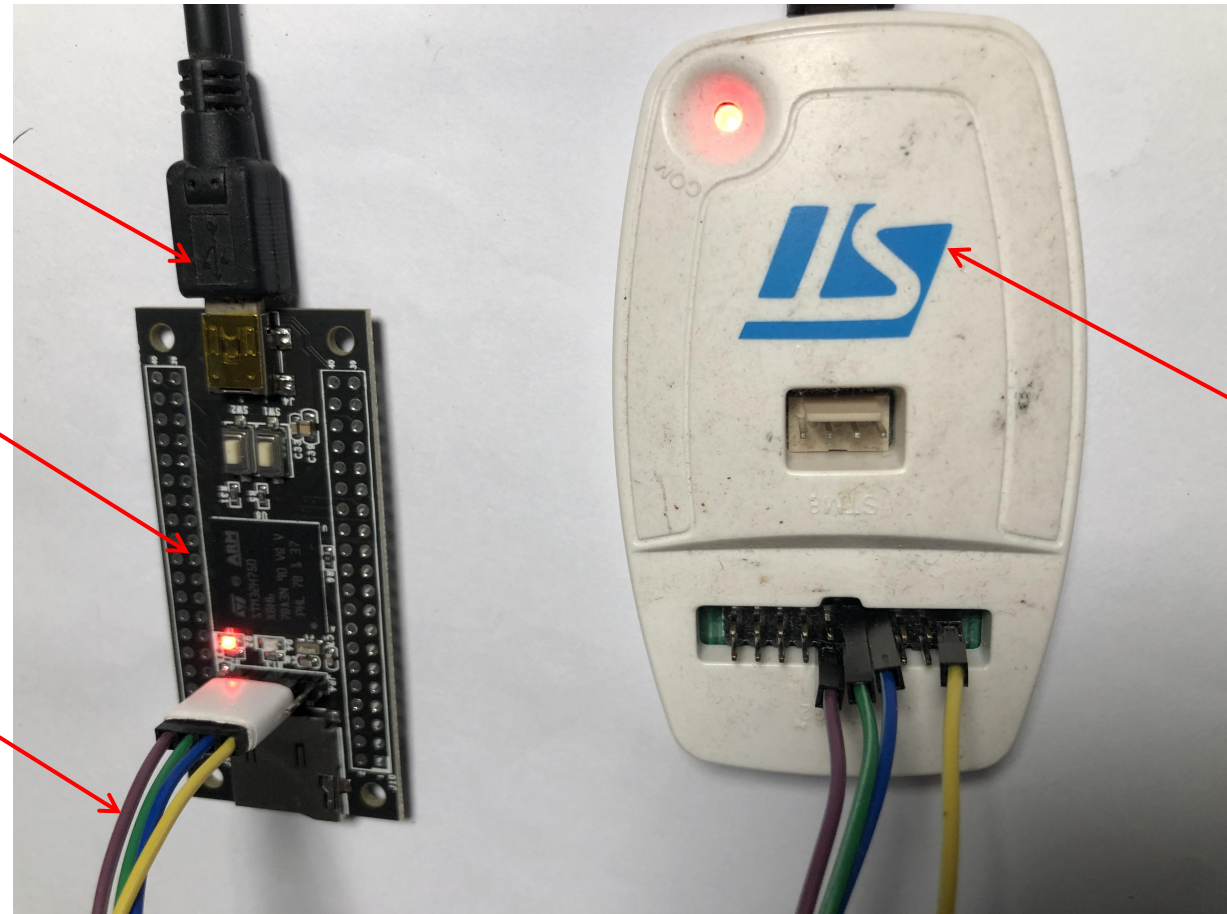
Silk Screen Bottom



Example ST-Link JTAG Cable

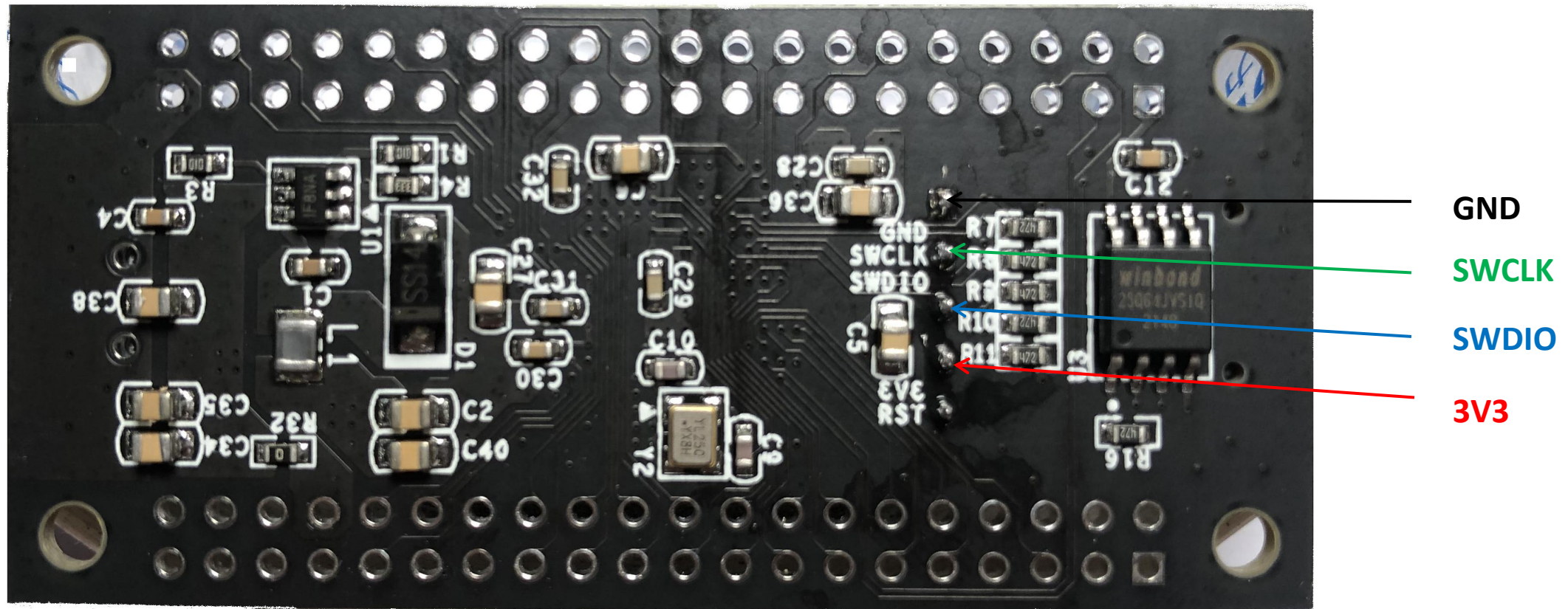
Mini USB Cable shall be connected to PC. Mini USB cable provides power supply and USB communication to the STM32H750XBH6 Core Board.

STM32H750XBH6 Core Board

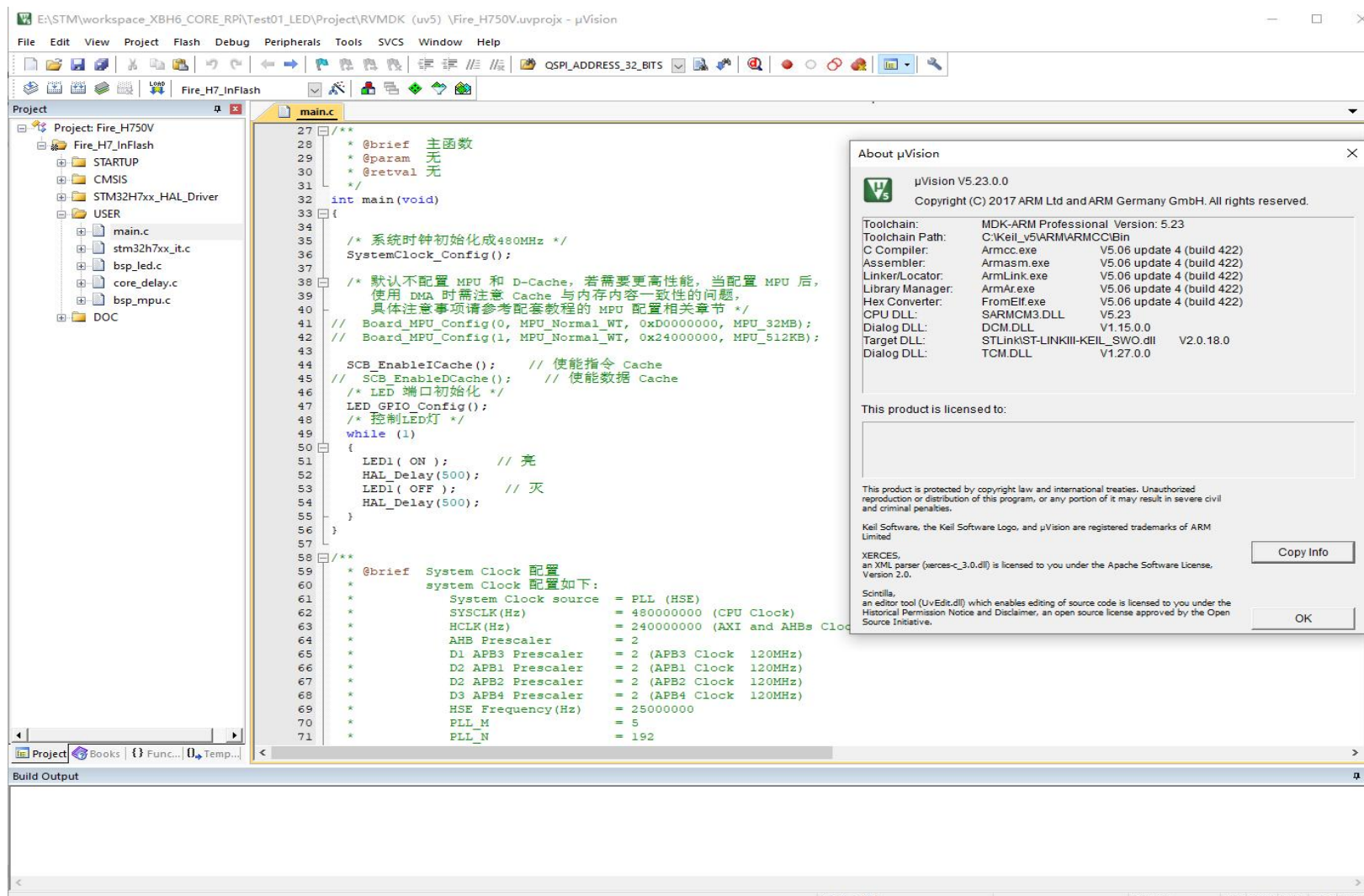


ST-Link

SWD PORT



Keil Version 5.23



Example Settings (1)

The screenshot shows the 'Options for Target' dialog box for the target 'Fire_H7_InFlash'. The 'Target' tab is selected, showing settings for the STM32H750XBHx device. The 'Xtal (MHz)' is set to 12.0. The 'Operating system' is set to 'None'. The 'System Viewer File' is 'STM32H750x.svd'. The 'Code Generation' section shows 'ARM Compiler' set to 'Use default compiler version', 'Use Cross-Module Optimization' is unchecked, 'Use MicroLIB' is checked, 'Big Endian' is unchecked, and 'Floating Point Hardware' is set to 'Double Precision'. The 'Read/Only Memory Areas' table shows 'IROM1' selected with start address 0x8000000 and size 0x20000. The 'Read/Write Memory Areas' table shows 'IRAM1' selected with start address 0x2000000 and size 0x20000, and 'IRAM2' with start address 0x2400000 and size 0x80000.

Options for Target 'Fire_H7_InFlash'

Device | Target | Output | Listing | User | C/C++ | Asm | Linker | Debug | Utilities

STMicroelectronics STM32H750XBHx

Xtal (MHz): 12.0

Operating system: None

System Viewer File: STM32H750x.svd

☐ Use Custom File

Code Generation

ARM Compiler: Use default compiler version

☐ Use Cross-Module Optimization

☒ Use MicroLIB ☐ Big Endian

Floating Point Hardware: Double Precision

Read/Only Memory Areas

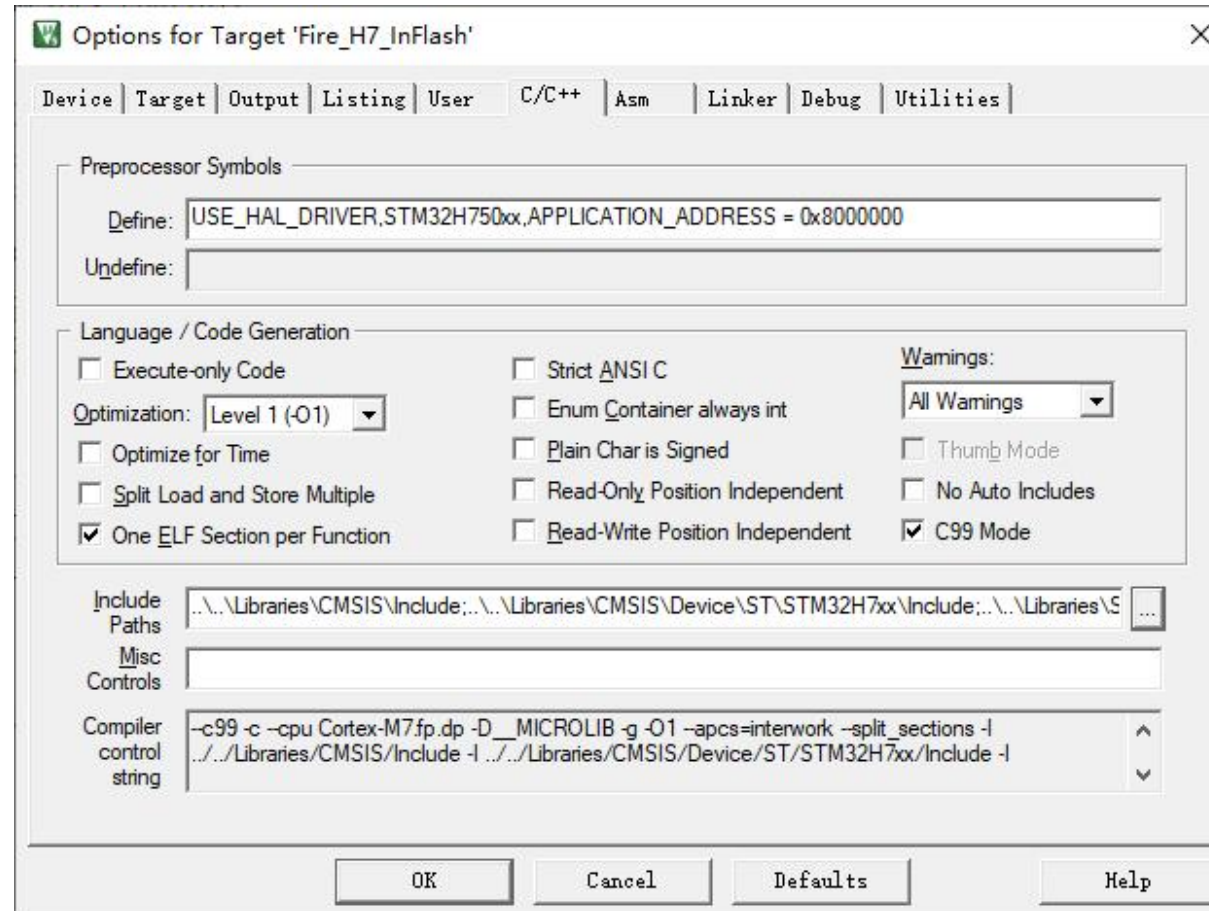
default	off-chip	Start	Size	Startup
<input type="checkbox"/>	ROM1:			<input type="radio"/>
<input type="checkbox"/>	ROM2:			<input type="radio"/>
<input type="checkbox"/>	ROM3:			<input type="radio"/>
	on-chip			
<input checked="" type="checkbox"/>	IROM1:	0x8000000	0x20000	<input checked="" type="radio"/>
<input type="checkbox"/>	IROM2:			<input type="radio"/>

Read/Write Memory Areas

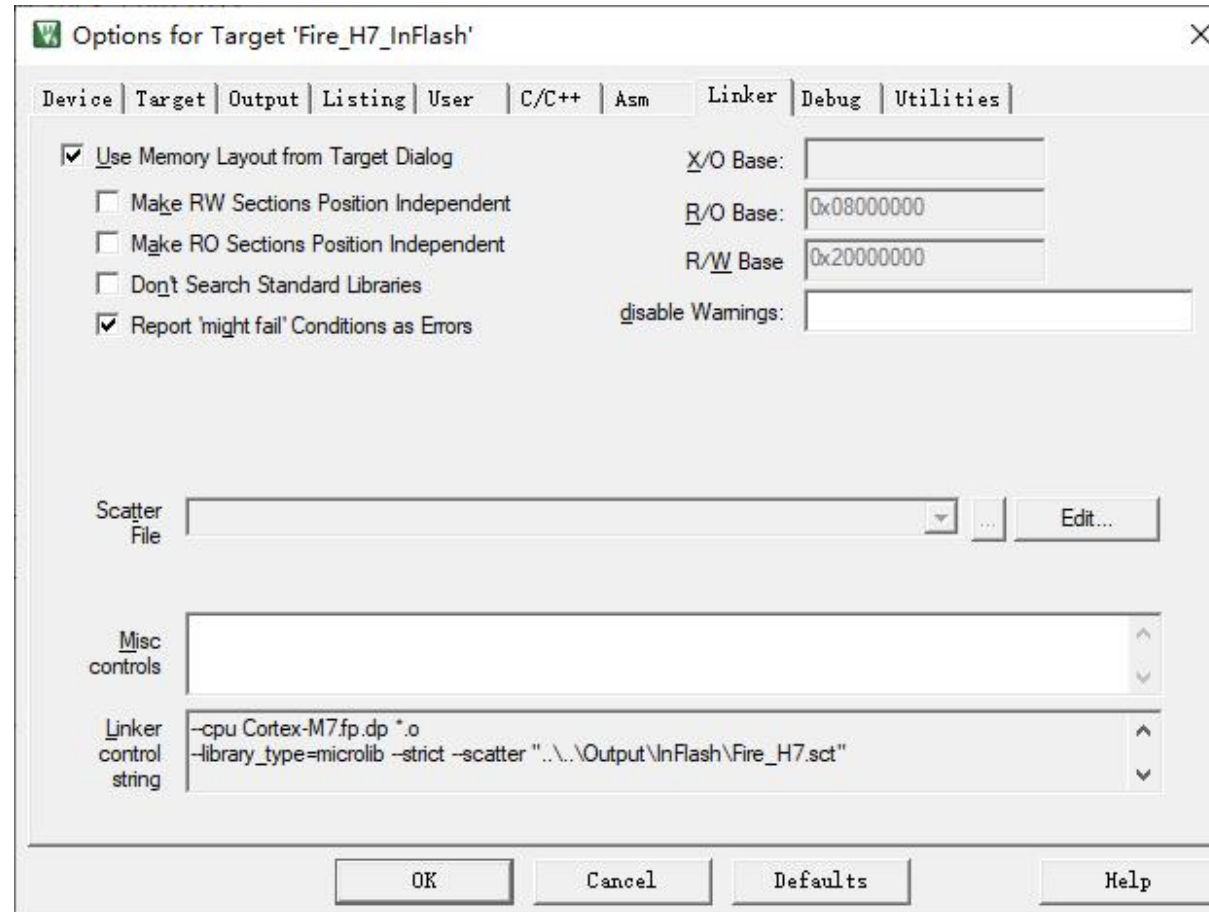
default	off-chip	Start	Size	NoInit
<input type="checkbox"/>	RAM1:			<input type="checkbox"/>
<input type="checkbox"/>	RAM2:			<input type="checkbox"/>
<input type="checkbox"/>	RAM3:			<input type="checkbox"/>
	on-chip			
<input checked="" type="checkbox"/>	IRAM1:	0x2000000	0x20000	<input type="checkbox"/>
<input type="checkbox"/>	IRAM2:	0x2400000	0x80000	<input type="checkbox"/>

OK Cancel Defaults Help

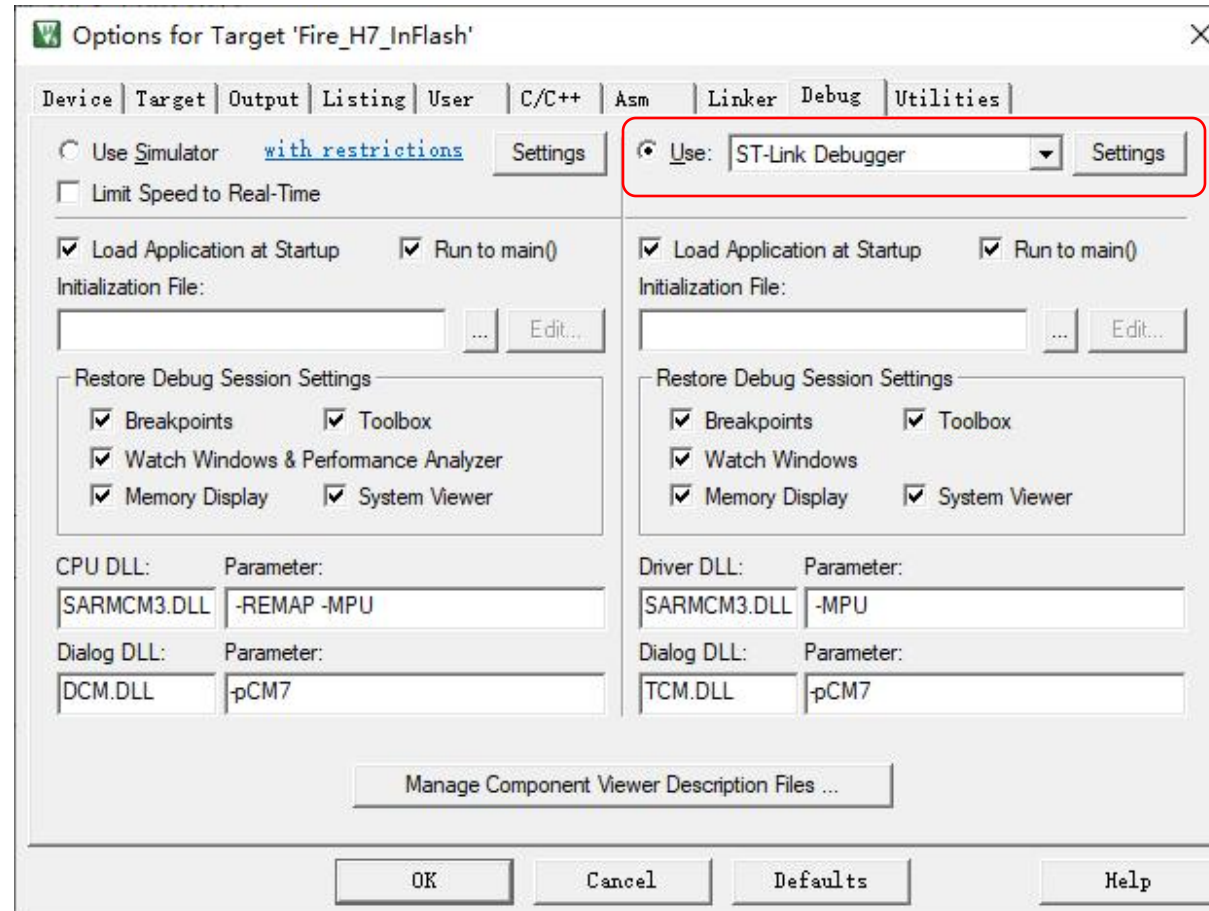
Example Settings (2)



Example Settings (3)



Example Settings (4)



Example Settings (5)

Cortex-M Target Driver Setup

Debug | Trace | Flash Download

Debug Adapter

Unit: ST-LINK/V2

Serial

HW Version: V2

FW Version: V2J24S4

Port: SW

Max: 1.8MHz

SW Device

IDCODE	Device Name	Move
SWDIO 0x6BA02477	ARM CoreSight SW-DP	Up Down

☒ Automatic Detection ID CODE:

☐ Manual Configuration Device Name:

Add Delete Update IR len:

Debug

Connect & Reset Options

Connect: Normal Reset: Autodetect

☒ Reset after Connect

Cache Options

☒ Cache Code

☒ Cache Memory

Download Options

☐ Verify Code Download

☐ Download to Flash


确定 取消 应用(A)

Example Settings (6)

Cortex-M Target Driver Setup

Debug | Trace | Flash Download

Download Function

 ☐ Erase Full Chip ☒ Program

☒ Erase Sectors ☒ Verify

☐ Do not Erase ☐ Reset and Run

RAM for Algorithm

Start: 0x20000000 Size: 0x1000

Programming Algorithm

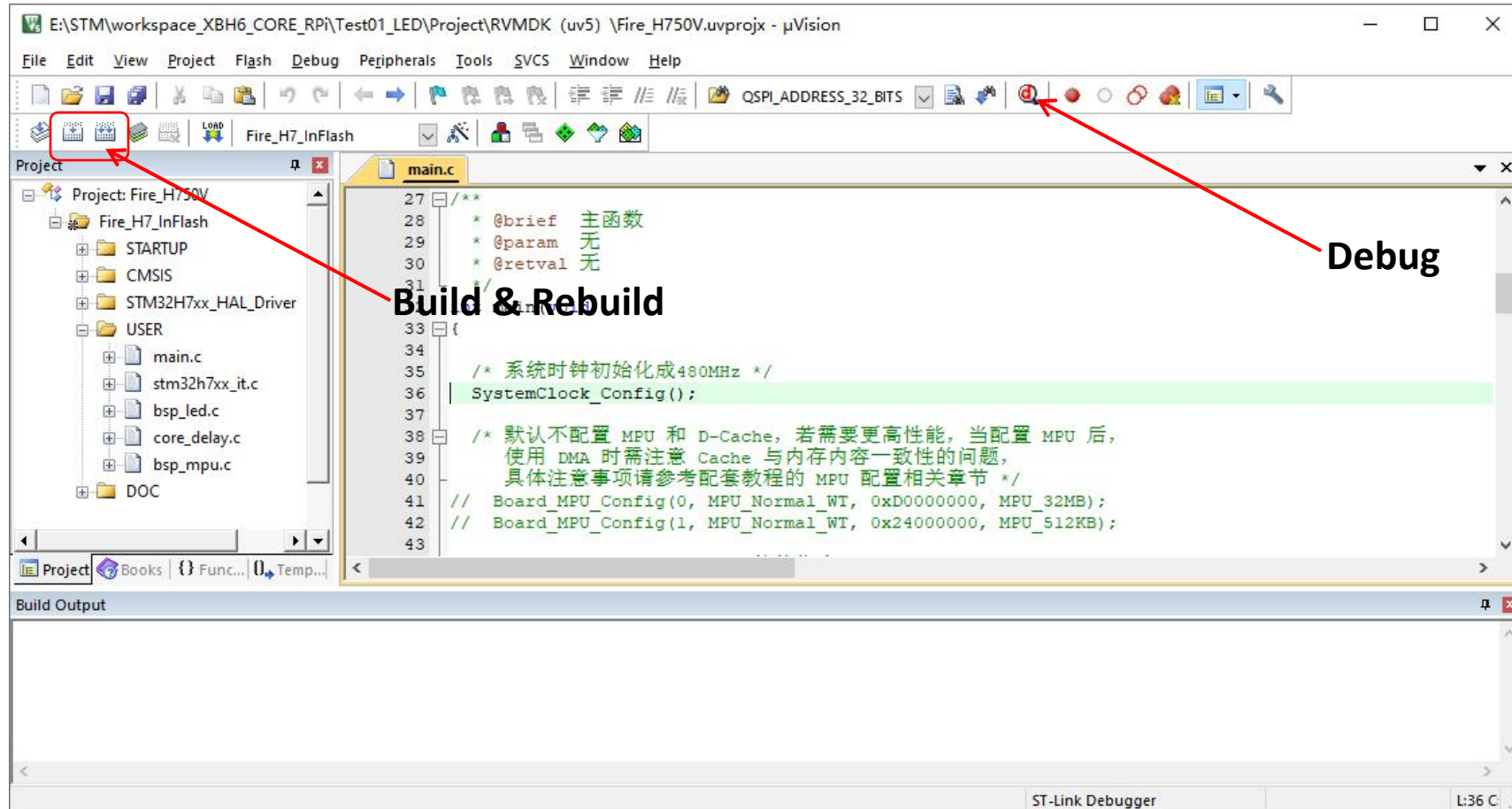
Description	Device Size	Device Type	Address Range
STM32H750xx	128k	On-chip Flash	08000000H - 0801FFFFH

Start: Size:

Add Remove

确定 取消 应用(A)

Main Icons



Any further question, kindly send mail to:
zyjnumber@hotmail.com