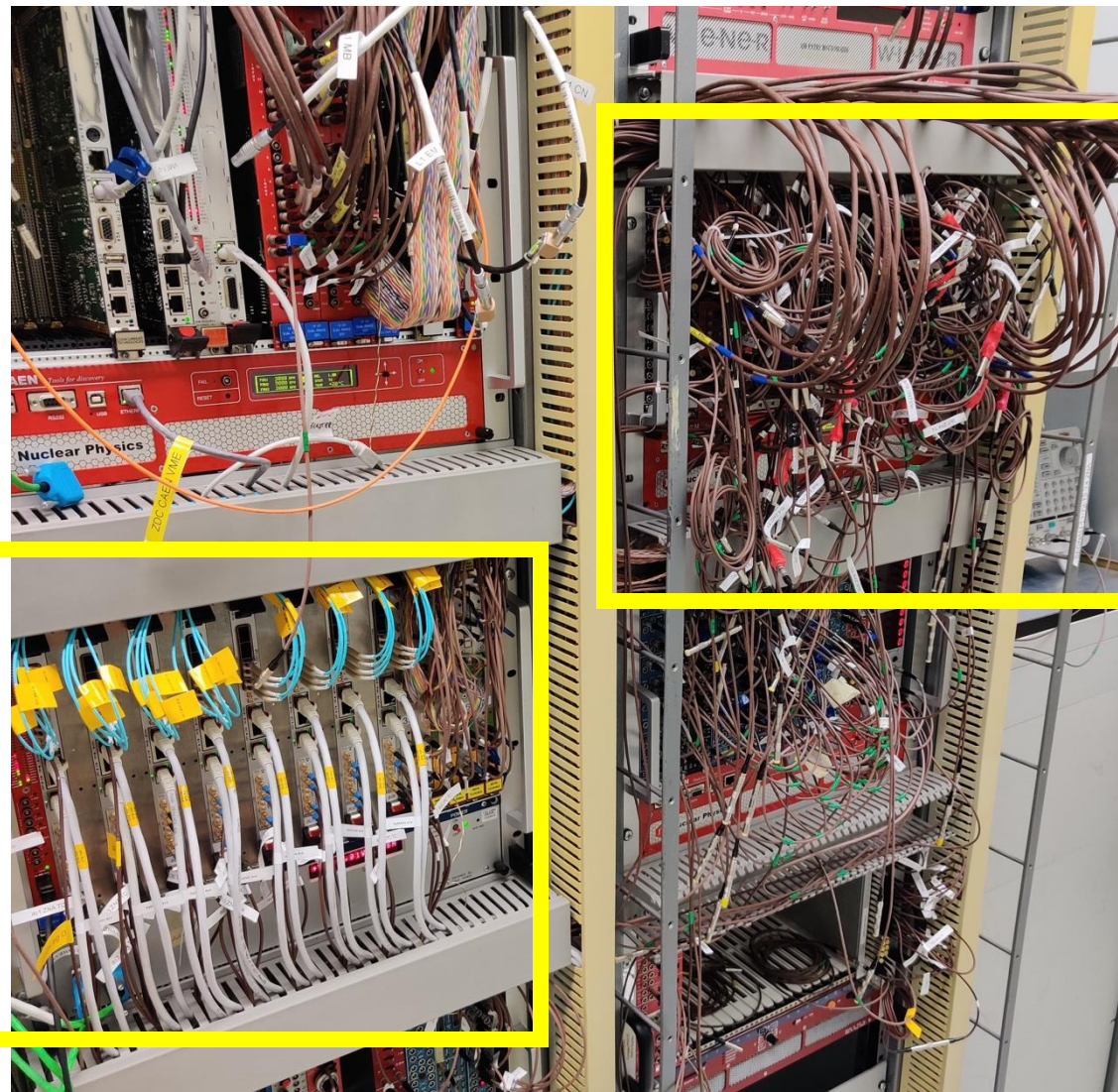


ZDC custom FIFO chain proposal

Stefan Cristi Zugravel
zugravel@to.infn.it

2025-02-26

Current setup at P2



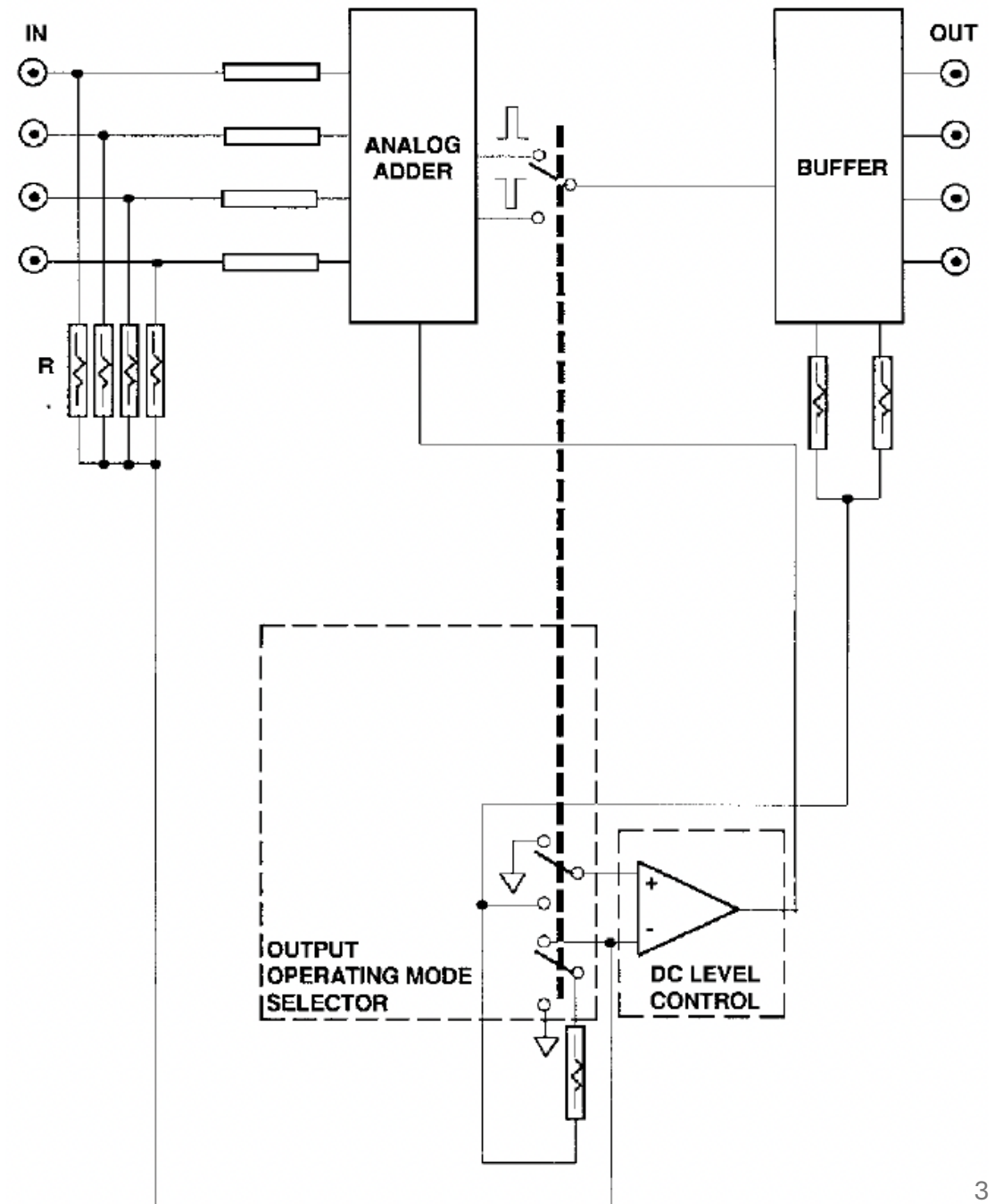
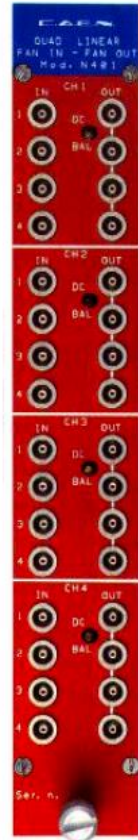
**FIFO
signal
chain**

**FPGA
Readout
system**

CAEN N401

N401

Quad Linear FAN IN - FAN OUT



PHILLIPS model 740

DATE: 6/18/89

MODEL 740 QUAD BIPOLAR LINEAR FAN-IN/FAN-OUT
(Front Panel Description)

Standard #1 NIM Packaging
in accordance with
TID-20893

Four Linear Inputs; Accepts
Up to ± 2.5 Volt Signal Levels;
50 Ohm Impedance; Direct
Coupled.

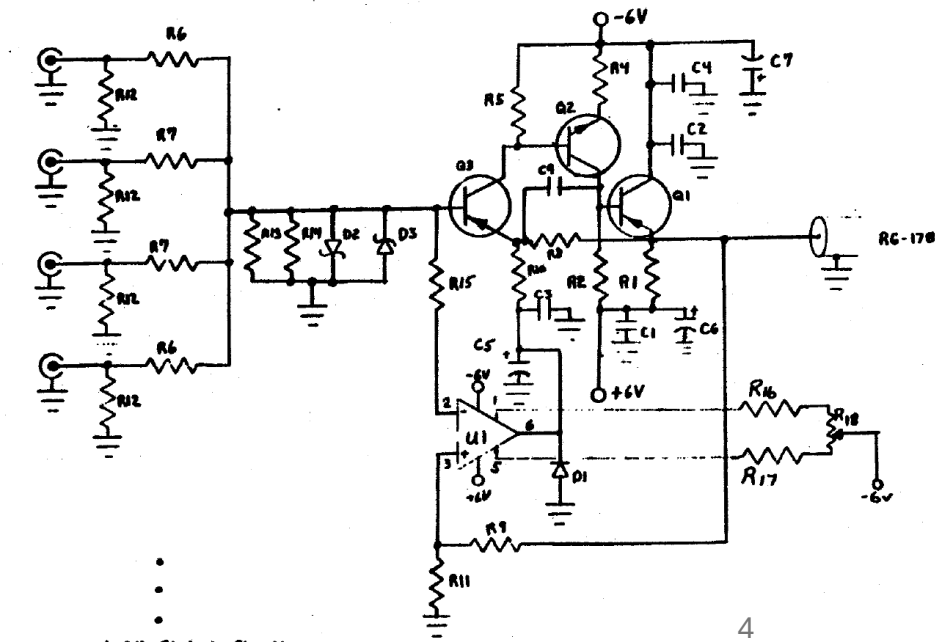
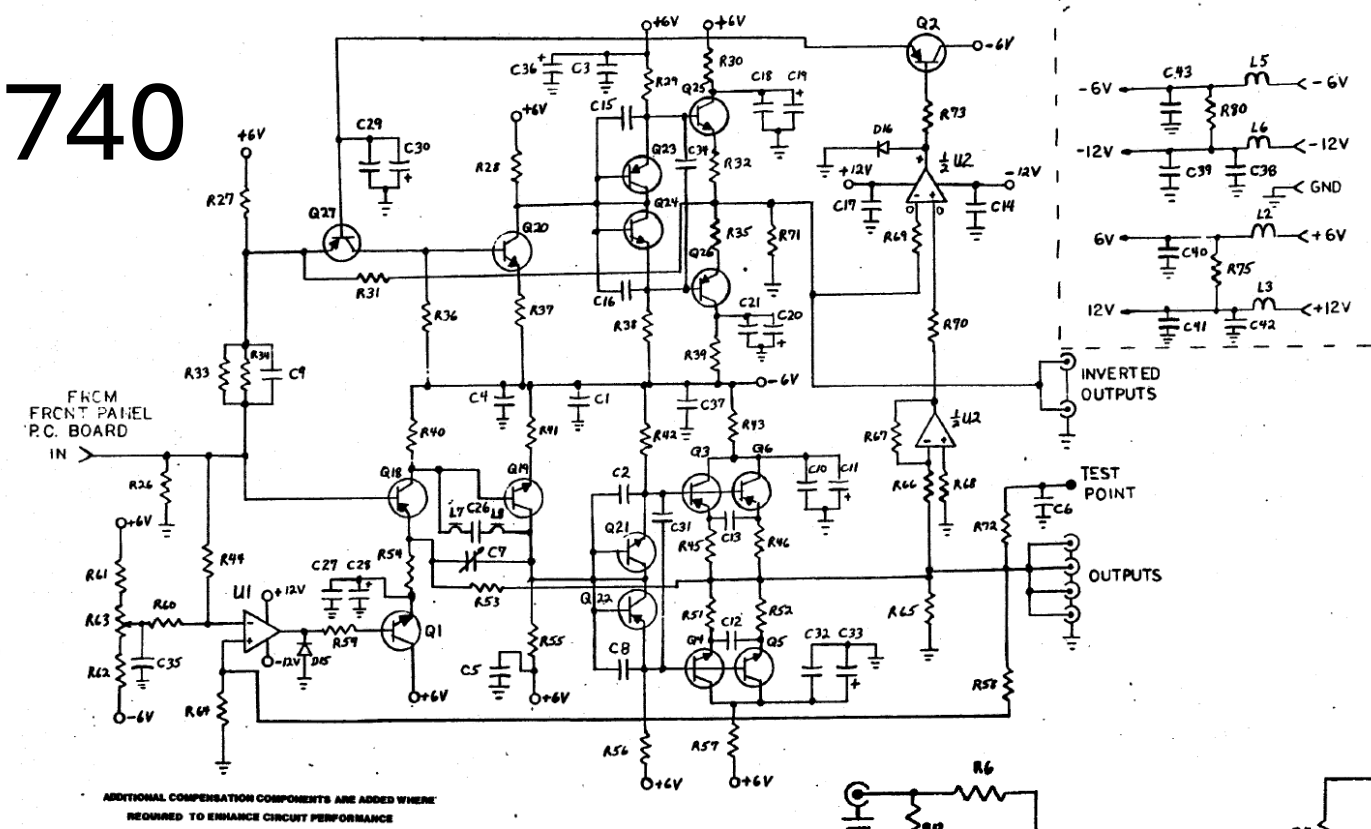
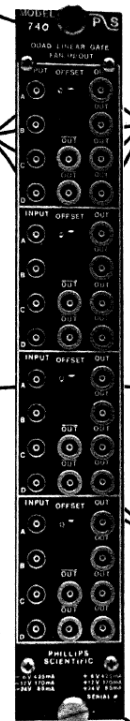
Test Point Provides Easy
Monitoring of Output DC Offset.

Four Linear Outputs; Each Capable
of Delivering ± 2.5 Volts Across
50 Ohm Load; Non-Inverting.

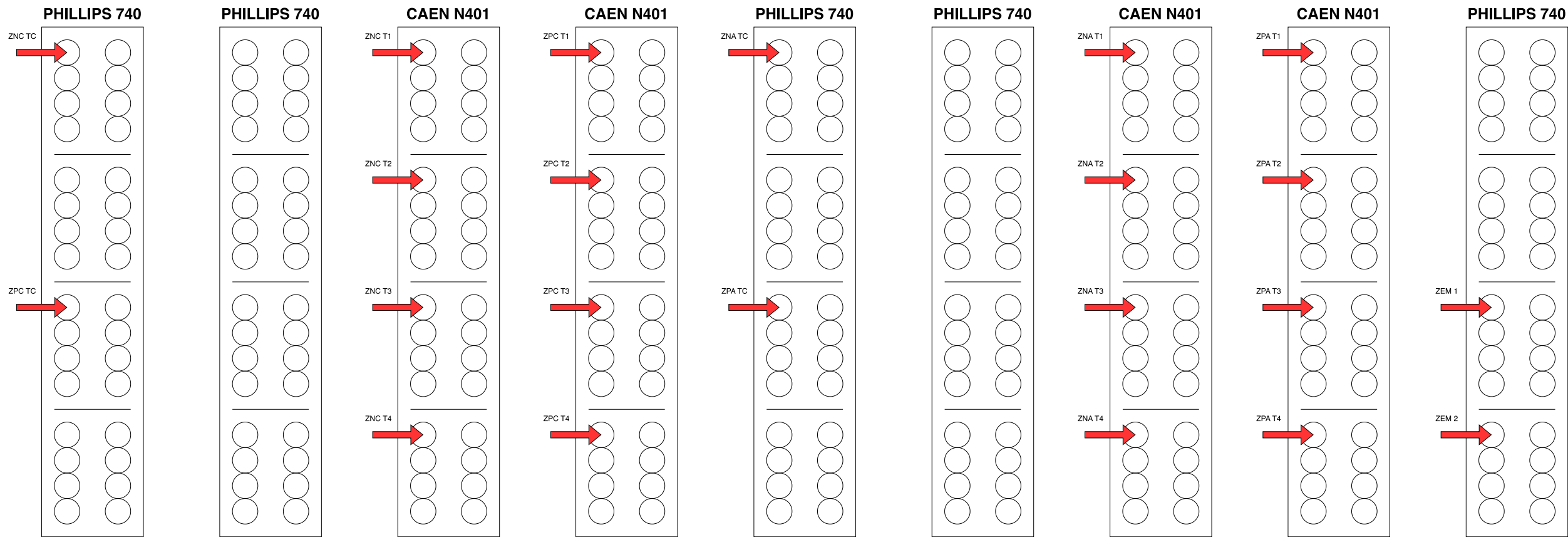
Output DC Offset Control; 15-turn
Screwdriver Adjustment, Variable
Over $\pm .5$ Volt Range.

Two Inverted Linear Outputs;
Each Capable of Delivering ± 2.5
Volts Across 50 Ohm Load.

Voltage and Current
Requirements

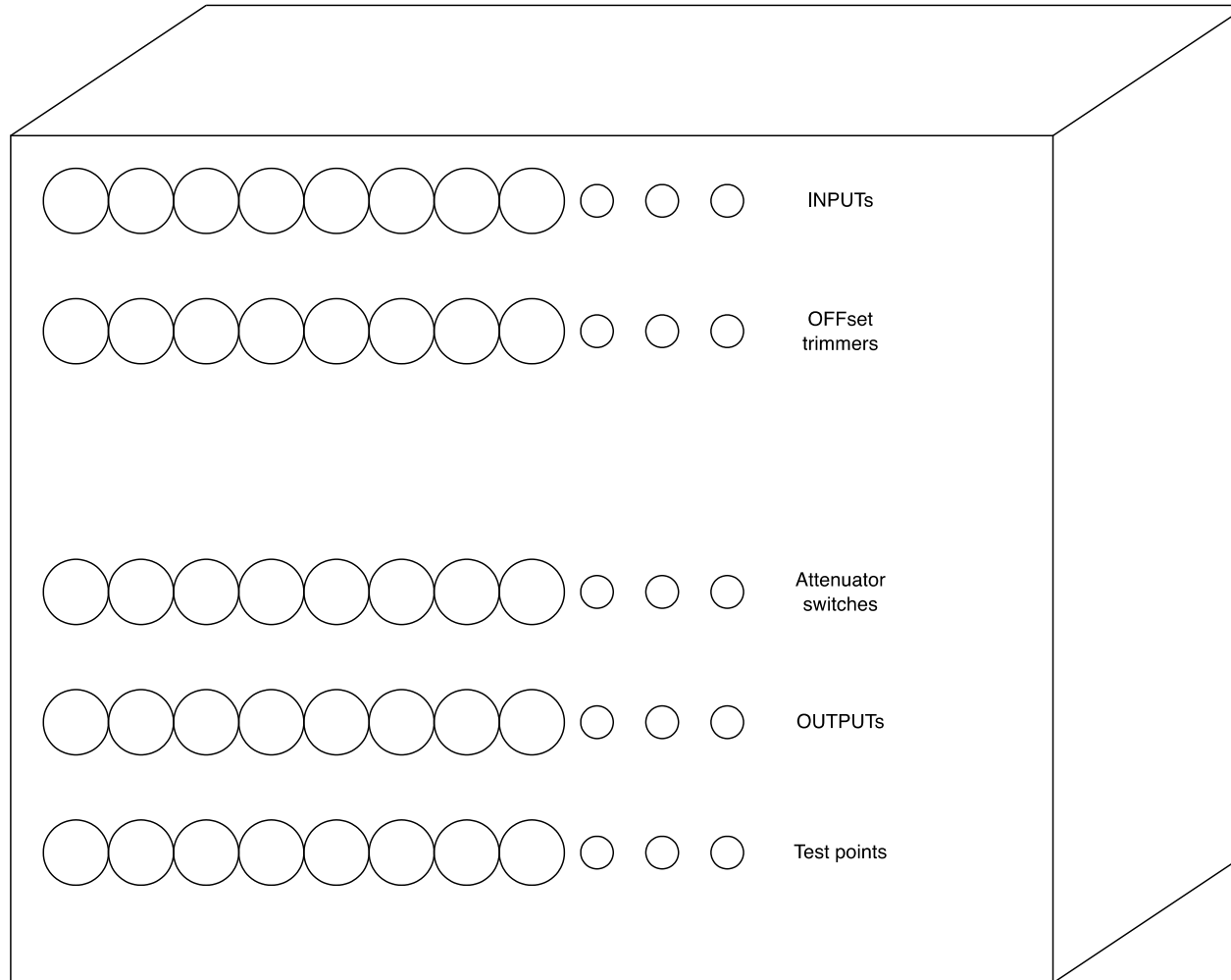


Current setup diagram



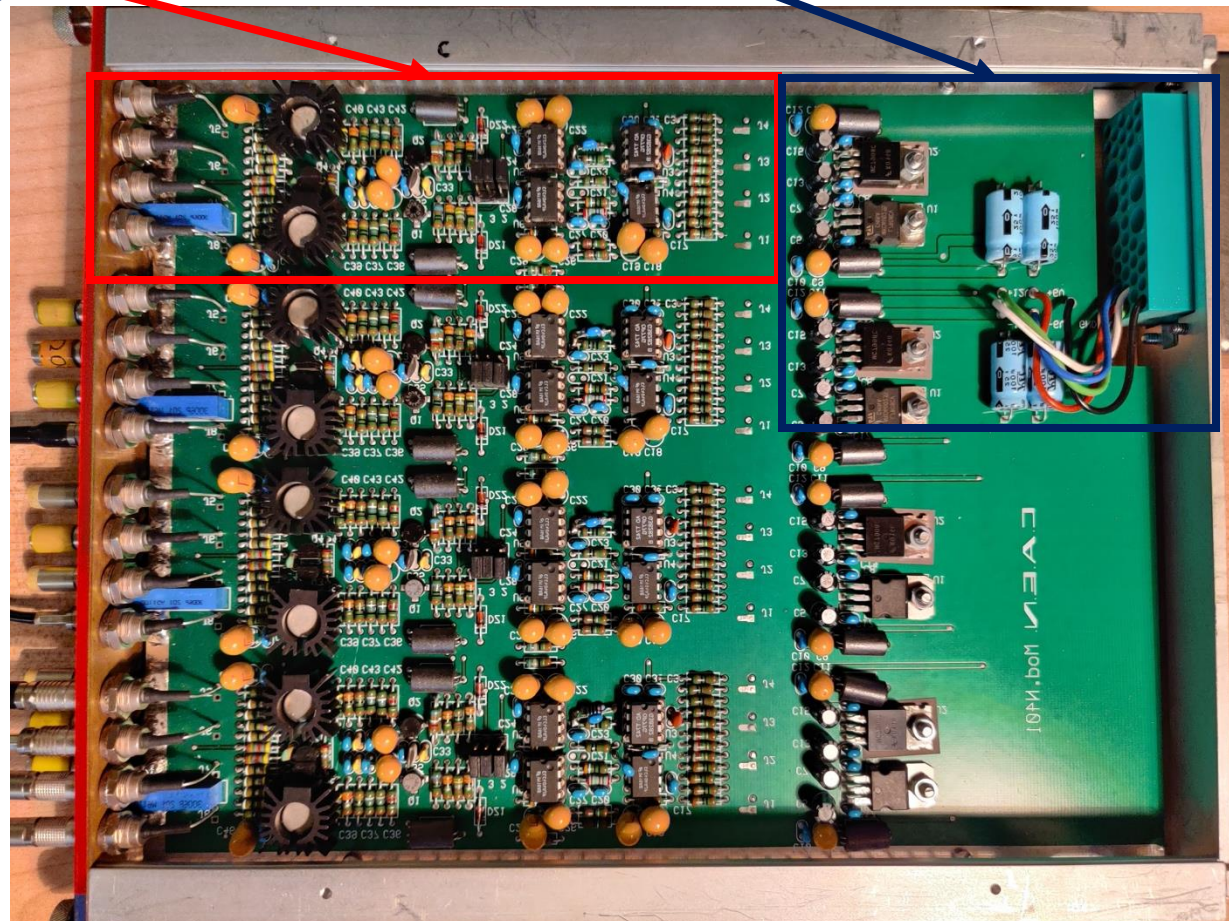
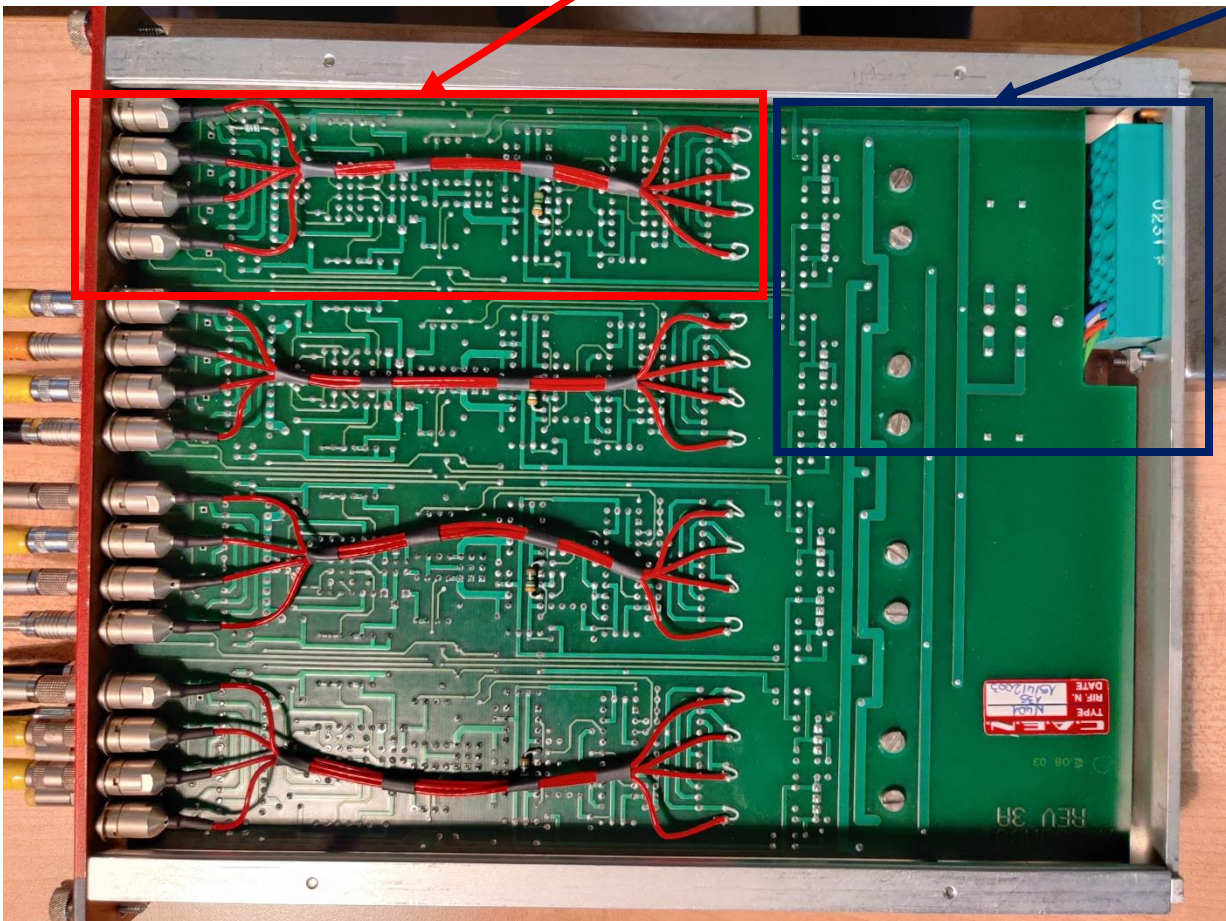
TO BE COMPLETED

Proposal for custom FIFO module

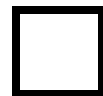


Signal

Power



Components used



T3006P



CLC404



OP77G



MC7908C



L7808CV



2N5583 0216

