MoveIt_v2 design document

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Abstract

This paper describes the MoveIt_v2 prototype that will be submitted on October 26^{th} 2020. The prototype contains 24 readout channels divided into two flavours, namely type A and type B.

1 Introduction

The MoVeIt experiment aims at the design of a system to measure the particle flux via single particle counting and to measure the beam energy via time of flight. The timeline of the project is 2017-2020. This document focuses on the first aspect. The typical particle rate for a therapeutical beam is :

- $10^6 \div 10^8$ particles/cm$^2 \cdot$ s for carbon ions
- $10^8 \div 10^{10}$ particles/cm$^2 \cdot$ s for protons

the beam size is gaussian shaped, with a spot of $\sim 0.5 \div 1$ cm^2 FWHM. The area to be covered by the detector is 3×3 cm^2 or 4×4 cm^2. The counting rate can go up to 1 GHz per channel, however the real limit will be much lower due to pile-up. Unfortunately it is not possible to disentangle a pile-up event by measuring the signal amplitude because of the Landau fluctuation. However there is interest for such a technique in radiobiology applications where the rates are much lower. At clinic level it could be an interest application for low beams, where the ionization detectors are not sufficiently sensitive.

2 Detector

The proposed sensor is a silicon strip detector with internal gain delveloped in the framework of the UFSD collaboration. The strips will be 1-1.5 cm long with a 200 μm pitch. With a sensor thickness of 50 μm the average charge is $\sim$0.7 fC. The detector provides a gain of 10$\div$15, thus giving a most probable MIP signal around 7.5-8 fC. The shape of the signal is approximately trapezoidal (because of the charges generated by the multiplication) with rise and fall times of 450 ps and a flat region of 300 ps. The current on the flat region is then $\sim$10 μA. A more precise picture of the detector signal is depicted in figure 1.

3 Prototype description

The prototype is a 24 channels ASIC designed in UMC 0.11 μm technology. The die size is 4.95×1.935 mm^2. The 24 channels are divided in two 12-channels groups. The two groups differs for the architecture of the first stage only. The first group (group A) is based on a TIA architecture with a two stage core amplifier. The second group (group B) is based on a regulated common gate (RCG) input stage followed by a single stage TIA. The pro and cons of the two architectures are briefly described in section 4.

3.1 Threshold setting

The two channel configurations are fully differential, therefore they require a differential threshold voltage, with a common mode equal to the common mode output voltage of the gain stage, which is set by the Gain_Vref[A|B] bias. The differential threshold is set for al channels by the Vth[A|B][p|m] as :

$$V_{THdiff} = V_{TH+} - V_{TH-}$$
$$V_{THcm} = \frac{V_{TH+} + V_{TH-}}{2}$$

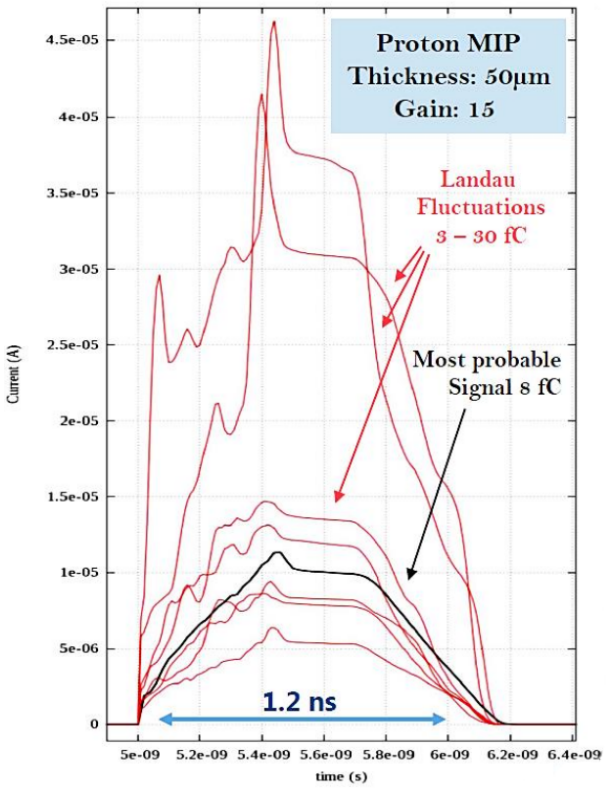

Figure 1: Simulated detector signal

The threshold can be fine-tuned at the channel level with two 6-bits DACs per channel. The DACs can linearly increase the threshold with a nominal LSB value of 0.94 mV. The LSB value can be tuned via the V_{ref}_LSB input. Figure 2 shows the schematic of the voltage DAC while table 1 summarize the tuning capabilities of the circuit (voltages in mV), assuming an external setting of $V_{TH+} = 751$ mV and $V_{TH-} = 741$ mV.

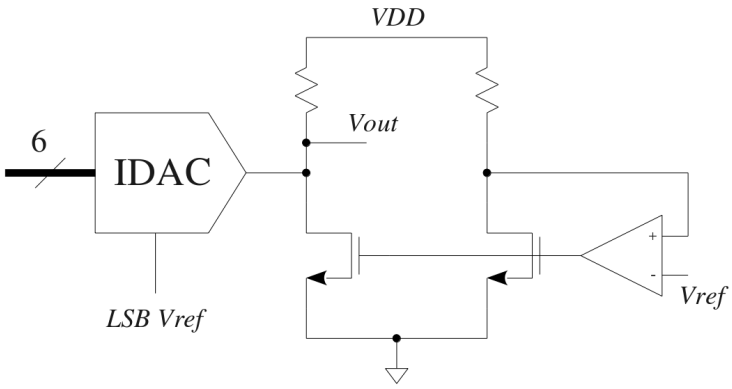

Figure 2: Voltage DAC for threshold tuning

Table 1: Voltage DAC settings

DAC value	0	32	63	63	63	Unit
Vref_LSB	600	600	600	500	700	mV
Vth+	750	780	809	799	820	mV
Vth-	740	770	799	789	810	mV
LSB		0.94	0.94	0.78	1.11	mV

The overall gain at the comparator input for the two stages is shown in table 2. Note that the equivalence

from μA to fC is calculated for the approximate signal shape described in section 2.

Table 2: Simulated gain at the comparator input

Channel scheme	**Gain** [mV/μA]	**Gain** [mV/fC]
A	103.1	137.4
B	64.3	85.8

3.2 Digital interface

The 2×24 threshold fine tuning DACs are controlled by 48 5-bits registers. These registers can be independently loaded and read-out via a serial interface protocol based on 16-bits words. The commands are send via a Serial INput pin (SIN) and the data are read-out on a Serial OUTput pin (SOUT). The two serial streams are synchronous to the CLK clock input and are sampled on the clock rising edge.

The write operations are performed according to the following sequence :

1. Send start sequence : hex A5A5
2. Send write command : $11a_{13}...a_8d_7...d_0$
3. Repeat point 2 if there are other write commands, otherwise send a $00x_{13}...x_0$ sequence

here $a_{13}...a_9$ is the channel address (with reference to the physical layout, address 0 is the leftmost channel and 23 is the rightmost one), while a_8 selects the V_{TH+} (when 1) or the V_{TH-} DAC (when 0). Addresses from 24 to 31 are not used. The bits $d_7...d_0$ are the data to be written in the DAC registers; the two MSBs are not used. "x" represents a don't care.

The read operations are performed as follows :

1. Send start sequence : hex A5A5
2. Send read command : $10a_{13}...a_800x_7...x_0$ sequence
3. Repeat points 1-2 if there are other read commands, otherwise send a $00x_{13}...x_0$ sequence

The serial output is a 16 bits word with format $11a_{13}...a_800d_5...d_0$.

4 Channel architecture

Both versions of the readout channel are based on the same 5 stages architecture, made of the following cells :

- Trans-Impedance Amplifier
- Gain stage version 1
- Gain stage version 2
- Comparator
- Gain stage version 2

the two channel versions differs only in the TIA stage implementation. The TIA is based on a transimpedance amplifier similar to the one used as first stage in optical receivers [1]. The signal from the UFSD detector is in the lower end range of the one from a photodiode, while the input capacitance is an order of magnitude higher. The gain of the TIA is approximately given by its feedback resistance RF, while its bandwidth is given by [2] :

$$f_{-3dB} = \frac{1}{2\pi}\frac{A_0\sqrt{2}}{R_F C_D} \tag{1}$$

where C_D is the detector capacitance and A_0 is the open-loop gain of the core amplifier. Therefore, an higher C_D combined with a lower input current (which set the required R_F) will require a high A_0 in order to obtain high bandwidth. Two options has been implemented :

- Transimpedance amplifier with two stages core amplifier

- Regulated Cascode common Gate (RCG) pre-driver followed by a single stage transimpedance amplifier

the first option increases the bandwidth by increasing the open loop gain by cascading two amplifier stages. However, due to compensation issues, the two-stages open loop banwidth will be lower than the single stage one.

The second option separates the TIA stage from the input capacitance via a RCG buffer. This configuration decouple the bandwidth from the input capacitance but the RCG noise is directly added at the circuit input.

Reference [3] describes the possible transimpedance architectures in terms of trade-off between transimpedance gain and bandwidth.

4.1 TIA

The transimpedance amplifier version A is based on a two stage fully differential amplifier with resistive load and gain boost, in feedback with two 10 kΩ resistors. The two core amplifiers are depicted in figures 3 and 4.

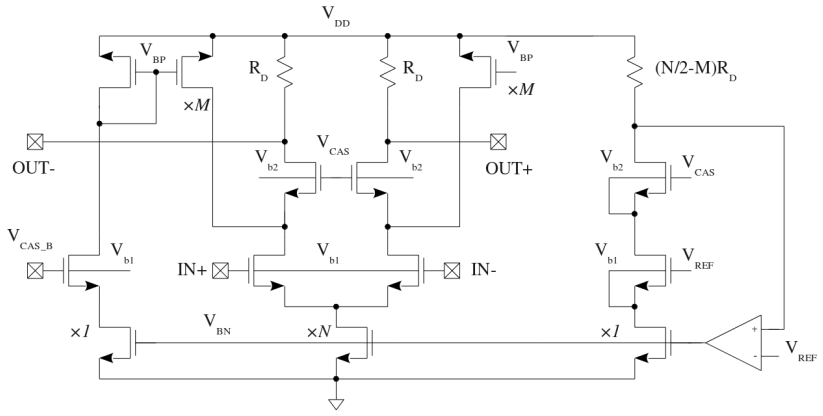

Figure 3: TIA version A first stage

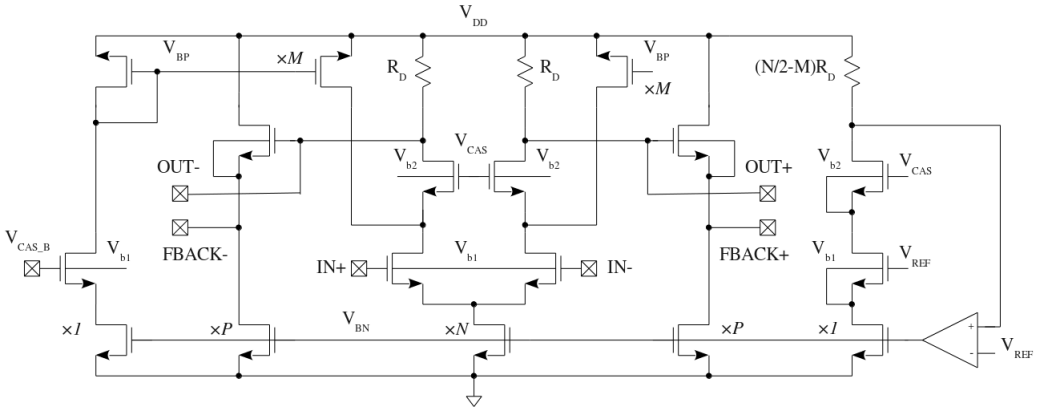

Figure 4: TIA second stage

In the second stage a source follower output has been added in order to equalize the voltage potential between the input and the output when the feedback is closed. The simulated gain of the stage is 5.3 mV/μA.

The transimpedance amplifier version b is based on the single stage fully differential amplifier depicted in figure 4, in feedback with two 10 kΩ resistors. The stage is driven by the Regulated Common Gate (RCG) stage depicted in figure 5. The RCG buffer acts as a current buffer to decouple the input capacitance from the TIA input capacitance. The simulated gain of the stage is 3.4 mV/μA.

4.2 Gain stages

The gain stages 1 and 2 are based on differential amplifiers with resistive load. The difference between the two stages is just an optimization for the common mode voltage. Each stage has a gain slightly higher than 4, for

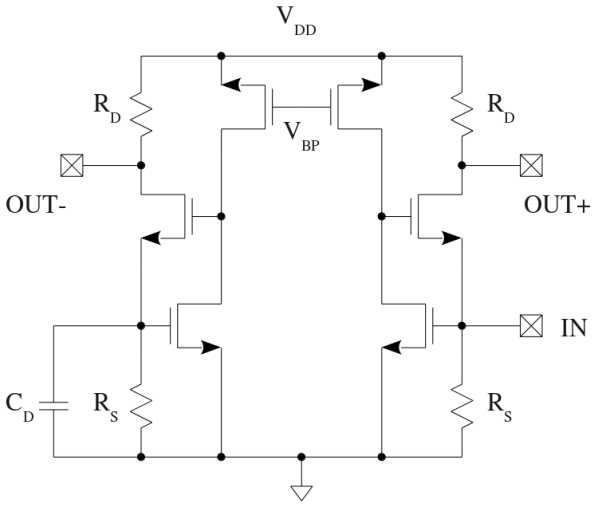

Figure 5: RCG stage

an overall gain of 19.6 (version A) and 19.1 (version B).

4.3 Comparator

The comparator follows the same differential architecture used for the previous stages. Two identical differential pairs connected to the gain stages inputs and the differential threshold, respectively, are loaded by the same couple of 1 kΩ resistors. The description of the threshold setting is described in subsection 3.1.

5 Prototype pinout

The prototype pinout is described in tables 3, 4 and 5.

Table 3: MoveIt_v1a prototype io pin description

Pin name	Description	Notes
inA± < 11 : 0 >	Type A differential input	(1a)
inB< 11 : 0 >	Type B differential input	
outA± < 11 : 0 >	Type A differential output	CML, (1b)
outB± < 11 : 0 >	Type B differential output	CML, (1b)
TestP_odd	Test pulse for odd channels	(1c)
TestP_even	Test pulse for even channels	(1c)

Note (1a) : the negative input should be capacitively connected to ground via a capacitor with the same value as the detector output capacitance in order to maintain the simmetry at the circuit input. The circuit can be very sensitive to the noise on this node.

Note (1b) : the CML outputs are terminated at the input with 50 Ω resistors.

Note (1c) : the signal falling edge gives the correct input charge polarity to the circuit. The calibration capacitance C_{TEST} = 40 fF.

Table 4: MoveIt_v2 prototype supply pin description

Pin name	Description	Notes
VDDA GNDA	Preamplifier supply voltage and ground	(2a)
VDD GND	Analogue supply voltage and ground	(2a)
VDDD GNDD	Digital supply voltage and ground	(2a)
VDDE GNDE	Periphery supply voltage and ground	(2a)

Note (2a) : all grounds (except GNDD) are connected to the die substrate.

Table 5: MoveIt_v2 prototype bias pin description

Pin name	Description	Nominal value	Notes
TIA_VrefA	TIA A Vref	900 mV	(3a)
TIA_VcA	TIA A V cascode 1	1 V	(3a)
TIA_Vc2A	TIA A V cascode 2	700 mV	(3a)
Gain_VrefA	Gain stage A Vref	750 mV	(3b)
CMP_VrefA	Comparator A Vref	750 mV	(3b)
VthAp	Positive threshold A	750 mV + ΔV	(3c)
VthAm	Negative threshold A	750 mV - ΔV	(3c)
Vref_CML_A	CML A output swing	800 mV	(3d)
Vref_LSB	DAC LSB regulation		(3c)
RCG_IbP	Regulated cascode bias current	800 μA	(3a)(3e)
TIA_VrefB	TIA B Vref	900 mV	(3a)
TIA_VcB	TIA B V cascode 1	1 V	(3a)
TIA_Vc2B	TIA B V cascode 2	700 mV	(3a)
Gain_VrefB	Gain stage B Vref	750 mV	(3b)
CMP_VrefB	Comparator B Vref	750 mV	(3b)
VthBp	Positive threshold B	750 mV + ΔV	(3c)
VthBm	Negative threshold B	750 mV - ΔV	(3c)
Vref_CML_B	CML B output swing	800 mV	(3d)

Note (3a) : Bias signals TIA_Vref(A|B), TIA_Vc(A|B), TIA_Vc2(A|B) and RCG_IbP are critical signals and should be kept at their nominal values.

Note (3b) : Bias signals Gain_Vref(A|B) and CMP_Vref(A|B) defines the common mode voltage of the gain and comparator stages. The stage voltage swing is also fixed between VDD and VDD-2Vref.

Note (3c) : Please refer to the threshold setting subsection.

Note (3d) : Bias signals Vref_CML_(A|B) defines the common mode voltage of the CML driver. The driver voltage swing is also fixed between VDD and VDD-2Vref.

Note (3e) : it corresponds to a gate voltage of 425 mV in typical simulations.

Table 6: MoveIt_v2 prototype digital signals

Pin name	Description	Notes
RSTb	Reset signal	active low
CLK	Clock	
SIN	Serial input	
SOUT	Serial output	

References

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