

Development and test of FPGA firmware for the readout of the ABACUS chip for beam monitoring applications in hadron therapy

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Hadron therapy

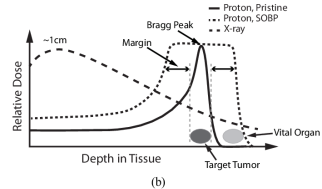
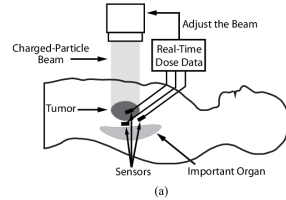
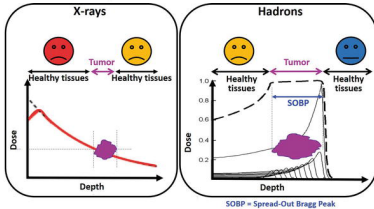
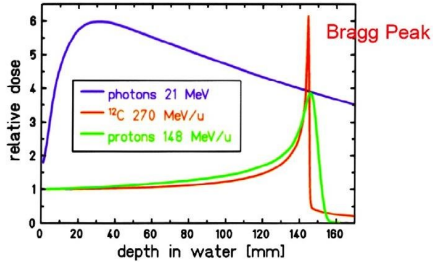
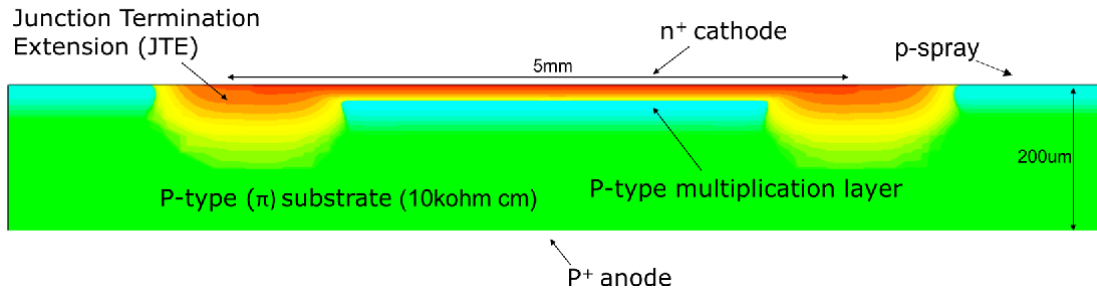


Fig. 1: Illustrations of (1) cancer treatment with *in vivo*

aggiungere informazioni sull'adrotepia



LGAD sensors



aggiungere informazioni su LGAD



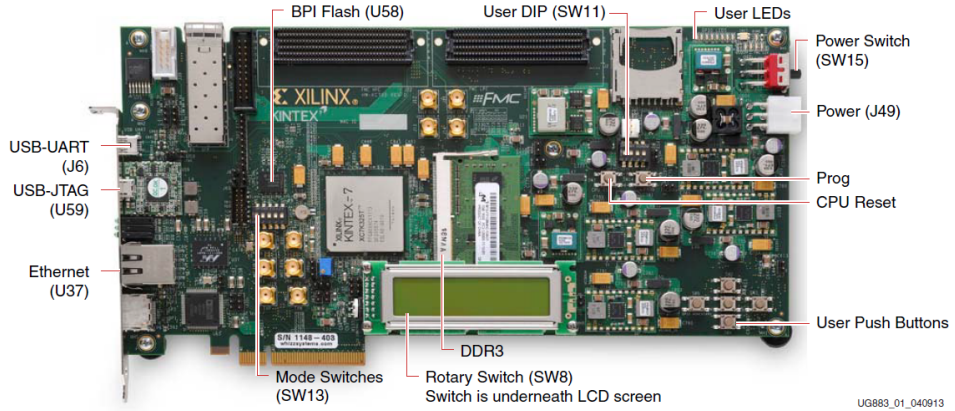
aggiungere informazioni su ABACUS2



seconda slide in cui parlerò di abacus 2



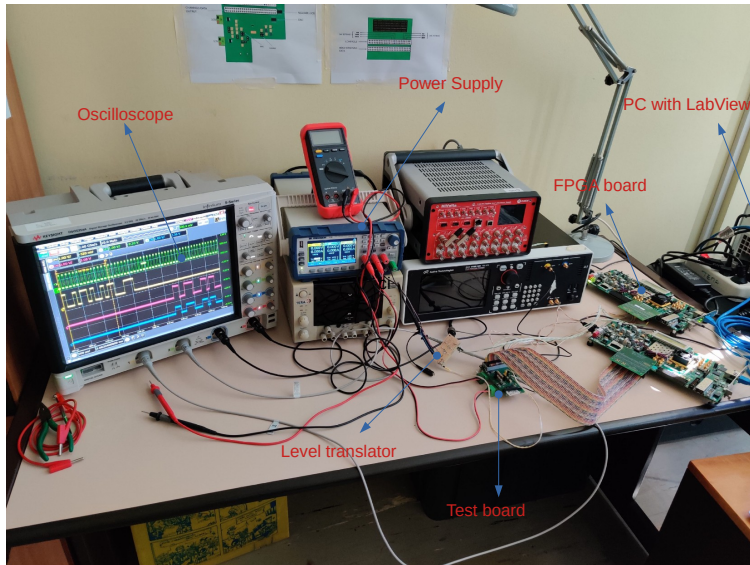
Kintex7 kc705 board



UG883_01_040913



Test bench



Test board with ABACUS2 ASIC



Step1: Signal names and identification.

```
pin68 : out std_logic;--H4  FMC_HPC_CLK0_M2C_P    LVDS D27      -P3 + v
pin69 : out std_logic;--H5  FMC_HPC_CLK0_M2C_N    LVDS C27      -P4 - v
```

Step2: Differential Signalling output buffer.

```
attribute IOSTANDARD of pin68_OBUFDS : label is "LVDS_25";
pin68_OBUFDS : unisim.vcomponents.OBUFDS
port map (
  I => pin68_int,
  O => pin68,
  OB => pin69);
```

Step3: Constraints settings.

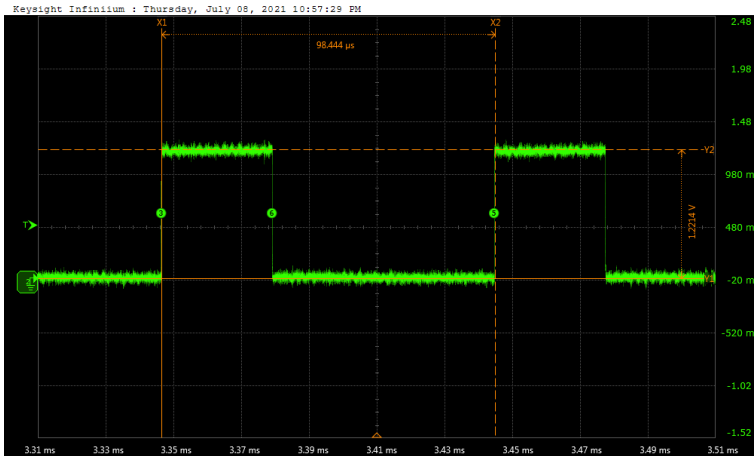
```
# FMC_HPC_CLK0_M2C_P
# FMC_HPC_CLK0_M2C_N
set_property -dict { PACKAGE_PIN D27 IOSTANDARD LVDS_25 DIFF_TERM TRUE } [get_ports pin68]
set_property -dict { PACKAGE_PIN C27 IOSTANDARD LVDS_25 DIFF_TERM TRUE } [get_ports pin69]
```



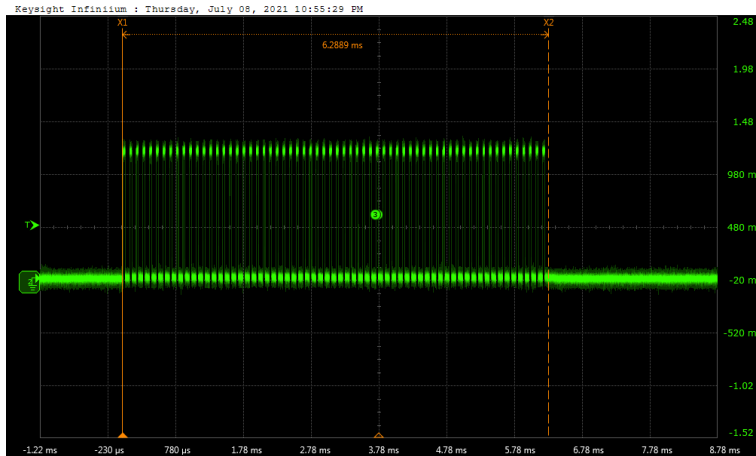
Writing Baseline DACs → code



Writing Baseline DACs → clock stats



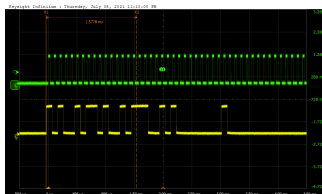
Writing Baseline DACs → clock stats



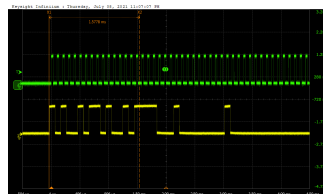
packet time



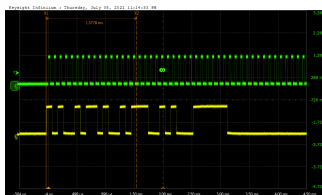
Writing Baseline DACs → data



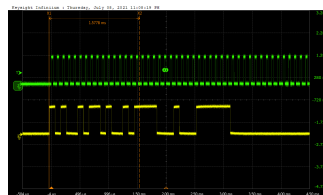
11-001010-00000001 ch05-write01-baslinedac1



11-100010-00000001 ch17-write01-baslinedac1



11-001010-00111111 ch05-write63-baslinedac1



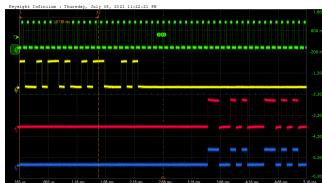
11-100010-00111111 ch17-write63-baslinedac1



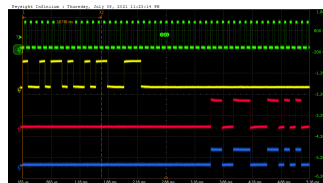




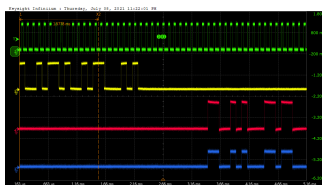
Reading Baseline DACs → data



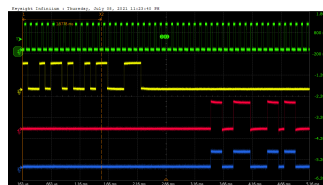
11-001010-00000001 ch05-write01-baselinedac1



11-100010-00000001 ch17-write01-baselinedac1



11-001010-00111111 ch05-write63-baselinedac1



11-100010-00111111 ch17-write63-baselinedac1



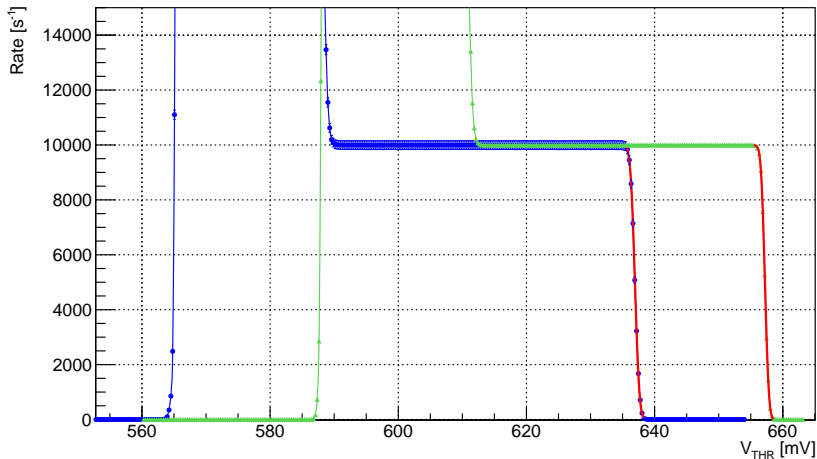
Constraints

```
##Single-ended signal for baseline dac1#####
# FMC_HPC_LA01_CC_P
set_property -dict { PACKAGE_PIN D26 IOSTANDARD LVCMOS25 DIFF_TERM TRUE} [get_ports baseline_dac1_sck]
# FMC_HPC_LA01_CC_N
set_property -dict { PACKAGE_PIN C26 IOSTANDARD LVCMOS25 DIFF_TERM TRUE} [get_ports gnd_10]
#
# FMC_HPC_LA06_P
set_property -dict { PACKAGE_PIN H30 IOSTANDARD LVCMOS25 DIFF_TERM TRUE} [get_ports baseline_dac1_mosi]
# FMC_HPC_LA06_N
set_property -dict { PACKAGE_PIN G30 IOSTANDARD LVCMOS25 DIFF_TERM TRUE} [get_ports gnd_11]
#
# FMC_HPC_LA05_P
set_property -dict { PACKAGE_PIN G29 IOSTANDARD LVCMOS25 DIFF_TERM TRUE} [get_ports baseline_dac1_miso]
# FMC_HPC_LA05_N
set_property -dict { PACKAGE_PIN F30 IOSTANDARD LVCMOS25 DIFF_TERM TRUE} [get_ports gnd_12]
```

Da aggiungere spiegazione

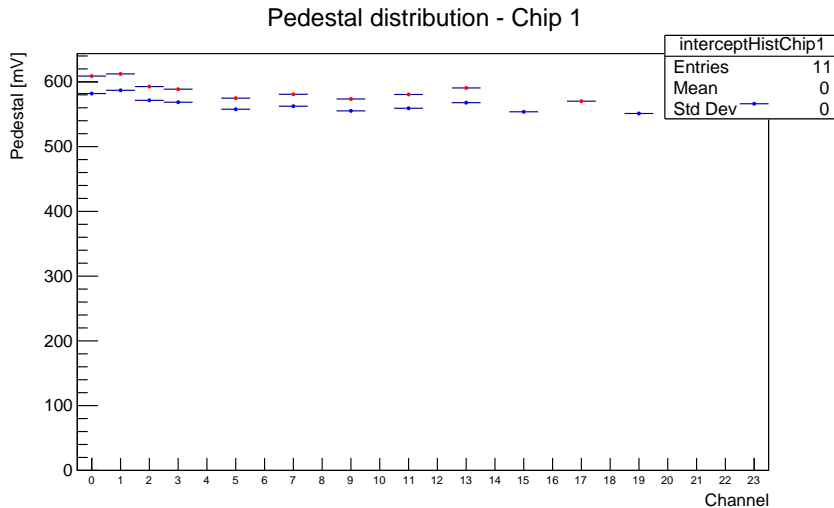


HV=0V-Pulse=600mV chip 1 channel 1



qua spiego il grafico e cosa rappresenta





qua spiego il grafico e cosa rappresenta



Future additions to the FPGA firmware

- timestamp
- latched counters

Thanks for the attention





www.researchgate.net/figure/Dose-depth-curve-for-monoenergetic-photons-protons-and-carbon-ions-courtesy-of-GSI_fig1_283521369



www.intechopen.com/books/novel-prospects-in-oxidative-and-nitrosative-stress/oxidative-stress-in-hadrontherapy



www.semanticscholar.org/paper/A-Millimeter-Scale-Single-Charged-Particle-for-Lee-Scholey/ae955a07a42e9c124a8473357cd485b0b9928090



[www.semanticscholar.org/paper/Low-Gain-Avalanche-Detectors-\(LGAD\)-for-particle-Moffat-Bates/0477d7bc2c9a3b26ad776874598f56d7d5b54c45](http://www.semanticscholar.org/paper/Low-Gain-Avalanche-Detectors-(LGAD)-for-particle-Moffat-Bates/0477d7bc2c9a3b26ad776874598f56d7d5b54c45)



