U?	U?	U?	U?	U?	U?
74LS02	74LS08	74LS245	74LS32	74LS540	74LS688
1Y VCC	1A VCC	DIR VCC	1A VCC	E1 VCC	G vcc
1A 4Y	1B 4B	A1 OE	1B 4B	D1 E2	P0 P=Q
1B 4B	1Y 4A	A2 B1	1Y 4A	D2 Y1	Q0 Q7
2Y 4A	2A 4Y	A3 B2	2A 4Y	D3 <u>Y2</u>	P1 P7
2A 3Y	2B 3B	A4 B3	2B 3B	D4 \(\overline{Y3}\)	Q1 Q6
2B 3B	2Y 3A	A5 B4	2Y 3A	D5 Y4	P2 P6
GND 3A	GND 3Y	A6 B5	GND 3Y	D6 \(\overline{Y5}\)	Q2 Q5
		A7 B6	<u> </u>	D7 <u>Y6</u>	P3 P5
		A8 B7		D8 <del>Y</del> 7	Q3 Q4
		GND B8		GND Y8	GND P4

U? 74LS74				
1CLR	vcc			
1D	2CLR			
1CLK	2D			
1PRE	2CLK			
1Q	2PRE			
1Q	2Q			
GND	2Q			

A	U ATMed	? a1284	
		(ADC0) PA0	]
Р	B1	(ADC1) PA1	
Р	B2 (INT2)	(ADC2) PA2	
Р	B3	(ADC3) PA3	
Р	B4 (SS)	(ADC4) PA4	
Р	B5 (MOSI)	(ADC5) PA5	
Р	B6 (MISO)	(ADC6) PA6	
Р	B7 (SCK)	(ADC7) PA7	
R	ESET	AREF	
ν	cc	AGND	
G	IND	AVCC	
×	TAL2	PC7	
х	TAL1	PC6	
Р	D0 (RX0)	PC5	
Р	D1 (TX0)	PC4	
Р	D2 (RX1/IN	T0) PC3	
Р	D3 (TX1/IN	T1) PC2	
Р	D4	(SDA) PC1	

PB0	(ADC0) PA0	GND	VCC
PB1	(ADC1) PA1	NC	TEST 1
PB2 (INT2)	(ADC2) PA2	ANALOG B	ANALOG C
PB3	(ADC3) PA3	ANALOG A	DAG
PB4 (SS)	(ADC4) PA4	NC	DA1
PB5 (MOSI)	(ADC5) PA5	IOB7	DA2
PB6 (MISO)	(ADC6) PA6	IOB6	DA3
PB7 (SCK)	(ADC7) PA7	IOB5	DA4
RESET	AREF	IOB4	DA5
VCC	AGND	IOB3	DA6
GND	AVCC	IOB2	DA7
XTAL2	PC7	IOB1	BC1
XTAL1	PC6	IOB0	BC2
PD0 (RX0)	PC5	IOA7	BDIR
PD1 (TX0)	PC4	IOA6	TEST 2
PD2 (RX1/IN	T0) PC3	IOA5	A8
PD3 (TX1/IN	T1) PC2	IOA4	A9
PD4	(SDA) PC1	IOA3	RESET
PD6	(SCL) PC0	IOA2	CLOCK
PD6	PD7	IOA1	IOA0

U? MCP23S17					
	GPB0	GPA7			
	GPB1	GPA6			
	GPB2	GPA5			
	GPB3	GPA4			
	GPB4	GPA3			
	GPB5	GPA2			
	GPB6	GPA1			
	GPB7	GPA0			
	VCC	INTA			
	GND	INTB			
	CS F	RESET			
	SCK	A2			
	SI	A1			
	so	A0			
			•		

U? MT5C1008				
	NC	vcc		
	A16	A15		
	A14	CE2		
	A12	WE		
	A7	A13		
	A6	A8		
	A5	A9		
	A4	A11		
	А3	ŌE		
	A2	A10		
	A1	CE		
	A0	DQ8		
	DQ1	DQ7		
	DQ2	DQ6		
	DQ3	DQ5		
	GND	DQ4		

-	U FMS	
	G	VCC
	DQ1	DQ4
	DQ2	CAS
	w	DQ3
	RAS	A0
	A6	A1
	A5	A2
	A4	А3
	GND	A7

U? V9958		
GND	XTAL2	
DHCLK	XTAL1	
DLCLK	RAS	
VRESET	CAS2	
HSYNC	CAS1	
CSYNC	CASX	
BLEO	vcc	
CPUCLK/VDS	WR	
RESET	AD7	
YS	AD6	
CBDR	AD5	
C7	AD4	
C6	AD3	
C5	AD2	
C4	AD1	
C3	AD0	
C2	RD7	
C1	RD6	
C0	RD5	
GND/DAC	RD4	
VCC/DAC	RD3	
G	RD2	
R	RD1	
B	RD0	
INT	CD0	
WAIT	CD1	
HRESET	CD2	
MODE1	CD3	
MODE0	CD4	
CSW	CD5	
CSR	CD6	

	U? Z80
A11	A10
A12	A9
A13	A8
A14	A7
A15	A6
CLK	A5
D4	A4
D3	A3
D5	A2
D6	A1
VCC	A0
D2	GND
D7	RFSH
D0	M1
D1	RESET
ĪNT	BUSRQ
NMI	WAIT
HALT	BUSACK
MREQ	WR
ĪORQ	RD