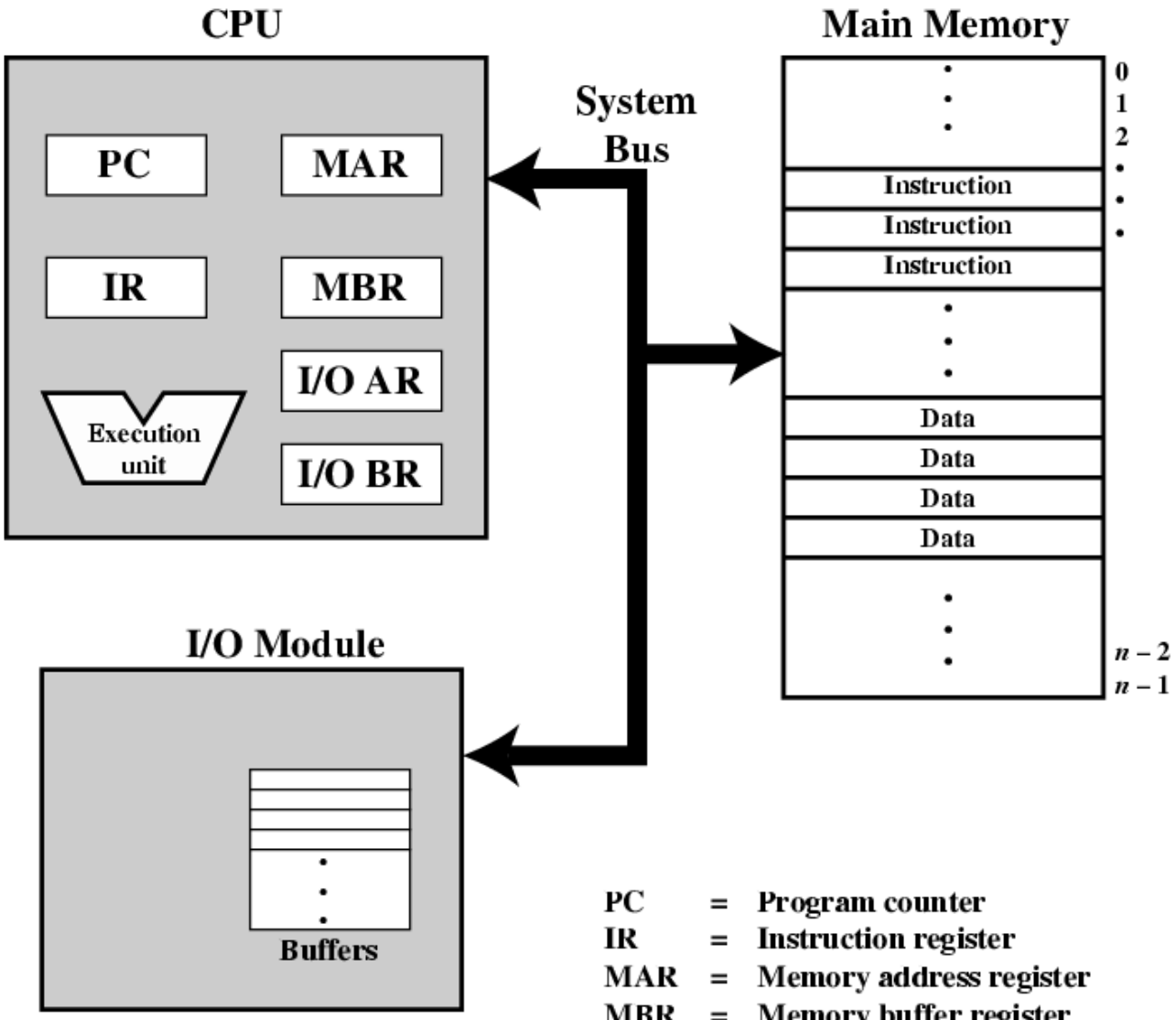
Chapter #3
A Top-Level View of Computer Function & Interconnection

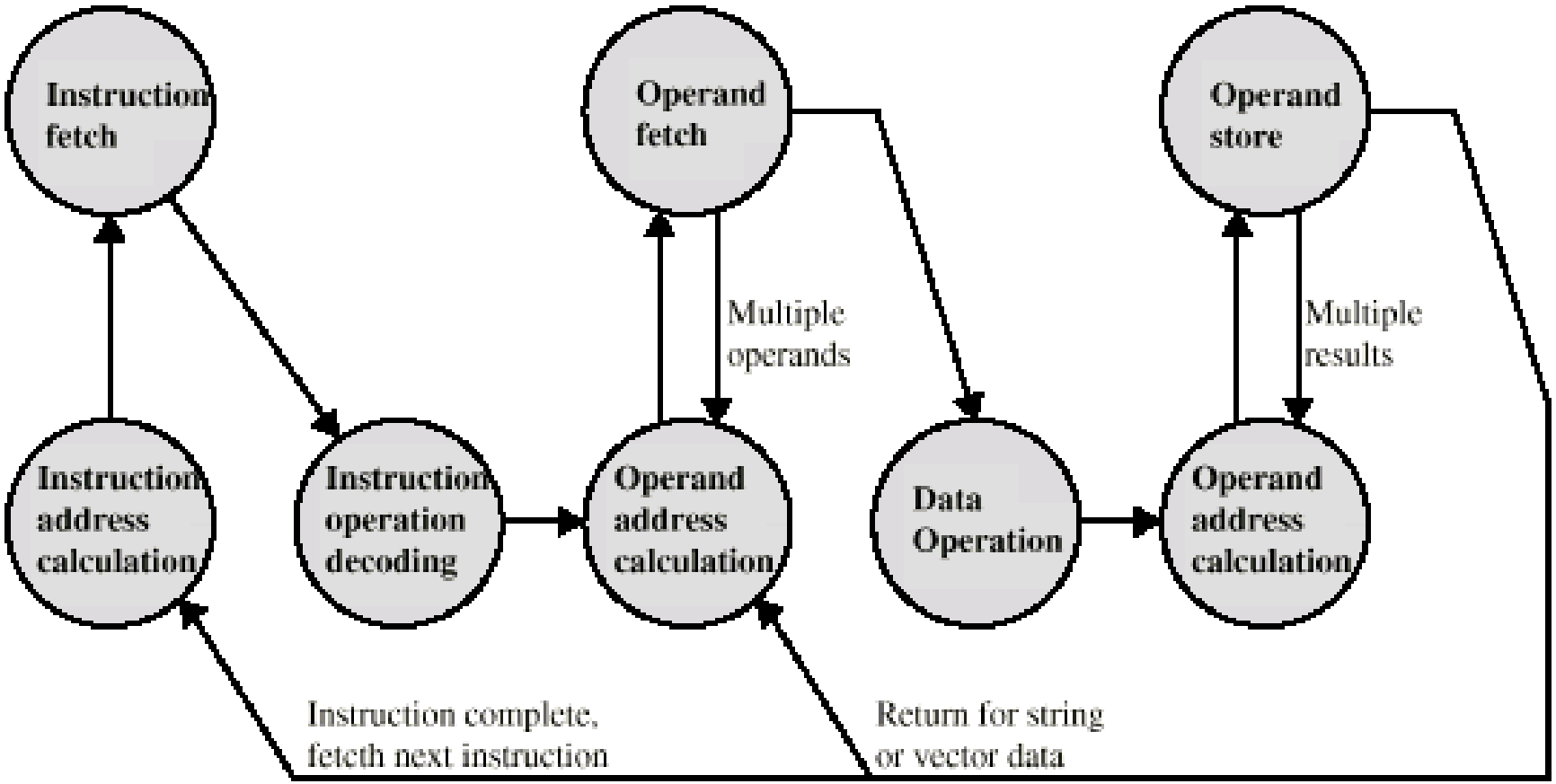
Computer Architecture Components

- Central Processing Unit:
  - —Control Unit (fetch & decode instruction)
  - —Arithmetic Logic Unit (execution)
- Main memory:
  - —Temporary storage of code and results
- I/O:
  - —“Permanent” storage of data and instructions, and display of results

Components: Top Level View



Instruction Cycle -- State Diagram



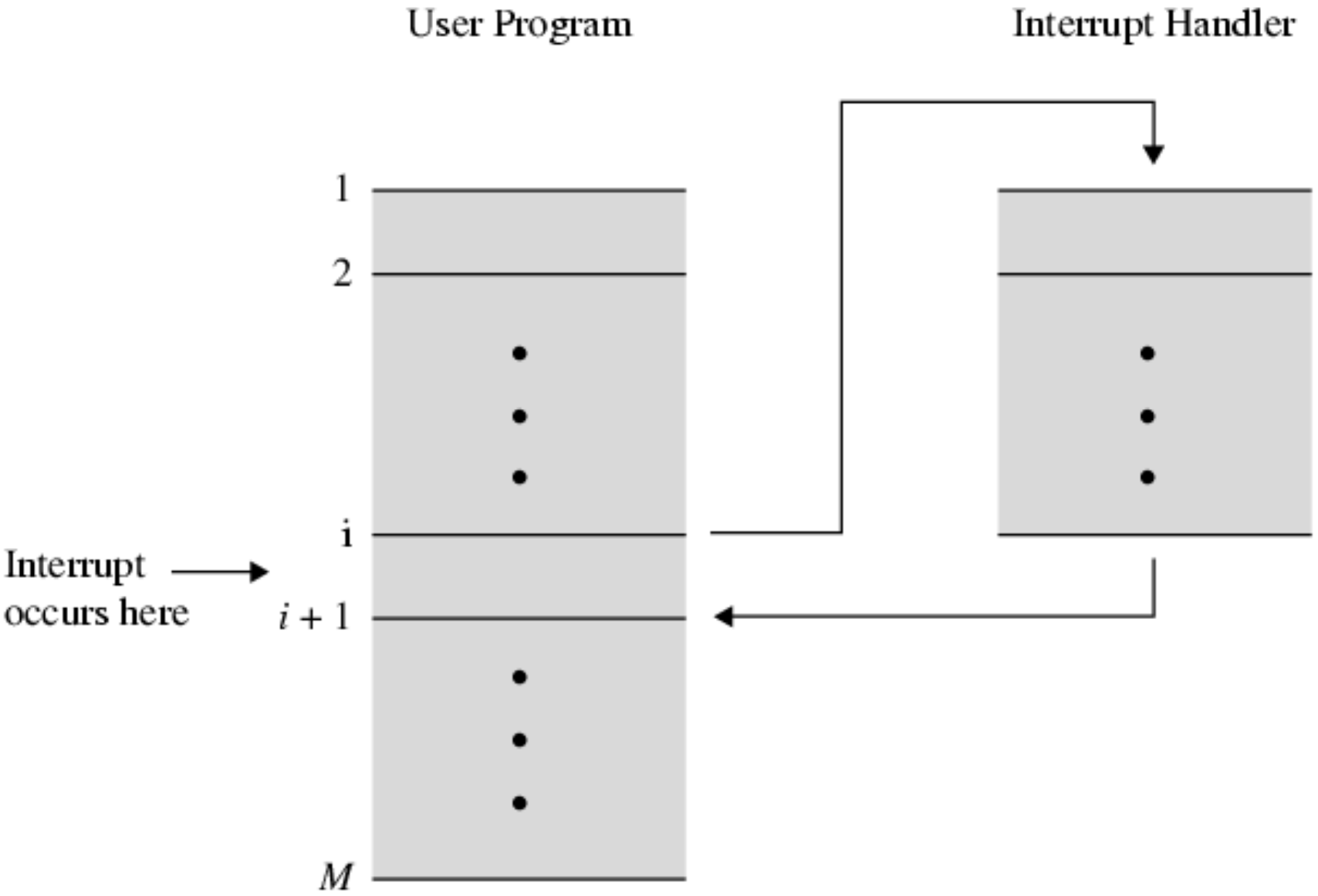
Interrupts

- Mechanism by which other modules (e.g. I/O) may interrupt normal sequence of processing
- Program
  - e.g. overflow, division by zero
- Timer
  - Timer w/in processor, allowing regular O/S functions
- I/O
  - from I/O controller
  - e.g. Printer, disk, communication
- Hardware failure
  - e.g. memory parity error

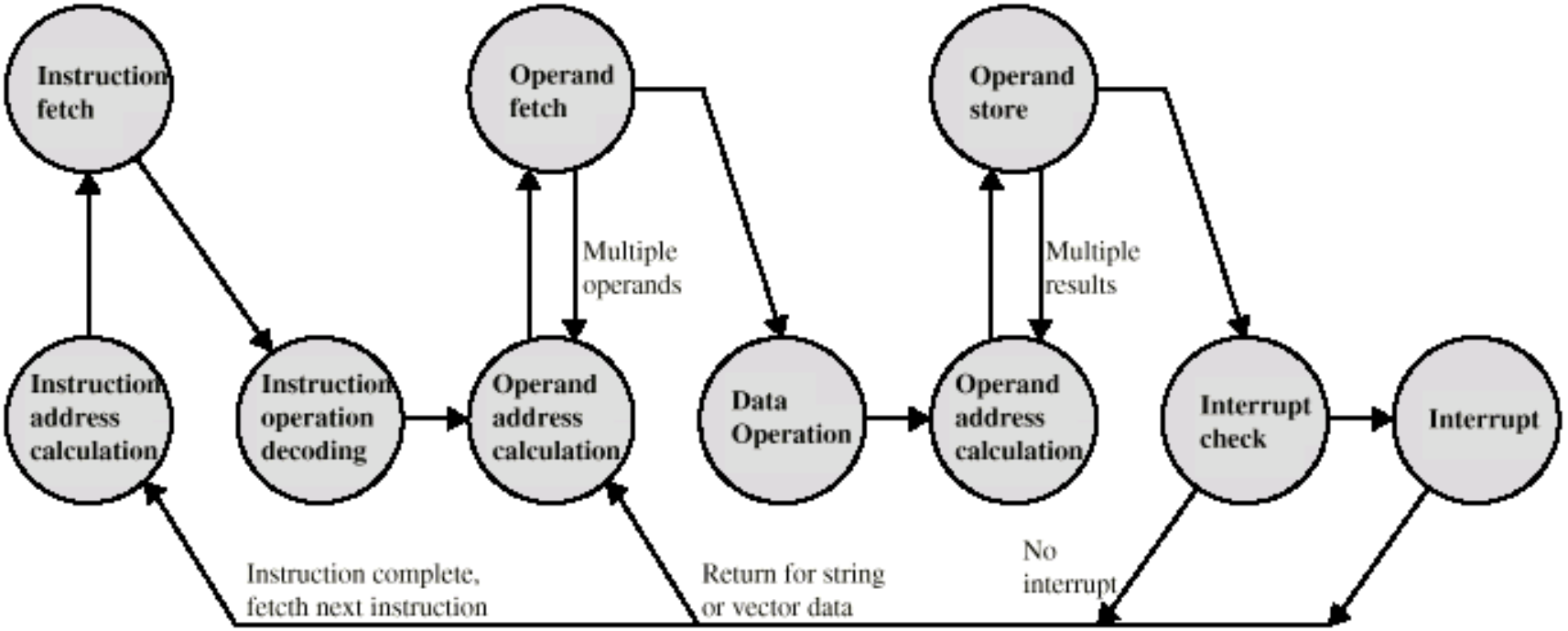
Interrupt Cycle

- Added to instruction cycle
- Processor checks for interrupt
  - Indicated by an interrupt signal
- If no interrupt, fetch next instruction
- If interrupt pending:
  - Suspend execution of current program
  - Save context
  - Set PC to start address of interrupt handler routine
  - Process interrupt
  - Restore context and continue interrupted program

Transfer of Control via Interrupts



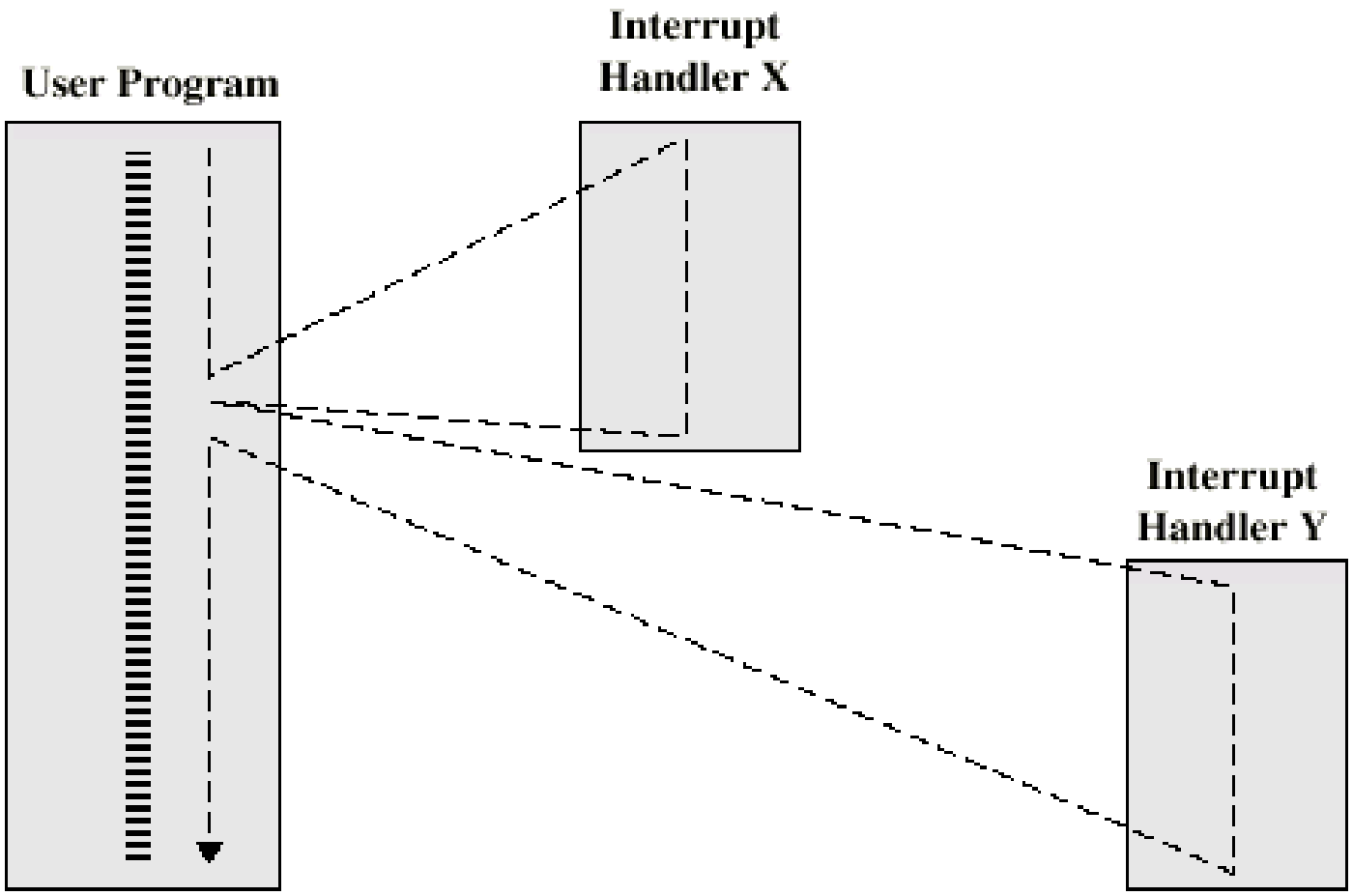
Instruction Cycle (with Interrupts) State Diagram



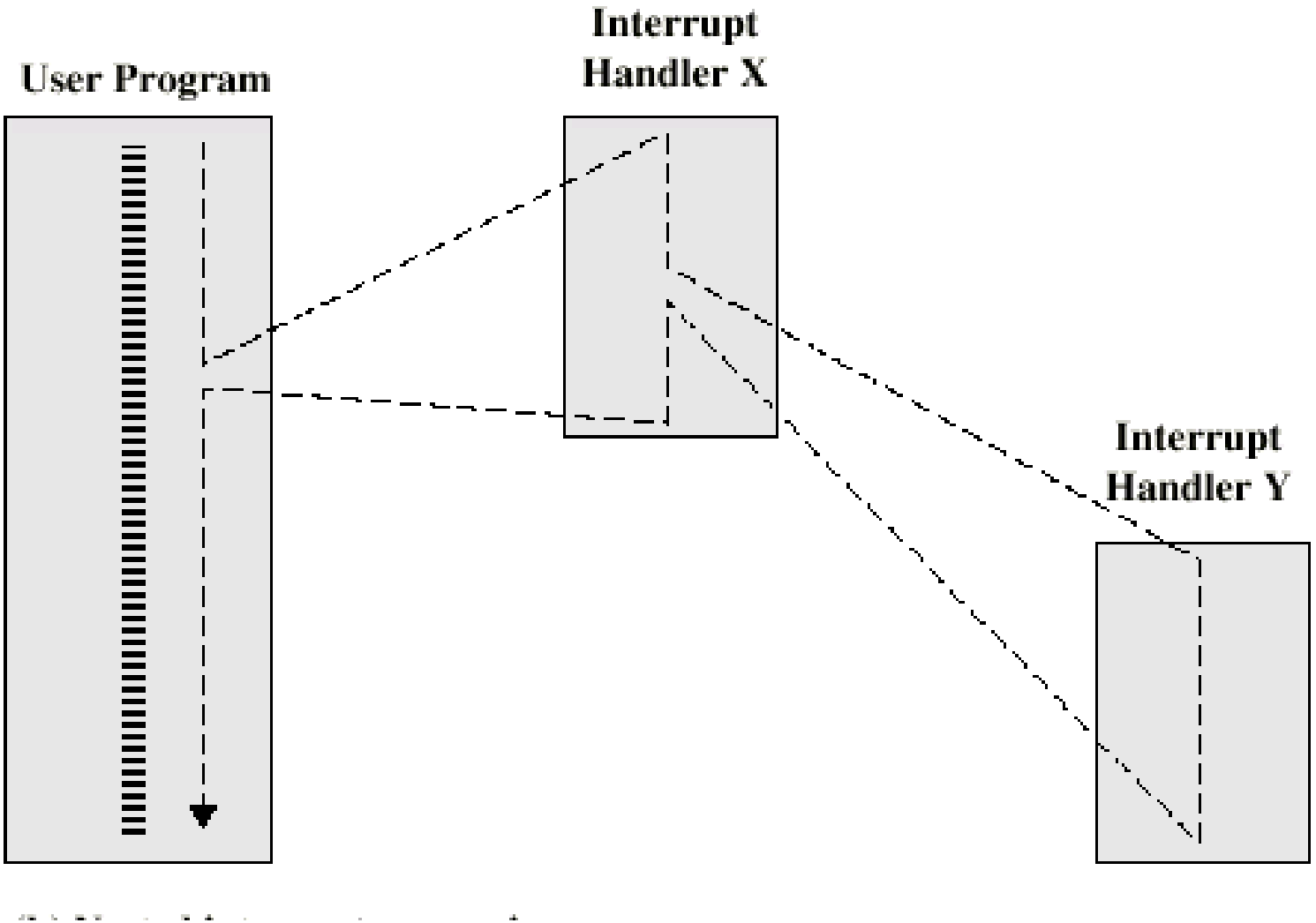
Multiple Interrupt Handling

- Disabled interrupt/Sequential
  - —Processor will ignore further interrupts while processing one interrupt
  - —Interrupts remain pending and are checked after first interrupt has been processed
  - —Interrupts handled in sequence as they occur
- Defined priorities/Nested
  - —Low priority interrupts can be interrupted by higher priority interrupts
  - —When higher priority interrupt has been processed, processor returns to previous interrupt

Multiple Interrupts - Sequential



Multiple Interrupts – Nested



Time Sequence of Multiple Interrupts