COMP 222
Sample Midterm #1 Solutions

Problem 1

Suppose we want to compare four sequences of code in terms of performance on a machine with a frequency of 4.0 GHz. Given the following information, determine: (i) the CPI (average number of cycles per instruction) of each code sequence, (ii) the CPU execution time of each code sequence; and (iii) the MIPS (millions of instructions per second) of each sequence; (iv) the best sequence in terms of lowest average CPI; (v) the best sequence in terms of lowest CPU execution time; (vi) the best sequence in terms of highest MIPS.

Instruction class	CPI of the Instruction class
A	1
B	2
C	3
D	5

Code sequence	Instruction count (in millions)			
	A	B	C	D
1	3	4	2	5
2	4	5	4	2
3	1	2	5	3
4	2	6	3	4

Sequence	**(i) CPI avg**	**(ii) Execution time (msec)**	**(iii) MIPS**
1	3.00	10.50	1333.33
2	2.40	9.00	1666.67
3	3.18	8.75	1257.14
4	2.87	10.75	1395.35

(iv) Sequence 2 has the lowest CPI
(v) Sequence 3 had lowest execution time
(vi) Sequence 2 has highest MIPS

Problem 2

Suppose the following enhancements are proposed for a program, with the following respective speedup factors and fraction of use. Determine the best choice of the five by calculating the total speedup for each option.

Enhancement	Speedup factor	Percent of use
A	2	35%
B	3	30%
C	5	20%
D	6	10%
E	7	5%

Enhancement	Total Speedup
A	1.21
B	1.25 (best)
C	1.19
D	1.09
E	1.04

Problem 3

Suppose that multiple I/O interrupts occur within the execution of a user program, including a printer interrupt (lowest priority), a disk controller interrupt (medium priority), and a communication line interrupt (highest priority). Each interrupt takes 15 cycles. Determine the actual starting and finishing time of each interrupt request, assuming nested interrupt processing, and that five printer interrupt requests, labeled **P1,P2,P3,P4,P5** are issued (and must be handled in order), one every 20 cycles (starting from the 15th cycle), five disk interrupt requests, labeled **D1,D2,D3,D4,D5** are issued (and must be handled in order), one every 15 cycles (starting from the 20th cycle), and five communication line interrupt requests, labeled **C1,C2,C3,C4,C5** are issued (and must be handled in order), one every 25 cycles (starting from the 10th cycle), by filling in the following table (the order of requests is not important):

Interrupt request	Requesting cycle	Starting cycle	Finishing cycle
P1	15	160	175
P2	35	175	190
P3	55	190	205
P4	75	205	220
P5	95	220	235
D1	20	25	55
D2	35	55	85
D3	50	100	130
D4	65	130	145
D5	80	145	160
C1	10	10	25
C2	35	35	50
C3	60	60	75
C4	85	85	100
C5	110	110	125

Problem 4

Suppose an architecture utilizes a 16-bit word-addressable addressing scheme for accessing main memory. Suppose there is a 4-way set-associative cache of total capacity 8192 words, which contains 16 words per block.

a) Fill in the number of bits necessary for each field of the address for mapping to the cache:

Tag	Set	Word
5	7	4

b) For the following main memory word-addressable address references, determine: (i) the corresponding cache tag (in decimal), (ii) set (in decimal), and (iii) word (in decimal), by filling in the following table. Initially the cache is empty.

Address	Tag	Set	Word
1097	0	68	9
2593	1	34	1
750	0	46	14
1181	0	73	13
2493	1	27	13
699	0	43	11
1173	0	73	5
607	0	37	15