COMP 222 Computer Organization
Assignment #5—Pipelining/Superscalar Architecture

Objective:

To calculate the performance of a program with dependent arithmetic instructions, by simulating the execution on (i) a simple 6-stage pipeline architecture; (ii) a superscalar 6-stage architecture of degree 2 (2 sets of functional units).

Inputs:

- Number of instructions in the program
- Set of automatically numbered instructions containing arithmetic register assignments
- Architecture to simulate program on (pipelined, superscalar)

Outputs:

- The total cycle count for the program
- Gantt chart showing delays of instructions

Specification:

The program calculates the performance of a set of arithmetic register assignment statements and prints out the aligned instructions based on choosing from a menu of choices, where each choice calls the appropriate procedure, where the choices are:

1) Enter instructions
2) Calculate total cycle count on a 6-stage pipelined architecture
3) Calculate total cycle count on a 6-stage superscalar architecture
4) Quit program

(Hint: to recognize data dependencies, store the register indices in a **struct** containing fields for the destination register index, both source register indices, and the dependency delay.

(Printing hint: To align stages, use printf("\t…"))

What to turn in:

Softcopy of source code submitted to http://moodle.csun.edu via the submission instructions. Be sure to name your source code: **asmt5_*yourlastname*.c**.

Any deviation from the format for submission will result in an automatic -10%. You can use any editor and/or compiler, but make sure your code compiles and executes under the gcc compiler—otherwise you will receive 0 points for compilation and execution.

```
% asmt5

Pipelined/Superscalar instruction performance
---------------------------------------------
1) Enter instructions
2) Calculate total cycle count on a 6-stage pipelined architecture
3) Calculate total cycle count on a 6-stage superscalar architecture
4) Quit program

Enter selection: 1

Enter total number of instructions: 5

1) r0=r1+r2
2) r1=r0+r3
3) r2=r3+r2
4) r0=r2+r0
5) r3=r3+r3

Pipelined/Superscalar instruction performance
---------------------------------------------
1) Enter instructions
2) Calculate total cycle count on a 6-stage pipelined architecture
3) Calculate total cycle count on a 6-stage superscalar architecture
4) Quit program

Enter selection: 2

Total number of cycles: 14

1)FI    DI      CO      FO      EI      WO
2)                      FI      DI      CO      FO      EI      WO
3)                              FI      DI      CO      FO      EI      WO
4)                                                      FI      DI      CO      FO      EI      WO
5)                                                              FI      DI      CO      FO      EI      WO

Pipelined/Superscalar instruction performance
---------------------------------------------
1) Enter instructions
2) Calculate total cycle count on a 6-stage pipelined architecture
3) Calculate total cycle count on a 6-stage superscalar architecture
4) Quit program

Enter selection: 3

Total number of cycles: 12

1)FI    DI      CO      FO      EI      WO
2)                      FI      DI      CO      FO      EI      WO
3)                      FI      DI      CO      FO      EI      WO
4)                                              FI      DI      CO      FO      EI      WO
5)                                              FI      DI      CO      FO      EI      WO


Pipelined/Superscalar instruction performance
---------------------------------------------
1) Enter instructions
2) Calculate total cycle count on a 6-stage pipelined architecture
3) Calculate total cycle count on a 6-stage superscalar architecture
4) Quit program

Enter selection: 4
%
```