COMP 222
Sample Midterm #1

Problem 1

Suppose we want to compare four sequences of code in terms of performance on a machine with a frequency of 4.0 GHz. Given the following information, determine: (i) the CPI (average number of cycles per instruction) of each code sequence, (ii) the CPU execution time of each code sequence; and (iii) the MIPS (millions of instructions per second) of each sequence; (iv) the best sequence in terms of lowest average CPI; (v) the best sequence in terms of lowest CPU execution time; (vi) the best sequence in terms of highest MIPS.

Instruction class	CPI of the Instruction class
A	1
B	2
C	3
D	5

Code sequence	Instruction count (in millions)			
	A	B	C	D
1	3	4	2	5
2	4	5	4	2
3	1	2	5	3
4	2	6	3	4

Problem 2

Suppose the following enhancements are proposed for a program, with the following respective speedup factors and fraction of use. Determine the best choice of the five by calculating the total speedup for each option.

Enhancement	Speedup factor	Percent of use
A	2	35%
B	3	30%
C	5	20%
D	6	10%
E	7	5%

Enhancement	Total Speedup
A	
B	
C	
D	
E	

Problem 3

Suppose that multiple I/O interrupts occur within the execution of a user program, including a printer interrupt (lowest priority), a disk controller interrupt (medium priority), and a communication line interrupt (highest priority). Each interrupt takes 15 cycles. Determine the actual starting and finishing time of each interrupt request, assuming nested interrupt processing, and that five printer interrupt requests, labeled **P1,P2,P3,P4,P5** are issued (and must be handled in order), one every 20 cycles (starting from the 15^{th} cycle), five disk interrupt requests, labeled **D1,D2,D3,D4,D5** are issued (and must be handled in order), one every 15 cycles (starting from the 20^{th} cycle), and five communication line interrupt requests, labeled **C1,C2,C3,C4,C5** are issued (and must be handled in order), one every 25 cycles (starting from the 10^{th} cycle), by filling in the following table (the order of requests is not important):

Interrupt request	Requesting cycle	Starting cycle	Finishing cycle

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Problem 4

Suppose an architecture utilizes a 16-bit word-addressable addressing scheme for accessing main memory. Suppose there is a 4-way set-associative cache of total capacity 8192 words, which contains 16 words per block.

a) Fill in the number of bits necessary for each field of the address for mapping to the cache:

Tag	Set	Word

b) For the following main memory word-addressable address references, determine: (i) the corresponding cache tag (in decimal), (ii) set (in decimal), and (iii) word (in decimal), by filling in the following table. Initially the cache is empty.

Address	Tag	Set	Word
1097			
2593			
750			
1181			
2493			
699			
1173			
607			