AREA I/O'S POTENTIAL FOR FUTURE PROCESSOR SYSTEMS

AS DESIGNERS SEEK TO ACHIEVE EVER SMALLER SYSTEMS WITH EVER MORE FUNCTIONALITY, INTERCONNECTION TECHNOLOGY IS RECEIVING RENEWED ATTENTION. AREA I/O TECHNIQUES CAN BE APPLIED TO REAP IMPROVEMENTS AT THE CHIP, PACKAGE, AND SYSTEM LEVELS.

Etienne Hirt
Michael Scheffler
Jean-Pierre Wyss
Swiss Federal Institute of Technology

"Faster microprocessor systems are just around the corner," we think, and each year a new generation of microprocessors seems to prove us right. Technical advances, however, occur primarily at the chip level—progress moves much slower at the system level. For example, internal clock rates in state-of-the-art processors have already beaten the timetable predicted by the Semiconductor Manufacturing Technology consortium, as shown in Table 1.[1] External clock rates and memory bus widths, unfortunately, have not progressed nearly as rapidly. To overcome the discrepancy between off-chip bandwidth and on-chip speed, designers have added several levels of cache hierarchies, resulting in a continuously growing latency.[2] Even the I/O bus widths predicted from 1994 in Table 1 pose implementation difficulties.

Bandwidth, latency, system speed, and, of course, the size of future microprocessor systems all highly depend on interconnection technologies. Interconnection will become the key performance bottleneck as semiconductor technology improvements continue to reduce feature size.

In this article, we describe the use of on-chip area I/O for future microprocessor systems on the basis of a case study we made of an Intel Pentium system. Area I/O is simply a method of locating I/Os over the entire chip instead of just the periphery. We show that system designers can achieve significant performance gains with area I/O and size reductions at both the system and chip levels. We also explain how area I/O in conjunction with high-density interconnects leads to a new package and chip partitioning concept.

A decade ago, designers made the first attempt to improve off-chip interconnectivity with multichip modules (MCMs).[3] In this technology, a chip has a block of functional components (called a partition) and numerous high-speed interconnects grouped together on a single substrate, forming a "new" component. This substrate is an interconnect level between the system board and the chip, on which unpackaged chips (bare dies) can be mounted.

For those early MCMs, designers wire bonded the bare dies to the substrate, an interconnect technique ill suited to wide, fast I/O buses and components having many I/Os. Bonding several hundred wires with small pitches to a substrate is a complex, time-consuming process. Moreover, the high inductivity of wire bonds ultimately degrades overall signal speed.

Looking at today's packages, more appropriate interconnect technologies redistribute peripheral I/O over the entire back side of the package. The use of solder balls instead of leads relieves pitch constraints. So, from the interconnect and packaging points of view, area I/O

0272-1732/98/$10.00 © 1998 IEEE

Table 1. Semiconductor Manufacturing Technology Consortium's performance predictions for microprocessors.

	Year				
Chip parameter	**1998–2000**	**2001–2003**	**2004–2006**	**2007–2009**	**2010–2012**
On-chip frequency (MHz)	200	300	400	500	625
Off-chip frequency (MHz)	66	100	100	125	150
I/O bus width (bits)	64	128	128	256	256

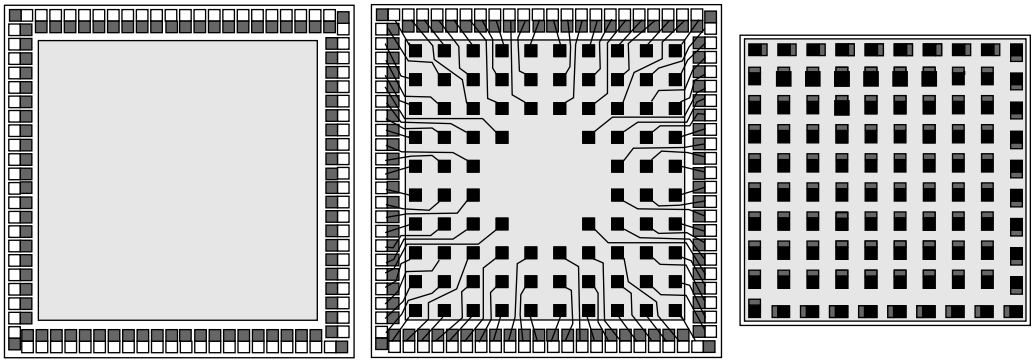

Figure 1. Three types of pad placement. White cells represent chip pads; black cells, package pads; dark-gray cells, pin electronics. Standard peripheral I/O layout (a); re-routing I/O layout (b); area I/O layout (c).

is already the method of the future. But instead of extending this concept to the chip level, designers still typically place a chip's I/O pads peripherally, chiefly because of beliefs regarding area I/O such as these:

- The chip area increases as no circuitry can be placed under the pad area.
- It's too complicated, and no tools can route the I/O pads on the core.
- There is no performance benefit, just added cost.
- Flexibility disappears, as area I/O must use bump/ball interconnect technology and cannot be wire bonded.

On the basis of our case study, we show how these beliefs should be reconsidered.

Peripheral and area I/Os

Figure 1a shows a traditional, standard chip layout with peripheral I/O pads. The core is gray, the I/O pads are white, and the I/O pin electronics are dark gray. (Pin electronics include I/O buffers and electrostatic discharge protection circuits.) This layout has several disadvantages, chiefly a low core-to-I/O-area ratio for a high pin count, and pad-limited ICs, even at small pitches. Second, pads can only be placed at the chip's edges. Finally, the wire bonding technique used with this layout causes parasitic effects.

A design alternative is flip-chip technology instead of wire bonding. Flip-chip solder bump connections eliminate parasitics, and assembly time lessens because the number of I/Os does not matter. However, high pin-count ICs with a potential 70-micron peripheral I/O pad pitch impose manufacturing constraints that make flip-chip technology infeasible. Such constraints include short circuits between neighboring bumps or misaligned bumps.

Alternatively, Figure 1b shows redistributed I/O pads over the entire surface as can be found on chip-size packages, relieving these constraints.[4] CSPs, almost the size of the die area, have additional dielectric and metal layers at the wafer level to spread the pads over the chip area. This additional process is expensive, however, and can cause yield loss due to possible wafer

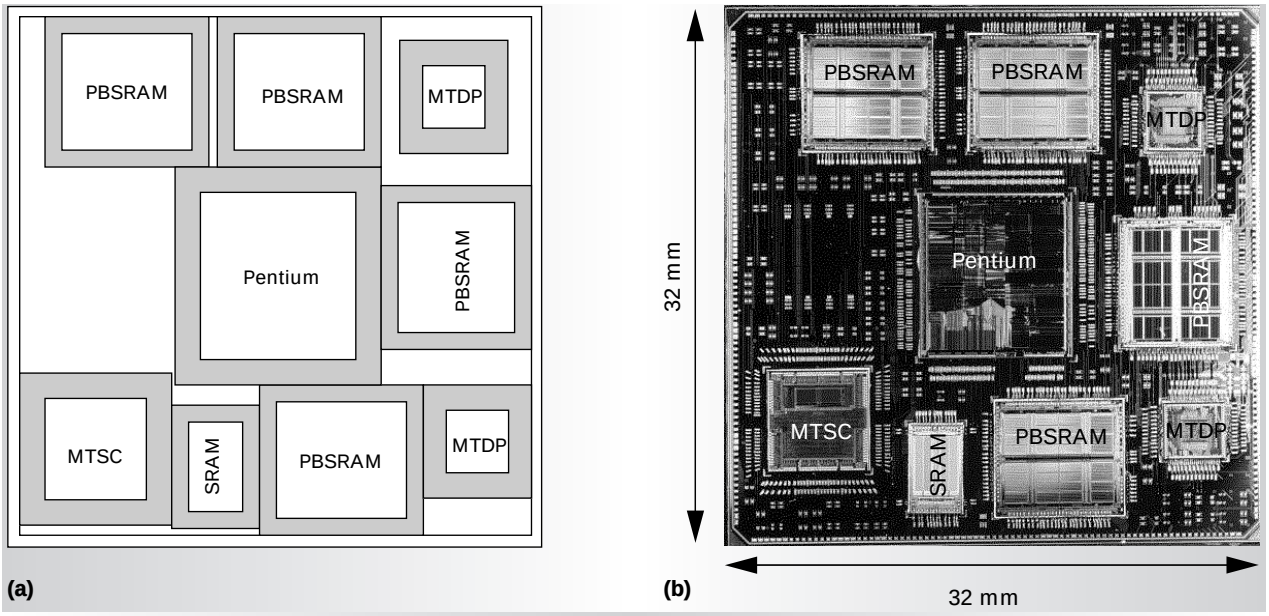

Figure 2. Module placement: footprint placement, indicating die size plus fan-out (gray) (a); final module (b). MTSC indicates Intel's system controller; MTDP, Intel's data path controller.

breakage. CSPs, about 1.2 times the size of the die area, connect the die to an interposer that redistributes the pads. For both package types, interconnects between nearest-neighbor chips lengthen significantly, with wires extending from the core to the periphery and back to the center before leaving the chip level.

Figure 1c shows an area I/O layout that eliminates this core-to-periphery wiring because the I/O pads can be placed adjacent to their related core area. Why, then, was this type of layout not used earlier? In the past, designers encountered two major problems with area I/O. First, placing pin electronics (especially large electrostatic discharge cells) near the pads consumed excessive area. Second, circuitry placed under I/O pads was destroyed by the pressure applied through wire bonding.

Nowadays, the area I/O technique requires fewer ESD restrictions when keeping the nets encapsulated so no human can touch them. This means that designers can make these cells smaller.[5] Bump interconnection allows circuitry to be placed under pads because it induces less stress than wire bonding. Initial attempts for a CAD tool, in fact, are now being pursued.[6] Overall, this permits an area arrangement that reduces on-chip routing and capacitance loads, with optimal power supply. Advantages include

- a released pad pitch, leading to higher manufacturing yield;
- an increased I/O count, allowing for better power distribution and a wider bus, and
- a reduced chip-to-chip interconnect length due to smaller die sizes.

State-of-the-art MCM technology

As a benchmark for our case study, we used a Pentium MCM on a high-density substrate that we designed.[7]

MCM technology[3] offers an intermediate layer—the high-density substrate—with vias and line pitches closely matched to the chip I/Os that have a pad pitch as low as 70 microns. Up to 80% of the total number of interconnections remain completely on the substrate, leading to significantly fewer I/Os. Compared to a packaged IC, the component size itself shrinks when designers use unpackaged bare dies; the fan-out also significantly shrinks. (Fan-out is the area overhead needed to mount and connect a component to the next level. Fan-out plus component area leads to the overall footprint, or the area where no other component can be placed.)

Figure 2 shows the high-performance part of a microprocessor system implemented on a 4-layer MCM-D (deposited) substrate with a 20-

micron line width, 30-micron spacing, and 50-micron via land. We encapsulated the MCM in a 320-pin plastic stud grid array, containing

- a Pentium 133-MHz processor CPU,
- 512-Kbyte second-level cache, pipeline burst SRAM (cache), and asynchronous SRAM (tag),
- system controller, and
- data path controller.

The MCM-D technology reduces the size of this functional block by 75%, compared to a standard printed circuit board (PCB) solution, as we show later. It also improves signal integrity resulting from shorter lines with better high-frequency characteristics.

Figure 2 shows how the component size and the I/O fan-out of the components limit the module size. This fan-out overhead, caused by the wire bond pads rather than by additional escape routing, provides the smallest module presently available.

Even the high-density substrates used today in MCM technology do not let designers increase the number of I/Os to achieve wider host buses. Designers could add more I/Os, however, by adopting area I/O for interconnections.

Case study

Our case study involved three system implementations. System S was a standard, off-the-shelf Pentium MCM with standard peripheral I/O components, as shown in Figure 2. System P was a PCB implementation of system S, which we included essentially for size and cost comparison. System A used area I/O components, featuring bump interconnections, to extend the functionality of system S. System A featured a wider host bus, like that predicted in Table 1. With a commercially available 400-MHz CPU, we also used a 100-MHz, 16-byte-wide host and DRAM data bus. The flip-chip interconnect's lower inductivity gave system A an improved power supply, which doubled the signal-to-power pin ratio.

Table 2 summarizes the system configurations in our case study. Figure 3 illustrates the system architecture used for all three systems.

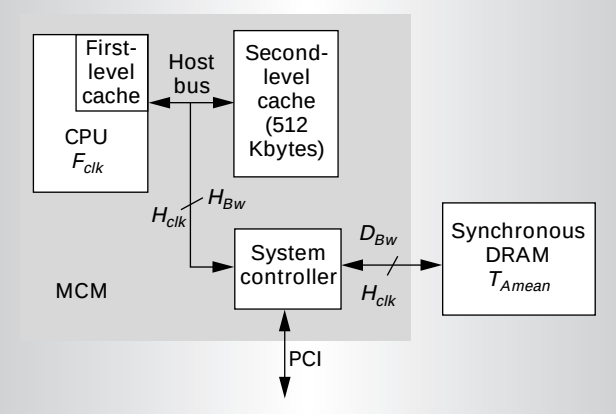

Figure 3. Pentium MCM system architecture underlying all three of our case study implementations.

Size implications

At the chip level, area I/O lets designers place pin electronics near the pads to reduce the chip's die size, as shown in Figure 1c. For the processor IC, designers can place the I/O pads atop the core area. This results in making the IC about 10% smaller than otherwise possible.

Area I/O lets designers reduce the space needed for the system controller and for the data path controller by roughly 30%. Static RAMs, on the other hand, do not need to be adapted for area I/O: A peripheral pad pitch of greater than 150 microns is manufacturable with bumps.

At the substrate level, bump connections permit greater system size reductions than wire bonding. Bumped dies need only about a 0.5-mm fan-out on each side—instead of 1.5 mm—for two rows of bond pads.

Including the reductions achieved at both

Table 2. Our case study used the specifications below, which were delineated by Intel and Sematech.[1,8]

System specifications	Symbol	Systems S and P (peripheral I/O; MCM/PCB; small bus)	System A (area I/O; MCM; wide bus)
CPU speed	F_{CLK}	200 MHz	400 MHz
Host bus speed	H_{CLK}	66 MHz	100 MHz
DRAM mean cycle time	T_{Amean}	30 ns	15 ns
DRAM bus width	D_{Bw}	8 bytes	16 bytes
Host bus width (data)	H_{Bw}	8 bytes	16 bytes
Signal-to-power ratio	*SPR*	4/1	8/1

Table 3. Assumptions we made in determining performance for the case study systems, based on Intel's Tillamook CPU design.[8,9]

System parameters	Symbol	Assumptions for systems A, P, S
Bytes/command	B_C	2
CPU cycles/command	C_C	3
Data bytes/command	B_D	4
Host address	H_A	29
General-purpose pins	GP	60
Core power pins	C_p	74

the chip and the substrate levels, we were able to reduce the size of system A by 44%. Figure 4 shows the relative sizes of systems S and A, compared to system P.

Performance implications

We used bandwidth as the key factor in determining performance gains. We based our calculations on the assumptions in Table 3 and the data in Table 2. Formulas 1 to 4 show how we arrived at our calculations. They also provide sufficient detail to roughly estimate the available and required bandwidth, and the pin count.

Table 4 shows the results of our case study, notably the considerable improvements we achieved with area I/O in system A. When we compared available bandwidth to required bandwidth, we found that systems P and S are bandwidth limited. However, data preloading is possible for system A (because the CPU may speculatively load data from the main memory into the cache). If we had designed system A with an 8-byte host bus, an available bandwidth of only 528 Mbytes/s would have resulted; thus, it would still be bandwidth limited. Only with area I/O techniques can designers unleash the computer's full performance.

Available bandwidth from

$$DRAM = D_{Bw}/T_{Amean} \quad (1)$$

Needed bandwidth by

$$CPU = (f_{CPU}/C_C) \times (B_C + B_D) \quad (2)$$

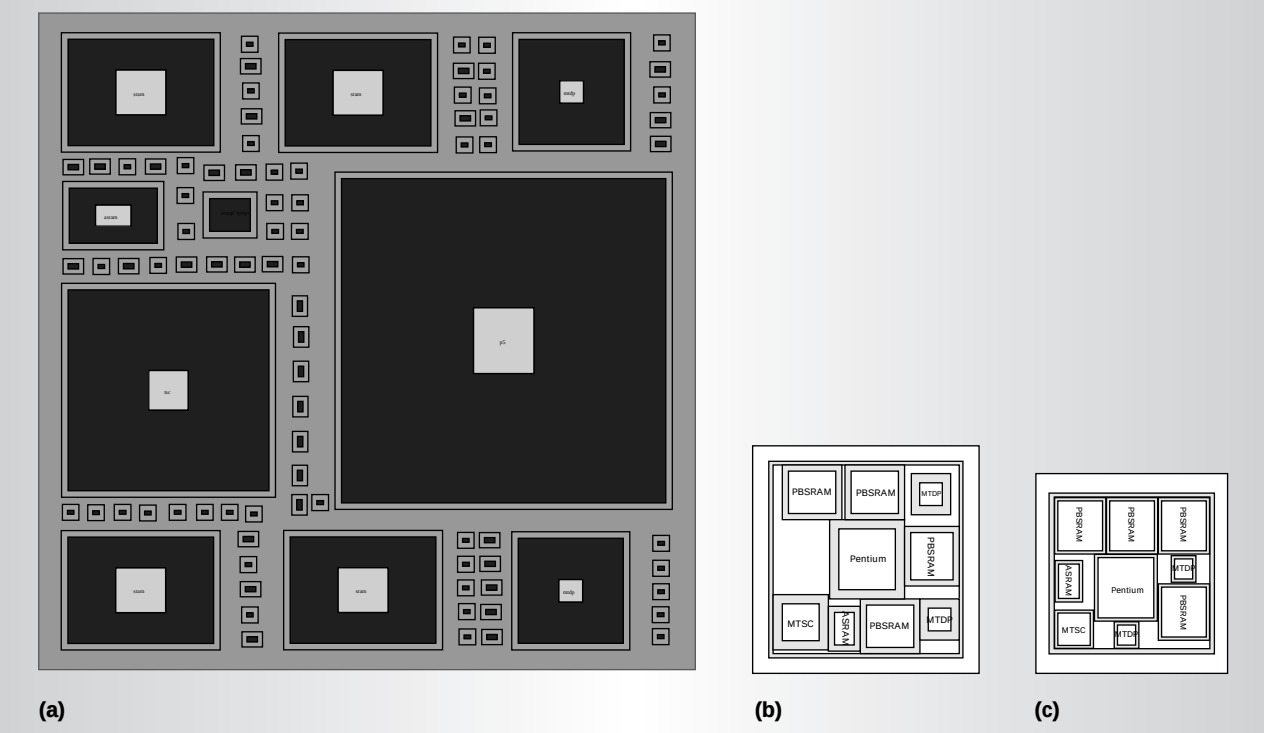

Figure 4. Size comparison of three different implementations (shown 80% to scale). System P: standard Pentium system with peripheral I/O ICs implemented as a PCB (a); system S: standard Pentium with peripheral I/O implemented as an MCM (b); and system A: standard Pentium with area I/O implemented as an MCM (c).

$$Signal\ pins = (H_{Bw} \times 10) + H_A + GP \quad (3)$$

$$Power\ pins = (Signal\ pins/SPR) \times 2 + C_p \quad (4)$$

Table 4 also shows the pad pitch required for the CPU IC. If we had implemented system A with peripheral I/O pads instead of area I/O, the CPU pad pitch would be below 60 microns. Such a configuration would be difficult to wire bond, and flip-chip mounting would be impossible. The area I/O technology used in system A, on the other hand, allows a comfortable pad pitch.

Table 4. Performance comparison of the three case study system implementations. With system A, speculative cache preloading is possible, thereby overcoming bandwidth limitations.

Performance parameters	Systems S and P (peripheral I/O; MCM/PCB; small bus)	System A (area I/O; MCM; wide bus)
Available bandwidth from DRAM	264 Mbytes/s	1,056 Mbytes/s
Needed bandwidth by CPU	400 Mbytes/s	800 Mbytes/s
Signal pins needed by CPU	169	249
Power pins needed by CPU	158	132
Total pins	327	381
Minimum pad pitch calculated for CPU I/Os	114 microns	455 microns
Minimum pad pitch measured for CPU I/Os	75 microns	300 microns*

* The ratio between calculated and measured pitch for system S can be expected to be similar for the other configurations.

Cost implications

In comparing the costs of the three case study implementations, we considered the area consumed on the PCB motherboard. All the cost data assumed a high-volume production per year (greater than 1,000,000). We therefore did not consider changes in nonrecurring expenses that would result from different design methodologies.

We based our assumptions for die/chip cost on two considerations. First, several known-good die programs offer the same cost and the same test level for packaged and bare dies. Second, die size drives die cost: decreasing die size reduces die cost (see system A in Table 5.

At the chip level, no additional metal layer is needed for area I/O, as pads for bump interconnection can be placed over the active area. Also, routing density is much lower on the top two IC metal layers because designers place pin electronics close to the I/O pads and the core's "output." Moreover, by connecting the power locally, we can remove the big power rails.

At the substrate level, system A's 44% size reduction of the MCM substrate requires an additional metal layer to provide sufficient wiring space.

Table 5. Cost implications of three different system implementations. Because we projected costs assuming high-volume production, we did not include nonrecurring expense costs. (KGD stands for known-good die.)

System cost contributors	System P (full PCB system; small bus)	System S (peripheral I/O MCM; small bus)	System A (area I/O MCM; wide bus)
System PCB			
Size	81.0 cm^2	20.0 cm^2	16.0 cm^2
Metal layers	6.0	4.0	4.0
Cost	\$0.12/cm^2	\$0.1/cm^2	\$0.1/cm^2
MCM substrate			
Type	Not applicable	4-layer MCM-D	5-layer MCM-D
Cost	\$2/cm^2	\$3/cm^2	
Size		10.2 cm^2	6.76 cm^2
MCM package	Not applicable	\$5	\$5
Die cost			
Processor	\$150	\$150	\$135
System controller	\$21	\$21	\$14
Data path controller	$2 \times$ \$7	$2 \times$ \$7	$2 \times$ \$4
Burst SRAM	$4 \times$ \$20	$4 \times$ \$20	$4 \times$ \$20
Number of I/Os (sum of all dies)	1,200	1,200	1,420
Assembly cost	\$0.05 per pin	\$0.05 per bond	\$0.05 per bump
Yield dies	0.999 all dies	All KGDs (0.999) Except SRAM (0.99)	All KGDs (0.999) Except SRAM (0.99)
Yield substrate	Not applicable	0.99	0.99
Yield assembly	0.999 per chip	0.9999 per bond wire	0.99 per flip-chip attach

At the PCB main board level, the area could be reduced by 20% compared to system S.

Table 6. Cost modeling results achieved with the Modular Optimization Tool.

Cost contributors	System P (full PCB system; small bus)	System S (peripheral I/O MCM; small bus)	System A (area I/O MCM; wide bus)
Direct cost	$281	$299	$267
Yield loss to be added per unit	$6	$63	$39
Overall cost	$283	$362	$306

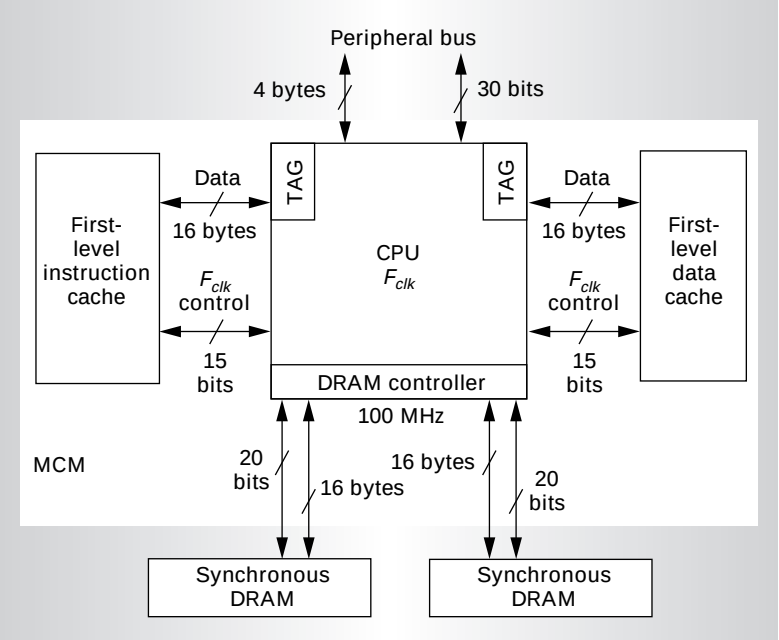

Figure 5. In a possible future system architecture, the first-level cache is moved off chip, but it remains accessible with no loss in speed.

We used the Modular Optimization Environment (MOE)[10] cost modeling tool to make the calculations. MOE's process-oriented cost structure representation lets us easily consider the different manufacturing configuration yields. Using Monte Carlo simulation, MOE calculates the cost for a virtual process line, including direct cost, nonrecurring expense, test, and yield. In this virtual process line, MOE assumes a functional test before the system is shipped, which sorts out any units containing errors. This yield loss is added to the direct cost of every shipped system. Table 6 details the results.

Table 6 shows that system S has a higher direct cost than system P. This is largely due to the high MCM substrate cost and the yield loss caused by wire bonding. System A has the lowest direct cost of all three implementations. Additionally, system A's higher substrate cost is expected to decrease due to large-area panel production of MCM-D substrate, which reduces the overall costs even more.[11]

Future architectures

Area I/O can immediately improve system performance as well as reduce system size, based on state-of-the-art architectures. Bus architectures such as Intel's dual independent bus and the advanced graphics port bus, and newer approaches,[5,12] can also benefit from area I/O's higher I/O count.

Area I/O also offers new partitioning options. Figure 5 shows a possible future architecture in which designers can move functional blocks on or off chip.[13] With the more efficient SRAM process, rather than SRAM integrated in a logic process, the active area shrinks by more than half. Therefore, the first-level cache can be moved off chip, which improves CPU die yield without performance loss. Additionally, Figure 5 shows the DRAM controller implemented on the CPU chip, which ensures low latency and permits two independent DRAM banks. With this architecture, designers could freely distribute a CPU's functionality on an MCM to achieve optimal performance and yield.

Interconnection is the key to closing the gap between on- and off-chip bus speed. Area I/O interconnect technology in particular shows promise to meet the increasing pin count foreseen by the NTRS. It offers both increased bandwidths (due to a higher I/O count), and fewer manufacturing constraints (due to the substrate's larger pad pitch) with less cost (due to the reduced chip size). Because of bump bonding, area I/O has shorter interconnect lengths and lower parasitics, which improves signal speed and quality. The relaxed pitch also improves manufacturability as well as assembly reliability. Area I/O would also benefit the CSP community because the interposer could be kept very simple, without pad redistribution. Finally, any speed degradation introduced by CSPs becomes marginal.

The next challenge will be the hardware proof-of-concept. Difficulties include the lack of suitable tools that allow data exchange

between package, IC, and PCB designers, and building virtual prototypes to design optimal systems. Chip-level area I/O, in an integrated chip-, package-, and system-level design, has the potential for offering much-improved computing performance. But meeting the challenging predictions of the NTRS road map, especially with regard to the optimistic off-chip buses, necessitates a closer cooperation among chip, package, and system designers. Then, we can be assured that a faster microprocessor system is indeed "just around the corner." MICRO

Acknowledgments

We thank colleagues D. Ammann, A. Thiel, and C. Habiger for valuable discussions and helpful comments.

References

1. *National Technology Roadmap for Semiconductors*, Sematech, Austin, Texas, 1994; http://www.sematech.org/public/ roadmap/.
2. D. Patterson et al., "A Case for Intelligent RAM," *IEEE Micro,* Vol. 17, No. 2, Apr. 1997, pp. 34-44.
3. P.D. Franzon, *Multichip Module—Technologies and Alternatives,* Van Nostrand Reinhold, New York, 1993.
4. R. Fillion et al., "Demonstration of a Chip-Scale Chip-on-Flex Technology," *Proc. Int'l Conf. Multichip Modules*, Int'l Soc. for Hybrid Microelectronics, Reston, Va., Apr. 1996, pp. 351-356.
5. Q. Zhu and S. Tam, "Package Clock Distribution Design Optimization for High-Speed and Low-Power VLSIs," *IEEE Trans. CPMT*, Part B, Feb. 1997.
6. P. Phiroze et al., "CAD Tools for Area-Distributed I/O Pad Packaging," *Proc. IEEE Multichip Module Conf.*, IEEE Press, Piscataway, N.J., 1997, pp. 125-129.
7. E. Hirt et al., "A Pentium-Based MCM for Embedded Computing," *Proc. 11th European Microelectronics Conf.*, Int'l Soc. for Hybrid Microelectronics, 1997, pp. 516- 523.
8. Intel Corp., *Mobile Pentium Processor with MMX Technology on .25 Micron*, 1997; http://developer.intel.com/design/mobile/datashts/243468.htm.
9. Intel Corp., *Pentium Processor Family Developer's Manual*, Mt. Prospect, Ill., 1995.
10. M. Scheffler et al., "MOE—A Modular Optimization Environment for Concurrent Cost Reduction," *Proc. Fifth European Concurrent Eng. Conf.*, SCS Europe Bvba, Ghent, Belgium, 1998, pp. 115-119.
11. N. Ammann, "Lap—The Key to Low Cost Multichip Packaging," *Future Circuits Int'l*, Vol. 2, 1997, pp. 25-28.
12. L. Schaper, "Seamless High Off-Chip Connectivity (SHOCC)," *Proc. IEEE Int'l Workshop on Chip Package Co-Design*, CPD '98 Secretary, c/o Electronics Laboratory ETH, Zürich, Switzerland, 1998, pp. 39-45.
13. E. Hirt et al., "On the Impact of Area I/O on Partitioning: A New Perspective," *Proc. IEEE Int'l Workshop on Chip Package Co-Design*, CPD '98 Secretary, c/o Electronics Laboratory ETH, 1998, pp. 33-38.

Etienne Hirt is a PhD candidate in the MCM group of the Electronics Laboratory at the Swiss Federal Institute of Technology (ETH) Zürich, Switzerland. His research interests include system and package design methodology using MCM technologies. Hirt received the MS degree in electrical engineering from ETH Zürich. He is a student member of the IEEE.

Michael Scheffler is a PhD candidate in the MCM group of the Electronics Laboratory, ETH Zürich. His research interests include electronic design automation, cost modeling, and optimization. Scheffler received the Dipl. Ing. (MS) degree in electrical engineering from the Technical University, Berlin, Germany. He is a student member of the IEEE.

Jean-Pierre Wyss is a PhD candidate in the MCM group of the Electronics Laboratory, ETH Zürich. His main interests include MCM test strategies and design of high-complexity MCMs. He is a cofounder of u-blox ag, an ETH Zürich spin-off company. u-blox ag provides innovative and cost-effective electronic packaging solutions for a broad range of applications. Wyss received the MS degree in electrical engineering from ETH Zürich. He is a student member of the IEEE and the IEEE Computer Society.

Direct questions concerning this article to Etienne Hirt, Electronics Laboratory, ETH Zürich, CH-8092, Zürich, Switzerland; hirt@ife.ee.ethz.ch.