APPENDIX K
DDR SRAM

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Double-data-rate (DDR) SDRAM was introduced in Chapter 5. The key feature of DDR SDRAM is that the data transfer is synchronized to both the rising and falling edge of the clock. Figure K.1 gives some idea of how DDR works by comparing the first two generations of DDR (DDR1 and DDR2) to ordinary synchronous data rate SDRAM transfer.

The DDR1 uses a 2-bit prefetch buffer so that it can operate at twice the data rate of an ordinary single data rate (SDR) SDRAM using the same chip frequency. DDR2 doubles this to a 4-bit prefetch buffer and also doubles the clock frequency for transfer from the buffer to the data bus. This enables a doubling of data rate over DDR1. Similarly, DDR3 uses and 8-bit prefetch buffer and a higher clock rate to each a greater data rate.

Table K.1 compares some basic characteristics of the DDR generations.

Table K.1 DDR Characteristics

	DDR1	DDR2	DDR3
Prefetch buffer (bits)	2	4	8
Voltage level (V)	2.5	1.8	1.5
Front side bus data rates (Mbps)	200, 266, 333, 400	400, 533, 677, 800	800, 1066, 1330, 1600

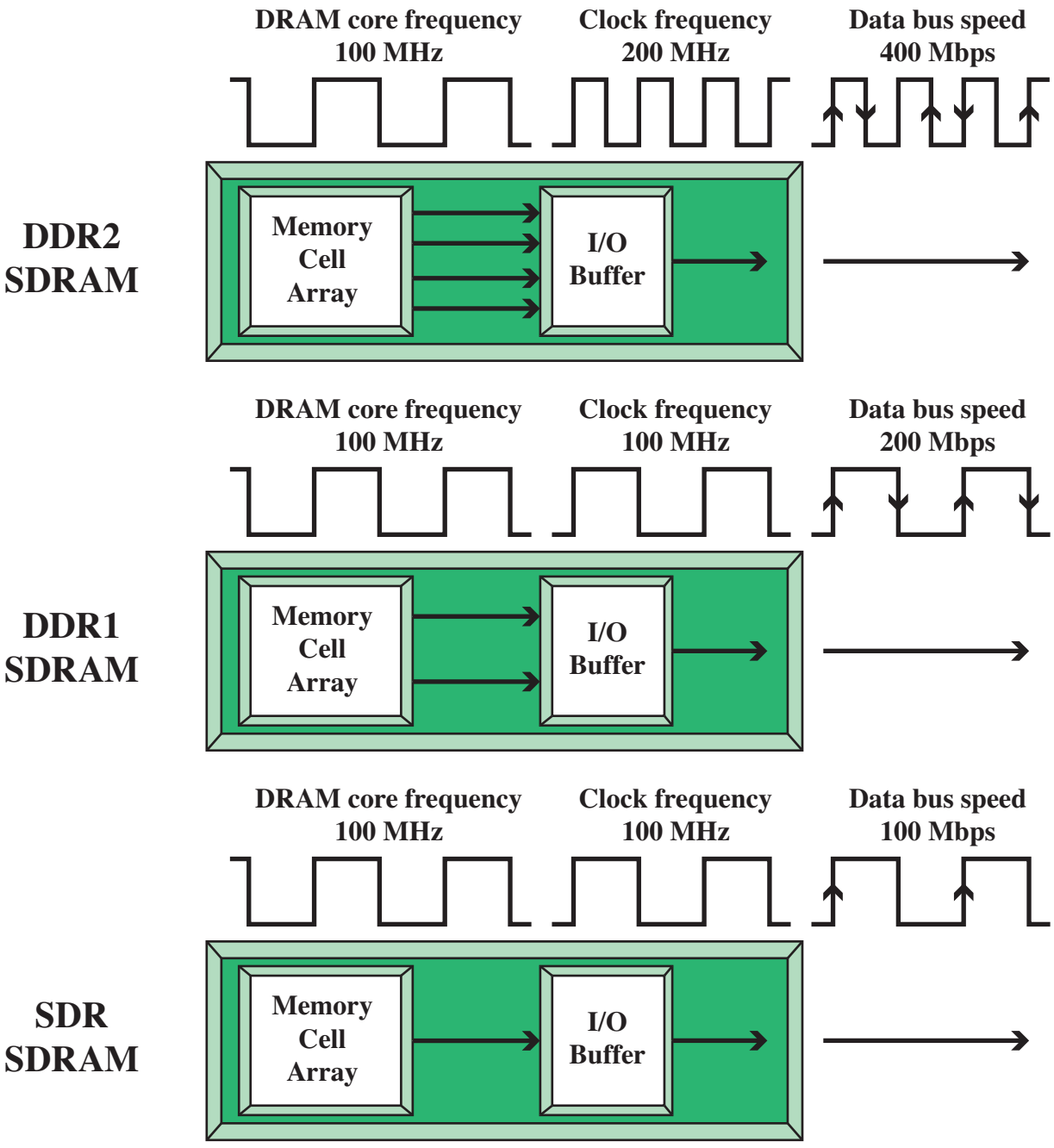

Figure K.1 DDR1 and DDR2 Comparison