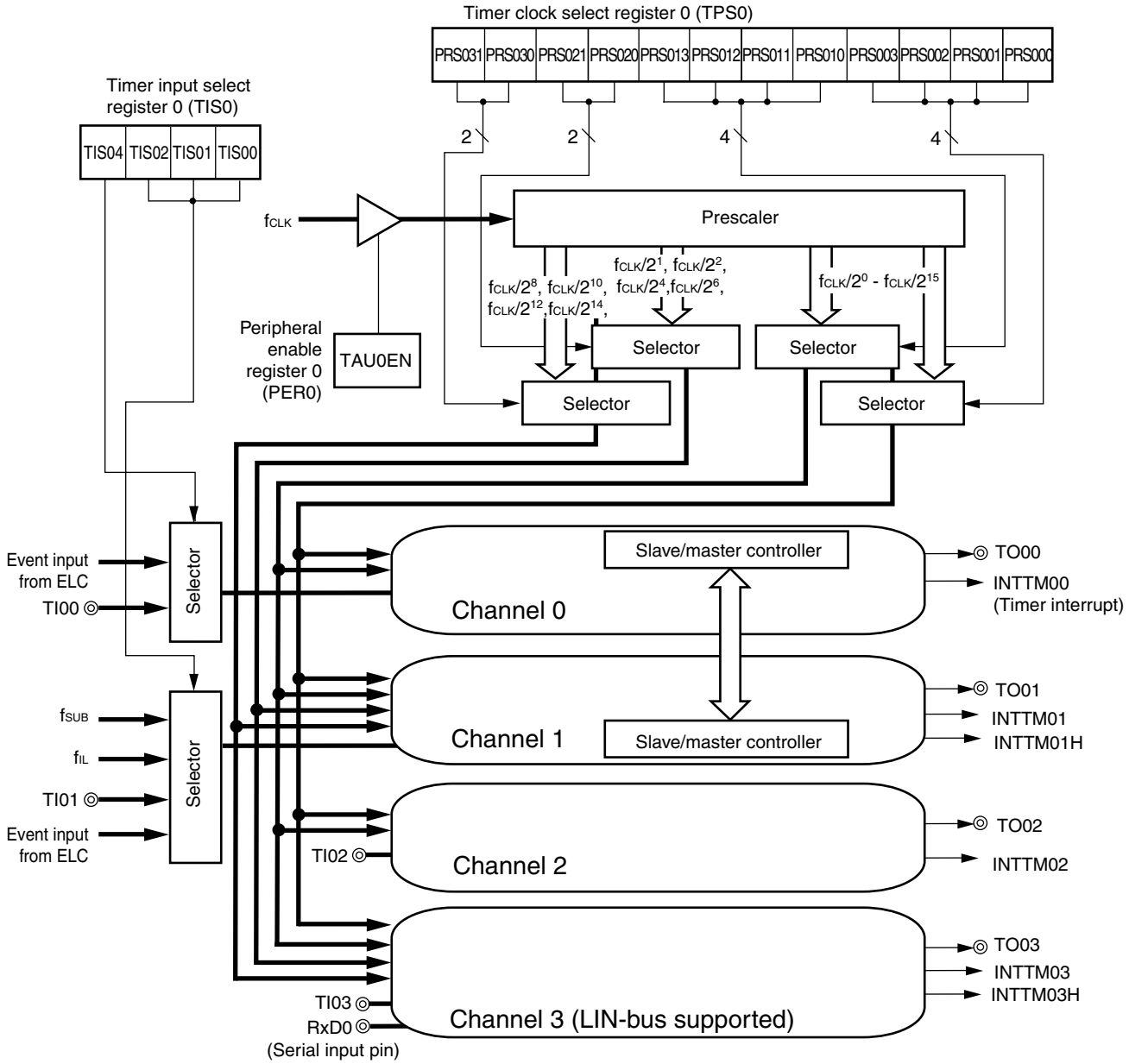
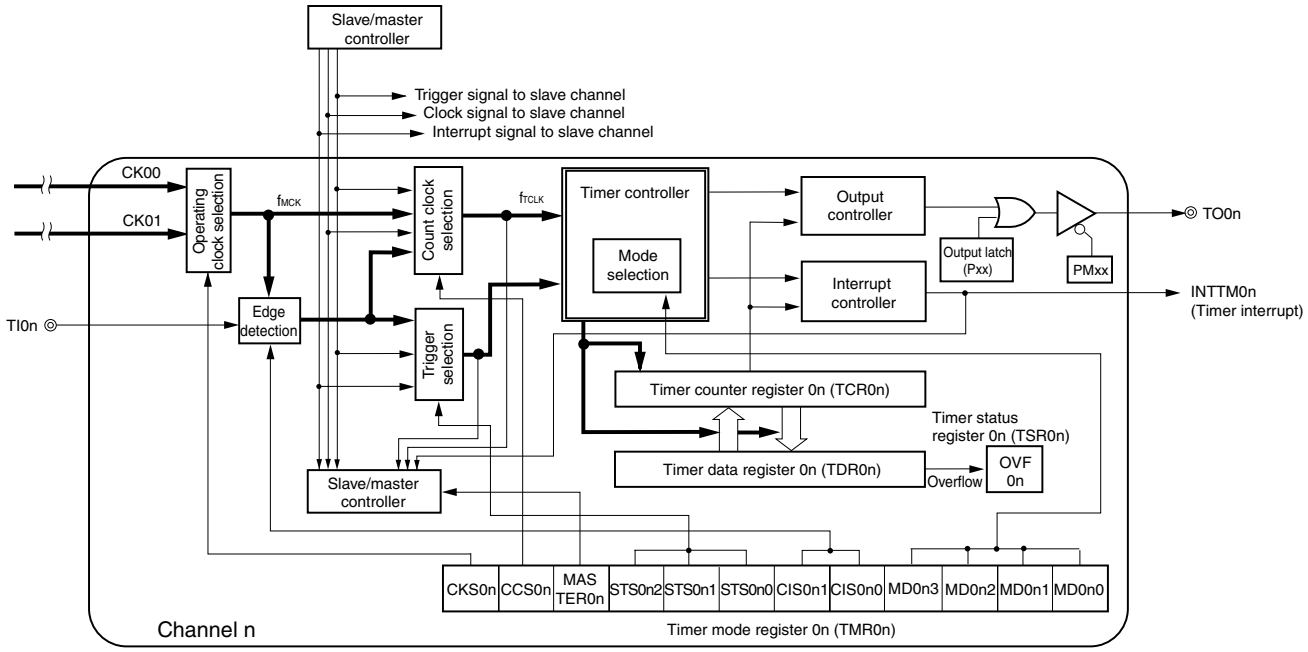
Figure 6-1. Entire Configuration of Timer Array Unit 0 (Example: 100-pin products)



Remark f_{SUB}: Subsystem clock frequency

f_{IL}: Low-speed on-chip oscillator clock frequency

Figure 6-2. Internal Block Diagram of Channel of Timer Array Unit 0



Remark n = 0, 2

(1) Timer count register mn (TCRmn)

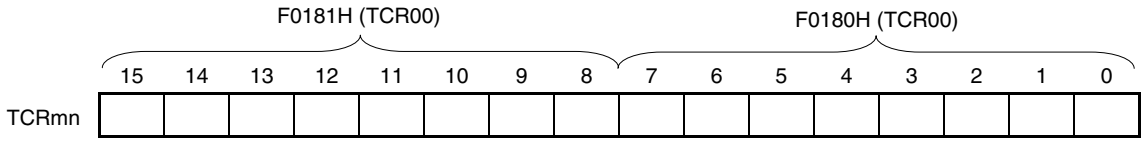
The TCRmn register is a 16-bit read-only register and is used to count clocks.

The value of this counter is incremented or decremented in synchronization with the rising edge of a count clock.

Whether the counter is incremented or decremented depends on the operation mode that is selected by the MDmn3 to MDmn0 bits of timer mode register mn (TMRmn) (refer to **6.3 (3) Timer mode register mn (TMRmn)**).

Figure 6-3. Format of Timer Count Register mn (TCRmn)

Address: F0180H, F0181H (TCR00) to F0186H, F0187H (TCR03), F01C0H, F01C1H (TCR10) to F01C6H, F01C7H (TCR13) After reset: FFFFH R



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)